SYNERGY SEMICONDUCTOR

FREQUENCY SYNTHESIZER

ClockWorks™
PRELIMINARY
SY89429

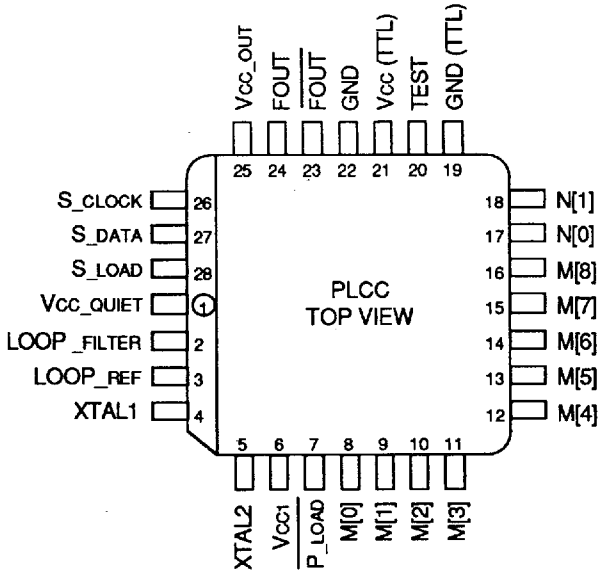
FEATURES

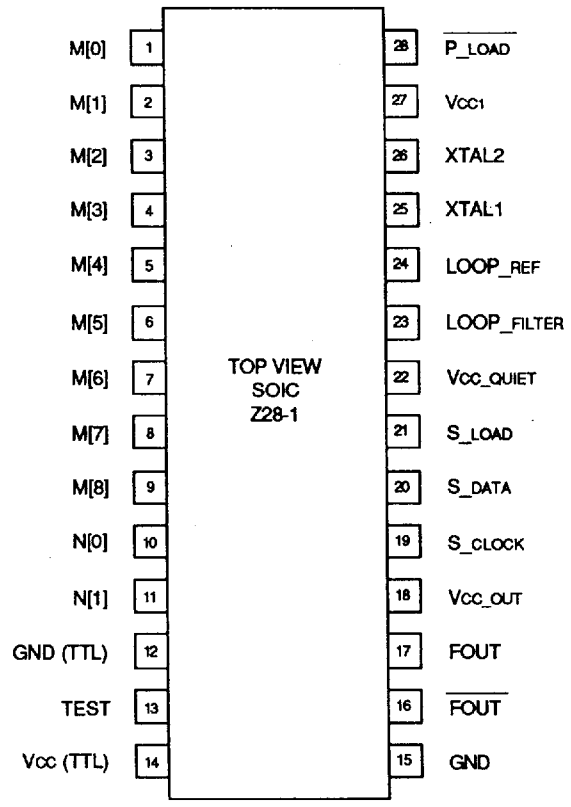
- 25 to 400MHz differential PECL outputs
- ±25ps output jitter within 100 cycles
- Minimal frequency over-shoot
- Synthesized architecture
- Serial 3 wire interface
- Parallel interface for power-on
- Internal quartz reference
- PECL output can operate with either +3.3V or +5V V_{CC_OUT} power supply
- Available in PLCC and SOIC 28 pin packages

DESCRIPTION

The SY89429 is a general purpose, synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 2, 4, 8 or 16. With the output configured to divide the VCO frequency by 2, and with a 16MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps.

PIN CONFIGURATION

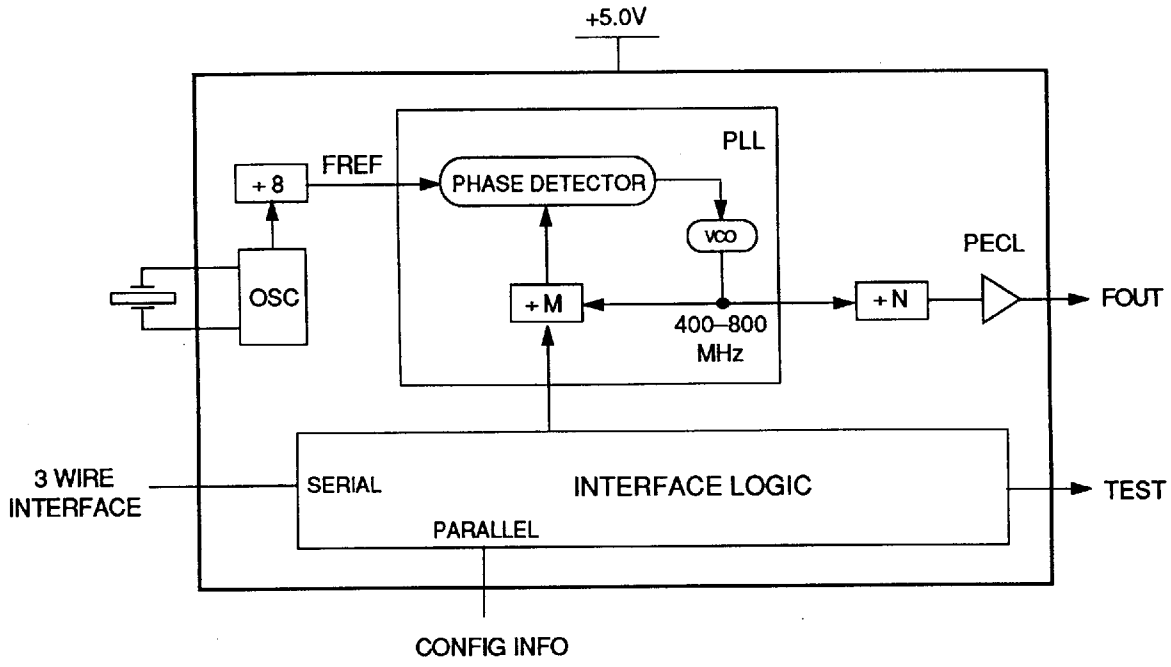




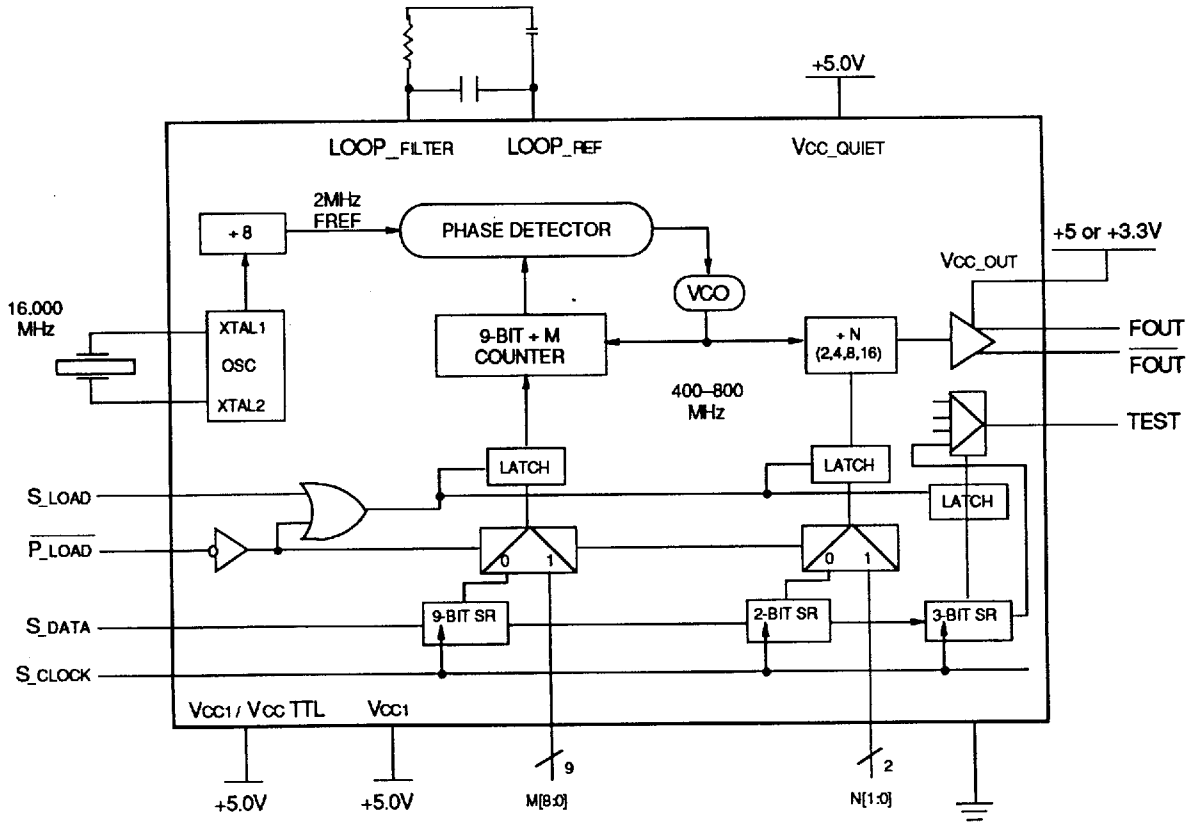
APPLICATIONS

- Workstations
- Advanced communications
- High end consumer
- High-performance computing
- RISC CPU clock
- Graphics pixel clock
- Test equipment
- Other high-performance processor-based applications

BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUTS

XTAL1, XTAL2

These pins form an oscillator when connected to an external crystal. The crystal is series resonant. Alternatively, these pins can be driven with 100K PECL level by an external source.

S_LOAD

This TTL pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the register data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.

S_DATA

This TTL pin is the input to the serial configuration shift registers.

S_CLOCK

This TTL pin clocks the serial configuration shift registers. On the rising edge of this signal, data from S_DATA is sampled.

$\overline{\text{P\_LOAD}}$

This TTL pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; thus, the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.

M[8:0]

These TTL pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD. M[8] is the MSB, M[0] is the LSB. The binary count on the M pins equates to the divide-by value for the PLL.

N[1:0]

These TTL pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	16

With 16MHz Input

VCO Frequency (MHz)	M Count	256 M8	128 M7	64 M6	32 M5	16 M4	8 M3	4 M2	2 M1	1 M0
400	200	0	1	1	0	0	1	0	0	0
402	201	0	1	1	0	0	1	0	0	1
404	202	0	1	1	0	0	1	0	1	0
406	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
794	397	1	1	0	0	0	1	1	0	1
796	398	1	1	0	0	0	1	1	1	0
798	399	1	1	0	0	0	1	1	1	1
800	400	1	1	0	0	1	0	0	0	0

PIN DESCRIPTIONS (CONT'D)

OUTPUTS

FOUT, $\overline{FOUT}$

These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.

TEST

The function of this TTL output is determined by the serial configuration bits T[2:0].

POWER

V_{CC1}

This is the positive supply for the chip and is normally connected to +5.0V.

V_{CC_OUT}

This is the positive reference for the PECL outputs, FOUT and $\overline{FOUT}$. It is constrained to be less than or equal to V_{CC1}.

V_{CC_QUIET}

This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation.

GND

These pins are the negative supply for the chip and are normally all connected to ground.

OTHER

LOOP_FILTER

This is an analog I/O pin that provides the loop filter for the PLL.

LOOP_REF

This is an analog I/O pin that provides a reference voltage for the PLL.

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_I	–0.5 to +7.0	V
Output Source	I_{OUT}	50	mA
Current (Continuous)			
Output Source	I_{OUT}	100	mA
Current (Surge)			
Storage Temperature	T_{STG}	–65 to +150	°C
Operating Temperature	T_{AMB}	0 to +75	°C

Note:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by eight before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz.

The VCO within the PLL operates over a range of 400–800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. External loop filter components are utilized to allow for optimal phase jitter performance.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. The output divider is configured through either the serial or the parallel interfaces and can provide one of four divider ratios (2, 4, 8 or 16). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω. The positive reference for the output driver is provided by a dedicated power pin (V_{CC_OUT}) to reduce noise and provide application flexibility.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the $\overline{P\_LOAD}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pull-up resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count.

The serial interface logic is implemented with a 14-bit shift register scheme. The register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet set-up and hold timing as specified in the AC parameters section of this data sheet. The configuration latches will capture the value in the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

PROGRAMMING INTERFACE

Programming the device is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$FOUT = \left(\frac{FXTAL}{8}\right) \times M + N$$

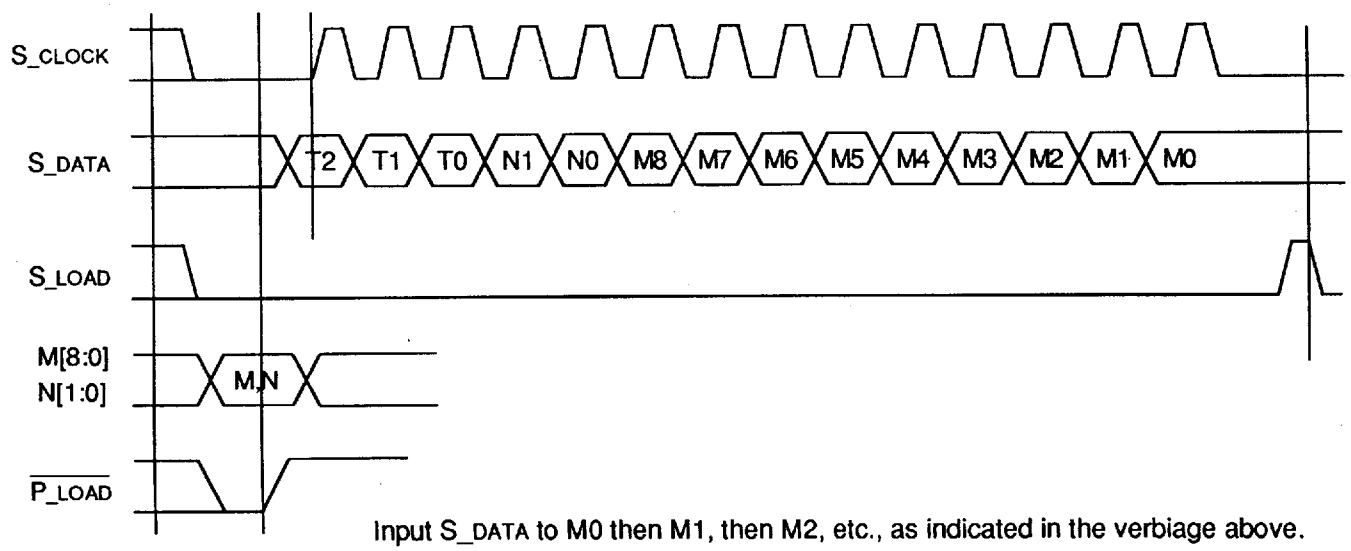
Where FXTAL is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$.

M[8:0] and N[1:0] are normally specified once at power-on, through the parallel interface, and then possibly again through the serial interface. This approach allows the designer to bring up the application at one frequency and then change or fine-tune the clock, as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible.

The TEST output provides visibility for one of several internal nodes (as determined by the T[1:0] bits in the serial configuration stream). It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the TTL output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1, T0 configuration latches are preset to 000 when P_LOAD is low, so that the FOUT outputs are as jitter-free as possible. The serial configuration port can be used to select one of the alternate functions for this pin. The serial data sequence is as follows:

Input S_DATA to M0, then M1, then M2, then M3, then M4, then M5, then M6, then M7, then M8, then N0, then N1, then T0, then T1, then T2, to TEST output mux.

T2	T1	T0	TEST
0	0	0	Data Out – Last Bit SR
0	0	1	HIGH
0	1	0	FREF
0	1	1	M Counter Out
1	0	0	FOUT
1	0	1	LOW
1	1	0	S_CLOCK/M
1	1	1	FOUT/4



Input S_DATA to M0 then M1, then M2, etc., as indicated in the verbiage above.

100H ECL DC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC_QUIET} = V_{CC} (TTL) = +5.0V ±10%; V_{CC_OUT} = +3.3V/+5.0V ±10%; T_A = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC_OUT} –1.025	V_{CC_OUT} –0.880	V	50Ω to V_{CC_OUT} –2V
V_{OL}	Output LOW Voltage	V_{CC_OUT} –1.810	V_{CC_OUT} –1.620	V	50Ω to V_{CC_OUT} –2V

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC_QUIET} = V_{CC} (TTL) = +5.0V ±10%; V_{CC_OUT} = +3.3V/+5.0V ±10%; T_A = 0°C to +75°C

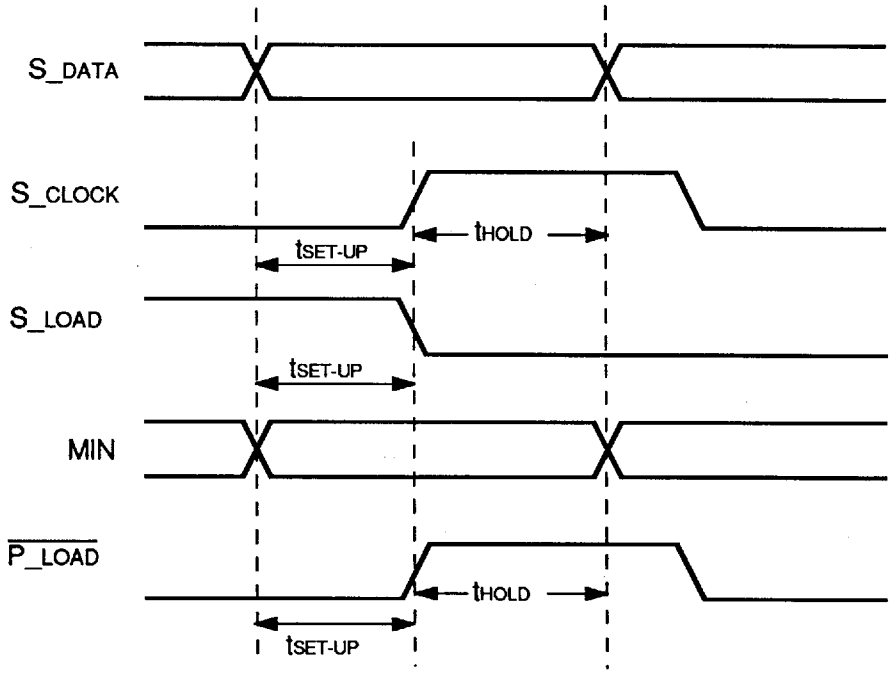
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	—	50	—	50	—	50	µA	V_{IN} = 2.7V
I_{IL}	Input LOW Current	—	–0.6	—	–0.6	—	–0.6	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	—	2.5	—	2.5	—	2.5	V	I_{OH} = –2.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 8mA
I_{OS}	Output Short Circuit Current	–80 (Typ.)		–80 (Typ.)		–80 (Typ.)		mA	V_{OUT} = 0V
I_{CC1}	Supply Current							mA	—
	V_{CC1}	—	200	—	200	—	200		
	V_{CC_OUT}	—	10	—	10	—	10		
	V_{CC_QUIET}	—	10	—	10	—	10		

AC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC_QUIET} = V_{CC} (TTL) = +5.0V ±10%; V_{CC_OUT} = +3.3V/+5.0V ±10%; T_A = 0°C to +75°C

Parameter	Min.	Typ.	Max.	Unit
S_CLOCK Max. Frequency	—	—	10.0	MHz
Oscillator Frequency	10	—	20	MHz
S_DATA to S_CLOCK Set-up	20	—	—	ns
S_DATA to S_CLOCK Hold	20	—	—	ns
S_CLOCK to S_LOAD Set-up	20	—	—	ns
S_LOAD Min. HIGH Time	50	—	—	ns
M,N to $\overline{P\_LOAD}$ Set-up	20	—	—	ns
M,N to $\overline{P\_LOAD}$ Hold	20	—	—	ns
$\overline{P\_LOAD}$ Min. LOW Time	50	—	—	ns
Reference OSC Max. Frequency	—	—	20	MHz
Reference OSC Min. Frequency	10	—	—	MHz
PLL Lock from $\overline{P\_LOAD}$	1	—	10	ms
VCO Max. Frequency	—	—	800	MHz
VCO Min. Frequency	400	—	—	MHz
FOUT Duty Cycle	—	—	45/55	%
FOUT Max. Jitter	—	—	10	ps rms

TIMING DIAGRAM



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89429JC	J28-1	Commercial
SY89429ZC	Z28-1	Commercial