Integrated Device Technology, Inc.

36 TO 9 BIFIFO

IDT 7MB2002

FEATURES:

- First-in/First-out memory module
- Asynchronous and simultaneous read and write
- 36-bit data bus on one side; 9-bit data bus on other side
- All logic required for conversion between 36 and 9-bit buses included on board
- 4K x 36-bit to 16K x 9-bit deep
- Selectable LSB or MSB first on 9-bit side
- Bidirectional
- Latching transceiver for LS 8 bits between the two buses
- Total cycle time 45ns

DESCRIPTION:

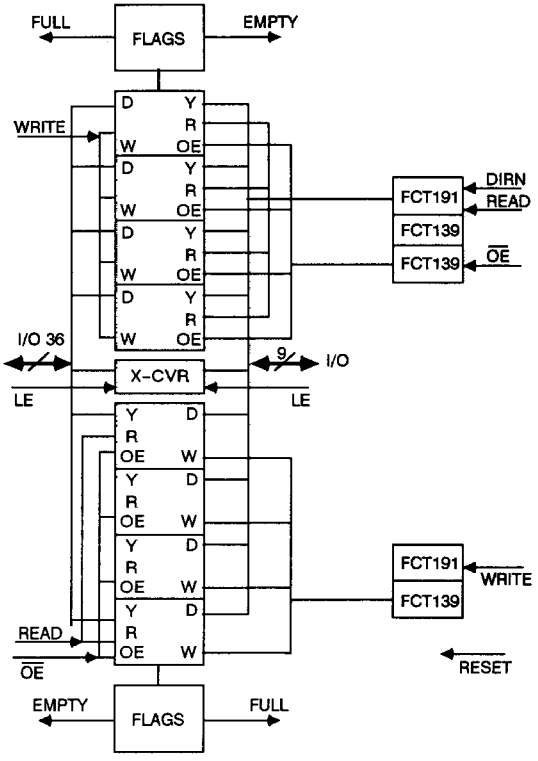
This module is a FIFO that has up to 8 IDT72041s (4K x 9) on board. The module is bidirectional with 4K x 36 transforming to 16K x 9 on one side and back to 4K x 36 on the other side. All logic necessary to control the conversion between 36 and 9 bits is included on the module.

On the 9-bit side, there is a DIRN pin which determines whether the 36 bits of data is presented to the 9-bit side's most significant byte first or least significant byte first and, conversely, whether the 9-bit side data is being entered MSB or LSB first.

Included on-board is an 8-bit transceiver with separate latch enables for each side to allow the passing of status between the buses.

The module is packaged on a 92 pin FR-4 substrate occupying less than 4 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION

GND	1	37	GND		V_{CC}	72	36	V_{CC}
I/OL_0	2	38	$\overline{OELR}$		$\overline{OERL}$	71	35	I/OR_8
I/OL_1	3	39	$\overline{LELR}$		$\overline{LERL}$	70	34	I/OR_7
I/OL_2	4	40	I/OL_3		I/OR_5	69	33	I/OR_6
I/OL_4	5	41	I/OL_5		I/OR_3	68	32	I/OR_4
I/OL_6	6	42	I/OL_7		GND	67	31	I/OR_2
I/OL_8	7	43	I/OL_9		I/OR_0	66	30	I/OR_1
I/OL_{10}	8	44	I/OL_{11}		I/OL_{35}	65	29	RESET
$\overline{FULL}_L$	9	45	$\overline{FULL}_R$	M25[1]	I/OL_{33}	64	28	I/OL_{34}
$\overline{EMPTY}_L$	10	46	$\overline{EMPTY}_R$		I/OL_{31}	63	27	I/OL_{32}
$\overline{WRITE}_L$	11	47	DIRN		I/OL_{30}	62	26	$\overline{WRITE}_R$
$\overline{READ}_L$	12	48	GND		GND	61	25	$\overline{READ}_R$
$\overline{OE}_L$	13	49	I/OL_{12}		I/OL_{29}	60	24	$\overline{OE}_R$
I/OL_{13}	14	50	I/OL_{14}		I/OL_{27}	59	23	I/OL_{28}
I/OL_{15}	15	51	I/OL_{16}		I/OL_{25}	58	22	I/OL_{26}
I/OL_{17}	16	52	I/OL_{18}		I/OL_{23}	57	21	I/OL_{24}
I/OL_{19}	17	53	I/OL_{20}		I/OL_{21}	56	20	I/OL_{22}
V_{CC}	18	54	V_{CC}		GND	55	19	GND

NOTE:

1. For module dimensions, please refer to module drawing M25 in the packaging section.

PIN DESCRIPTIONS

SIGNAL NAME	DESCRIPTION
V_{CC}	Power
GND	Ground
I/OL	36 bit I/O bus
I/OR	9 bit I/O bus
FULL	FIFO Full Flag
EMPTY	FIFO Empty Flag
WRITE	Write Enable
READ	Read Enable
$\overline{OE}$	Output Enable
OELR	Transceiver Output Enable (L - R)
OERL	Transceiver Output Enable (R - L)
LELR	Transceiver Latch Enable (L - R)
LERL	Transceiver Latch Enable (R - L)
DIRN	LSB/MSB Selection on 9 bit side
RESET	System Reset

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	50V ±10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} (1)	Input High Voltage Commercial	2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
$I_{L1\ LEFT}$	Leakage Current Left		-10	10	µA
$I_{L1\ RIGHT}$	Leakage Current Right		-40	40	µA
I_{CC1}	Ave. V_{CC} Supply Current		–	680(1)	mA
I_{CC2}	Ave. Standby Current		–	130	mA
I_{CC3}	Power Down Current		–	90	mA
V_{OH}	Output High Voltage	I_{OH} = -2mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = -8mA	–	0.4	V

NOTE:
1. I_{CC1} = 780mA at 45ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	pF

NOTE:
1. This parameter is sampled and not 100% tested.

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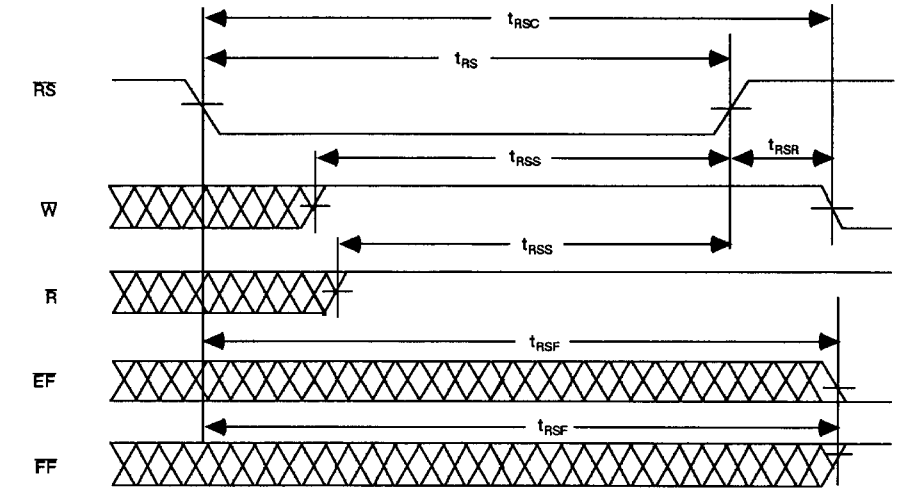
AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7MB2002S45 MIN.	7MB2002S45 MAX.	7MB2002S60 MIN.	7MB2002S60 MAX.	7MB2002S75 MIN.	7MB2002S75 MAX.	7MB2002S90 MIN.	7MB2002S90 MAX.	7MB2002S130 MIN.	7MB2002S130 MAX.	UNIT
READ CYCLE												
f_s	Frequency Shift	–	18	–	13	–	11	–	9	–	7	MHz
t_{RC}	Read Cycle Time	55	–	75	–	90	–	110	–	150	–	ns
t_A	Access Time	–	45	–	60	–	75	–	90	–	130	ns
t_{RR}	Read Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width	45	–	60	–	75	–	90	–	130	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	ns
t_{REF}	Read Low to Empty Flag Low	–	45	–	60	–	75	–	75	–	75	ns
t_{RFF}	Read High to Full Flag High	–	45	–	60	–	75	–	75	–	75	ns
t_{RLZ}	Read Low to Data Low Z	5	–	10	–	10	–	10	–	10	–	ns
t_{RHZ}	Read High to Data High Z	–	30	–	40	–	40	–	40	–	40	ns
WRITE TIMING												
t_{WC}	Write Cycle Time	55	–	75	–	90	–	110	–	150	–	ns
t_{WPW}	Write Pulse Width	45	–	60	–	75	–	90	–	130	–	ns
t_{WR}	Write Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	20	–	32	–	32	–	42	–	42	–	ns
t_{DH}	Data Hold Time	0	–	5	–	10	–	10	–	10	–	ns
t_{WEF}	Write High to Empty Flag High	–	45	–	60	–	75	–	75	–	75	ns
t_{WFF}	Write Low to Fall Flag Low	–	45	–	60	–	75	–	75	–	75	ns
RESET TIMING												
t_{RSC}	Reset Cycle Time	50	–	70	–	85	–	105	–	145	–	ns
t_{RS}	Reset Pulse Width	40	–	55	–	70	–	85	–	125	–	ns
t_{RSS}	Reset Set-up Time	40	–	55	–	70	–	85	–	125	–	ns
t_{RSR}	Reset Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{OHZ}	$\overline{OE}$ High to Data High Z	–	23	–	31	–	40	–	40	–	40	ns
t_{OLZ}	$\overline{OE}$ Low to Data Low Z	–	23	–	31	–	40	–	40	–	40	ns
t_{OE}	$\overline{OE}$ Low to Valid Data	–	26	–	36	–	50	–	50	–	50	ns
t_{RSF}	Reset Empty/Full Flag	–	55	–	75	–	90	–	110	–	150	ns



NOTES:
1. $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_H around the rising edge of $\overline{RS}$.

Figure 1. Reset

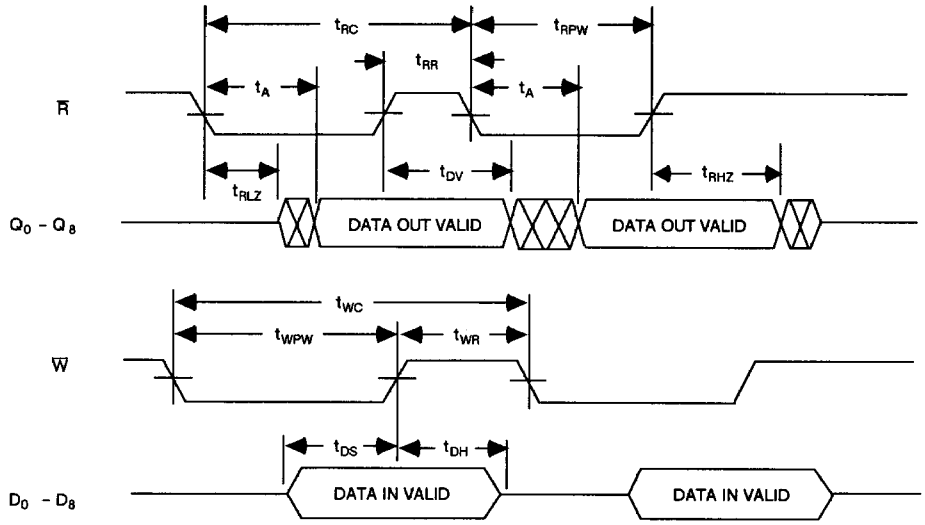


Figure 2. Asynchronous Write and Read Operation

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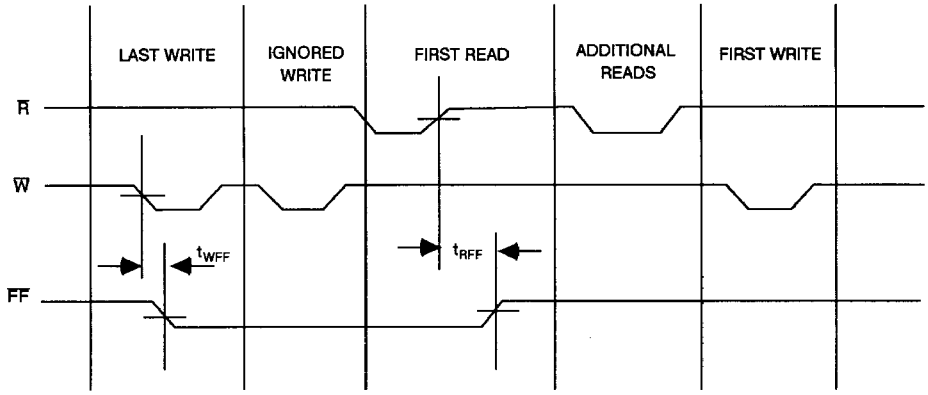


Figure 3. Full Flag from Last Write to First Read

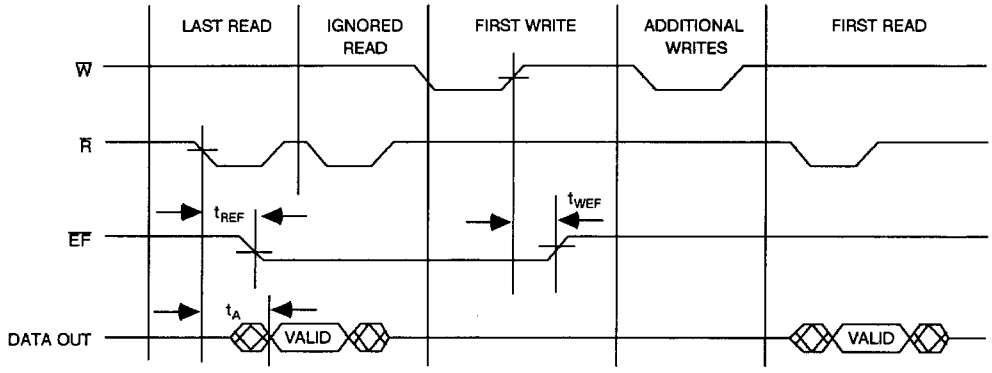


Figure 4. Empty Flag from Last Read to First Write

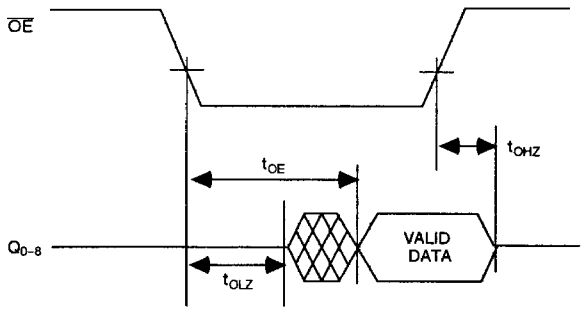


Figure 5. Output Enable Timing

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

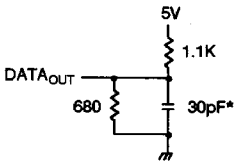


Figure 1. Output Load

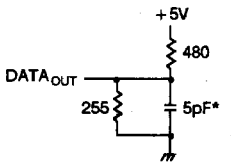
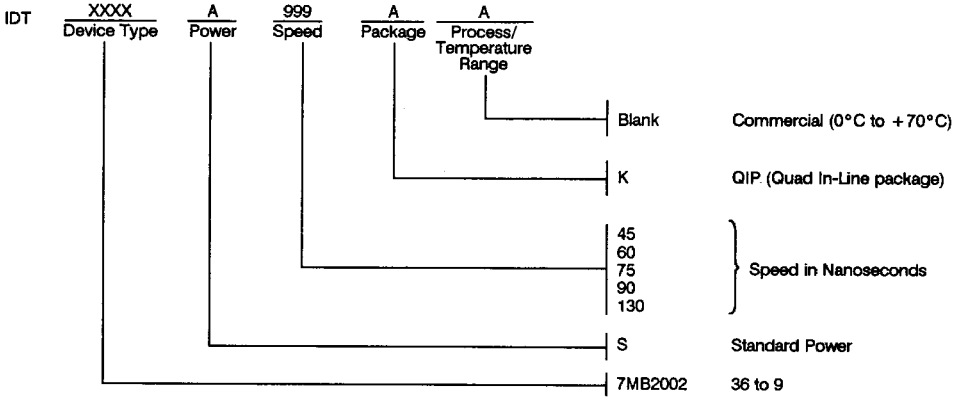


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

* Includes jig and scope capacitances.

ORDERING INFORMATION



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