Standard Products

UT8SDMQ64M40 2.5-Gigabit SDRAM MCM
UT8SDMQ64M48 3.0-Gigabit SDRAM MCM

Preliminary Datasheet
October 25, 2011

FEATURES

- Organized as 64M x 40 (16Meg x 40 x 4 banks) and 64Meg x 48 (16Meg x 48 x 4 banks)
- Single JEDEC standard 3.3V power supply
- PC100-compliant
- Operation -40°C to +105°C
- LVTTL compatible with multiplexed address
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Programmable burst lengths: 1,2,4,8, or full page
- Auto-precharge, includes concurrent auto precharge, and auto-refresh mode
- 32ms, 8,192-cycle refresh
- Operational environment:
  - Total dose: 100 krad(Si)
  - SEL Immune 111 MeV-cm^2/mg
- Package options:
  128-lead Ceramic Quad Flatpack
- Standard Microcircuit Drawing TBD
  - UT8SDMQ64M40: 5962-10229
  - UT8SDMQ64M48: 5962-10230
    - QML Q and Q+ pending

INTRODUCTION

The UT8SDMQ64M40 and UT8SDMQ64M48 are high performance, highly integrated Synchronous Dynamic Random Access Memory (SDRAM) multi-chip modules (MCMs). Total module density is 2,684,354,560 bits for the 2.5G device and 3,221,225,472 bits for the 3G device. Each bit bank is organized as 8192 rows by 2048 columns.

Read and write accesses to the DRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The programmable READ and WRITE burst lengths (BL) are 1, 2, 4, or 8 locations, or the full page, with a burst terminate option.

Aeroflex's SDRAMs are designed to operate at 3.3V. An auto-refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL compatible. SDRAMs offer significant advances in DRAM operating execution, including the capability to synchronously burst data at a high data rate with automatic column-address generation, to interleave between internal banks to mask precharging time, and to randomly change column addresses on each clock cycle during a burst access.

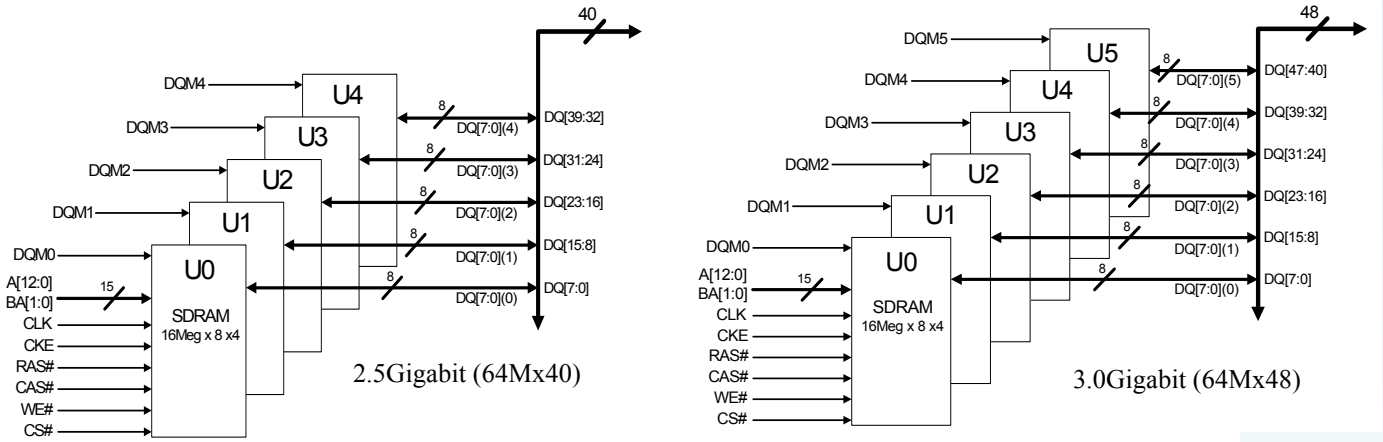

Figure 1. Block Diagrams

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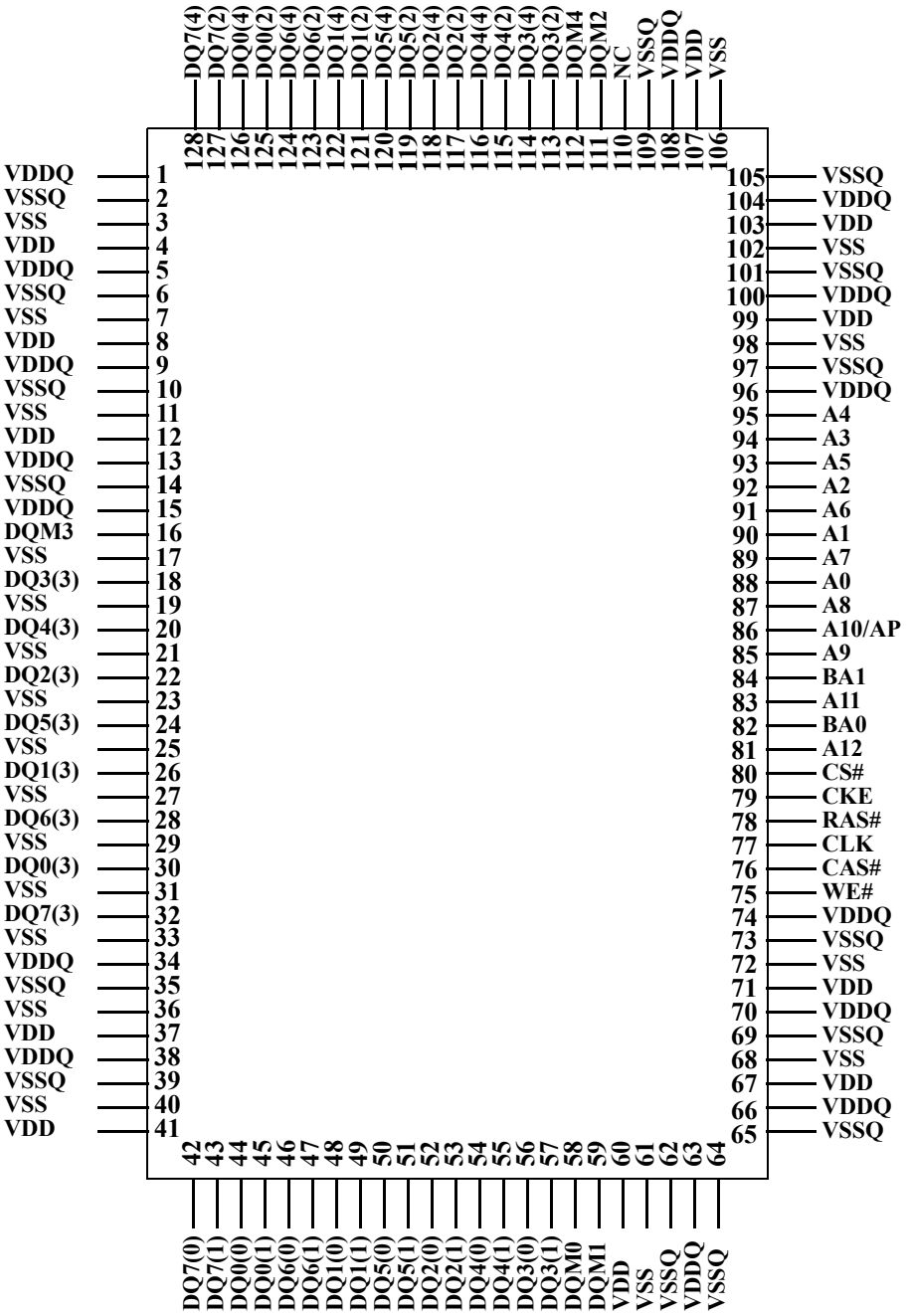


Figure 2: 128-lead Package 2.5G (512Mb x 5) SDRAM Module

2.5G (512Mb x 5) SDRAM Module

Table 1. Pin Descriptions

Pin Numbers	Symbols	Type	Description
77	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
79	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down, ACTIVE power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down providing low standby power. CKE may be tied HIGH.
80	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
78, 76, 75	RAS#,CAS#, WE#	Input	Input Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
112, 16, 111, 59, 58	DQM(4:0)	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle.
84 ,82	BA (1:0)	Input	Bank address inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
81, 83, 86, 85, 87, 89, 91, 93, 95, 94, 92, 90, 88	A(12:0)	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command (column-address A0–A9, A11); with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10[HIGH]) or bank selected by (A10 [LOW]). The address inputs also provide the opcode during a LOAD MODE REGISTER command.
42, 46, 50, 54, 56, 52, 48, 44	DQ[7.0](0)	Data I/O	Data input/output
43, 47, 51, 55, 57, 53, 49, 45	DQ[7:0](1)	Data I/O	Data input/output
127, 123, 119, 115, 113, 117, 121, 125	DQ[7:0](2)	Data I/O	Data input/output
32, 28, 24, 20, 18, 22, 26, 30	DQ[7:0](3)	Data I/O	Data input/output

Table 1. Pin Descriptions

Pin Numbers	Symbols	Type	Description
128, 124, 120, 116, 114, 118, 122, 126	DQ[7:0](4)	Data I/O	Data input/output
110	NC		No connect: This pin should be left unconnected.
1, 5, 9, 13, 15, 34, 38, 63, 66, 70, 74, 96, 100, 104, 108	VDDQ	Supply	DQ power: Isolated DQ power to the die for improved noise immunity.
2, 6, 10, 14, 35, 39, 62, 64, 65, 69, 73, 97, 101, 105, 109	VSSQ	Supply	DQ ground: Isolated DQ ground to the die for improved noise immunity.
4, 8, 12, 37, 41, 60, 67, 71, 99, 103, 107	VDD	Supply	Power supply: +3.3V $\pm$0.3V
3, 7, 11, 17, 19, 21, 23, 25, 27, 29, 31, 33, 36, 40, 61, 68, 72, 98, 102, 106	VSS	Supply	Ground

PACKAGE DRAWING

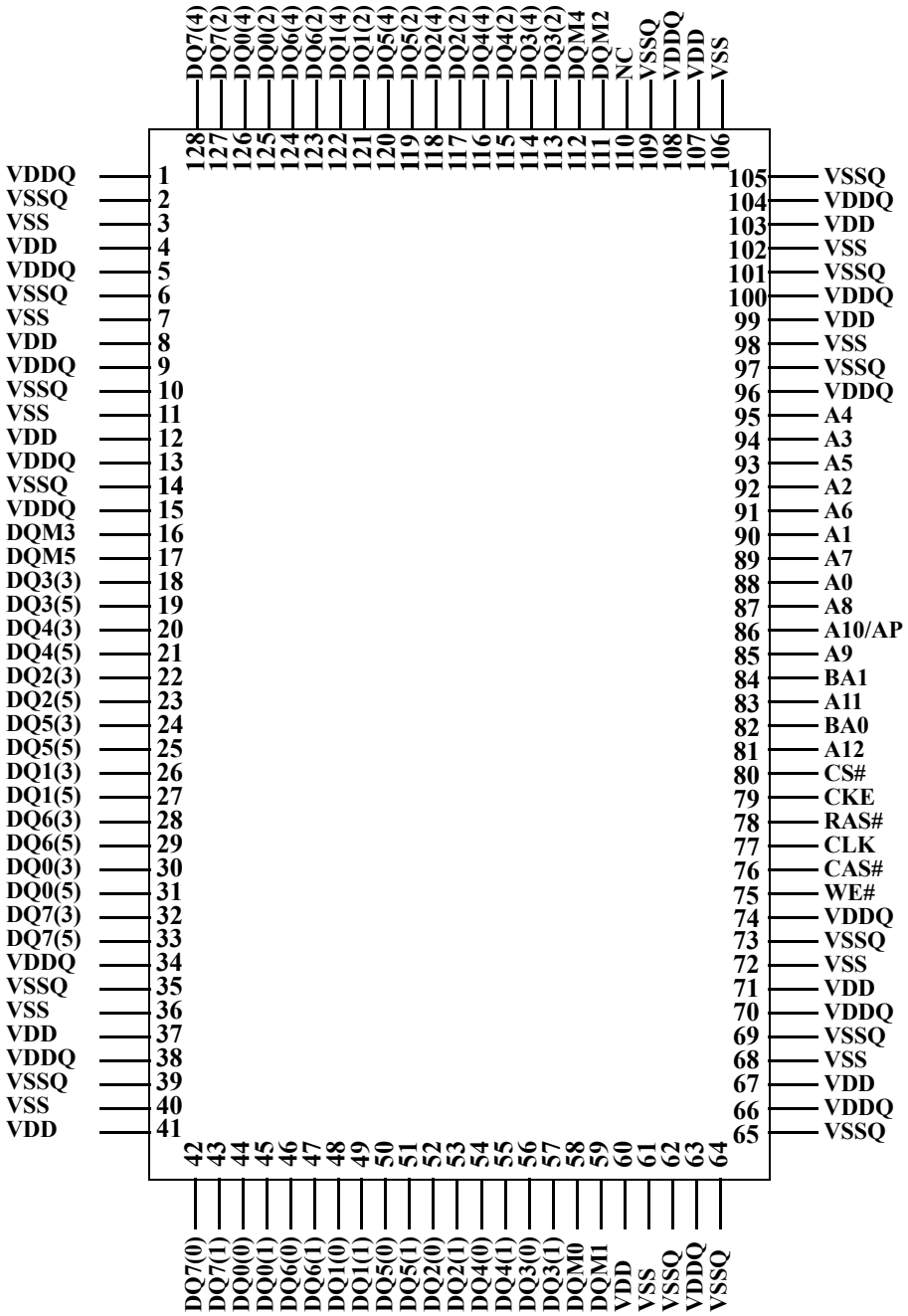


Figure 3: 128-lead Package 3.0G (512Mb x 6) SDRAM Module

3.0G (512Mb x 6) SDRAM Module

Table 2. Pin Descriptions

Pin Numbers	Symbols	Type	Description
77	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
79	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down, ACTIVE power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down providing low standby power. CKE may be tied HIGH.
80	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
75, 76, 78	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
16, 17, 58, 59, 111, 112	DQM(5:0)	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle.
82 ,84	BA(1:0)	Input	Bank address inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
81, 83, 85, 86, 87, 88, 89, 90, 91,92, 93, 94, 95	A(12:0)	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command (address A0–A9, A11 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10[HIGH]) or bank selected by (A10 [LOW]). The address inputs also provide the opcode during a LOAD MODE REGISTER command.
42, 44, 46, 48, 50, 52, 54, 56	DQ(7:0)(0)	Data I/O	Data input/output
43, 45, 47, 49, 51, 53, 55, 57	DQ[7:0](1)	Data I/O	Data input/output
113, 115, 117, 119, 121, 123, 125, 127	DQ[7:0](2)	Data I/O	Data input/output
18, 20, 22, 24, 26, 28, 30, 32	DQ[7:0](3)	Data I/O	Data input/output

Table 2. Pin Descriptions

Pin Numbers	Symbols	Type	Description
114, 116, 118,120, 122, 124,126, 128	DQ[7:0](4)	Data I/O	Data input/output
19, 21, 23, 25, 27, 29, 31, 33	DQ[7:0](5)	Data I/O	Data input/output
110	NC		No connect: This pin should be left unconnected.
1, 5, 9, 13, 15, 34, 38, 63, 66, 70, 74, 96, 100, 104, 108	VDDQ	Supply	DQ power: Isolated DQ power to the die for improved noise immunity.
2, 6, 10, 14, 35, 39, 62, 64, 65, 69, 73, 97, 101, 105, 109	VSSQ	Supply	DQ ground: Isolated DQ ground to the die for improved noise immunity.
4, 8, 12, 37, 41, 60, 67, 71, 99, 103, 107	VDD	Supply	Power supply: +3.3V ±0.3V.
3, 7, 11, 36, 40, 61, 68, 72, 98, 102, 106	VSS	Supply	Ground

FUNCTIONAL DESCRIPTION

The 2.5G and 3.0G SDRAMs are organized as 16M x 40 x 4 banks and 16M x 48 x 4 banks that operate on 3.3V using a synchronous interface (signals are registered on the positive CLK edge). Read and write accesses to the SDRAM are burst oriented. Accesses start at address locations selected and continue for programmed number of locations in a programmed sequence. Device accesses start with the registration of the ACTIVE command followed by a READ or WRITE command. Some address and both bank bits are registered coincident to the ACTIVE command registration and are used to select the row and bank locations, while column location to initiate burst access address bits A0-A9 are registered at time of READ/WRITE command.

Previous to normal operation the device must initialized properly.

Initialization

The SDRAMs must be powered up and initialized in a certain manner. Failure to initial devices may result in unpredictable behavior. Once stable power is applied to VDD and VDDQ (simultaneously), and the clock is running and stable (cycling within specified parameters) the device requires a minimum 100µs delay prior to issuing any command other than NOP or COMMAND INHIBIT. At some time during this period the COMMAND INHIBIT or NOP can be issued and should continue through the end of the 100µs period. After the delay has been completed with at least one COMMAND INHIBIT or NOP command, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing all banks in the device into the idle state. Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register powers up in an unknown state, it should be loaded prior to applying any operational command.

The recommended power-up sequence for SDRAMs:
1. Simultaneously apply power to VDD and VDDQ.
2. Assert and hold CKE at a LVTTL logic LOW since all inputs and outputs are LVTTL-compatible.
3. Provide stable CLOCK signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
4. Wait at least 100µs prior to issuing any command other than a COMMAND INHIBIT or NOP.
5. Starting at some point during this 100µs period, bring CKE HIGH. Continuing at least through the end of this period, one or more COMMAND INHIBIT or NOP commands must be applied.
6. Perform a PRECHARGE ALL command.
7. Wait at least ^{t}RP time; during this time, NOPs or DESELECT commands must be given. All banks will complete their precharge, thereby placing the device in the all banks idle state.
8. Issue an AUTO REFRESH command.
9. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
10. Issue an AUTO REFRESH command.
11. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
12. The SDRAM is now ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded with desired bit values prior to applying any operational command. Using the LMR command, program the mode register. The mode register is programmed via the MODE REGISTER SET command with BA1 = 0, BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the mode register upon initialization will result in default settings which may not be desired. Outputs are guaranteed High-Z after the LMR command is issued. Outputs should be High-Z already before the LMR command is issued.
13. Wait at least ^{t}MRD time, during which only NOP or DESELECT commands are allowed.

At this point, the DRAM is ready for any valid command.

Note: If desired, more than two AUTO REFRESH commands can be issued in the sequence. After steps 9 and 10 are complete, repeat them until the desired number of AUTO REFRESCH + ^{t}RFC loops is achieved.

REGISTER DEFINITION

Mode Register

The mode register is used to set a specific mode of operation for the SDRAM. These definitions include Burst length (BL), the CAS latency (CL), and the write burst mode as shown in Figure 4. The mode register is programmed using the LOAD MODE REGISTER command and retains the stored setting information until either reprogrammed or device power is lost. Mode register bits M0-M2

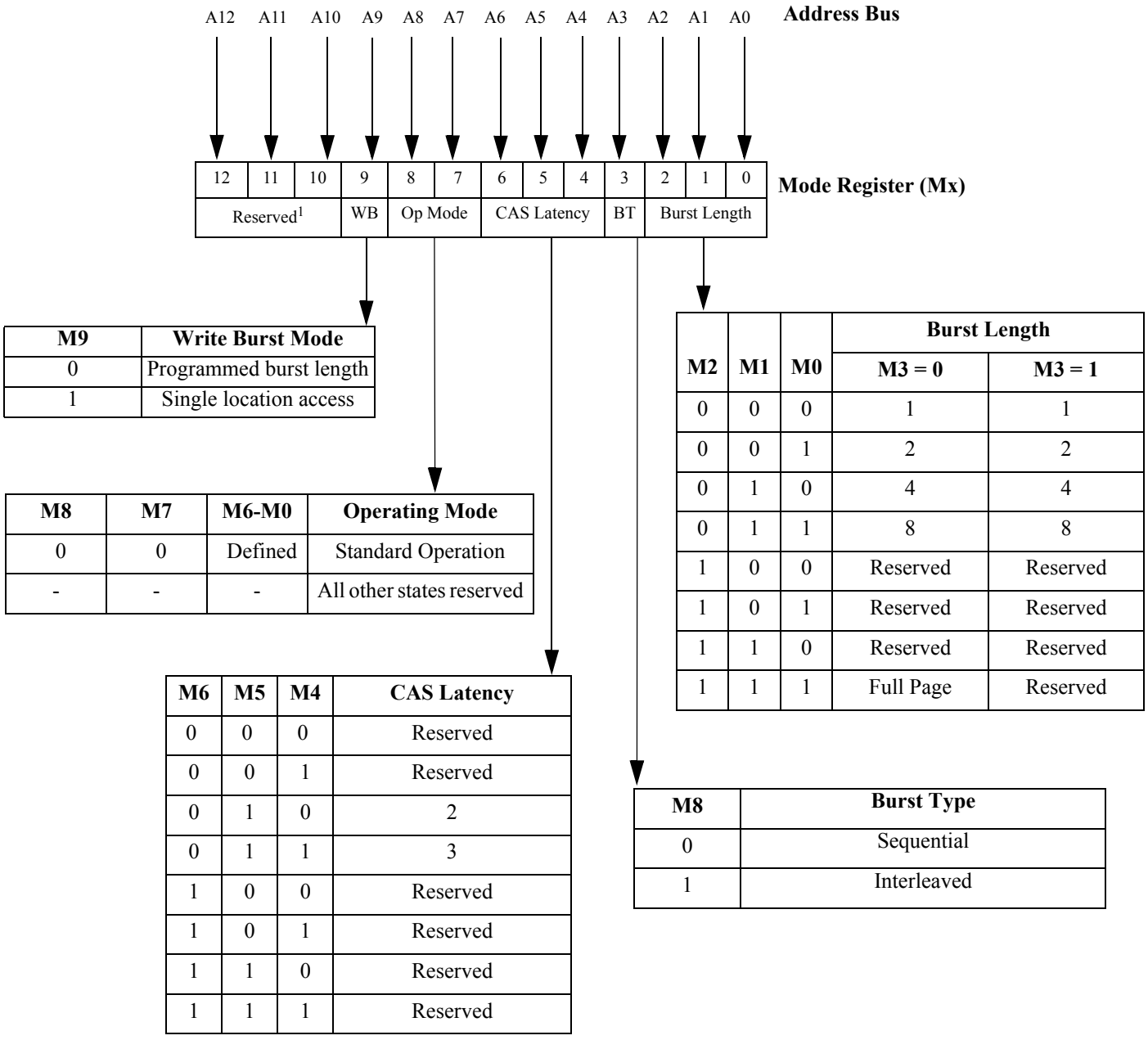
specifies the BL, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CL, M7 and M8 specifies the operation mode, M9 specifies the write burst mode, M10 and M11 are reserved. Address M12 is undefined, but should be driven low during mode register programming. All references to bit(s) Mx in this document affect the mode register.

Burst Length (BL)
All read and write activity to the SDRAMs are burst oriented. The burst mode is selected by programming BL as described above. Burst length of 1, 2, 4, and 8 locations are available for both sequential and interleaved burst types. A full page burst is also available in sequential mode only and is used in conjunction with BURST TERMINATE command to generate arbitrary burst lengths. Reserved states for BL should not be used as they may result in undefined operations.

Whenever a read or write command is issued a block of columns is selected that is equal to the BL. All access for that burst takes place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-A9, and A11when BL = 2, A2-A9, and A11when BL = 4, A3-A9, and A11when BL = 8. The remaining least significant address bits are used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type
Accesses within a given burst may be programmed to be either sequential or interleaved: this is referred to as the burst type and is selected via bit M3.

The ordering of the accesses with the burst is determined by BL_1, the burst type and the staring column address, as shown in Table 3.



M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M2	M1	M0	Burst Length	
			M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

M8	Burst Type
0	Sequential
1	Interleaved

Notes:
1. Program M12, M11, M10 = "0, 0, 0" to ensure compatibility with future devices.

Figure 4: Mode Register Definition

Table 3. Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	-	-	A0		
	-	-	0	0-1	0-1
	-	-	1	1-0	1-0
4	-	A1	A0		
	-	0	0	0-1-2-3	0-1-2-3
	-	0	1	1-2-3-0	1-0-3-2
	-	1	0	2-3-0-1	2-3-0-1
	-	1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page (y)	n = A0-A12/11/9 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3 Cn + 4... ...Cn - 1 Cn...	Not Supported

Notes:

1. For full-page accesses: y = 2,048
2. For BL = 2, A1–A9, A11 select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A9, A11 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A9, A-11 select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A9, A11 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A9, A11 select the unique column to be accessed, and mode register bit M3 is ignored.

CAS Latency (CL)

CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n* and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, as shown in Figure 5, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs start driving after T1 and the data will be valid by T2. Table 4 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

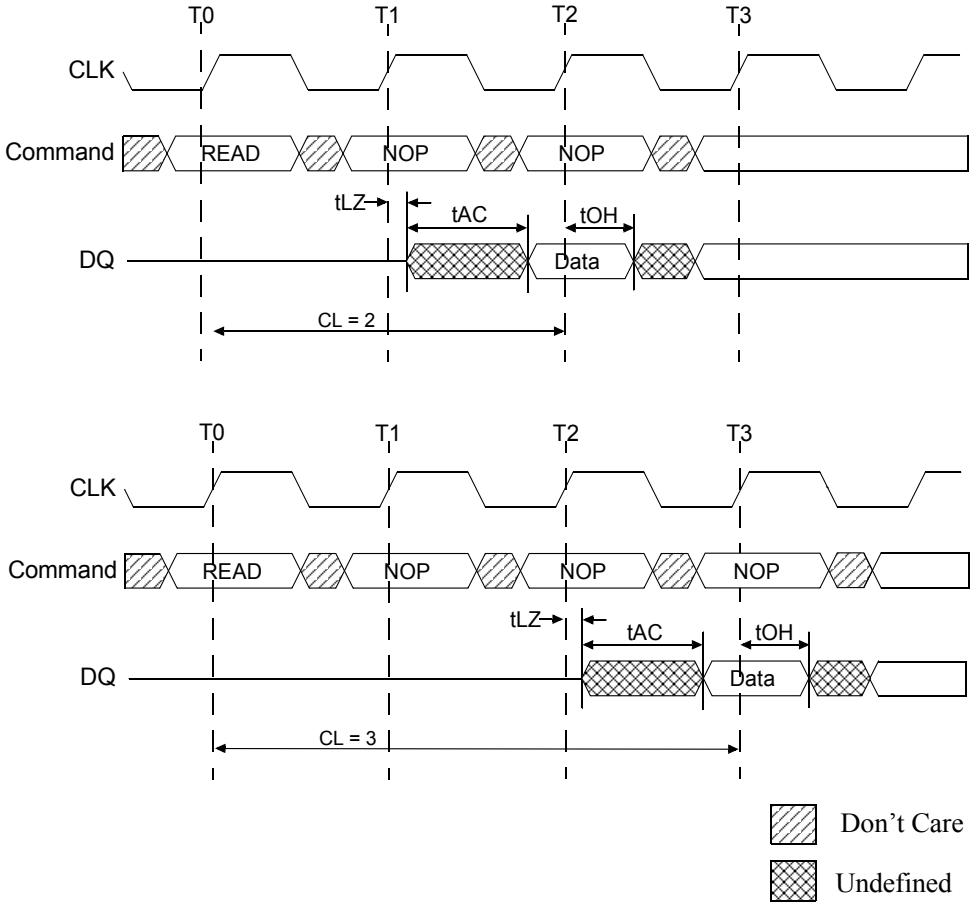


Figure 5: CAS Latency

Table 4. CAS Latency

Allowable Operating Frequency (MHz)	
Frequency	**Latency**
≤ 100	**CL = 2**

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

WRITE Burst Mode

When M9 = 0, BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ burst, but write accesses are single-location (nonburst) accesses.

COMMANDS

Table 5 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear in the Operations section; these tables provide current state/next state information.

Table 5: Truth Table 1 Commands and DQM Operation

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	Address	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/ row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/ col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/ col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	4
Write enable/output enable	--	--	--	--	L	--	Active	8
Write inhibit/output High-Z	--	--	--	--	H	--	High-Z	8

Notes:

1. CKE is HIGH for all commands shown.
2. A0–A11 define the op-code written to the mode register, and A12 should be driven LOW.
3. A0–A12 provide row address, and BA0, BA1 determine which bank is made active.
4. A0–A9, A11 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM that is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11 (A12 should be driven LOW). See "Mode Register" on page 13. The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank and the address provided on inputs; A0–A9, A11 selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs provides valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9, A11 selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access at a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is non-persistent in that it is either enabled or disabled for each individual READ or WRITE command.
Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operations section.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the "Operations" section on page 17. The BURST TERMINATE command does not precharge the row; the row will remain open until a PRECHARGE

command is issued.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum tRP has been met after the PRECHARGE command as shown in the Operations section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 512Mb SDRAM requires 8,192 AUTO REFRESH cycles every 32ms (tREF). Providing a distributed AUTO REFRESH command every 3.9µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRC), once every 32ms.

OPERATIONS

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command which selects both the bank and the row to be activated (see Figure 6).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 7, which covers any case where $2 < t\text{RCD (MIN)}/t\text{CK} \leq 3$ (the same procedure is used to convert other specification limits from time units to clock cycles). A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

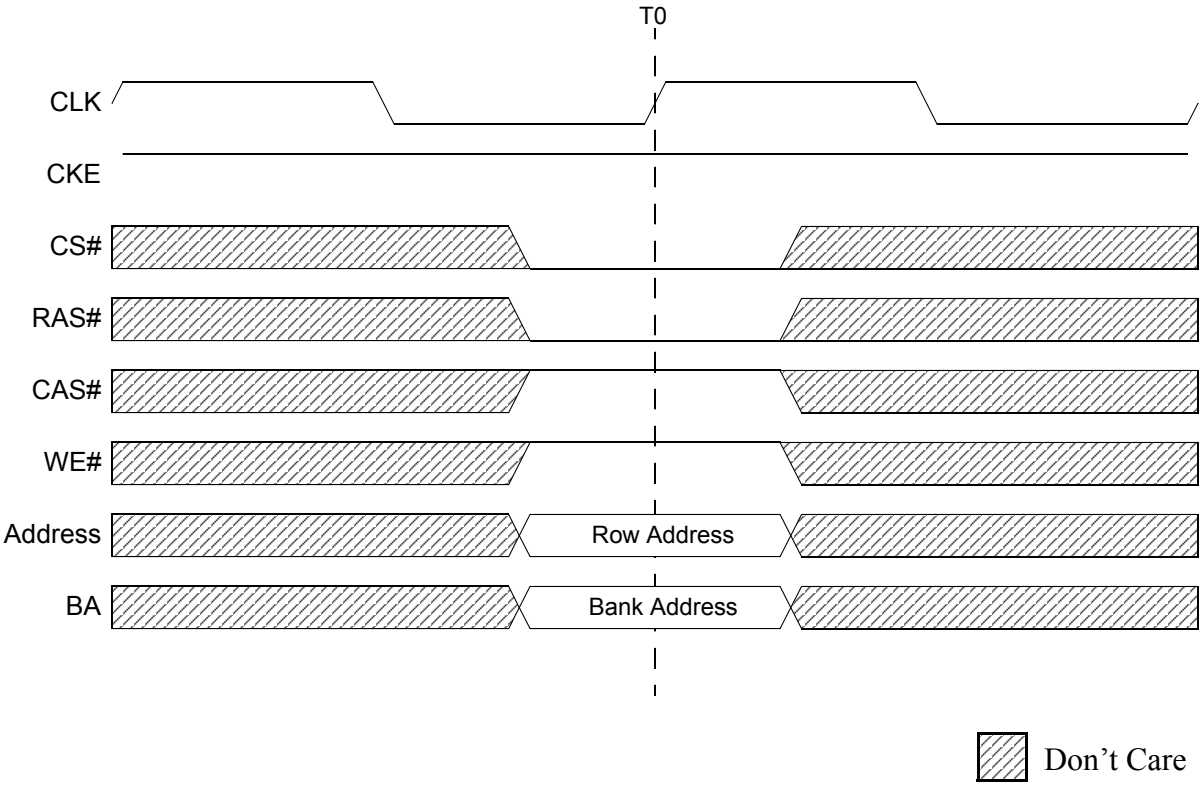


Figure 6: Activating a Specific Row in a Specific Bank

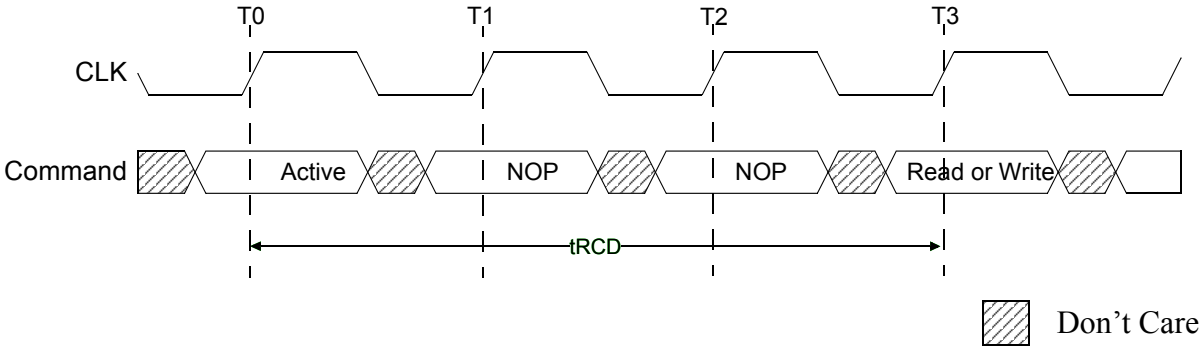


Figure 7: Example Meeting $^{t}_{RCD}$ (MIN) when 2 < $^{t}_{RCD}$ (MIN)/tCK ≤ 3

READs

READ bursts are initiated with a READ command, as shown in Figure 8.

The starting column and bank addresses are provided with the READ command, and auto precharge either is enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 9 on page 20 shows general timing for each possible CL setting.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

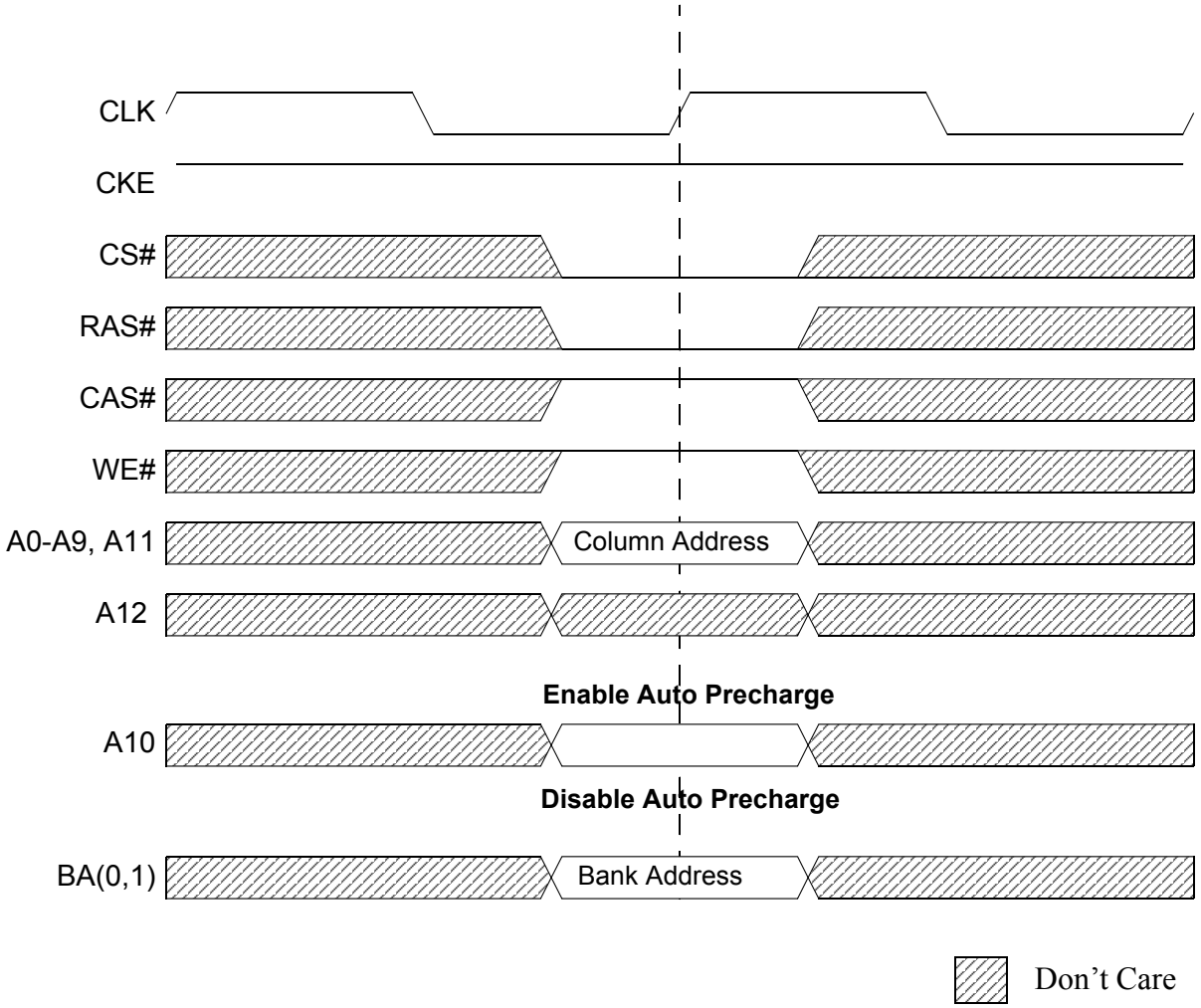


Figure 8: READ Command

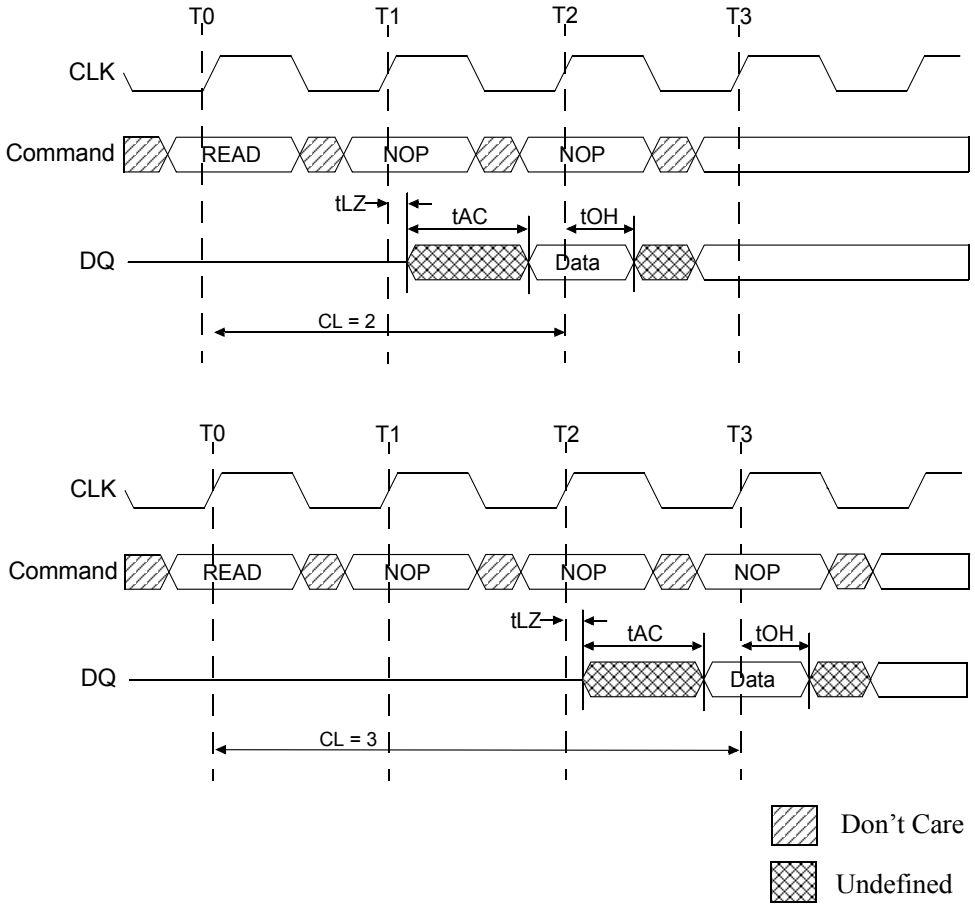


Figure 9: CAS Latency

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated (at the end of the page, it wraps to the start address and continue). Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command.

In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid where *x* = CL - 1. This is shown in Figure 9 for CL = 2 and CL = 3; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst.

The SDRAM uses a pipelined architecture and, therefore, does not require the 2*n* rule associated with a pre-fetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 11, or each subsequent READ may be performed to a different bank.

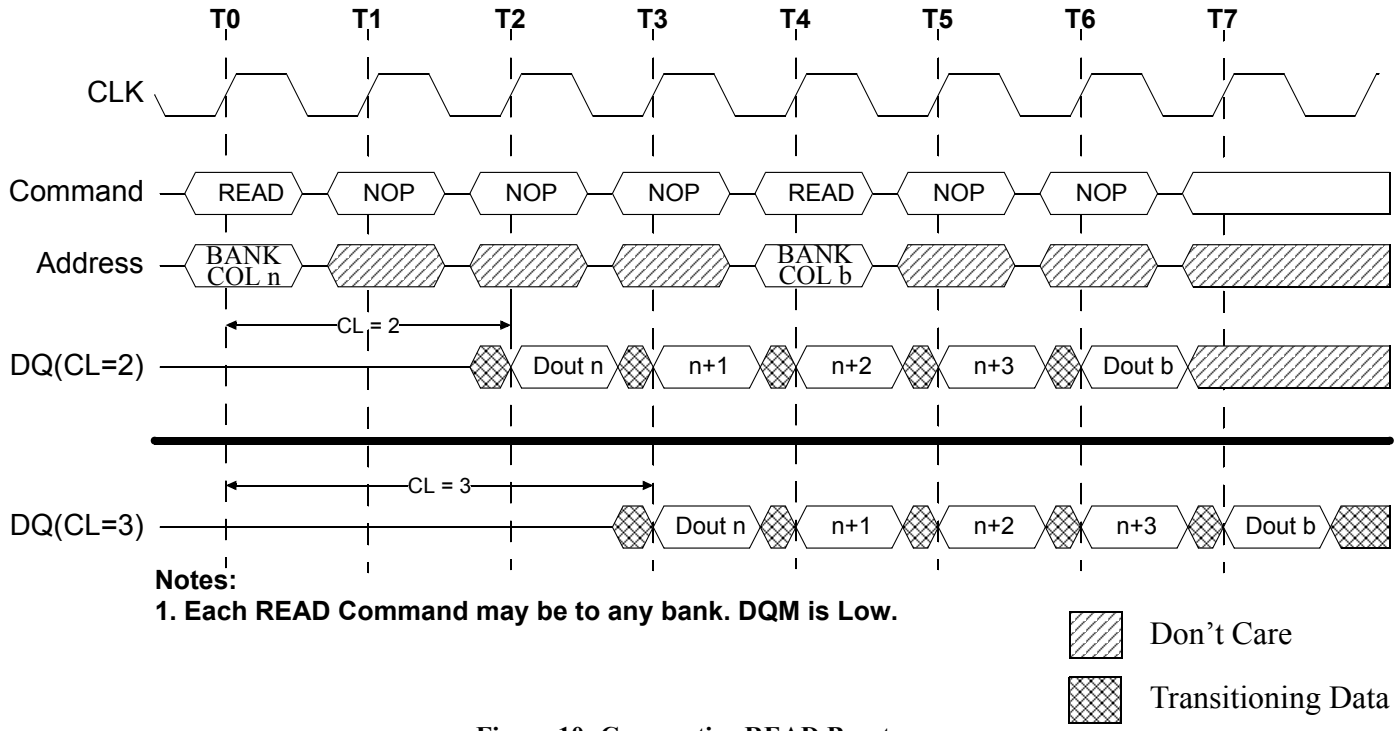


Figure 10: Consecutive READ Bursts

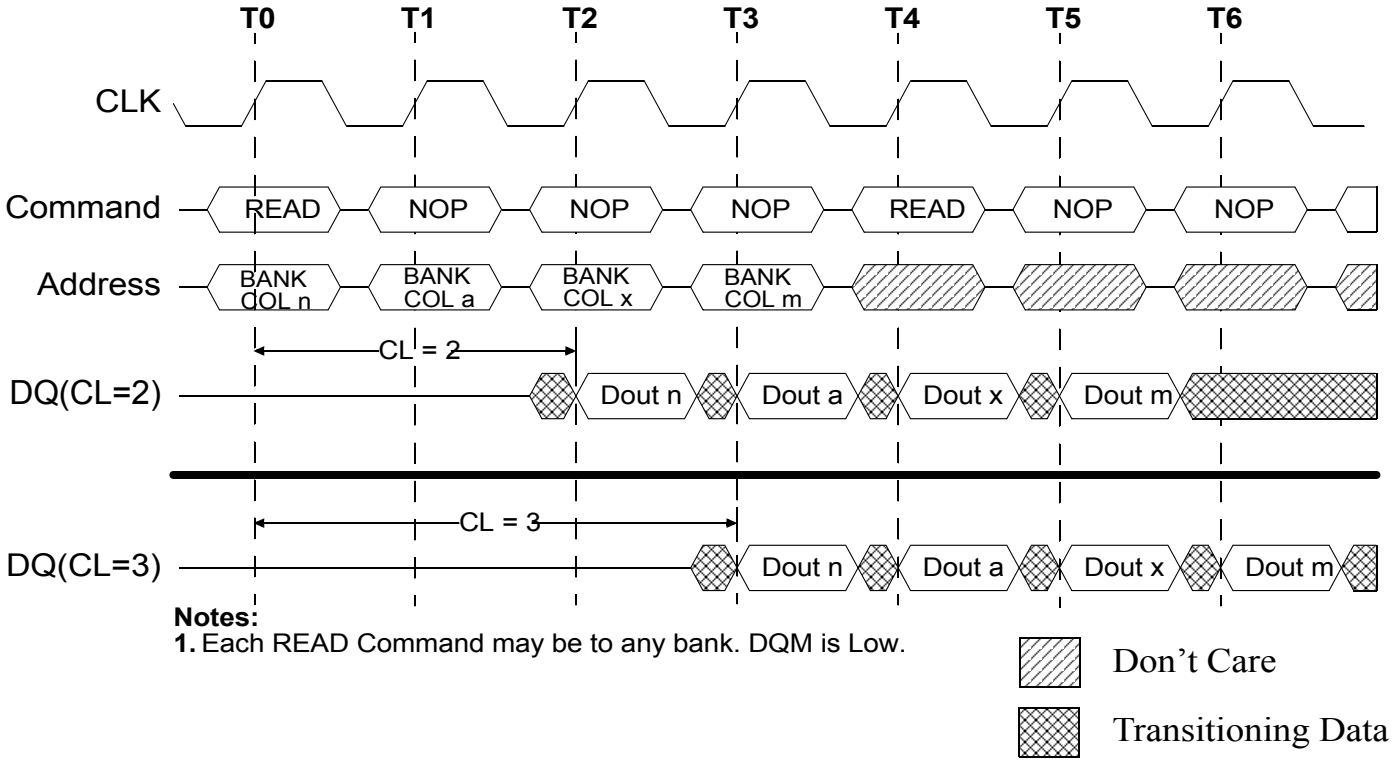
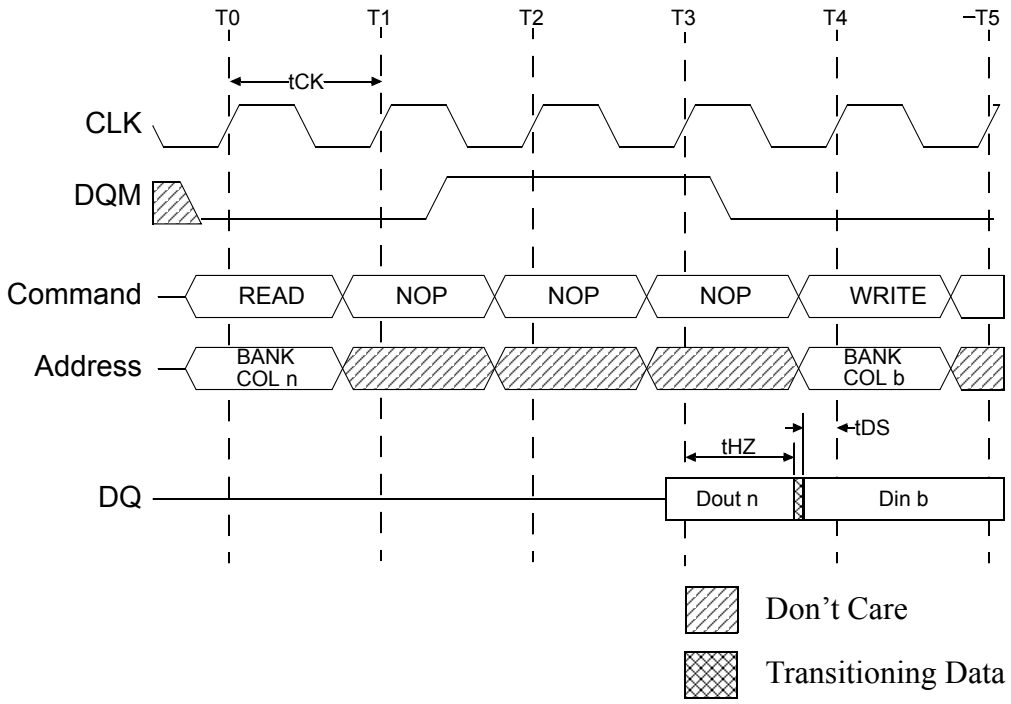


Figure 11: Random READ Accesses

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

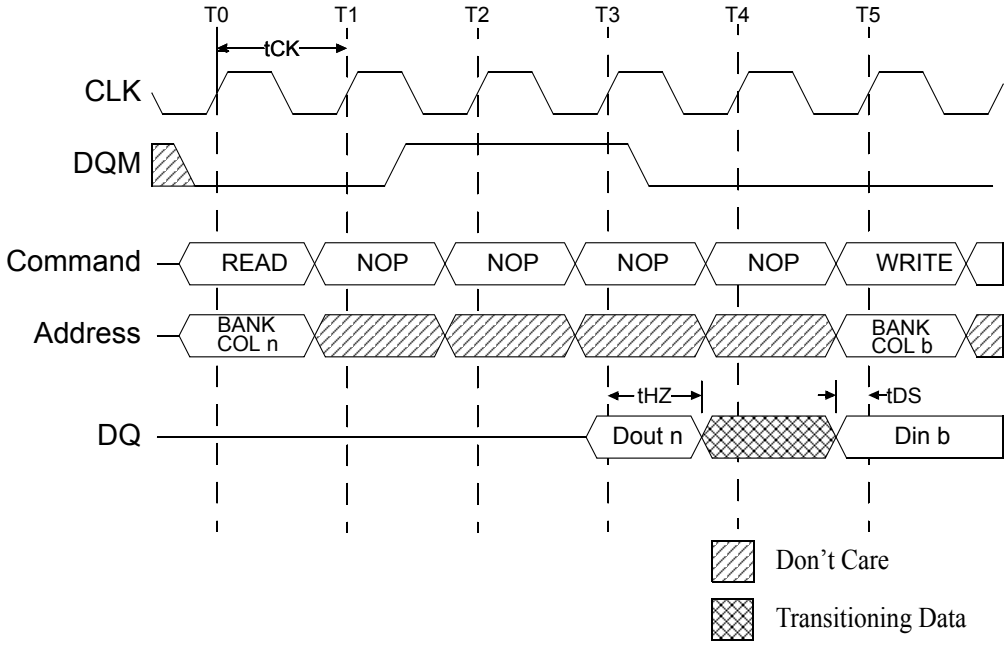
The DQM input is used to avoid I/O contention, as shown in Figure 12 and Figure 13. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress dataout from the READ. After the WRITE command is registered, the DQs go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 in Figure 13, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 12 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 13 shows the case where the additional NOP is needed.



Notes:
1. CL = 3 is used for illustration. The READ or WRITE Command may be to any bank. If a burst of one is used, DQM is not required.

Figure 12: READ-to-WRITE



Notes:

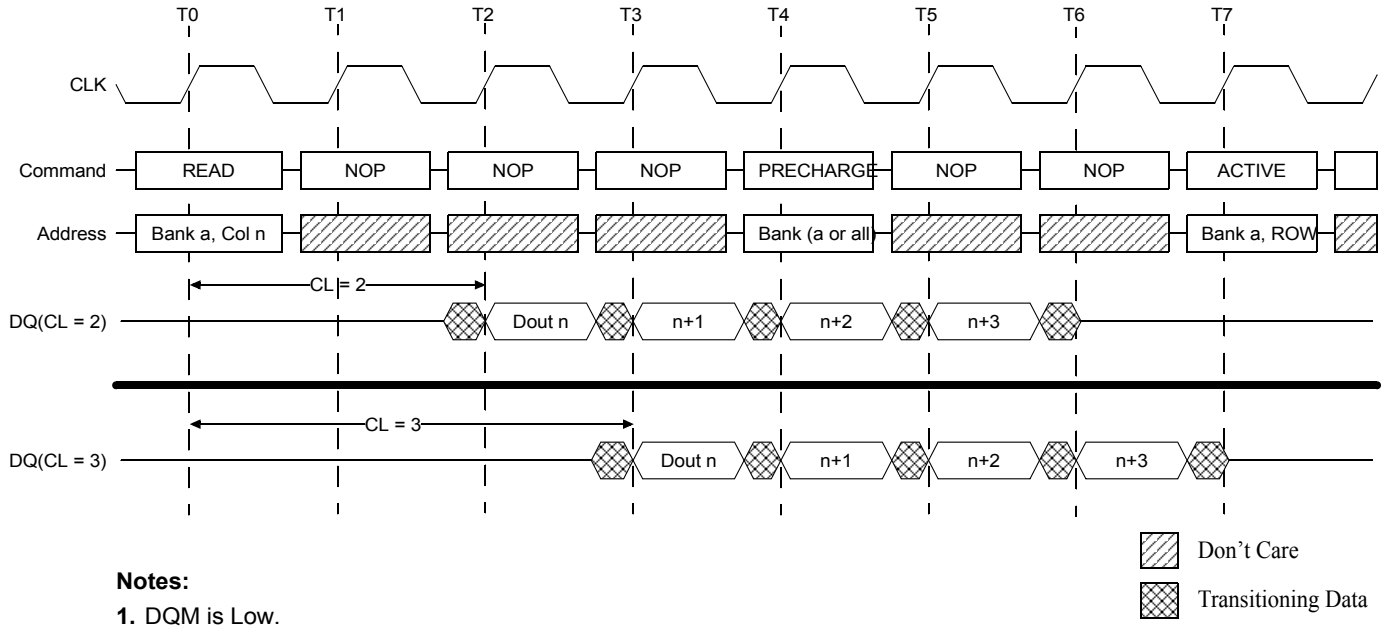
1. CL = 3 is used for illustration. The READ or WRITE Command may be to any bank. If a burst of one is used, DQM is not required

Figure 13: READ-to-WRITE with Extra Clock Cycle

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGEcommand to the same bank (provided that auto precharge was not activated), and a full page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 14 for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. **Note:** Part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is it can be used to truncate fixed-length or full-page bursts.

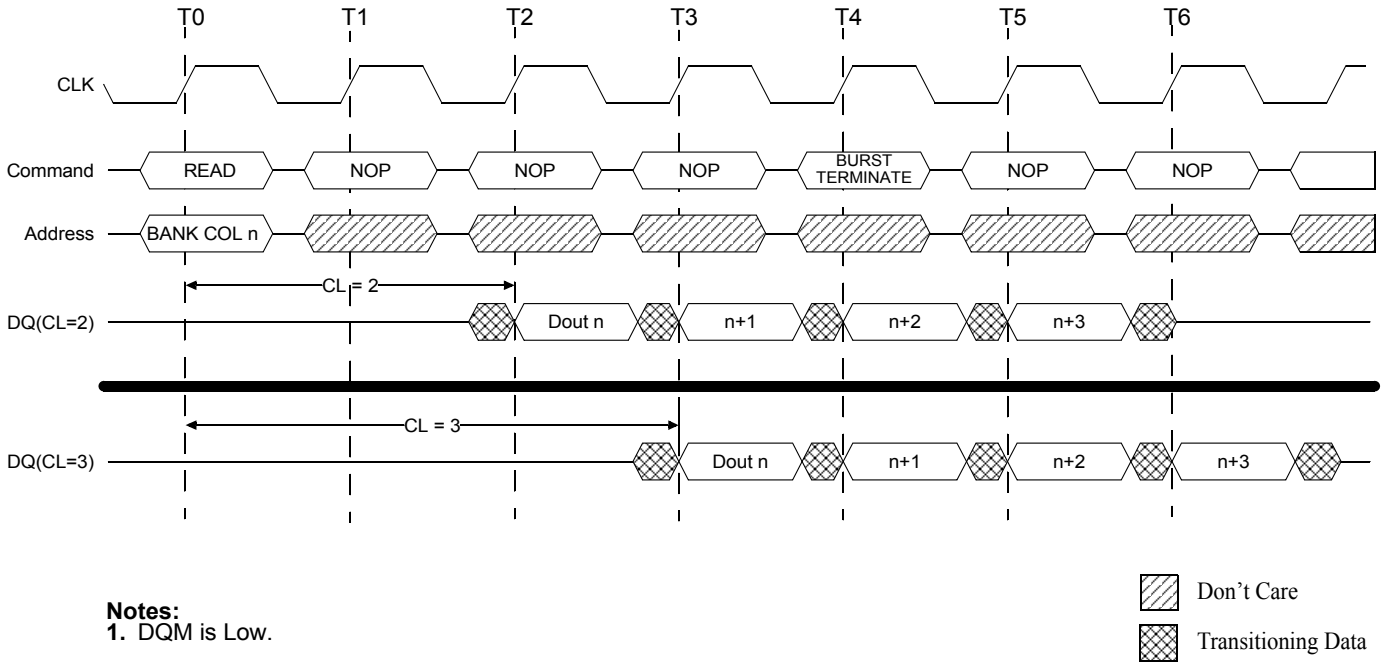
Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 15 for each possible CL; data element *n* + 3 is the last desired data element of a longer burst.



Notes:

1. DQM is Low.

Figure 14: READ-to-PRECHARGE



Notes:

1. DQM is Low.

Figure 15: Terminating a READ Burst

WRITES

WRITE bursts are initiated with a WRITE command, as shown in Figure 16.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs remains High-Z and any additional input data will be ignored (see Figure 17 on page 26). A full-page burst will continue until terminated (at the end of the page, it will wrap to the start address and continue). Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 18. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. The 512Mb SDRAM uses a pipelined architecture and, therefore, does not require the 2*n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 19, or each subsequent WRITE may be performed to a different bank.

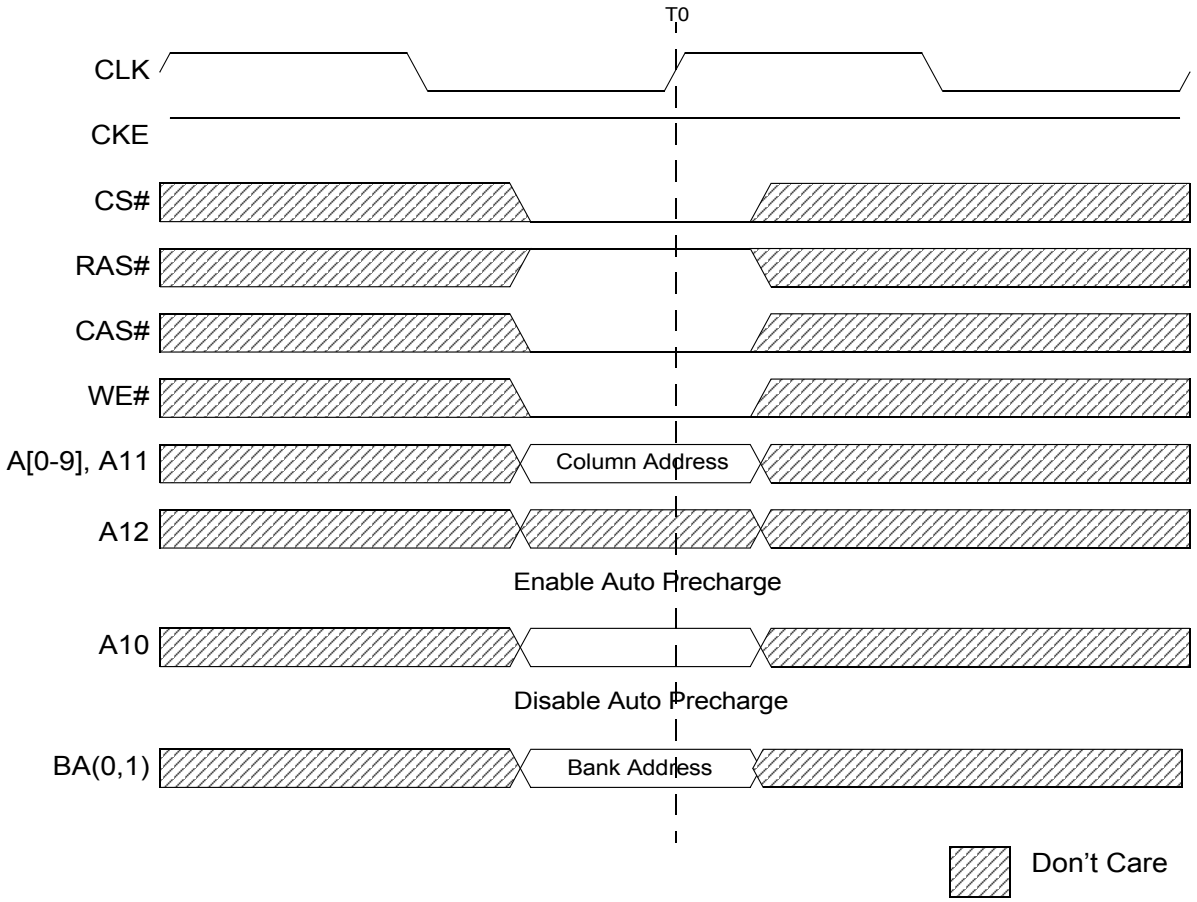
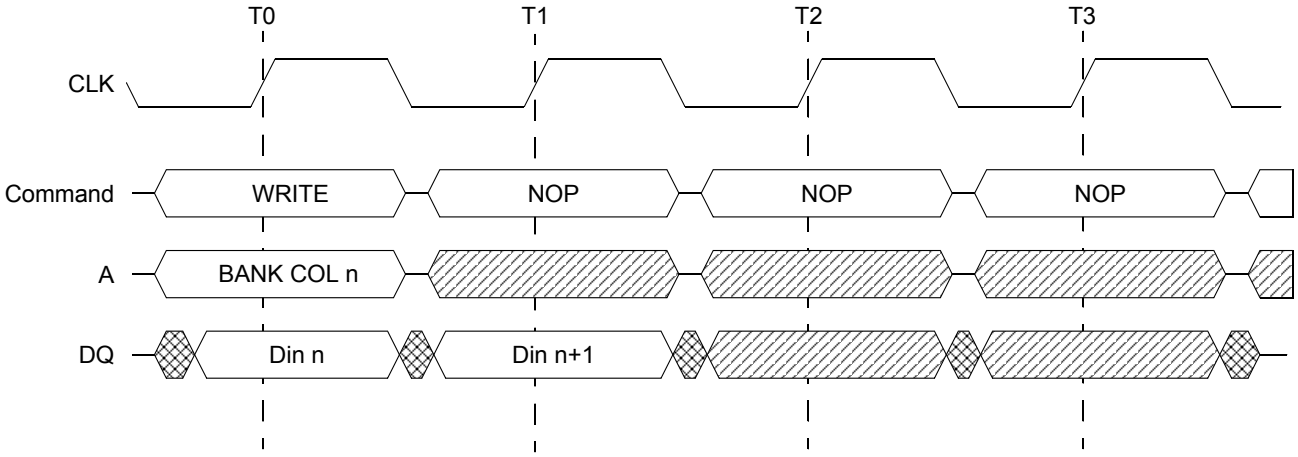


Figure 16: Write Command

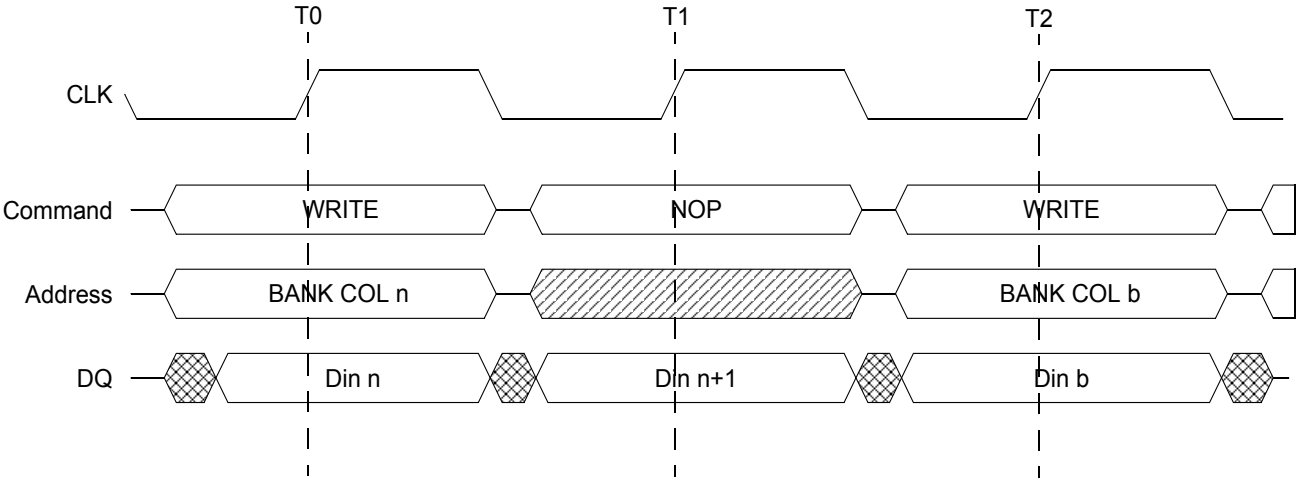


Notes:
1. BL = 2. DQM is Low.

Don't Care

Transitioning Data

Figure 17: WRITE Burst



Notes:
1. DQM is LOW. Each WRITE command may bo to any bank.

Don't Care

Transitioning Data

Figure 18: WRITE-TO-WRITE

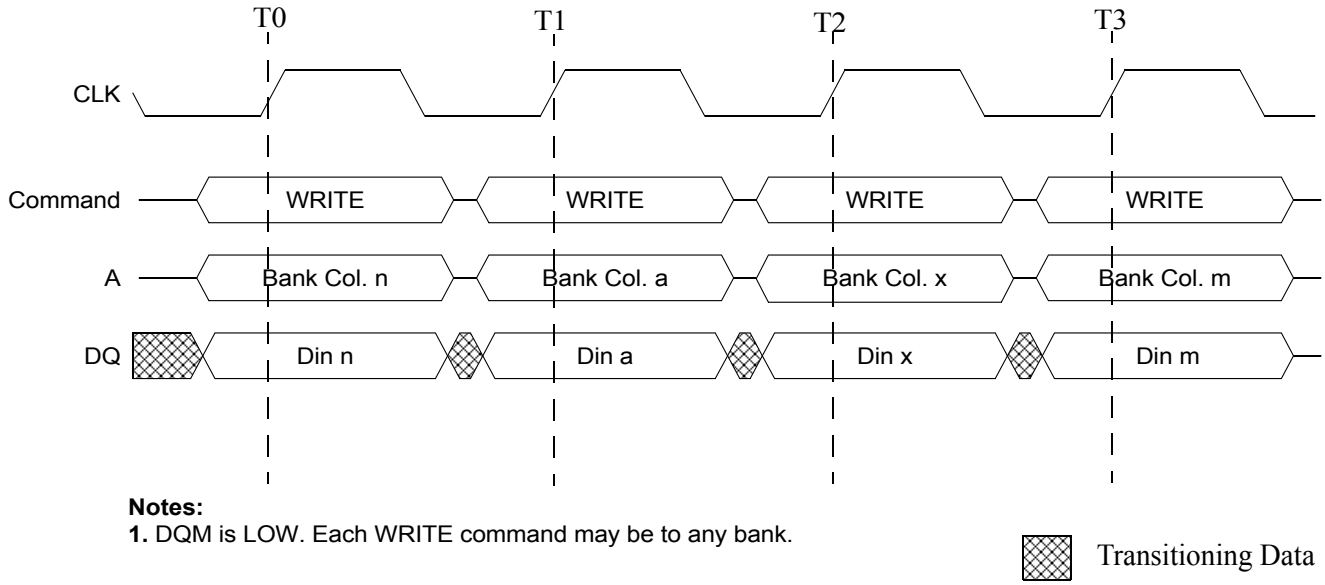


Figure 19: Random WRITE Cycles

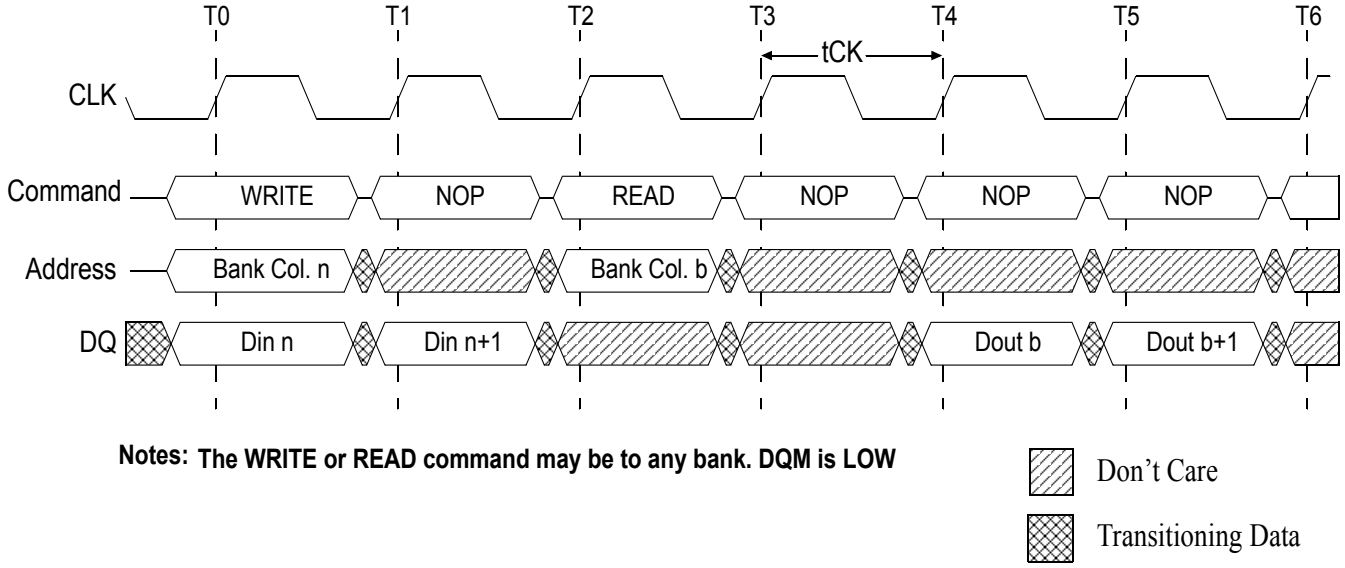
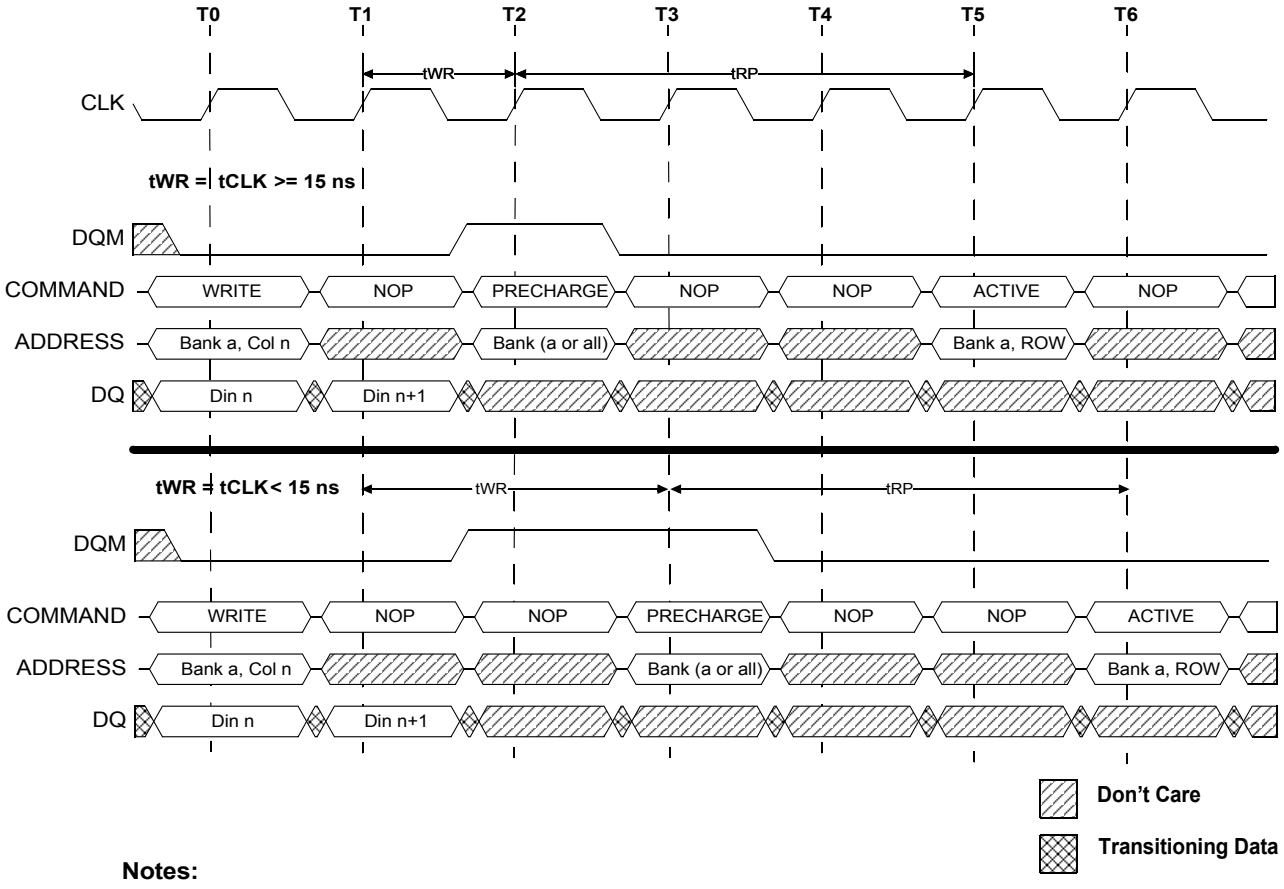


Figure 20: WRITE-to-READ

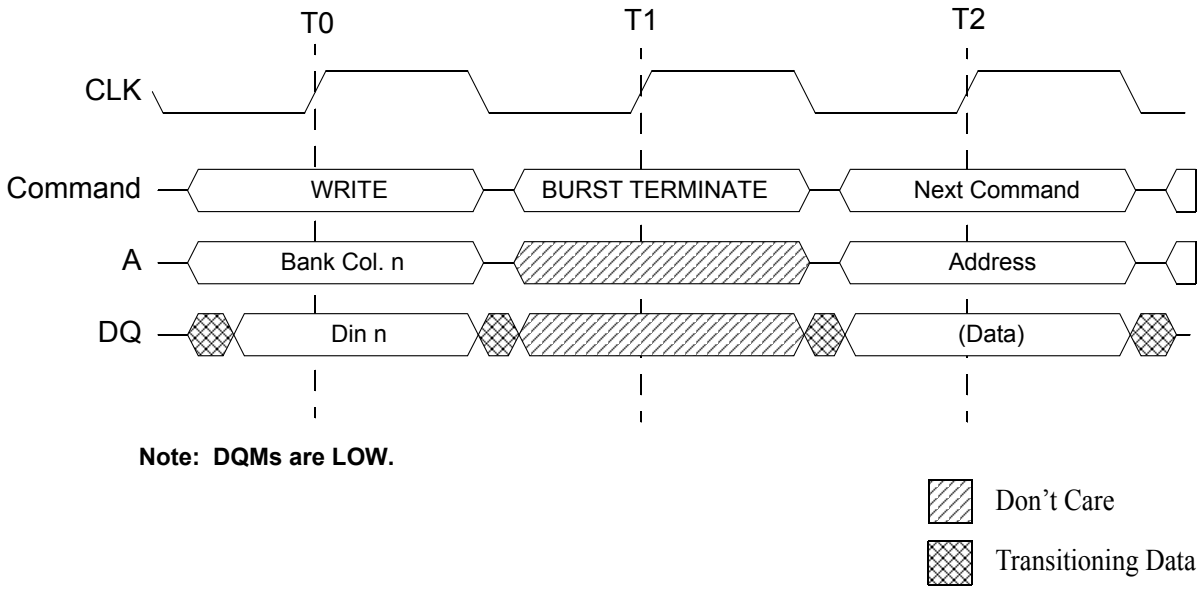
Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued tWR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a tWR of at least one clock plus time, regardless of frequency. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 21. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The precharge can be issued coincident with the first coincident second clock (Figure 21). In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 22, where data *n* is the last desired data element of a longer burst.



Notes:

1. **DQM could remain low in this example if the write burst is a fixed length of two.**

Figure 21: WRITE-to-PRECHARGE



Note: DQMs are LOW.

Figure 22: Terminating a WRITE Burst

Precharge

The PRECHARGE command shown in Figure 23 is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access at the specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

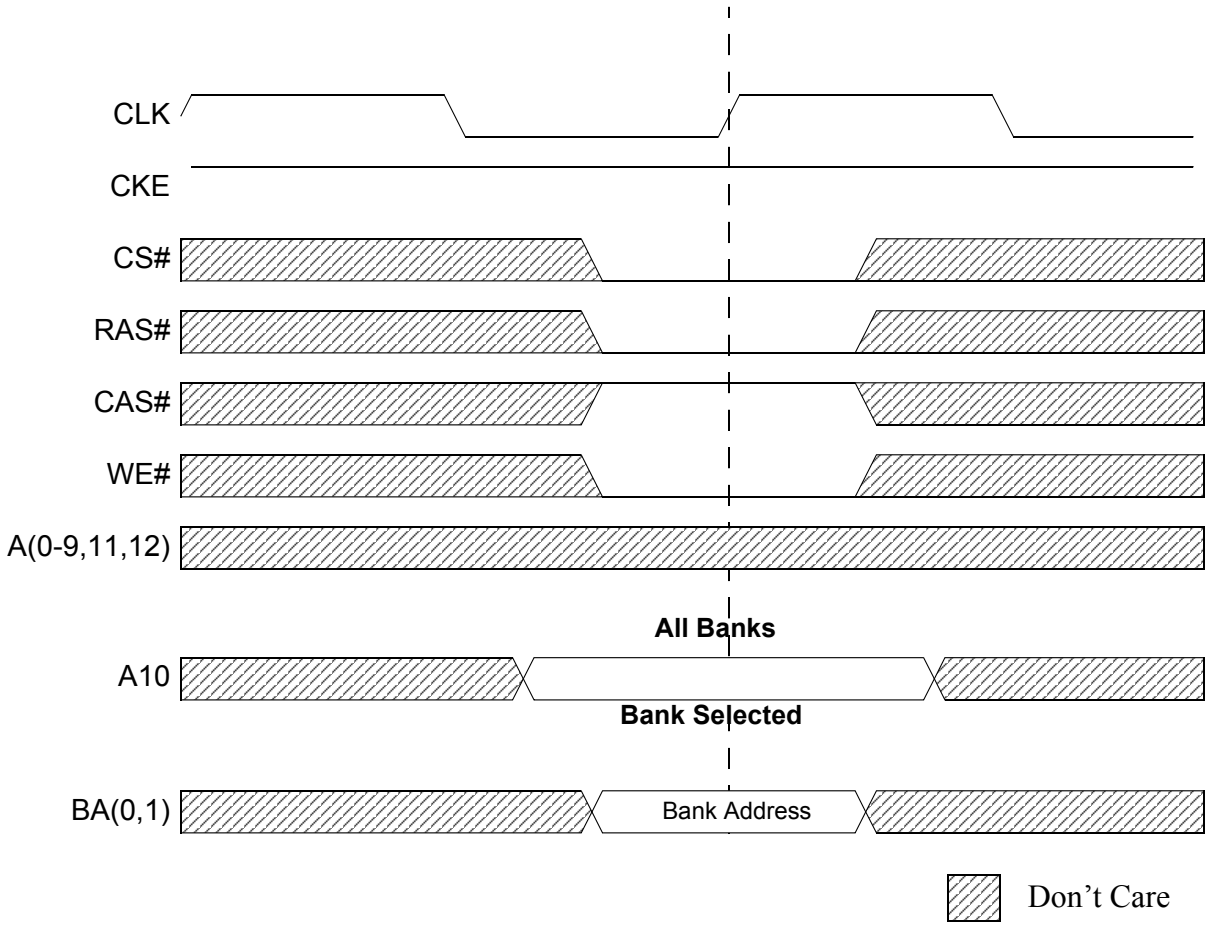


Figure 23: PRECHARGE Command

Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximumpower savings while in standby. The device may not remain in the power-down state longer than the refresh period (32ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting tCKS). See Figure 24.

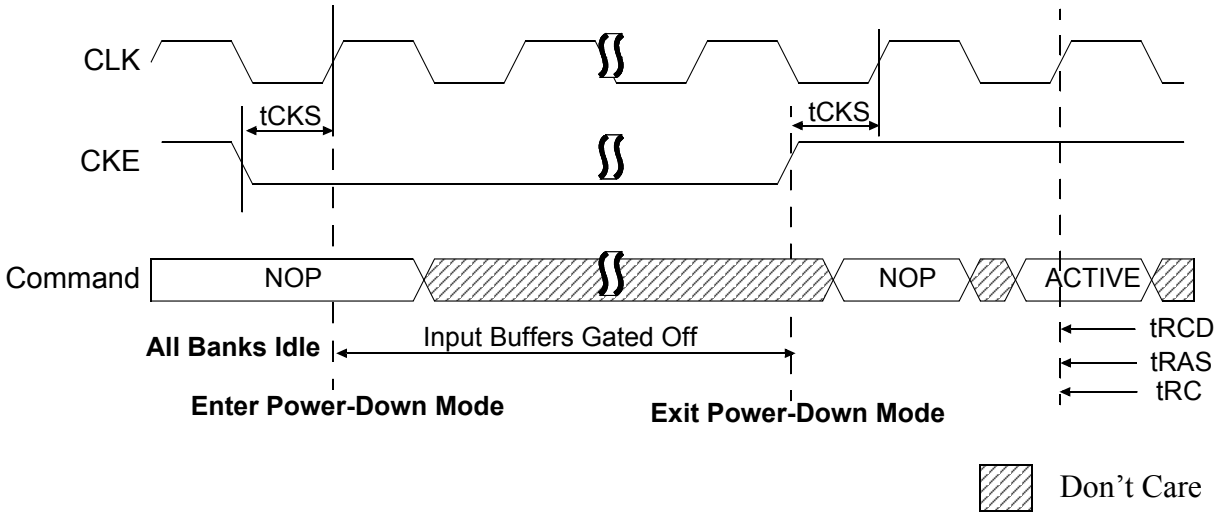


Figure 24: POWER-DOWN

Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven. Burst counters are not incremented, as long as the clock is suspended (see examples in Figures 25 and 26).
Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation resumes on the subsequent positive clock edge. The device may not remain in clock suspend state longer than the refresh period (32ms) since no refresh operations are performed in this mode.

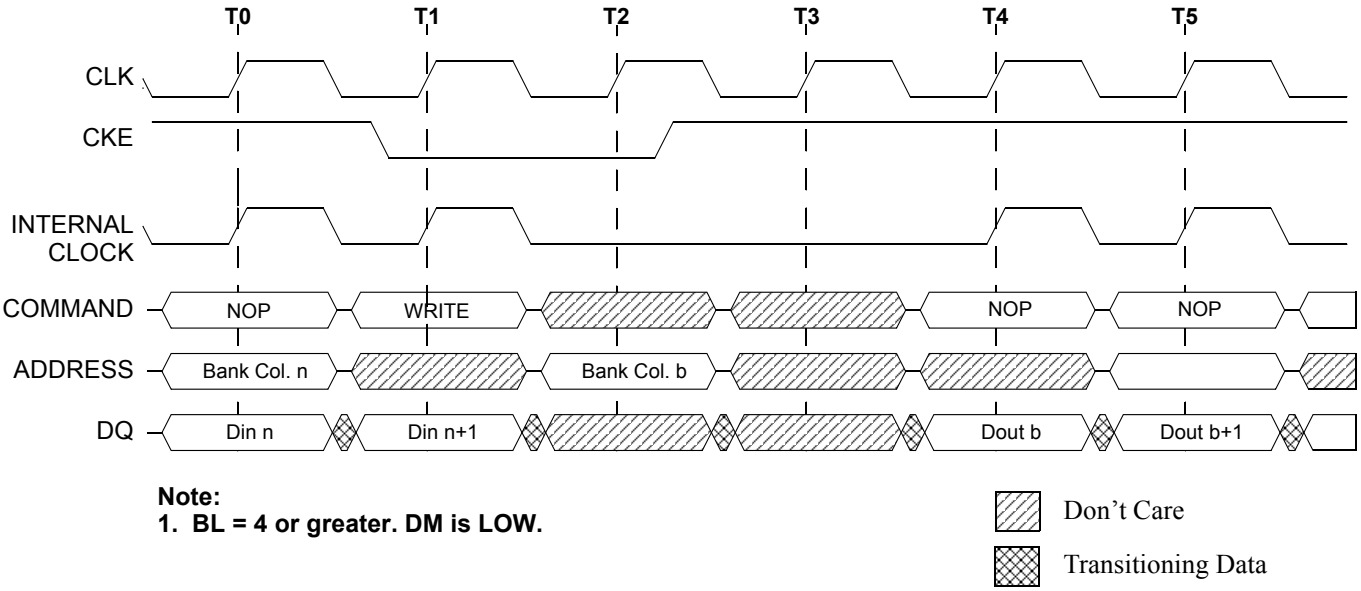


Figure 25: CLOCK SUSPEND During WRITE Burst

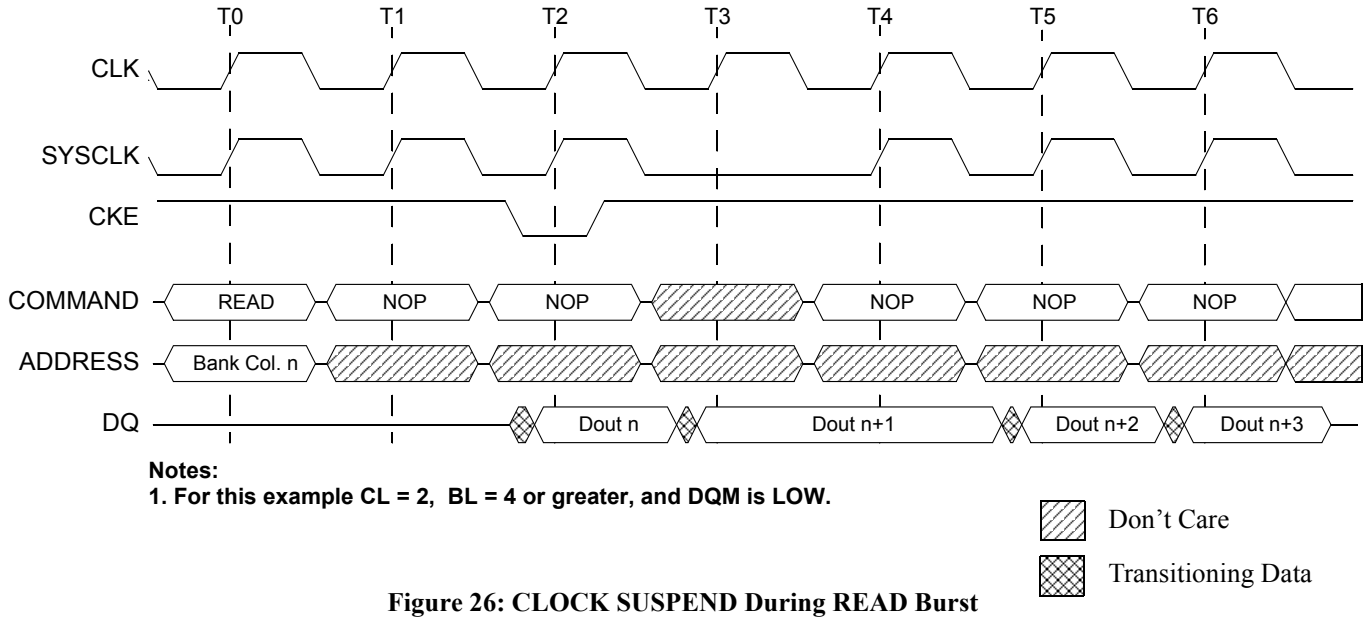


Figure 26: CLOCK SUSPEND During READ Burst

Burst READ/Single WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

Concurrent Auto Precharge

An access command to (READ or WRITE) another bank, while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports concurrent auto precharge. SDRAMs support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined below.

READ with Auto Precharge

Interrupted by a READ (with or without auto precharge): A READ to bank *m* interrupts a READ on bank *n*, CL later. The PRECHARGE to bank *n* begins when the READ to bank *m* is registered (see Figure 28).

Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* interrupts a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begins when the WRITE to bank *m* is registered (see Figure 29).

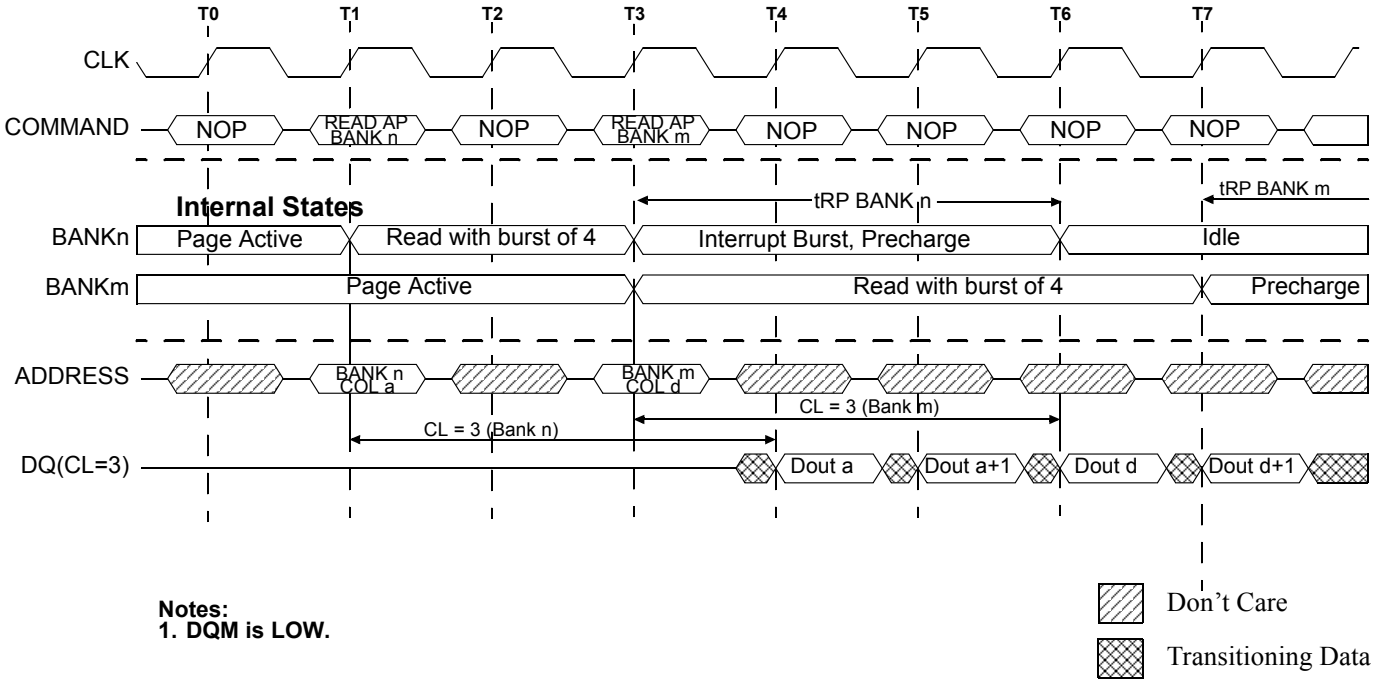
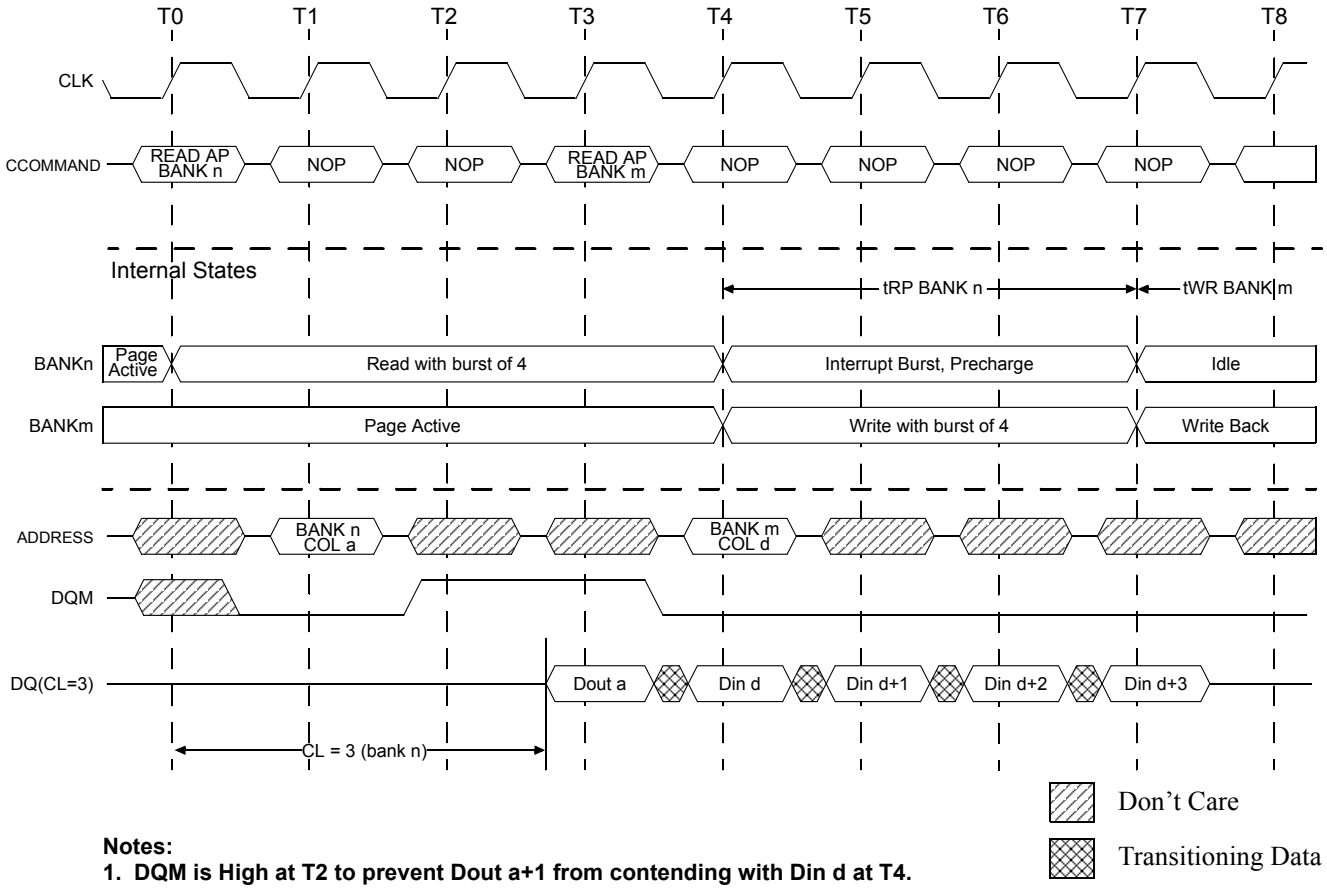


Figure 27: READ with Auto Precharge Interrupted by a READ



Notes:
1. DQM is High at T2 to prevent Dout a+1 from contending with Din d at T4.

Figure 28: READ with Auto Precharge Interrupted by a WRITE

Data for any WRITE burst may be truncated with a subsequent READ comment, and data for a fixed-length WRITE burst may be immediately followed by a READ command. After the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown. Data n+1 is either the last of a burst of two or the latest desired of a longer burst.

WRITE with Auto Precharge

Interrupted by a READ (with or without auto precharge): A READ to bank *m* interrupts a WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* begins after tWR is met, where tWR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 29).

Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* interrupts a WRITE on bank *n* when registered. The PRECHARGE to bank *n* begins after tWR is met, where tWR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 30).

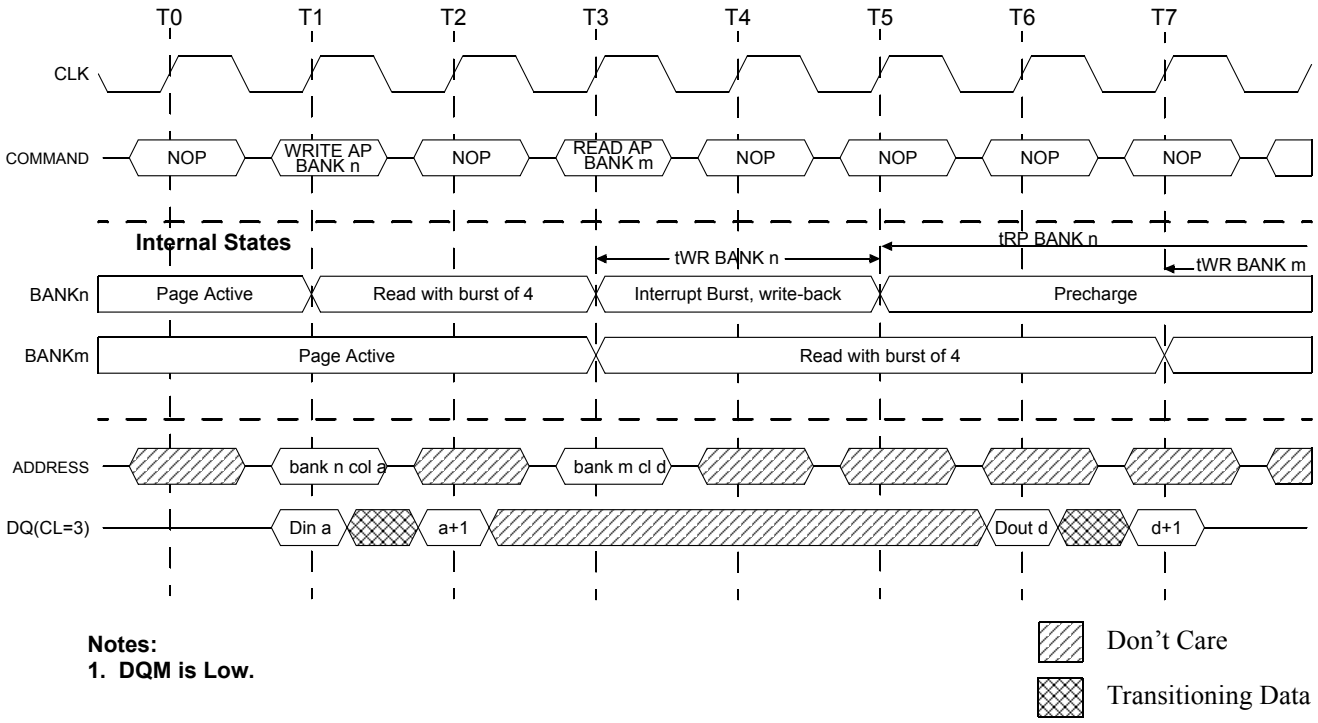


Figure 29: WRITE with Auto Precharge Interrupted by a READ

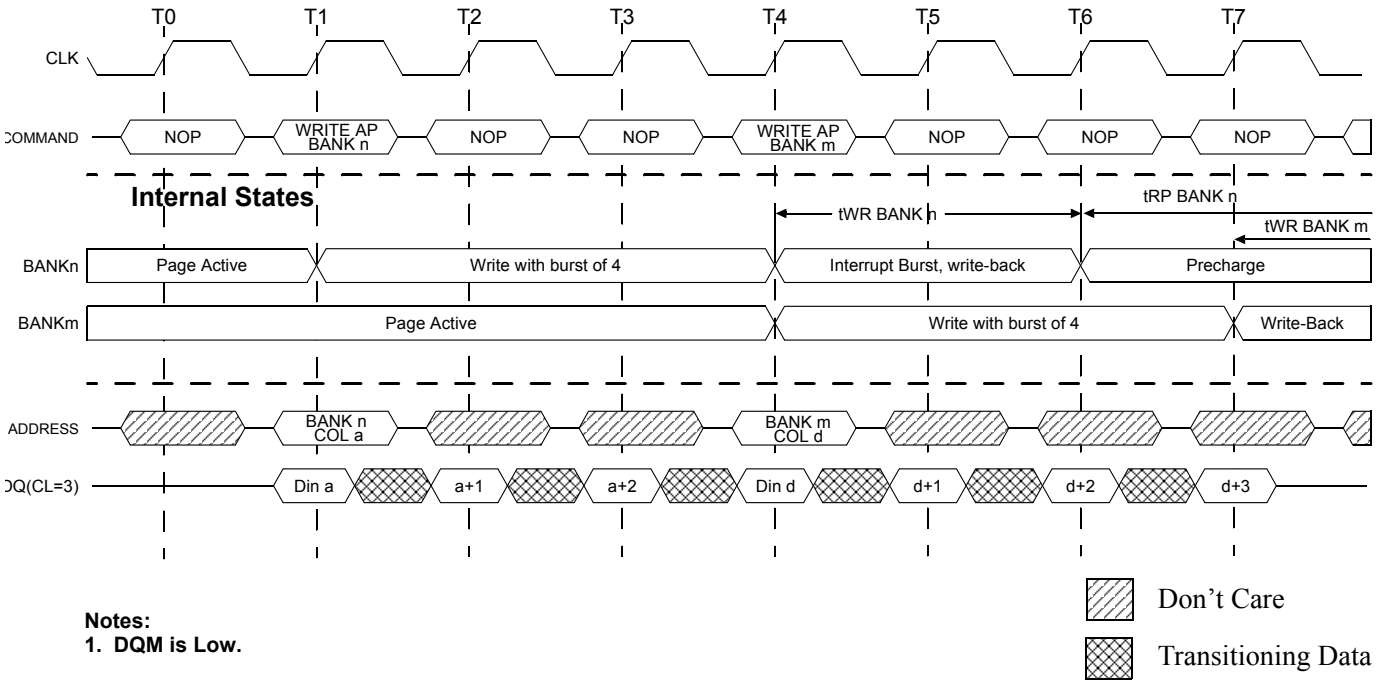


Figure 30: WRITE with Auto Precharge Interrupted by a WRITE

Table 6: Truth Table 2 - CKE
Notes 1-4 apply to entire table; Notes appear below.

CKE_{n-1}	CKE_n	Current State	$COMMAND_n$	$ACTION_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Clock suspend	X	Maintain clock suspend	
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Clock suspend	X	Exit clock suspend	6
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All banks idle	AUTO REFRESH		
		Reading or writing	VALID	Clock suspend entry	
H	H		See Table 7		

Notes:
1. CKEn is the logic state of CKE at clock edge *n*; CKEn - 1 was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that tCKS is met).
6. After exiting clock suspend at clock edge n, the device resumes operation and recognize the next command at clock edge *n* + 1.

Table 7: Truth Table 3 - Current State Bank *n*, Command to Bank *n*

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activiate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

Table 7: Truth Table 3 - Current State Bank *n*, Command to Bank *n*

Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

Notes:

1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH (see Table 7) and after tXSR has been met.
2. This table is bank-specific (except where noted) the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and tRP has been met.
   - Row active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 7 and according to Table 8.
   - Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank will be in the idle state.
   - Row activating: Starts with registration of an ACTIVE command and ends when tRCD is met. After tRCD is met, the bank will be in the row active state.
   - Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.
   - Write w/auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. After tRC is met, the SDRAM will be in the al banks idle state.
   - Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. After tMRD is met, the SDRAM will be in the all banks idle state.
   - Precharging all: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. After tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

Table 8: Truth Table 4 - Current State Bank *n*, Command to Bank *m*

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:

1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH (see Table 6) and after tXSR has been met.
2. This table describes alternate bank operation, except where noted; that is, the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminate

   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled, and ends when tRP has been met. After tRP is met, the bank will be in the idle state.

   Write with autoprecharge enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when tRP has been met. After tRP is met, the bank will be in the idle state.

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* initiates the auto precharge command when its burst has been interrupted by bank *m*'s burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* interrupts the READ on bank *n*, CL later (Figure 10).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupts the READ on bank *n* when registered (Figure 12 and Figure 13). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m*interrupst the WRITE on bank *n* when registered (Figure 20), with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupts the WRITE on bank *n* when registered (Figure 18). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m*interrupts the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 27).
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupts the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 28).
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m*interrupts the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after tWR is met, where tWR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be datain registered one clock prior to the READ to bank *m* (Figure 29).
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m*interrups the WRITE on bank *n* when registered. The PRECHARGE to bank *n* begins after tWR is met, where tWR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock prior to the WRITE to bank *m* (Figure30).

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
$V_{DD\ and}\ V_{DDQ}$	DC supply voltage	-1.0 to +4.3V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3 to V_{DD} +0.3V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	5W
T_J	Maximum junction temperature	+125°C
Θ_{JC}	Thermal resistance, junction-to-case	TBD°C/W

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
$V_{DD\ and}\ V_{DDQ}$	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-40 to 105°C
V_{IN}	DC input voltage	0V to V_{DDQ}

OPERATIONAL ENVIRONMENT SPECIFICATIONS

TOTAL DOSE	100K	RAD(SI)
Heavy Ion Event Rate[2]	1.1 E-10	Events/Bit-Day

DC Electrical Characteristics and Operating Conditions (Pre/Post-Radiation)*

Notes 1, 4, and 5 apply to entire table. (V_{DD}, V_{DDQ} = +3.3V +/-0.3V; Unless otherwise noted, Tc is per temperature range ordered.)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high voltage: Logic 1; All inputs	V_{IH}	2		V	
Input low voltage: Logic 0; All inputs	V_{IL}		0.8	V	
Input leakage current: Any input 0V≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-5	5	µA	
Output leakage current: DQs are disabled; 0V < V_{OUT} < V_{DDQ}	I_{OZ}	-5	5	µA	
Output levels: Output high voltage (IOUT = -4mA)	V_{OH}	2.4	--	V	
Output low voltage (IOUT = 4mA)	V_{OL}	--	0.4	V	

I_{DD} Specifications and Conditions (Pre/Post-Radiation)*

Notes 1, 4, 5, 9, and 11 apply to entire table. (V_{DD}, V_{DDQ} = +3.3V +/-0.3V; Unless otherwise noted, Tc is per temperature range ordered.)

Parameter/Condition		Symbol	Max		Units	Notes
			x40	x48		
Operating current: active mode; Burst = 2; READ or WRITE; t_{RC} = t_{RC} (MIN)		$I_{DD}1$	600	720	mA	3, 12, 13, 15
Standby current: power-down mode; CKE = LOW; All banks idle		$I_{DD}2$	17.5	21	mA	15
Standby current: active mode; CS# = HIGH CKE = HIGH; All banks active after t_{RCD} met; No accesses in progress		$I_{DD}3$	225	270	mA	3, 10,13, 15
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		$I_{DD}4$	625	750	mA	3, 12, 13, 15
Auto refresh current: CS# = HIGH; CKE = HIGH	t_{RFC} = t_{RFC} (MIN)	$I_{DD}5$	1300	1300	mA	3, 12, 13, 15, 16
	t_{RFC} =3.9 µs	$I_{DD}6$	30	36	mA	

Capacitance

Notes 2 apply to entire table

Parameter	Condition	Symbol	Max	Units
Input capacitance: All other input-only pins	f=1MHz @ 0V C_{IN}	Cl_1	TBD	pF
Input/output capacitance: DQs	f=1MHz @ 0V C_{IO}	Cl_1	TBD	pF

AC CHARACTERISTICS and RECOMMENDED OPERATING CONDITIONS (Pre/Post-Radiation)*

Notes 4, 5, 6, 7, 8 and 9 apply to entire table. (V_{DD}, V_{DDQ} = +3.3V +/-0.3V; Unless otherwise noted, Tc is per temperature range ordered.)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
$t_{AC(3)}$	Access time from CLK (positive edge) CL=3		5.4	ns	
$t_{AC(2)}$	Access time from CLK (positive edge) CL=2		6		
t_{AH}	Address hold time	0.8		ns	
t_{AS}	Address setup time	1.5		ns	
t_{CH}	CLK high-level width	2.5		ns	
t_{CL}	CLK low-level width	2.5		ns	
t_{CK3}	Clock cycle time CL=3	7.5		ns	
t_{CK2}	Clock cycle time CL = 2	10		ns	14
t_{CKH}	CKE hold time	0.8		ns	
t_{CKS}	CKE setup time	1.5		ns	
t_{CMH}	CS#, RS#, CAS#, WE#, DQM hold time	0.8		ns	
t_{CMS}	CS#, RS#, CAS#, WE#, DQM setup time	1.5		ns	
t_{DH}	Data-in hold time	0.8		ns	
t_{DS}	Data-in setup time	1.5		ns	
t_{HZ3}	Data-out High-Z time CL = 3		5.4	ns	
t_{HZ2}	Data-out High-Z time CL = 2		6.0	ns	
t_{LZ}	Data-out Low-Z time	1		ns	
t_{OH}	Data-out Hold time (load)	2.7		ns	
t_{OHN}	Data-out hold time (no load)	1.8		ns	
t_{RAS}	ACTIVE-to-PRECHARGE command	44	120,000	ns	
t_{RC}	ACTIVE-to-ACTIVE command period	66		ns	
t_{RCD}	ACTIVE-to-READ or WRITE delay		20	ns	
t_{REF}	Refresh period (8,192 rows)		32	ms	
t_{RFC}	AUTO REFRESH period	66		ns	
t_{RP}	PRECHARGE command period	20		ns	
t_{RRD}	ACTIVE bank a-to-ACTIVE bank b command	15		ns	
t_T	Transition time	0.3	1.2	ns	6
t_{WR}	WRITE recovery time	1 CLK + 7ns			
		15		ns	

AC Functional Characteristics (Pre/Post-Radiation)*

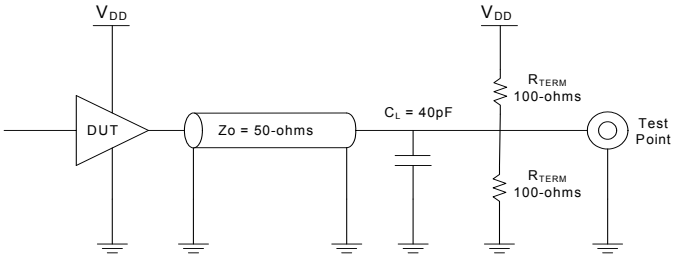
Notes 4, 5, 6, 7, 8, and 9apply to entire table. (V_{DD}, V_{DDQ} = +3.3V +/-0.3V; Unless otherwise noted, Tc is per temperature range ordered.)

PARAMETER	Symbol	x40	x48	Units	Notes
READ/WRITE command-to-READ/WRITE command	t_{CCD}	1	1	t_{CK}	
CKE to clock disable or power-down entry mode	t_{CKED}	1	1	t_{CK}	
CKE to clock enable or power-down exit setup mode	t_{PED}	1	1	t_{CK}	
DQM input data delay	t_{DQD}	0	0	t_{CK}	
DQM to data mask during WRITEs	t_{DQM}	0	0	t_{CK}	
DQM to data High-Z during READs	t_{DQZ}	2	2	t_{CK}	
WRITE command to input data delay	t_{DWD}	0	0	t_{CK}	
Data-in to ACTIVE command	t_{DAL}	5	5	t_{CK}	
Data-in to PRECHARGE command	t_{DPL}	2	2	t_{CK}	
Last data-in to burst STOP command	t_{BDL}	1	1	t_{CK}	
Last data-in to new READ/WRITE command	t_{CDL}	1	1	t_{CK}	
Last data-in to PRECHARGE command	t_{RDL}	2	2	t_{CK}	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	t_{MRD}	2	2	t_{CK}	
Dataout to High-Z form PRECHARGE command	$t_{ROH(3)}$	3	3	t_{CK}	
	$t_{ROH(2)}$	2	2	t_{CK}	

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

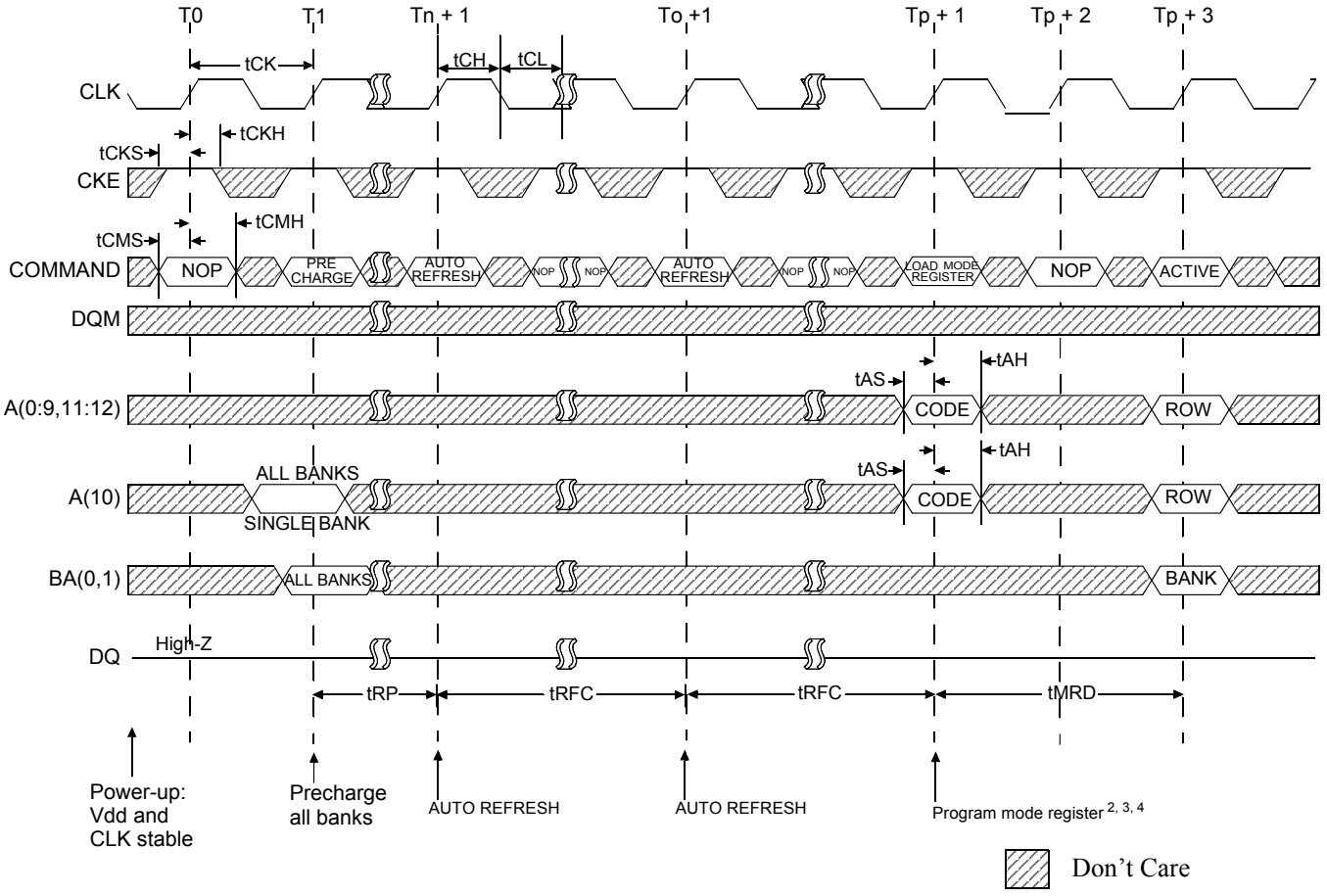
1. All voltages referenced to V_{SS}.
2. Measured only for initial qualification and after process or design change that could affect this parameter.
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (–40°C ≤ TC ≤ 105°C) is ensured.
5. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
6. AC characteristics assume t_T = 1ns, supplied as a design limit, neither tested nor guaranteed.
7. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
8. Outputs measured at 1.5V with equivalent load:



Equivalent Test Load Circuit

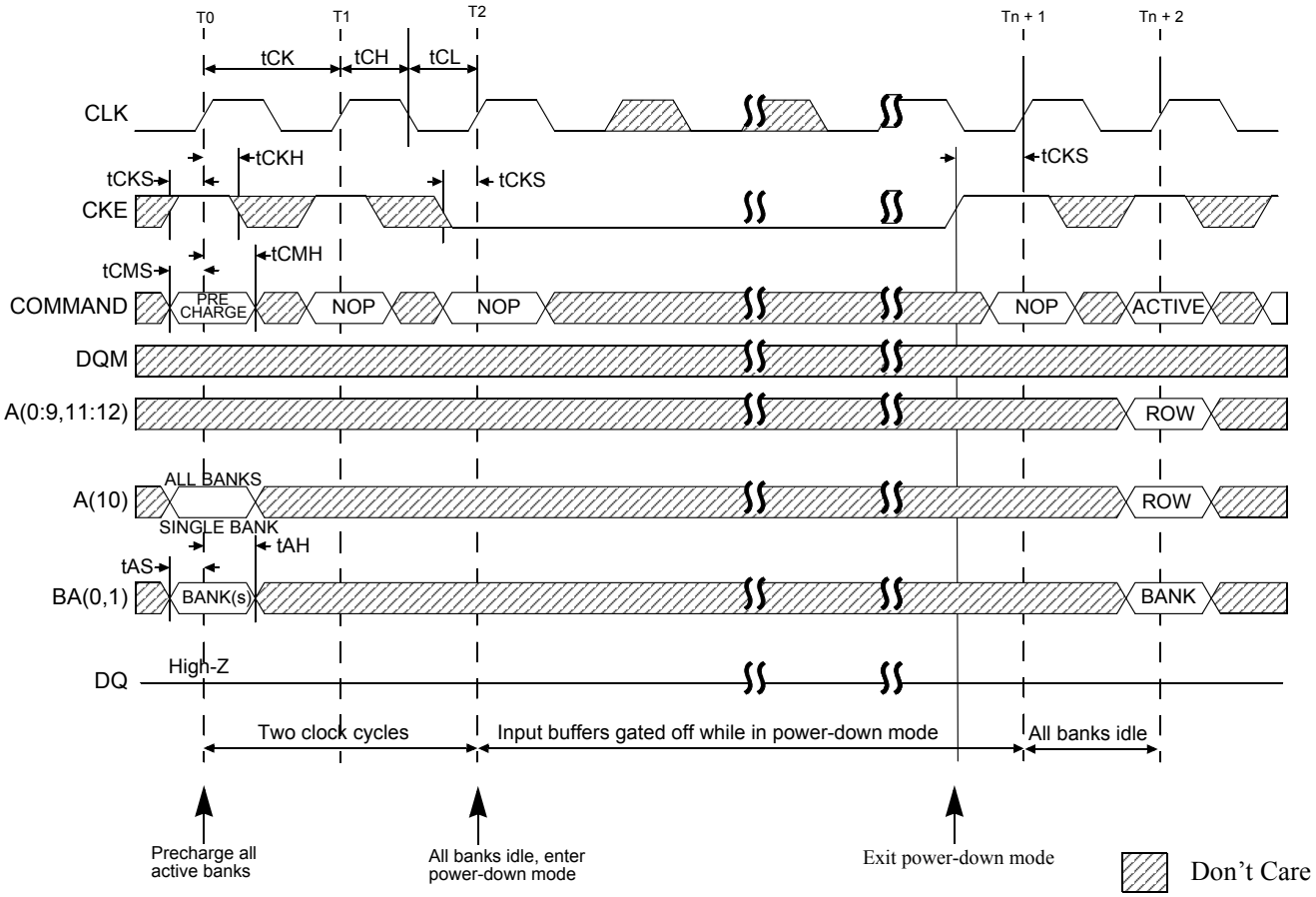
9. AC timing and IDD tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5Vcrossover point. If the input transition time is longer than 1ns, then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the 1.5V crossover point.
10. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
11. IDD specifications are tested after the device is properly initialized.
12. The IDD current will increase or decrease in a proportional amount by the amount the frequency is altered for the test condition.
13. Address transitions average one transition every two clocks.
14. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
15. CL = 2, tCK = 7.5ns.
16. CKE is HIGH during refresh command period tRFC (MIN) else CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value.

TIMING DIAGRAMS



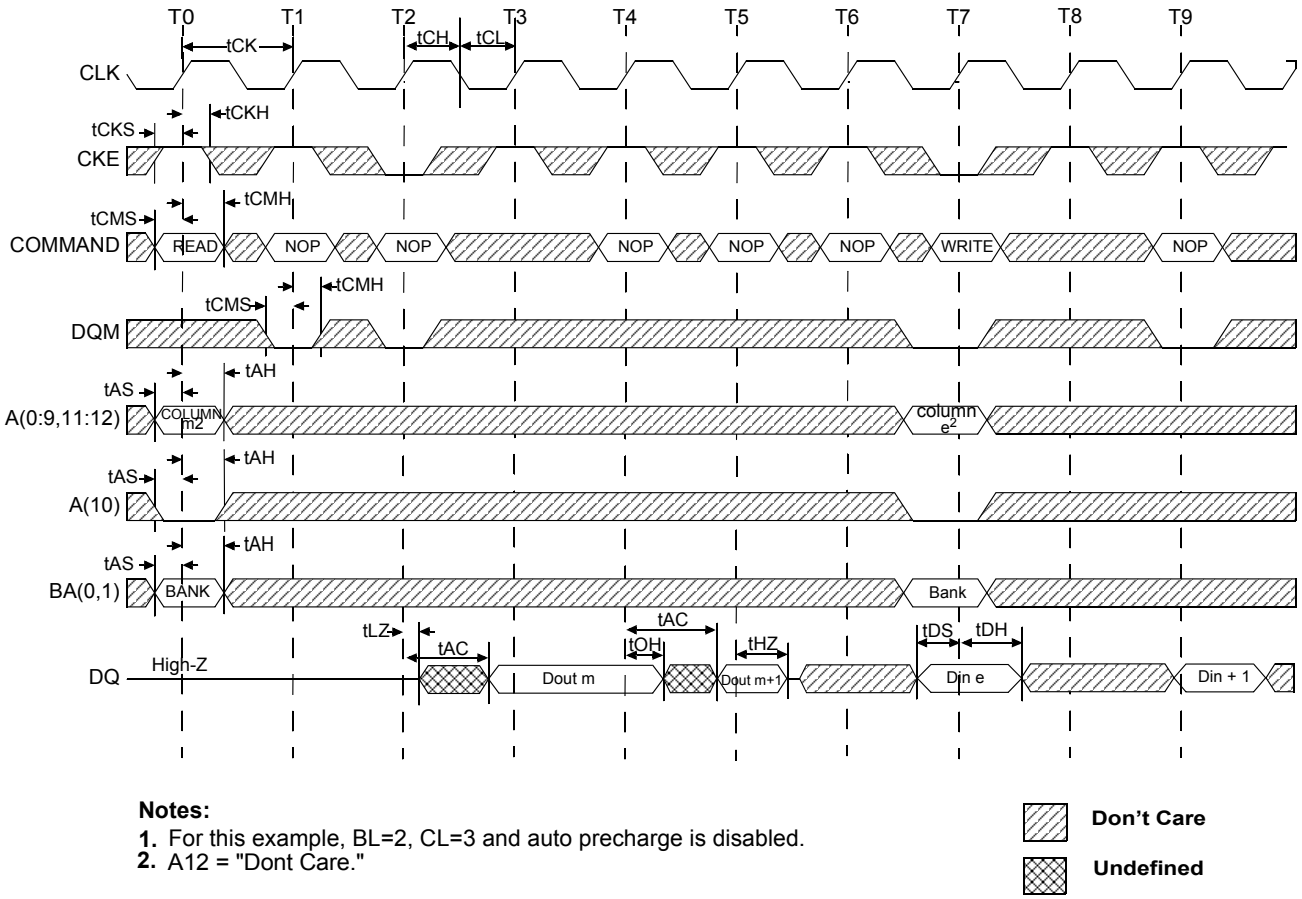
Notes:
1. If CS is HIGH at clock HIGH time, all commands applied are NOP.
2. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after command is issued.
5. A12 should be a LOW at Tp+1.

Figure 31: Initialize and Load Mode Register



Note: Violating refresh requirements during power down may result in a loss of data.

Figure 32: Power-Down Mode



Notes:

1. For this example, BL=2, CL=3 and auto precharge is disabled.
2. A12 = "Dont Care."

Don't Care

Undefined

Figure 33: Clock Suspend Mode

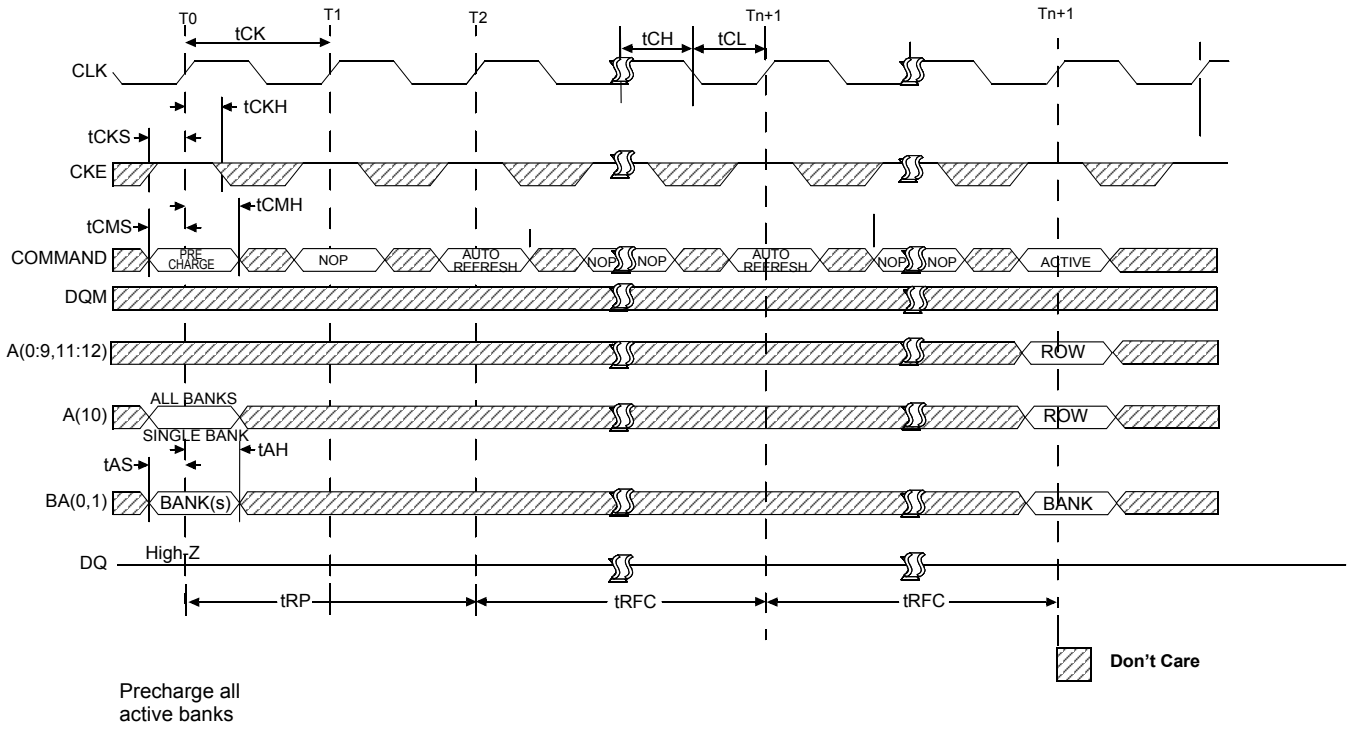
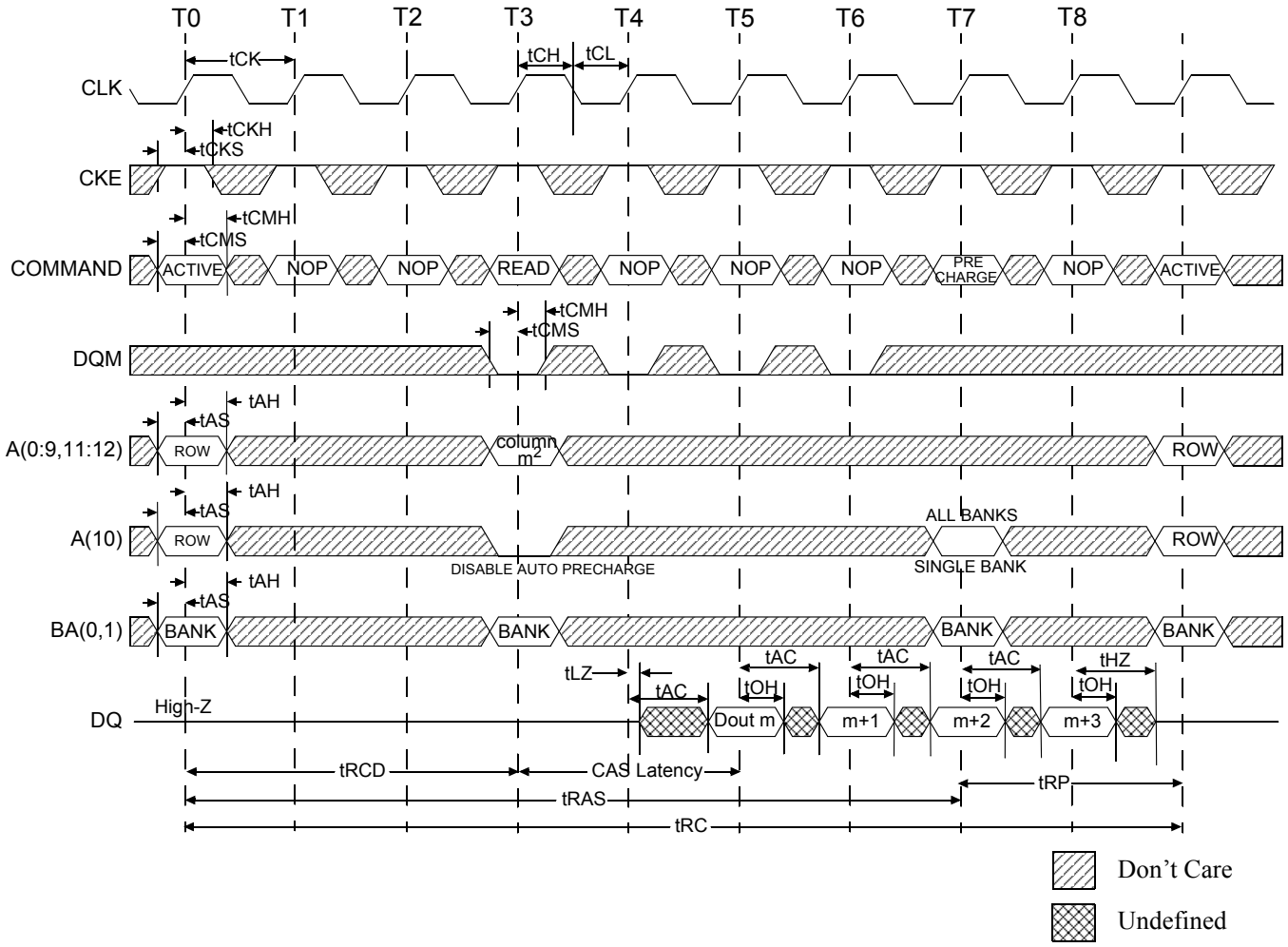


Figure 34: Auto-Refresh Mode



Notes:
1. For this example BL = 4, CL = 2, and the read burst is followed by a "manual" PRECHARGE
2. A12 = "Don't Care"

Figure 35: READ - Without Auto Precharge

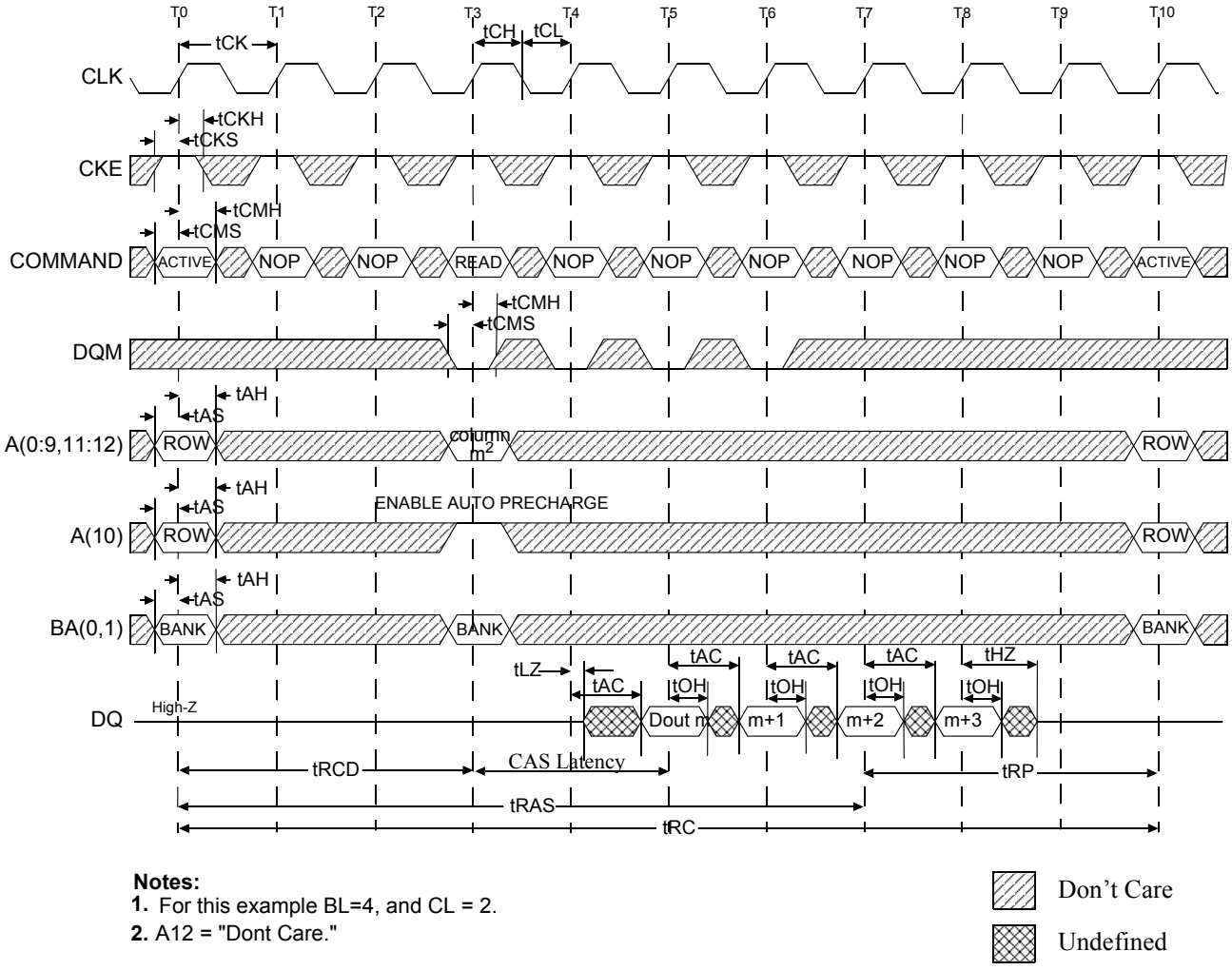
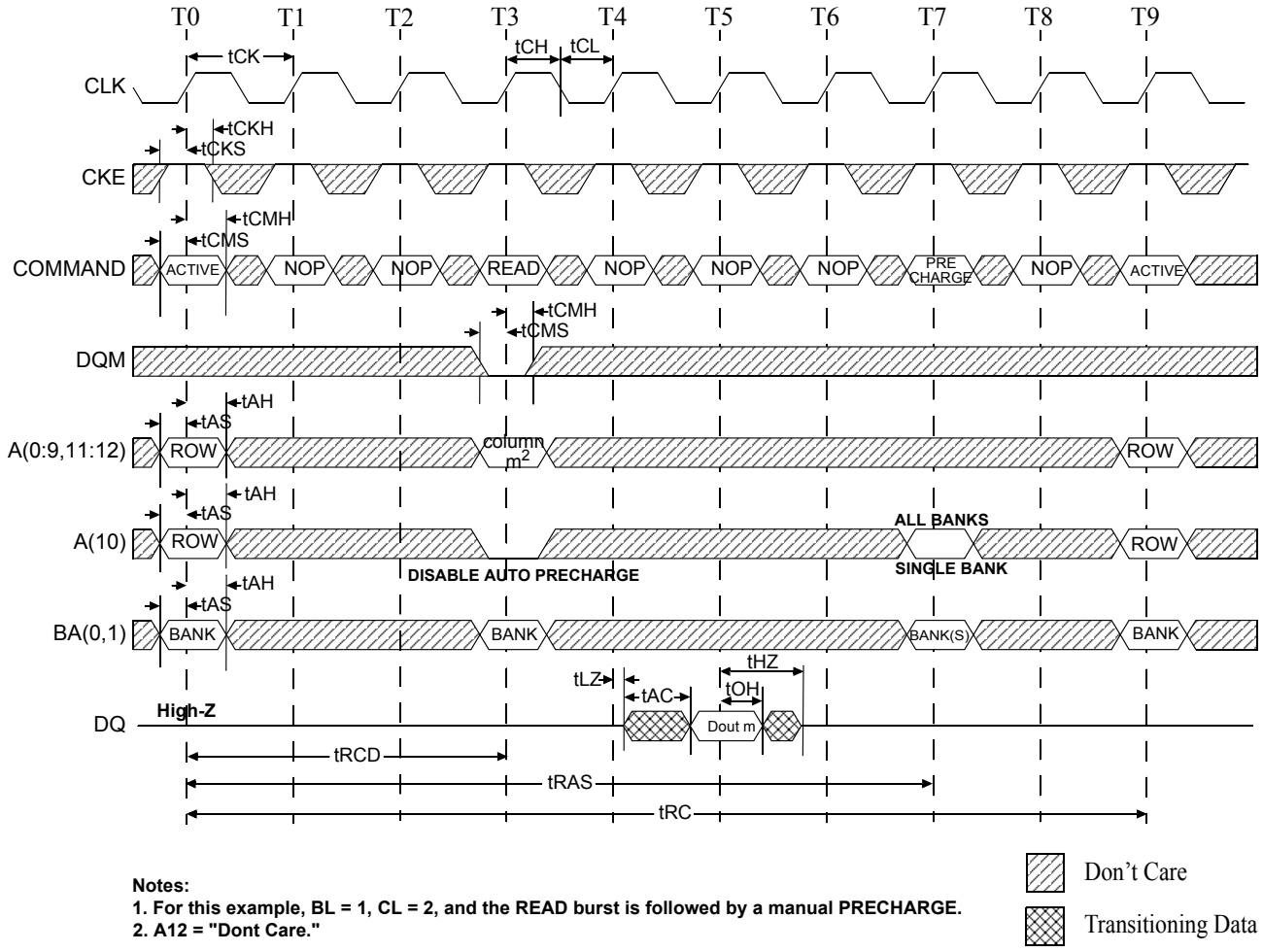
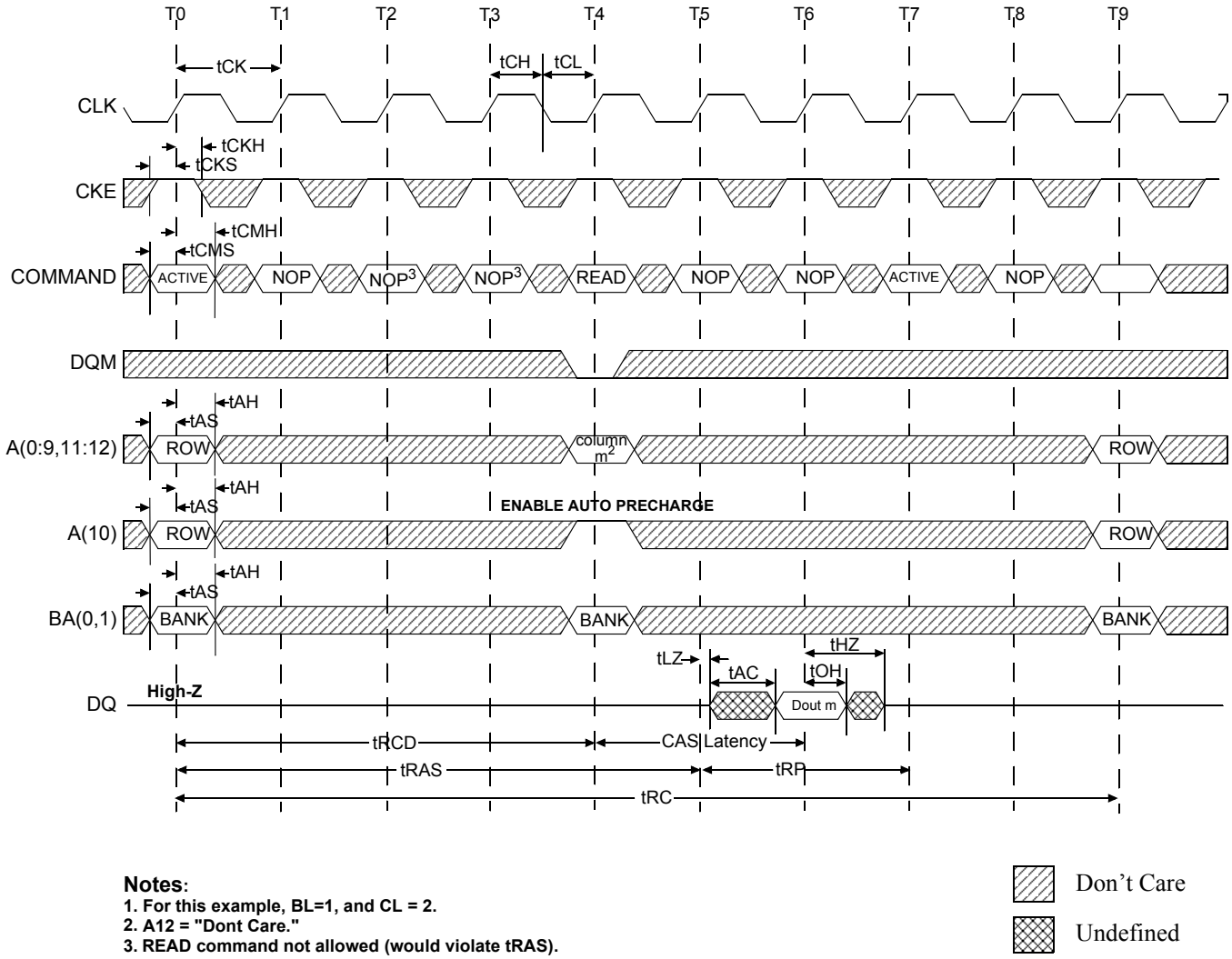


Figure 36: READ - With Auto Precharge



Notes:
1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.
2. A12 = "Dont Care."

Figure 37: Single READ - Without Auto Precharge



Notes:
1. For this example, BL=1, and CL = 2.
2. A12 = "Dont Care."
3. READ command not allowed (would violate tRAS).

Don't Care

Undefined

Figure 38: Single READ - With Auto Precharge

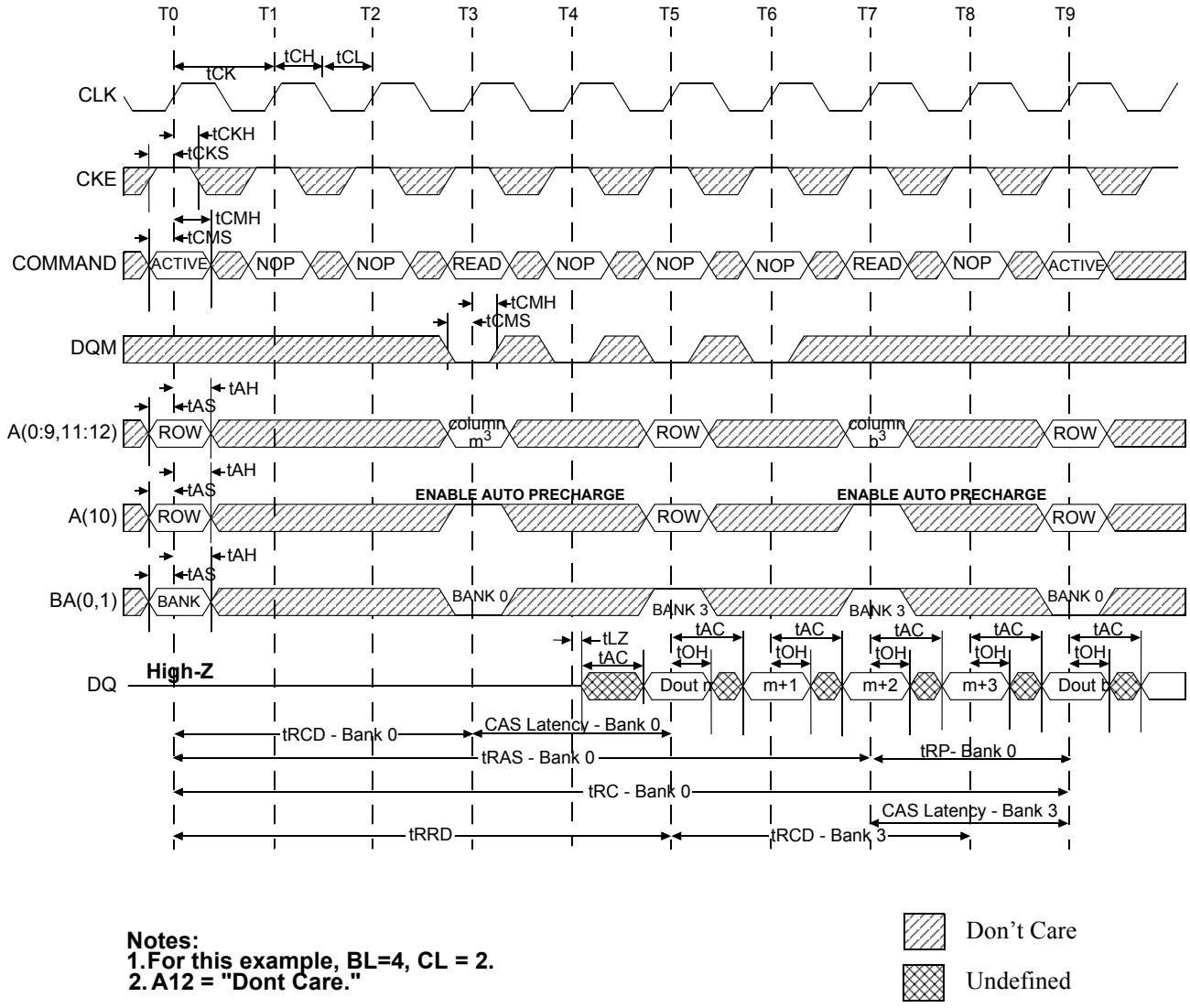


Figure 39: Alternating Bank Read Accesses

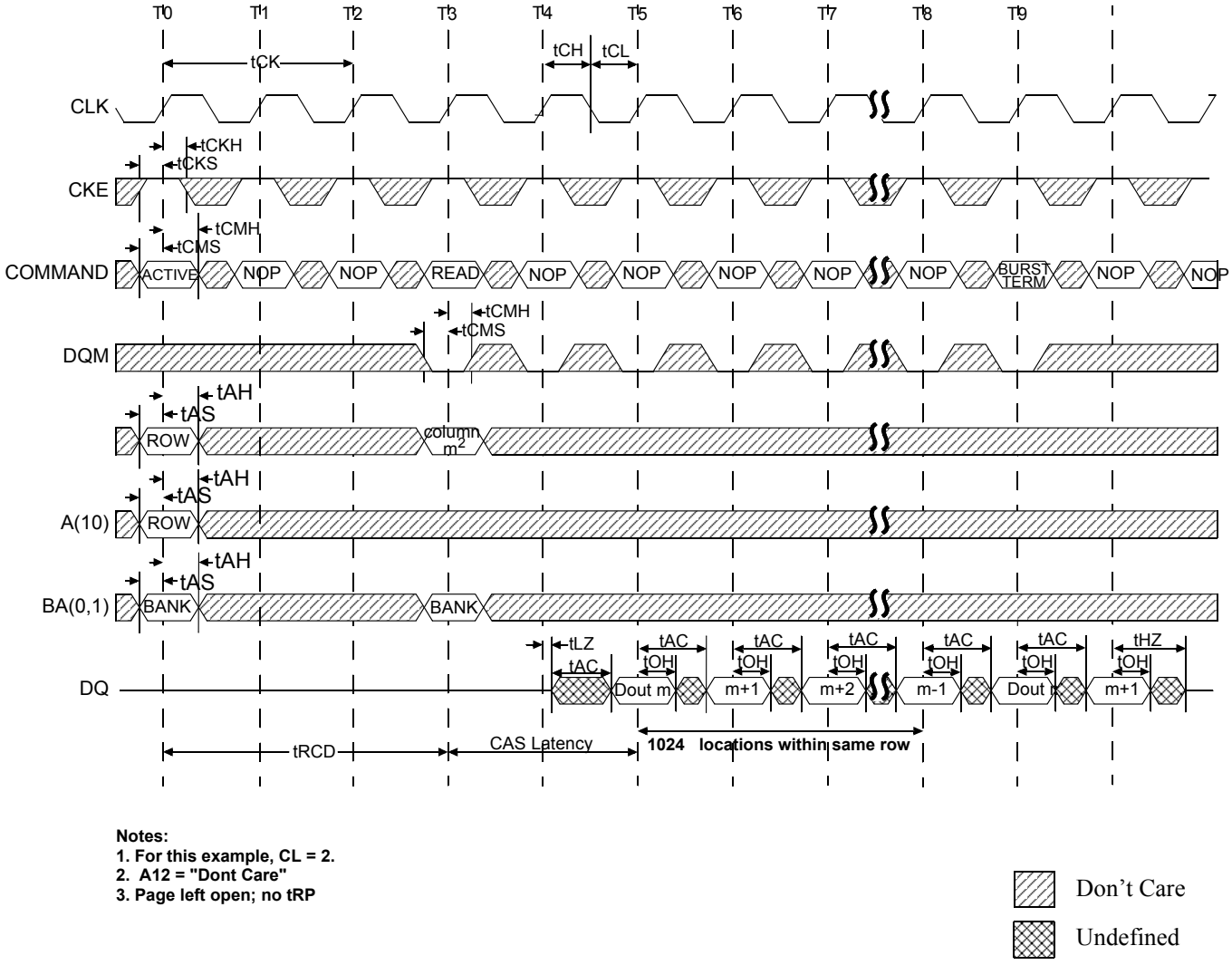


Figure 40: READ - Full-Page Burst

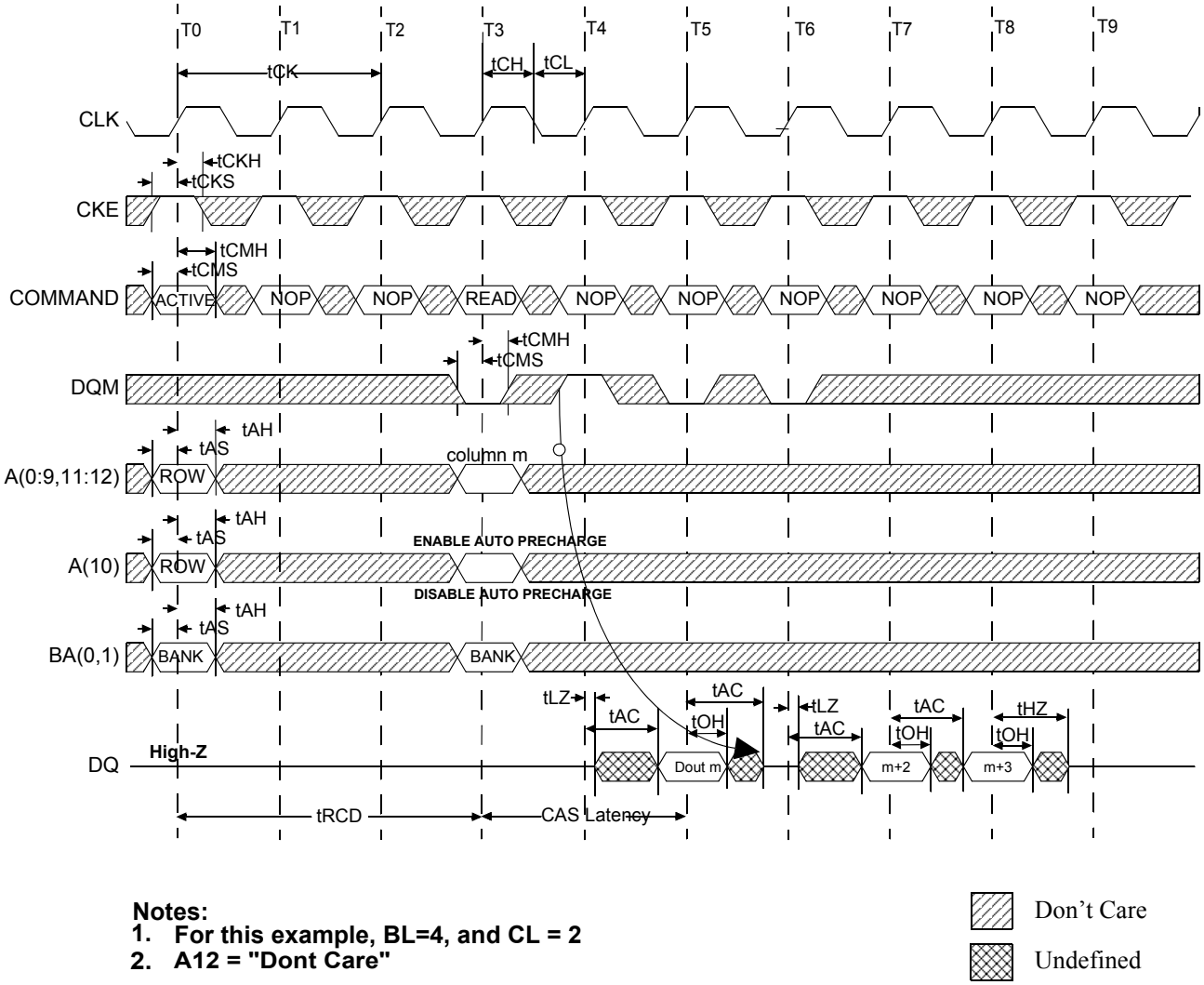
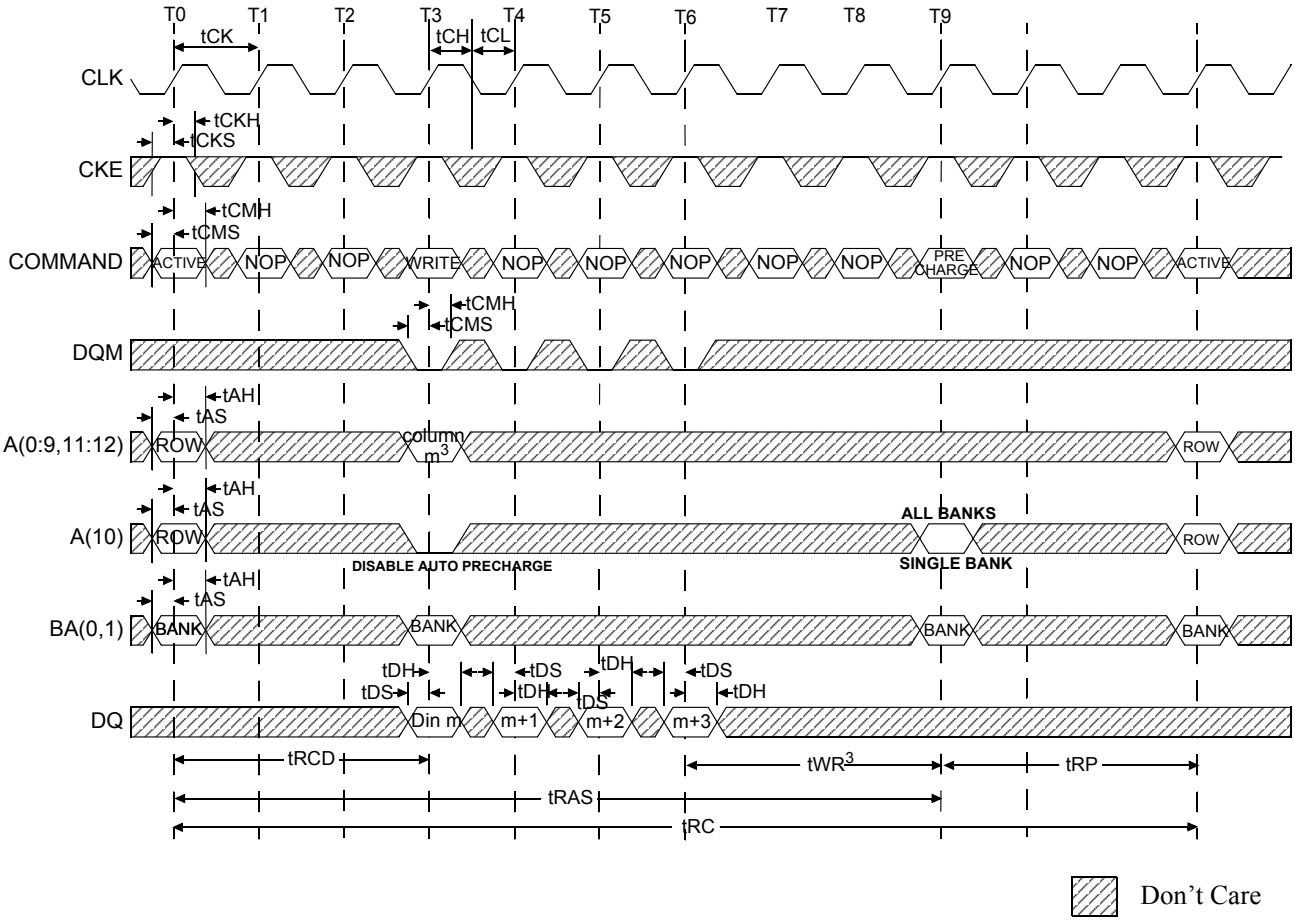


Figure 41: READ DQM Operation



Notes:

1. **For this example, BL= 4, and the WRITE burst is followed by a manual PRECHARGE.**
2. **14ns to 15 ns is required between <Din m+3 > and the PRECHARGE command, regardless of frequency.**
3. **A12 = "Dont Care."**

Figure 42: WRITE - Without Auto Precharge

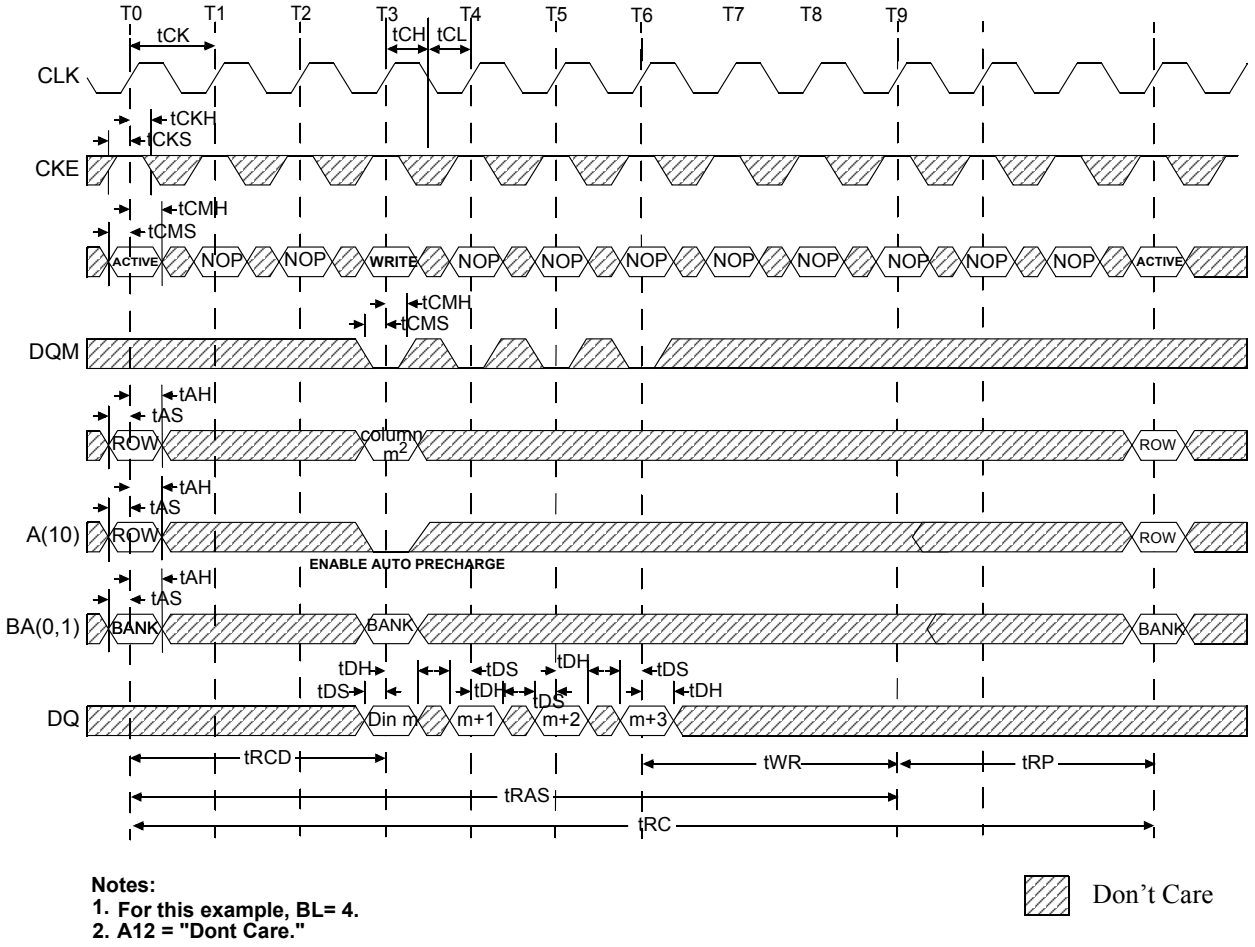
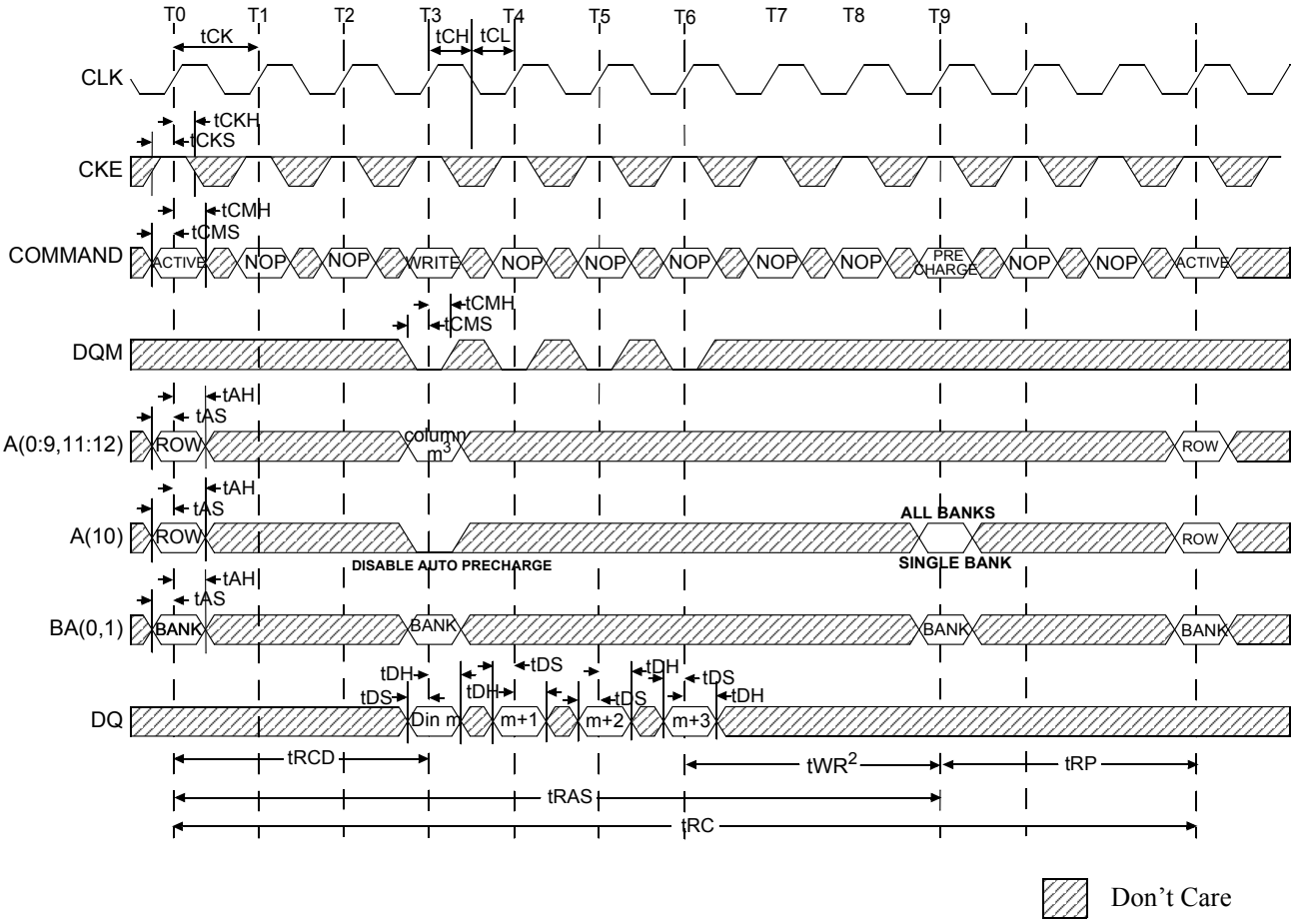


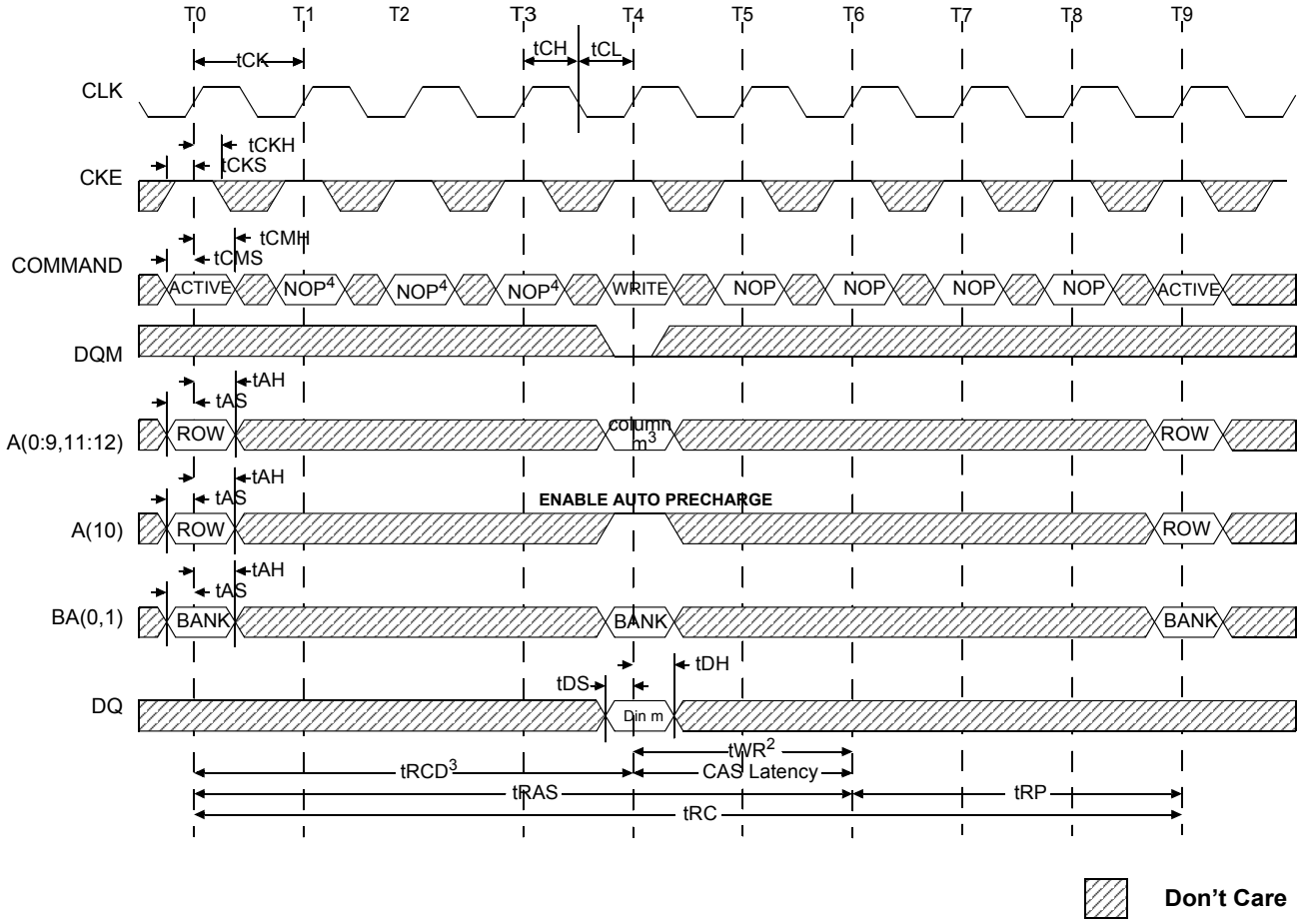
Figure 43: WRITE - With Auto Precharge



Notes:

1. **For this example, BL= 1, and the WRITE burst is followed by a manual PRECHARGE.**
2. **14ns to 15ns is required between <Din m > and the PRECHARGE command, regardless of frequency.**
3. **A12 = "Dont Care."**
4. **PRECHARGE command not allowed else t_{RAS} would be violated.**

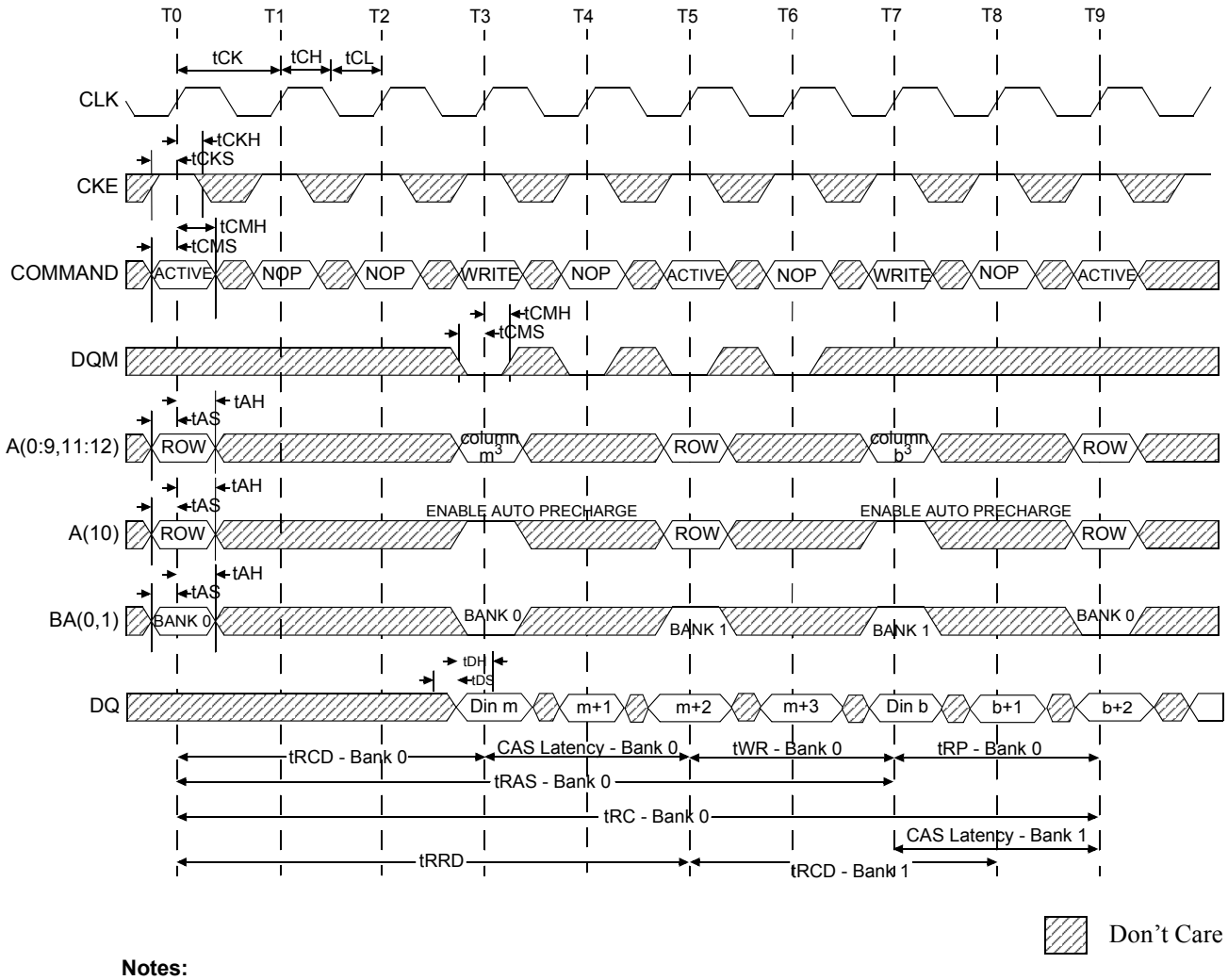
Figure 44: Single WRITE - Without Auto Precharge



Notes:

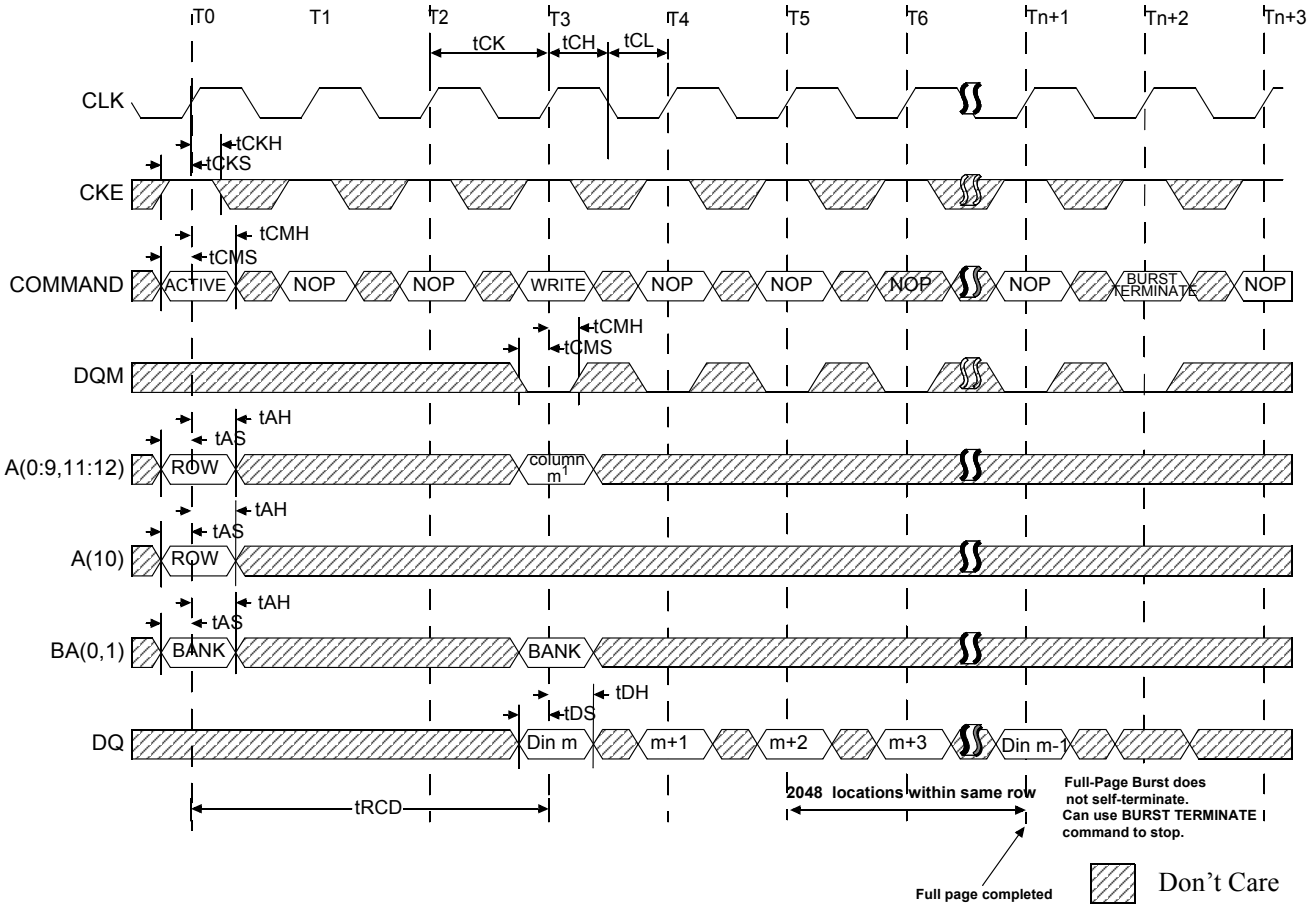
1. **For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.**
2. **14 to 15 ns is required between <Din m> and the PRECHARGE command, regardless of the frequency.**
3. **A12 = "Dont Care."**
4. **PRECHARGE command not allowed (would violate tRAS).**

Figure 45: Single WRITE - With Auto Precharge



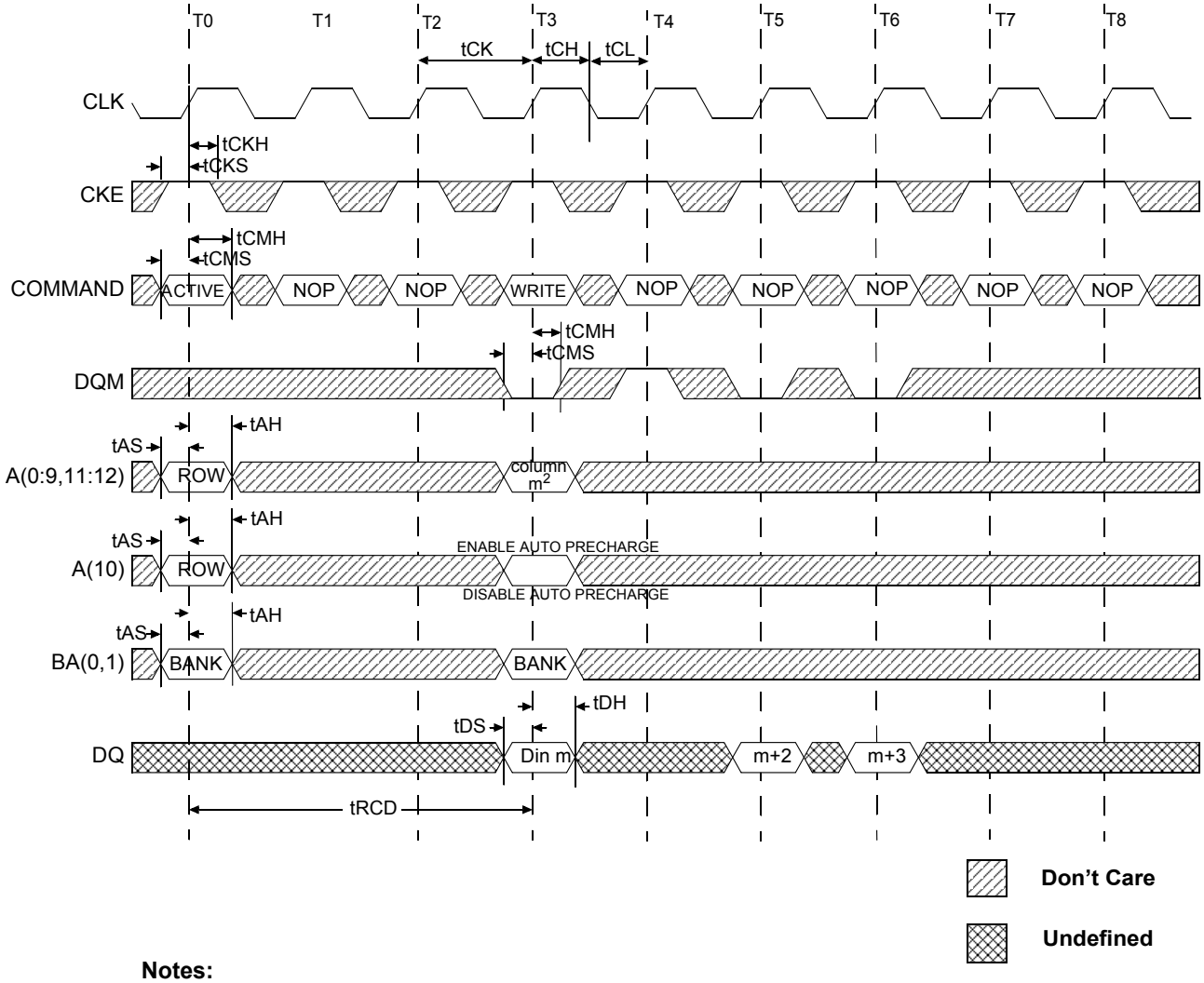
Notes:
1. For this example, BL=4, CL=2.
2. Requires one clock plus time (7ns to 7.5ns) with auto precharge or 14 to 15ns with PRECHARGE.
3. A12 = "Dont Care."

Figure 46: Alternating Bank WRITE Accesses



Notes:
1. **A12 = "Dont Care."**
2. **tWR must be satisfied prior to PRECHARGE command.**
3. **Page left open; no tRP.**

Figure 47: WRITE Full-Page Burst



Notes:
1. **For this example, BL=4.**
2. **A12 = "Dont Care."**

Figure 48: WRITE - DQM Operation

Packaging Prototypes Only

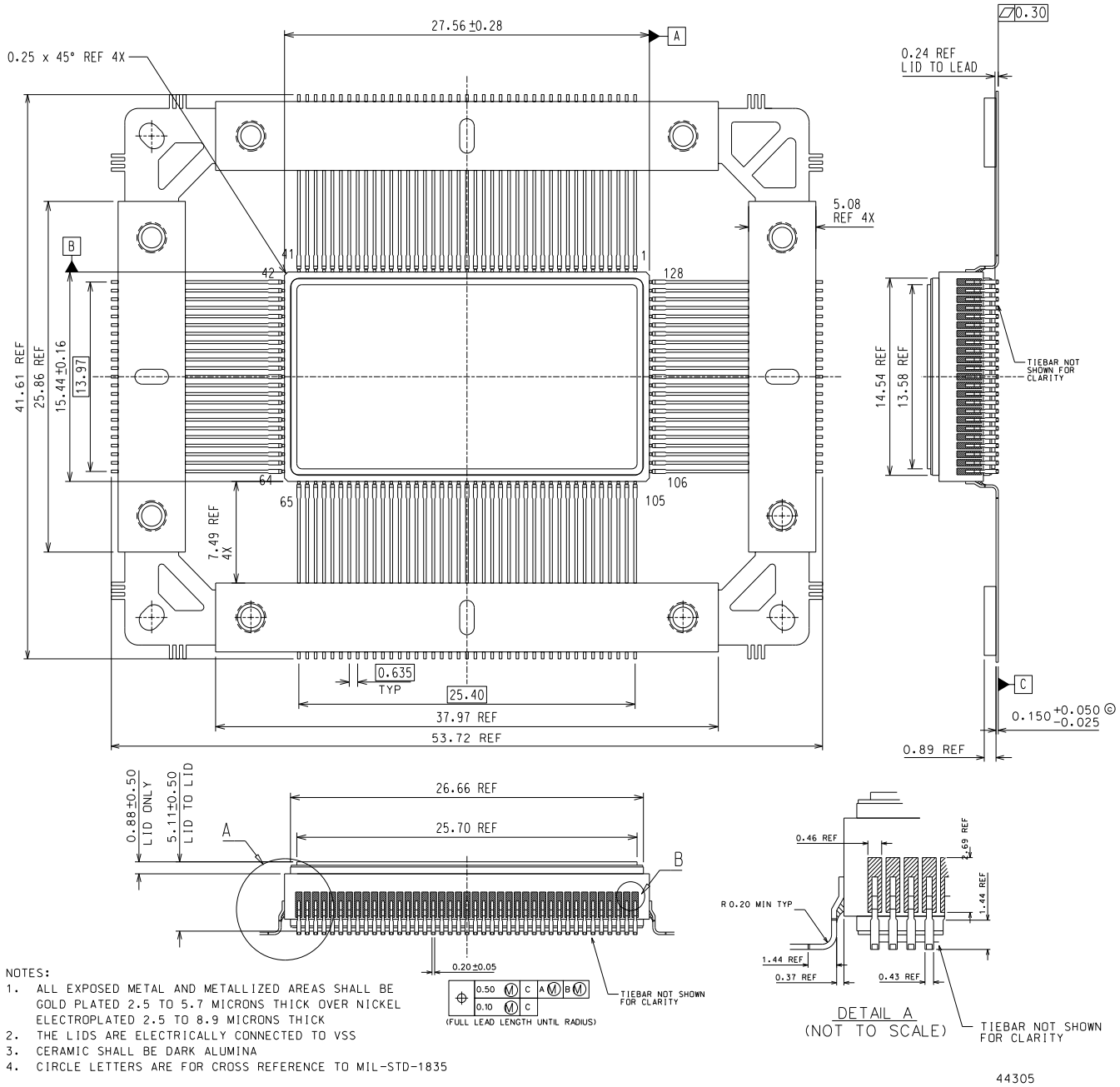


Figure 49: 128-lead Ceramic, Extended Side-Braze, Dual Sided Quad Flatpack (Datasheet Case Outline: X)

Packaging Production

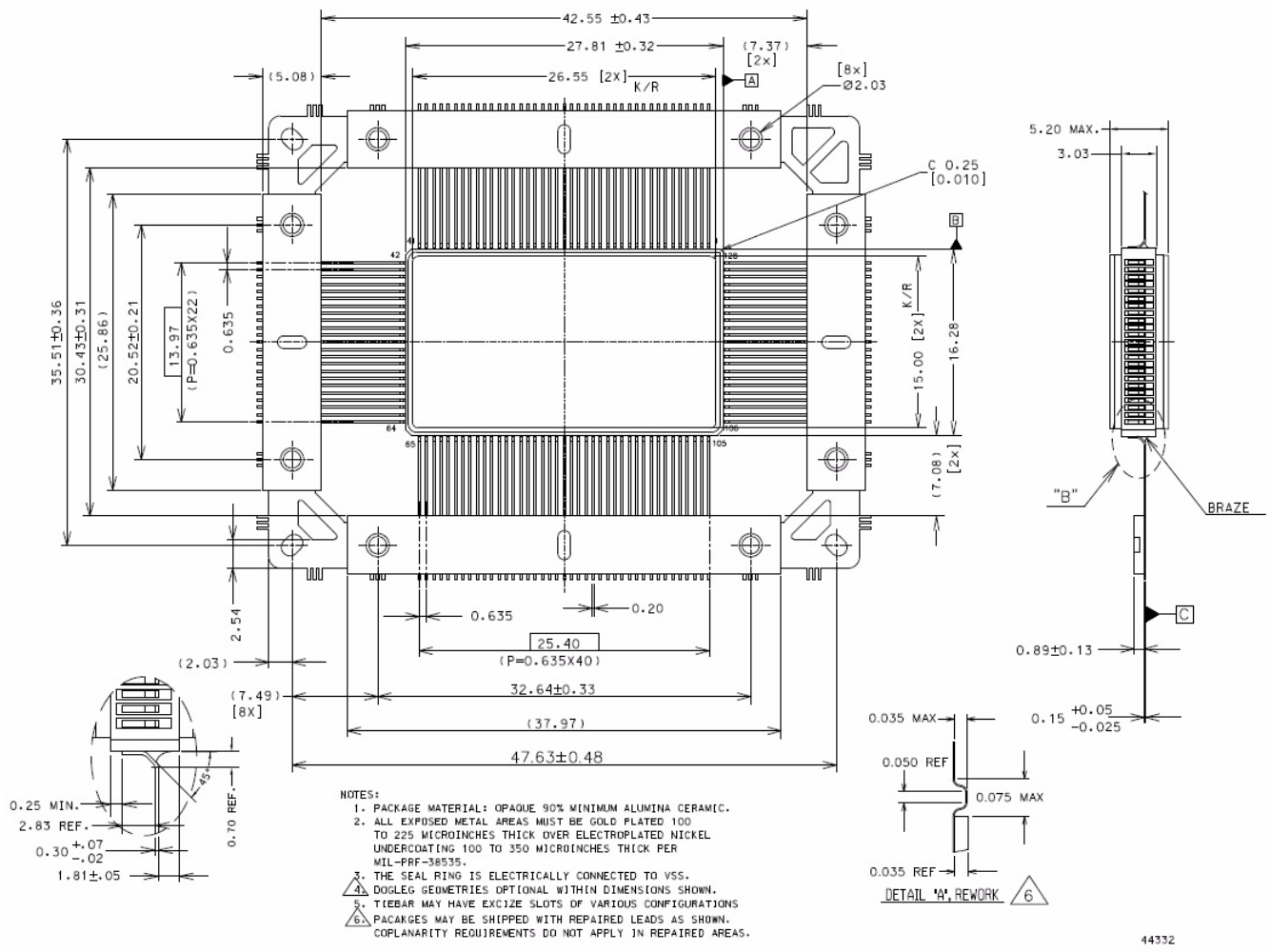


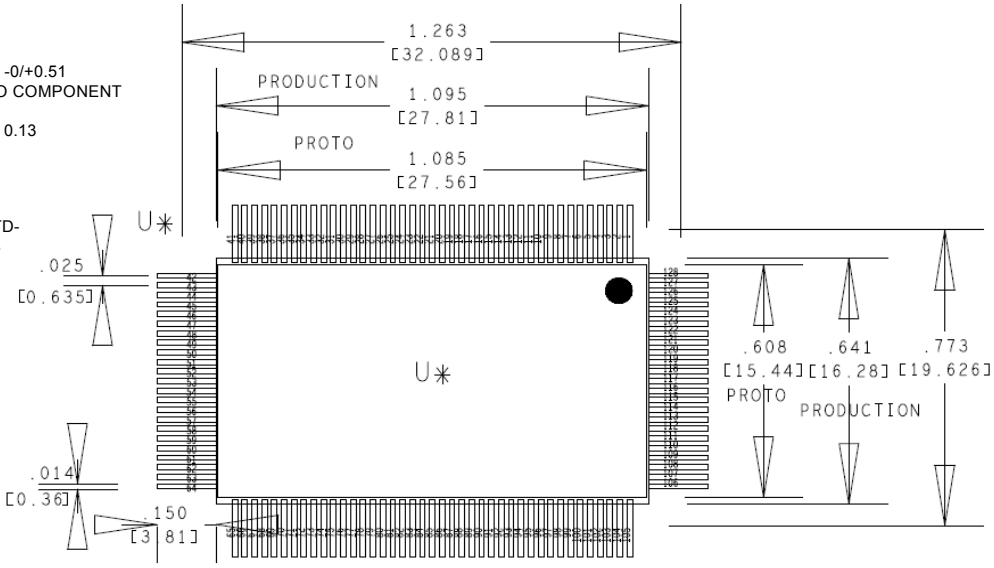
Figure 50: 128-lead Ceramic, Shallow Side-Braze, Dual Sided Quad Flatpack (Datasheet Case Outline: Y / SMD Case Outline: X)

Recommended Universal Footprint and Lead Forming Guidelines

LEAD FORMING GUIDELINES:
APPLY THE FOLLOWING LEAD FORMING GUIDELINES TO ENSURE THE 128 LEAD CERAMIC QFP WILL FIT THIS FOOTPRINT.

1) FIRST LEAD BEND IS 1.14 +/- 0.13 (0.045 +/- 0.13) FROM THE BODY.
2) SECOND LEAD BEND IS MADE 2.67 -0/+0.51 (0.105 -0/+0.020) TO ALLOW PWB TO COMPONENT BODY CLEARANCE.
3) THE FOOT OF THE LEAD IS 1.14 +/- 0.13 (0.045 +/- 0.005)

THESE LEAD FORMING GUIDELINES ARE COMPATABLE WITH IPC/EIA J-STD-001C FOR NOMINAL SOLDER FILLETS AND IPC-SM-782 FOR LAND PATTERN DESIGN

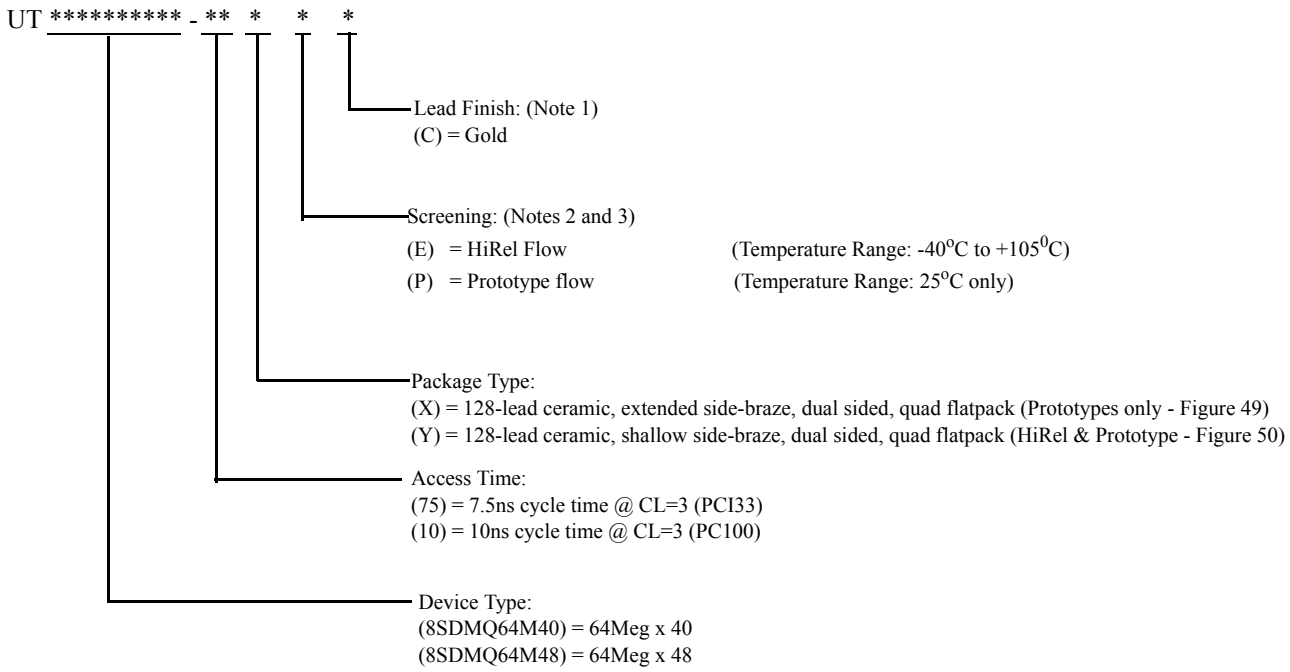


PAD SIZE = 0.356 X 3.81
(0.014 X 0.150)

Figure 51: Recommended Footprint for Combination of Aeroflex UT8SDMQ64 Prototype and Production Packages

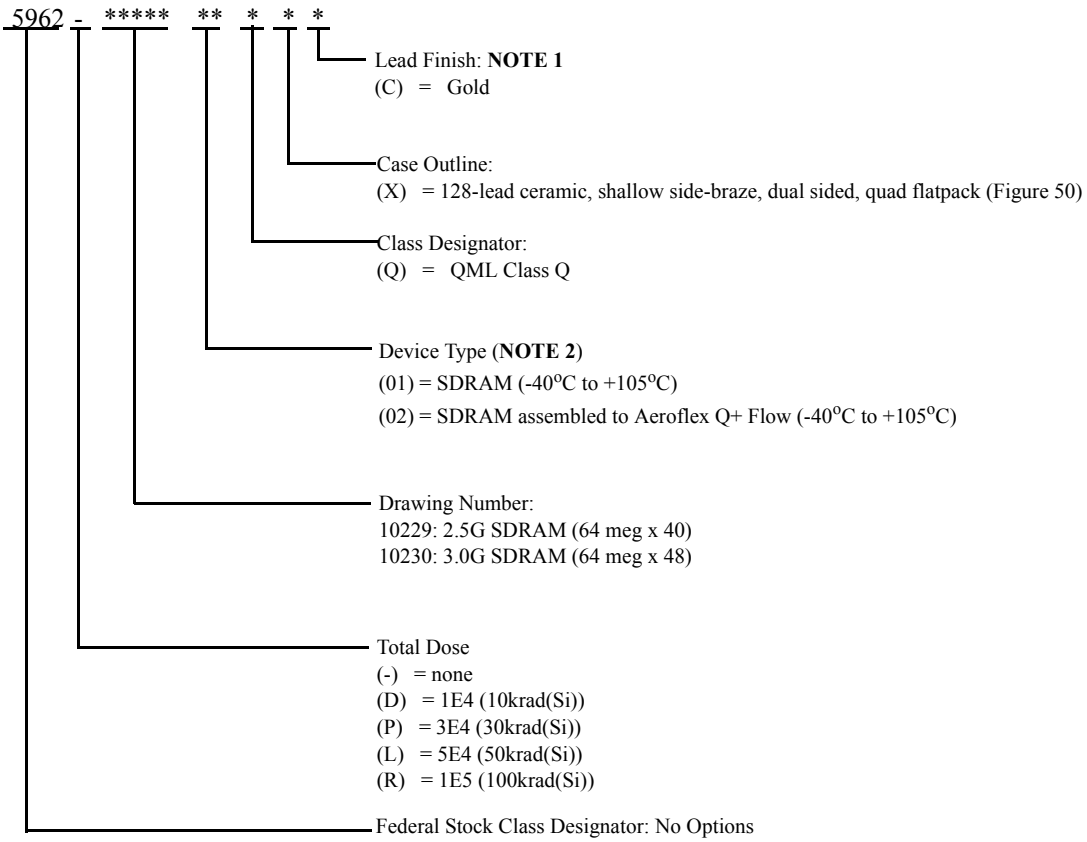
ORDERING INFORMATION

64Meg x 40 SDRAM
64Meg x 48 SDRAM



Notes:
1. Lead finish is "C" (Gold) only, and must be specified.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.
3. HiRel flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

64Meg x 40 SDRAM: SMD
64Meg x 48 SDRAM: SMD



Notes:
1. Lead finish is "C" (Gold) only.
2. Aeroflex's Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML Q product through the SMD that is manufactured with Aeroflex's standard QML V flow.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

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