MOTOROLA

MC54F/74F191

Product Preview

UP/DOWN BINARY COUNTER
(With Preset and Ripple Clock)

DESCRIPTION — The MC54F/74F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH-SPEED — 110 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

FUNCTIONAL DESCRIPTION — The F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}/D$ input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}/D$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐	⌐
H	X	X	H
X	L	X	H

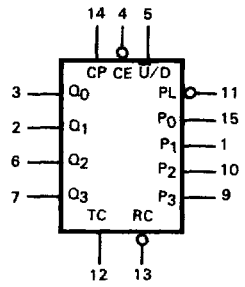
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

UP/DOWN BINARY COUNTER
(With Preset and Ripple Clock)

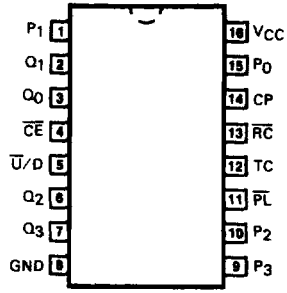
FAST™ SCHOTTKY TTL

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

FUNCTIONAL DESCRIPTION (continued)

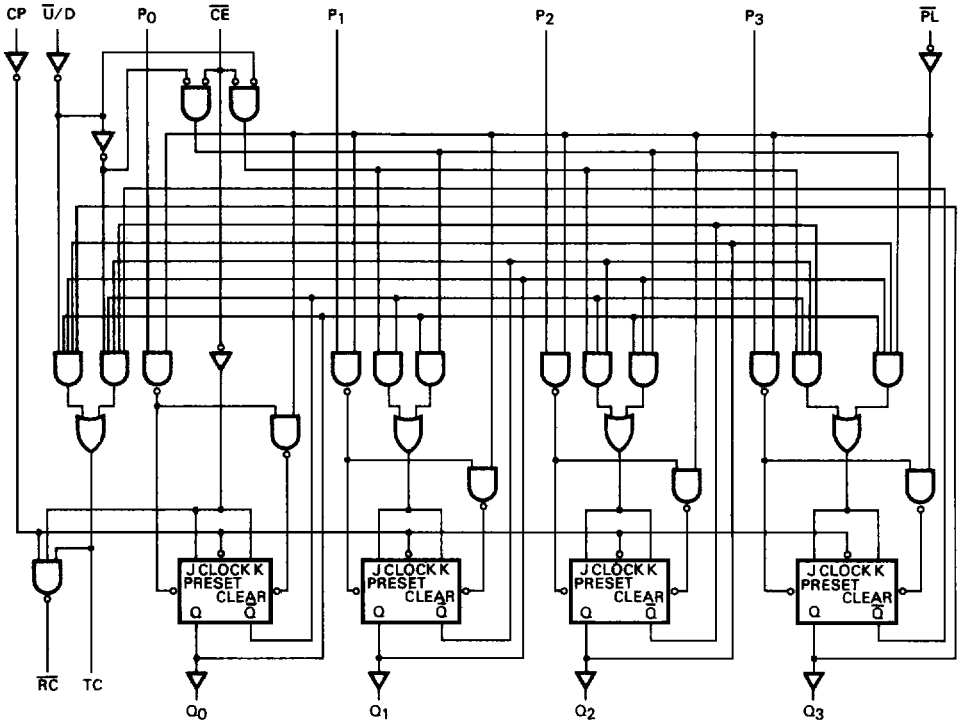
Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}/D$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

FIGURE A — N-Stage Counter Using Ripple Clock

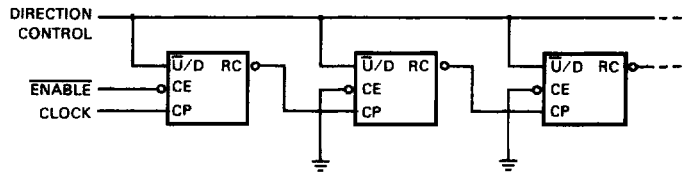


FIGURE B — Synchronous N-Stage Counter Using Ripple Carry/Borrow

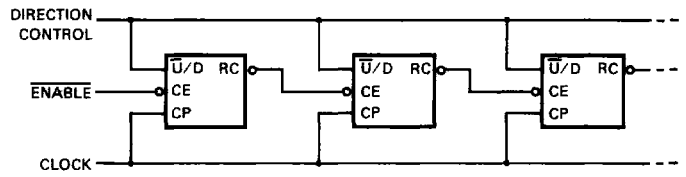
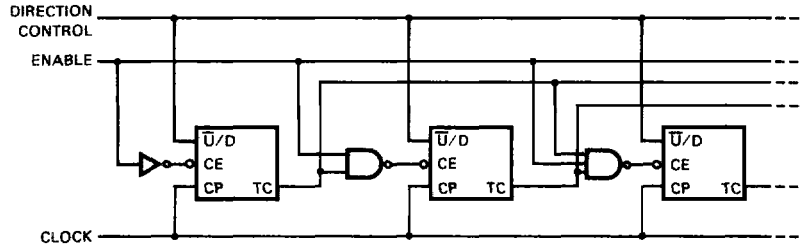


FIGURE C — Synchronous N-Stage Counter with Parallel Gated Carry/Borrow



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = -18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.50 V
		74	2.7	3.4		V	I_{OH} = -1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					100	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Other Inputs				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
	$\overline{CE}$ Input				-1.8			
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current			38	55	mA	V_{CC} = MAX	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0 to +70°C V_{CC} = 5.0 V ± 10% C_L = 50 pF		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum Count Frequency	80	110		80		80		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 3.0	5.5 6.5	9.0 10	3.0 3.0	12.5 14	3.0 3.0	10 11	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC	8.0 5.0	12.5 9.5	16 13	8.0 5.0	22.5 18	8.0 5.0	17 14	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	4.0 3.0	7.0 5.0	9.5 8.0	4.0 3.0	13.5 11	4.0 3.0	10.5 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.0 3.0	4.6 4.5	7.0 7.0	3.0 3.0	10 10	3.0 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	7.0 5.0	11 9.0	18 12	7.0 5.0	25.5 17	7.0 5.0	19 13	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.0 3.0	6.0 6.5	11 11	3.0 3.0	15.5 15.5	3.0 3.0	12 12	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	3.0 8.0	4.6 13.4	7.0 17	3.0 8.0	10 24	3.0 8.0	8.0 18	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.0 4.0	6.7 7.2	11 15	3.0 4.0	15.5 21	3.0 4.0	12 16	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A = −55 to +125°C V_{CC} = 5.0 V ±10%		74F T_A = 0 to +70°C V_{CC} = 5.0 V ± 10%		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW P_n to $\overline{PL}$	5.0 8.0			5.0 8.0		5.0 8.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0			3.0 3.0		3.0 3.0		
t_s (L)	Set up Time LOW $\overline{CE}$ to CP	10			10		10		ns
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0			0		0		
t_w (L)	$\overline{PL}$ Pulse Width, LOW	6.0			6.0		6.0		ns
t_w (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns
t_{rec}	Recovery Time $\overline{PL}$ to CP	7.0			7.0		7.0		ns