



Integrated Device Technology, Inc.

RISC FLOATING POINT ACCELERATOR (FPA)

PRELIMINARY IDT 79R2010A

FEATURES:

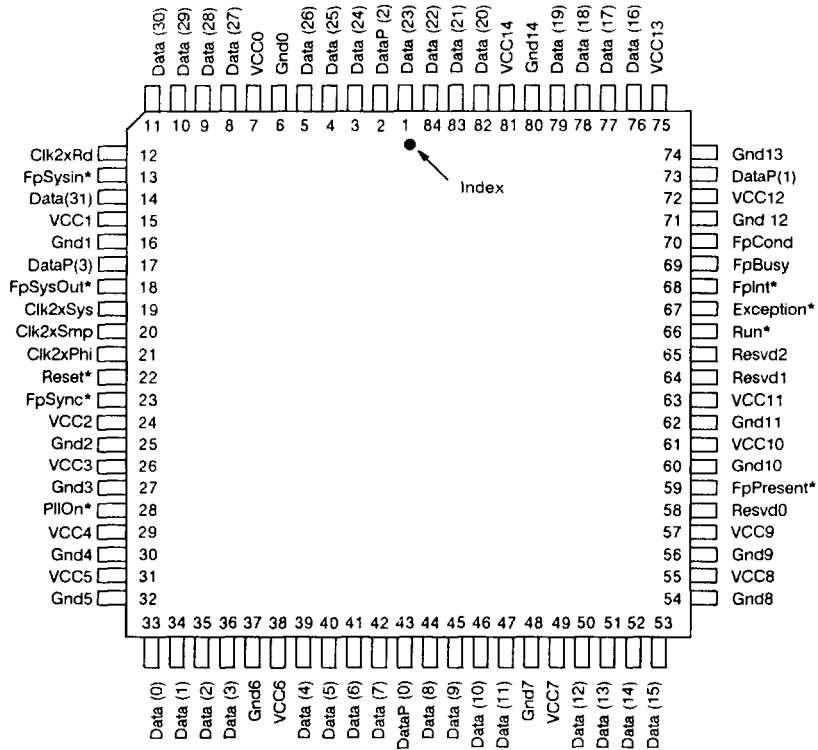
- Hardware Support of Single- and Double-Precision Operations:
 - Floating-point Add
 - Floating-Point Subtract
 - Floating-Point Multiply
 - Floating-Point Divide
 - Floating-Point Comparisons
 - Floating-Point Conversions
- Peak Speed: 13-17 mips (loads, stores and moves)
- Peak Speed: 6-8 MFLOPS (single- or Double-precision)
- Cycle Time: 60-80 ns (12.5 or 16.7 MHz)

- Direct High-Speed Interface to IDT79R2000A Processor
- Supports Full Conformance With IEEE 754-1985 Floating-Point Specification.
- Floating-Point Registers: Sixteen 64-bit registers.
- High-Speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer System's R2010A RISC FPA.
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

Please see the Data Sheet for 79R3010 for complete description.

PIN CONFIGURATION (TOP VIEW)



84-PIN J-BEND CERQUAD

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JANUARY 1989

ABSOLUTE MAXIMUM RATINGS ^(1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage ⁽²⁾	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed $V_{CC} + 0.5$ volts.
- Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

**DC ELECTRICAL CHARACTERISTICS –
COMMERCIAL TEMPERATURE RANGE** ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz		16.67 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	–	0.5	–	0.5	V
V_{OLFP}	Output LOW Voltage ⁽⁵⁾	$V_{CC} = \text{Min.}, I_{OL} = 1.5\text{mA}$	–	0.5	–	0.5	V
V_{IH}	Input HIGH Voltage ⁽⁶⁾		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage ⁽¹⁾		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage ^(2, 6)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage ^(1, 2)		–	0.4	–	0.4	V
V_{IHC}	Input HIGH Voltage ^(4, 6)		4.0	–	4.0	–	V
V_{ILC}	Input LOW Voltage ^(1, 4)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	$V_{CC} = \text{Max.}$	–	550	–	625	mA
C_{LD}	Load Capacitance		–	50	–	50	pF
I_{IH}	Input HIGH Leakage ⁽³⁾	$V_{IH} = V_{CC}$	-10	10	-10	10	μA
I_{IL}	Input LOW Leakage ⁽³⁾	$V_{IL} = \text{GND}$	-10	10	-10	10	μA
I_{OZ}	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-40	40	-40	40	μA

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE ($T_A = 0^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz		16.67 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	–	0.5	–	0.5	V
V_{OLFP}	Output LOW Voltage ⁽⁵⁾	$V_{CC} = \text{Min.}, I_{OL} = 1.5\text{mA}$	–	0.5	–	0.5	V
V_{IH}	Input HIGH Voltage ⁽⁶⁾		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage ⁽¹⁾		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage ^(2, 6)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage ^(1, 2)		–	0.4	–	0.4	V
V_{IHC}	Input HIGH Voltage ^(4, 6)		4.0	–	4.0	–	V
V_{ILC}	Input LOW Voltage ^(1, 4)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	$V_{CC} = \text{Max.}$	–	675	–	720	mA
C_{LD}	Load Capacitance		–	50	–	50	pF
I_{IH}	Input HIGH Leakage ⁽³⁾	$V_{IH} = V_{CC}$	-10	10	-10	10	μA
I_{IL}	Input LOW Leakage ⁽³⁾	$V_{IL} = \text{GND}$	-10	10	-10	10	μA
I_{OZ}	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-40	40	-40	40	μA

NOTES:

- V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
- V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2sRd, Clk2xPhr, CpBusy, and Reset"
- These parameters do not belong to the clock inputs
- V_{IHC} and V_{ILS} apply to Run and Exception*.
- V_{OLFP} applies to the FPPresent* pin only.
- V_{IH} and V_{IHS} should not be held above $V_{CC} + 0.5$ Volts

**AC ELECTRICAL CHARACTERISTICS –
COMMERCIAL TEMPERATURE RANGE** ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz		16.67 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
CLOCK							
TckHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TckLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TckP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	t _{cy} /4	0	t _{cy} /4	ns
	Clk2xSmp to Clk2xRd		0	t _{cy} /4	0	t _{cy} /4	ns
	Clk2xSmp to Clk2xPhi		11	t _{cy} /4	9	t _{cy} /4	ns
TIMING PARAMETERS							
TDEn	Data Enable ⁽³⁾		–	-2.5	–	-2	ns
TDDIs	Data Disable ⁽³⁾		0	–	0	–	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TDS	Data Set-up		11.5	–	9	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TFpCond	Fp Condition		–	45	–	35	ns
TFpBusy	Fp Busy		–	20	–	15	ns
TFpInt	Fp Interrupt		–	55	–	40	ns
TFpMov	Fp Move To		–	45	–	35	ns
TExS	Exception Set-up		15	–	10	–	ns
TExH	Exception Hold		0	–	0	–	ns
TRunS	Run Set-up		15	–	10	–	ns
TRunH	Run Hold		-2	–	-2	–	ns
RESET INITIALIZATION							
TrstPLL	Reset timing, Phase-lock on		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

- All timings are referenced to 1.5V.
- The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
- This parameter is guaranteed by design.
- These parameters reference timing diagrams shown in the "Hardware User's Manual"

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**AC ELECTRICAL CHARACTERISTICS –
MILITARY TEMPERATURE RANGE** ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz		16.67 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	
CLOCK							
TCKHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCKLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCKP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	t _{cy} /4	0	t _{cy} /4	ns
	Clk2xSmp to Clk2xRd		0	t _{cy} /4	0	t _{cy} /4	ns
	Clk2xSmp to Clk2xPhi		11	t _{cy} /4	9	t _{cy} /4	ns
TIMING PARAMETERS							
TDEn	Data Enable ⁽³⁾		–	-2.5	–	-2	ns
TDDIs	Data Disable ⁽³⁾		0	–	0	–	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRsDS	Reset Set-up		18	–	15	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TFpCond	Fp Condition		–	45	–	35	ns
TFpBusy	Fp Busy		–	20	–	15	ns
TFpInt	Fp Interrupt		–	55	–	40	ns
TFpMov	Fp Move To		–	45	–	35	ns
TExS	Exception Set-up		15	–	10	–	ns
TExH	Exception Hold		0	–	0	–	ns
TRunS	Run Set-up		15	–	10	–	ns
TRunH	Run Hold		-2	–	-2	–	ns
RESET INITIALIZATION							
TrstPLL	Reset timing, Phase-lock on		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

- All timings are referenced to 1.5V.
- The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
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ORDERING INFORMATION

