Marconi
Electronic Devices

MA7010

Radiation Hard 16x16 Multiplier Accumulator (Signal Slice™)

FEATURES

- Radiation Hard To 1 MRad (Si)
- High SEU immunity, Latch-up free
- Silicon-on-Sapphire technology
- High speed, low power
- 16 bit by 16 bit Multiplier/Accumulator with selectable accumulation and subtraction
- Pin and function compatible with IDT7210 and TDC1010 multiplier/accumulators
- 55 ns typical multiply/accumulate time
- 35 ns typical cycle time with optional pipeline stage
- 16 bit two's complement or unsigned magnitude inputs
- Full precision 35 bit result with optional rounding up to 19 bits
- Accumulator can be pre-loaded with a 35 bit value
- All inputs and outputs TTL compatible

APPLICATIONS

- Fast Fourier transform processing
- Array processing
- Matrix manipulations
- Radar signal processing
- General signal processing
- Minicomputer/microprocessor multiply accelerator
- High speed digital filtering

GENERAL DESCRIPTION

The MA7010 is a high speed 16x16 bit multiplier-accumulator. The input data can be specified as either two's complement or unsigned magnitude and the multiplier generates a full precision 32 bit product. Accumulation can take place to 35 bits precision.

The MA7010 is pin-for-pin compatible with the TDC1010 and IDT7210 multiplier-accumulators and offers the additional features controlled by the FT and $\overline{RST}$ inputs. One facility is the provision of an optional pipeline register R_P which can greatly improve multiply-accumulate rate.

Additionally, the output register R_A can be set to zero. Both features are highly relevant to digital filter and matrix operations.

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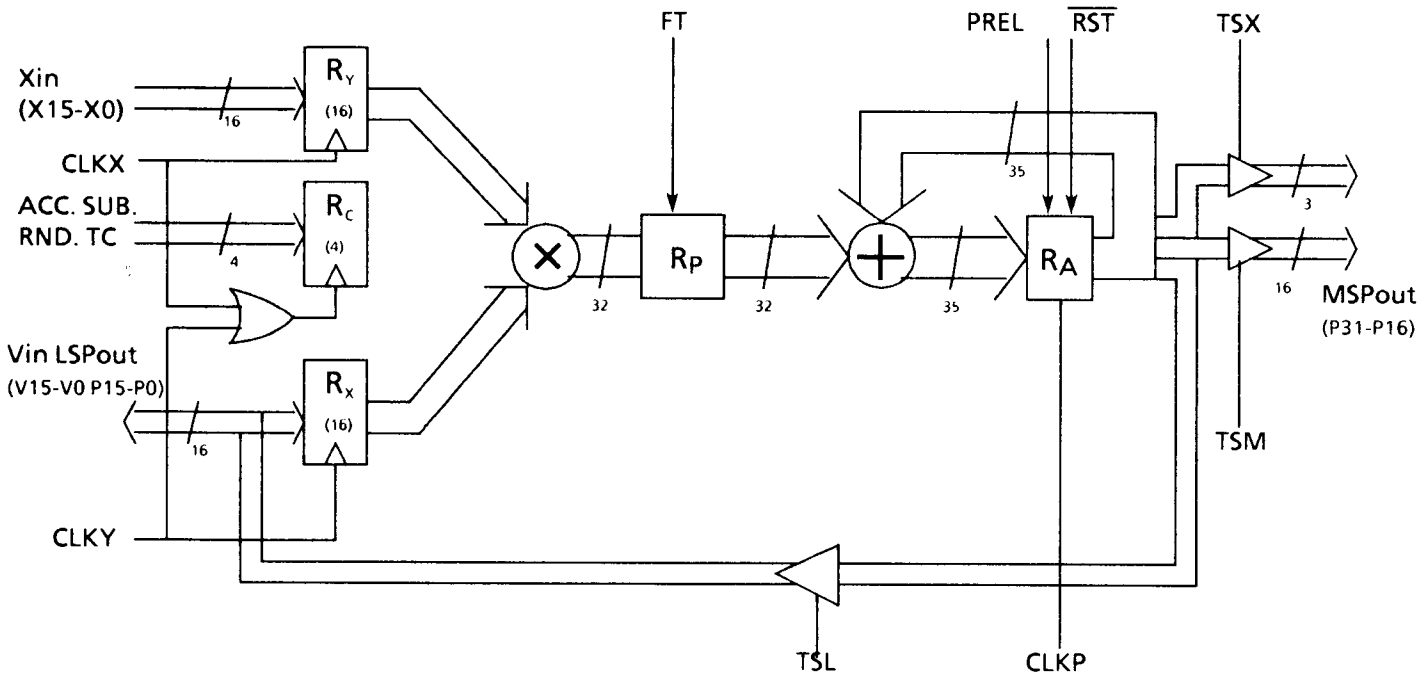
BLOCK DIAGRAM (Figure 1)



FUNCTIONAL DESCRIPTION

The MA7010 has two 16-bit data inputs, X and Y, which may be specified as two's complement or unsigned magnitude numbers using the control input TC. Two clock inputs, CLKX and CLKY, are provided to load X and Y into D-type registers, and a third clock input, CLKP, to load the D-type accumulator register with the result of the operation. The MA7010 performs multiply-only, multiply-accumulate or multiply-subtract, under the control of signals ACC and SUB.

The multiplier in the MA7010 produces a full-precision 32-bit output comprising a 16-bit least significant product (LSP) and a 16-bit most significant product (MSP). Three additional bits, known as the extended product (XTP), are provided to allow for word-growth during accumulation. The output can be rounded to 19 bits using the control input RND. The 16 least significant bits (LSP) of the 35-bit output are multiplexed with the Y inputs.

There is provision for pre-loading the accumulator registers XTP, MSP, and LSP with an external input. This operation is controlled by signals TSX, TSM, TSL, and PREL.

The 68-pin version of the MA7010 has two control pins, FT and $\overline{RST}$. These must be connected to V_{DD} for pin and function compatibility with industry standard equivalents. With FT connected to GND, the device operates in the pipeline mode (Figure 3). In this mode, the device can be operated with a 35ns clock cycle. Pulsing $\overline{RST}$ low has the effect of resetting the output registers to zero. It is important to note here that the reset facility and the accumulator register preload facility are not available while in the pipeline mode of operation.

PIPELINE MODE OF OPERATION

The pipeline mode of operation can offer a substantial increase in throughput when a large number of multiply-accumulates are required, such as in array or vector processing.

A low level on the FT control input switches the device into this pipeline mode by enabling a pipeline register between the multiplier and the accumulator for 32 bits (P3-P34) as shown in Figure 3. The three least significant bits (P0-P2) are accumulated separately before the pipeline register is loaded on the rising edge of CLKP. Pipelining separates the multiply and accumulate functions of the device enabling current accumulation and subsequent multiplication to be performed simultaneously. It can be seen that pipelining introduces a latency of a clock period, however, the clock period can, as a result of pipelining, be reduced from a minimum of 55ns to 35ns.

Data (X[0], Y[0]) is loaded on the first clock cycle with ACC control set low (refer to Figures 2 and 3). Multiplication follows and the result is placed in the pipeline register. On the following clock cycle the next data values (X[1], Y[1]) are loaded (with ACC high and SUB set for either subtraction or addition), meanwhile the first multiplication result (X[0]Y[0]) is transferred to an output register. The next clock cycle sees the loading of new data values, the accumulation of the second multiplication result with the value in the output register and the outputting of the contents of the output register.

It should be noted that in the accumulator it is the accumulation result which is added to, or subtracted from, the latest product of the multiplier and not vice versa. Hence an operation such as

$$P = \pm X(0)\,Y(0) \pm X(1)\,Y(1) \pm X(2)\,Y(2) \pm \ldots$$

should be written as

$$P = \pm (\ldots \pm (X(2)\,Y(2) \pm (X(1)\,Y(1) \pm X(0)\,Y(0)))\ldots)$$

PIPELINE MODE OF OPERATION (cont)

The timing diagram for this mode of operation is shown in Figure 2. Note that the control signals ACC and SUB are also pipelined. These are clocked into the device on the rising edge of CLKX or CLKY and into the pipeline register on the rising edge one clock period later.

The output register reset facility is not available during pipelining and hence $\overline{RST}$ must be held high with FT low. Note also that the preload facility is not available in this pipeline mode.

This mode of operation is only currently available in the 68 pin Pin Grid Array version of the MA7010 and is not present in any of the industry standard components.

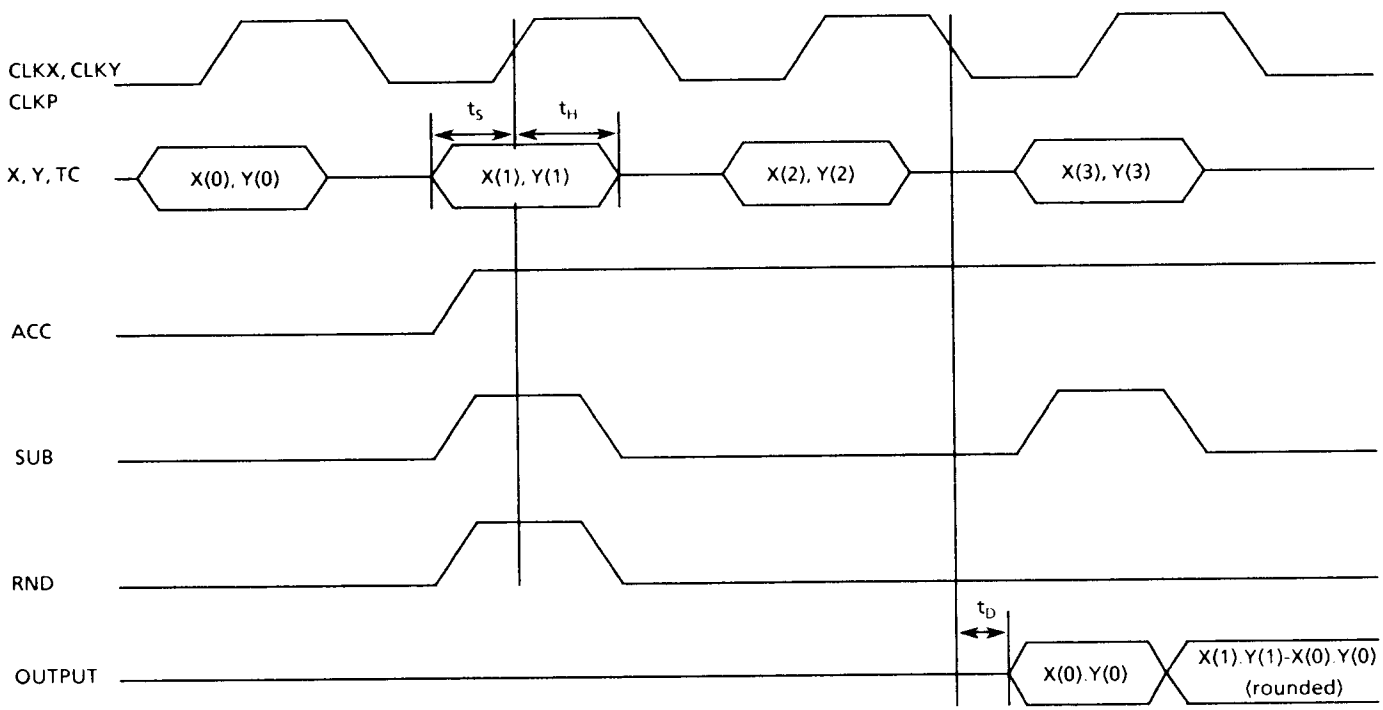


Figure 2. Timing diagram for an example of the use of the MA7010 in Pipeline Mode

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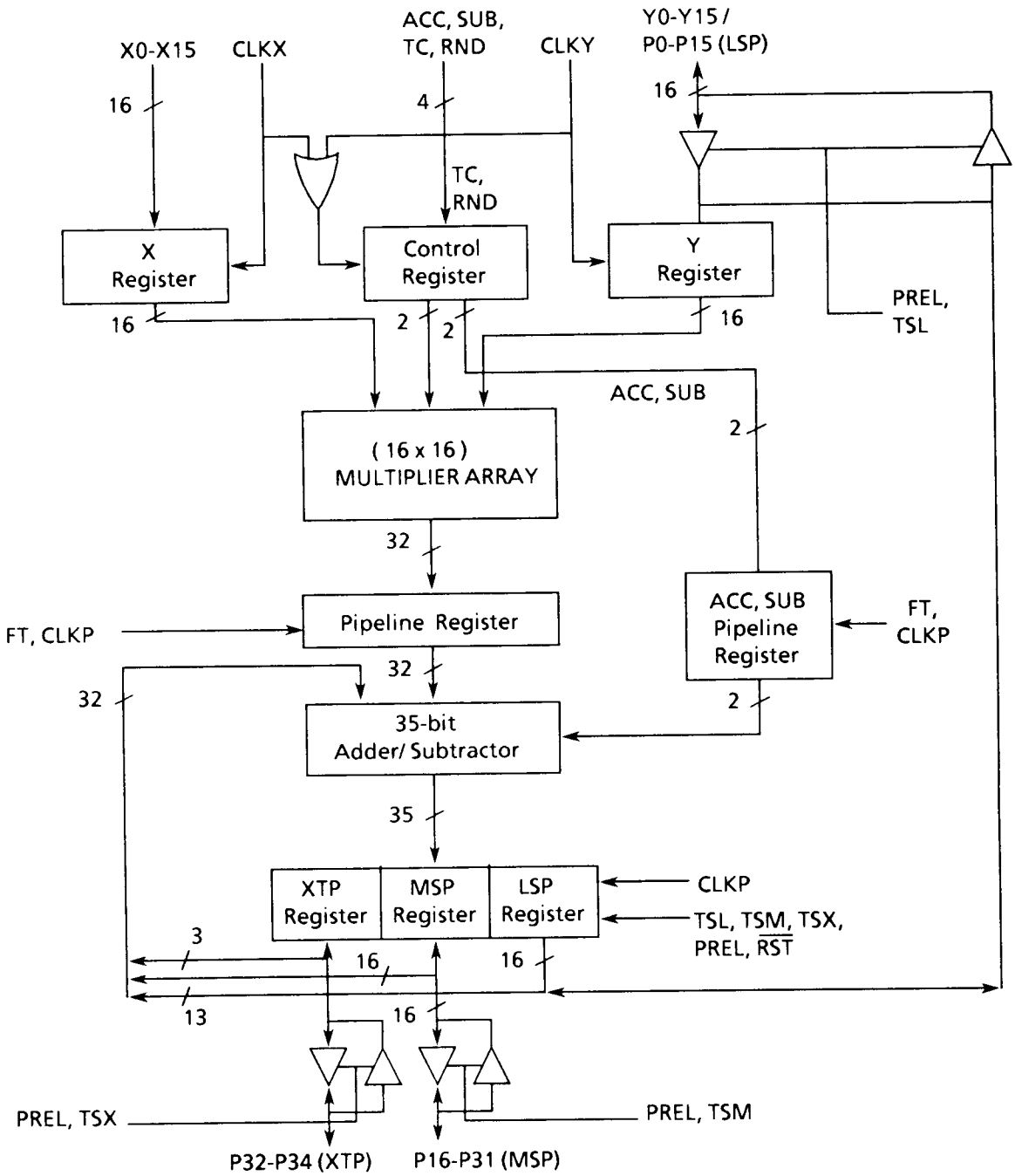
FUNCTIONAL BLOCK DIAGRAM OF MA7010 MULTIPLIER ACCUMULATOR (Figure 3)



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PIN DESCRIPTIONS

X0-X15 16-bit data input
X inputs are loaded on the rising edge of CLKX.

Y0-Y15 / P0-P15 16-bit data input / LSB output
These pins are shared betwen the 16-bit data input Y and the 16-bit LSP (least significant product) output. They are also used for loading the LSP part of the accumulator register. The multiplexing operations are controlled by inputs TSL and PREL.
The input Y is loaded on the rising edge of CLKY. The output LSP is available following the rising edge of CLKP. Preloading occurs on the rising edge of CLKP.

P16-P31 MSP result output / MSP pre-load input
The 16-bit MSP (most significant product) output is available following the rising edge of CLKP. Preloading of the MSP part of the accumulator register, controlled by inputs TSM and PREL, occurs on the rising edge of CLKP.

P32-P34 XTP extended product / XTP preload input
These three bits are provided to allow for wordgrowth during accumulation. XTP is available at the output following the rising edge of CLKP. Preloading of the XTP part of the accumulator register, controlled by inputs TSX and PREL, occurs on the rising edge of CLKP.

CLKX, CLKY Input clocks
X and Y are loaded on the rising edges of CLKX and CLKY respectively.

CLKP Output clock
The output register is loaded with the results of the operation on the rising edge of CLKP. The product output P0-P34 is available following this rising edge. Preloading of the accumulator register also occurs on the rising edge of CLKP.
In the pipeline mode the register is loaded on the rising edge of CLKP.

ACC, SUB Accumulate / Subtract
When ACC is LOW the device functions as a multiplier with no accumulation; generating a full precision 32-bit product, P0-P31. The three bits P32-P34 (XTP) are equal to P31 when TC is HIGH and are zero when TC is LOW.
When ACC is HIGH and SUB is LOW the accumulator register contents are added to the next product output. When ACC and SUB are both HIGH, accumulator register contents are subtracted from the next product output.
Both ACC and SUB signals are loaded on the rising edge of CLKX or CLKY and must be valid for the duration of the data input. In the pipelined mode ACC and SUB are also pipelined. ACC and SUB are loaded into the pipeline register on the rising edge of CLKP.

RND Rounding control input
RND input is added to the most significant bit of the LSP (i.e. P15), which results in the output being rounded to 19 bits. RND is loaded on the rising edge of CLKX or CLKY, and must be valid for the duration of the data input.

TC Two's complement / unsigned magnitude control input
A HIGH level defines X and Y as two's complement data, while a LOW level defines X and Y as unsigned magnitude data. TC is loaded on the rising edge of CLKX or CLKY and should be valid for the duration of the data input.

TSX, TSM, TSL, PREL Three-state output controls and preload control
These are register control inputs.
The XTP register is controlled by TSX and PREL. When TSX and PREL are both LOW, the XTP output drivers are enabled. For other combinations of TSX and PREL, the XTP output is in a high impedance state (disabled). When TSX and PREL are both HIGH, the preloading of the XTP register is enabled.
The MSP register is controlled by TSM and PREL. When TSM and PREL are both LOW, the MSP output drivers are enabled. For other combinations of TSM and PREL, the MSP output is in a high impedance state (disabled). When TSM and PREL are both HIGH, the preloading of the MSP register is enabled.
The LSP register is controlled by TSL and PREL. When TSL and PREL are both LOW, the LSP output drivers are enabled. For other combinations of TSL and PREL, the LSP outputs are in a high impedance state (disabled)

PIN DESCRIPTIONS (cont)

When TSL and PREL are both HIGH, the LSP part of the accumulator register can be preloaded using CLKP.

FT **Feedthrough control input (only in 68-pin devices)**

This is a control input which should be connected to V_{DD} for compatibility with industry standard equivalents. A LOW level on FT switches the device into pipeline mode. The pipeline register, which is operated using CLKP, is located between the multiplier and the accumulator. This register is bypassed when FT is HIGH. It is important to note that the RST input should be kept HIGH in the pipeline mode. There is no reset facility in the pipeline mode.

$\overline{RST}$ **Reset control input (only in 68-pin devices)**

This is an unregistered control input which should be connected to V_{DD} for compatibility with industry standard equivalents. The accumulator output register is reset to zero by holding $\overline{RST}$ LOW for a short period. It is important to note that this reset facility is not available while in the pipeline mode of operation. Hence when FT is LOW, $\overline{RST}$ must be kept HIGH.

PRELOAD TRUTH TABLES

PREL	TSX	XTP
0	0	Q
0	1	HiZ
1	0	HiZ
1	1	PL

PREL	TSM	MSP
0	0	Q
0	1	HiZ
1	0	HiZ
1	1	PL

PREL	TSL	LSP
0	0	Q
0	1	HiZ
1	0	HiZ
1	1	PL

Notes:
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
HiZ = Output buffers at high impedance.
PL = Ouptput buffers at high impedance.Preload data supplied externally at output pins will be loaded into the output register on the rising edge of CLKP.

DATA FORMATS

1. The locations of the binary points in the X and Y inputs are arbitrary, as long as the outputs are interpreted accordingly.

2. In the non-accumulating mode (ACC = 0), if the inputs are two's complement numbers (TC = 1), the four bits P31-P34 will all indicate the sign of the product. If the inputs are unsigned magnitude numbers (TC = 0), the three bits P32-P34 will all be zero.

3. In the accumulation mode (ACC = 1), if the inputs are two's complement numbers (TC = 1) and/or if subtractions are involved (SUB = 1), the 35-bit output should be interpreted as a two's complement number. If the inputs are unsigned magnitude numbers (TC = 0) and only if additions are involved, the output can be regarded as an unsigned magnitude number.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
SUPPLY VOLTAGE	-0.5	10	V
INPUT VOLTAGE	-0.3	V_{DD} + 0.3	V
CURRENT THROUGH ANY PIN	-20	20	mA
OPERATING TEMP.	-55	125	°C
STORAGE TEMP.	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10%. Over full operating temperature range.

SYMBOL	PARAMETER	TOTAL DOSE RADIATION NOT EXCEEDING $3x10^5$ RAD (Si)			TOTAL DOSE ≤ 1 MRAD (Si)		UNITS	CONDITION
		MIN	TYP	MAX	MIN	MAX		
V_{DD}	SUPPLY VOLTAGE	4.5	5.0	5.5	4.5	5.5	V	
V_{IH}	Input High Voltage	2.0			2.0		V	
V_{IL}	Input Low Voltage			0.8		0.3	V	
V_{OH}	Output High Voltage	2.4			2.4		V	I_{OH} = -0.8mA
V_{OL}	Output low Voltage			0.4		0.4	V	I_{OL} = 4.0mA
I_{IL}	Input Low Current			100		100	uA	V_{DD} = max; V_{IN} = 0
I_{IH}	Input High Current			100		100	uA	V_{DD} = max; V_{IN} = V_{DD}
I_{DD}	Power Supply Current		15	25		25	mA	$V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$
I_{DDYN}	Dynamic Power Supply Current		40	60		60	mA	Output open; V_{IN} = TTL voltage; Max clk cycle

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10% and C_{CL} = 50pF. Over full operating temperature range.

PARAMETER	MIN	MAX	UNITS	CONDITIONS
t_{MA} Multilply-Accumulate Time	-	55	ns	See Figure 4
Multiply-Accumulate Time with optional pipeline stage	-	35	ns	
t_D Output Delay	-	40	ns	See Figure 4
t_{ENA} Output Enable Delay	-	40	ns	See Figure 5
t_{DIS} Output Disable Delay	-	40	ns	See Figure 5
t_S Input Register Set-up Time	15	-	ns	
t_H Input Register Hold Time	10	-	ns	
t_{PW} Clock Pulse Width	20	-	ns	

1. Input Pulse V_{SS} to 3.0 Volts
2. Times Measurement Reference Level 1.5 Volts.
3. Input Rise and Fall Times 5ns.

Test Circuits

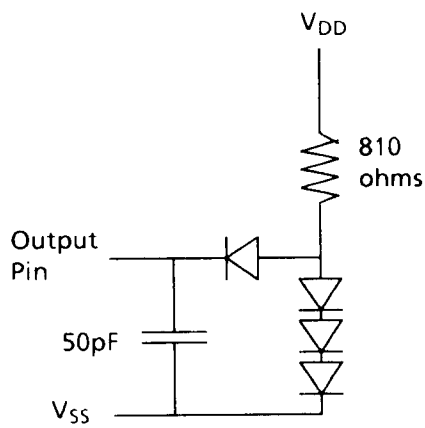

Figure 4. A.C. Output Test Load

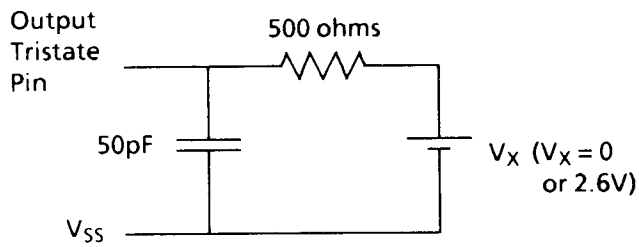

Figure 5. Tri-state Output Delay Load

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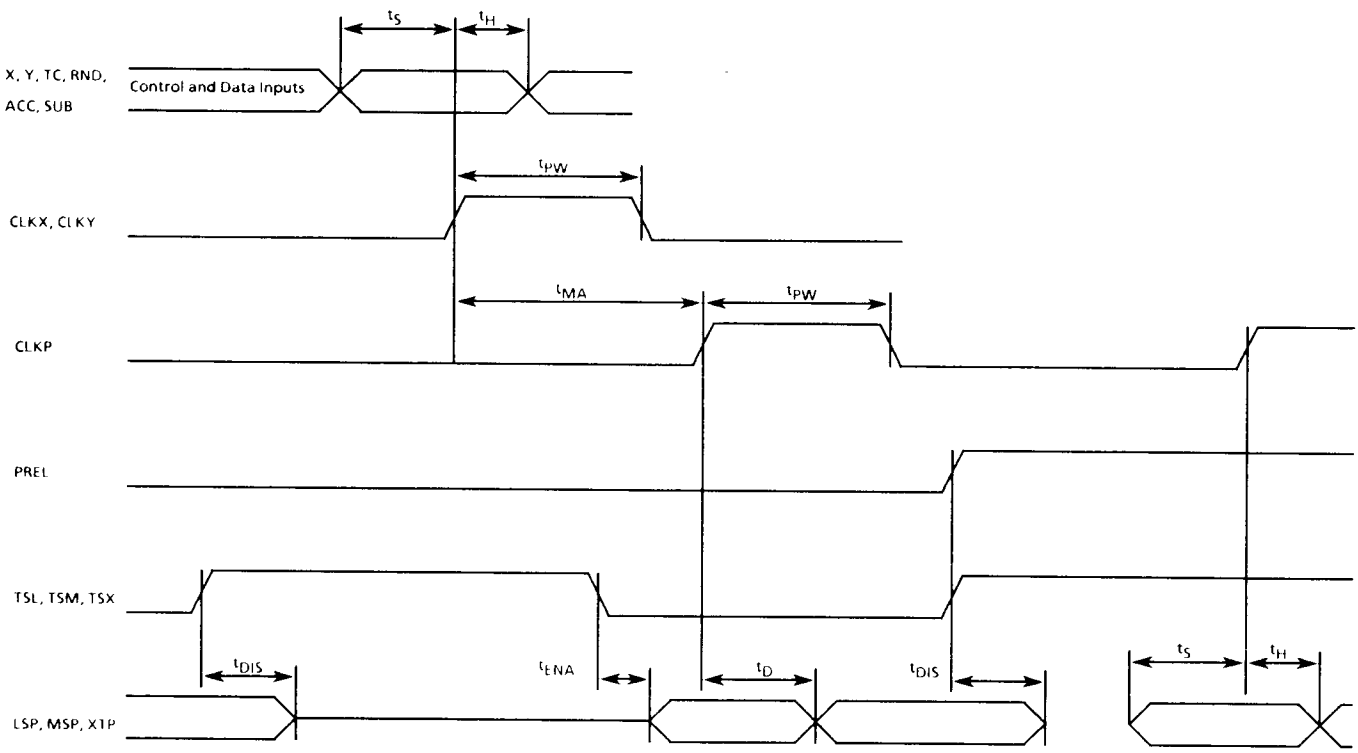
TIMING DIAGRAM



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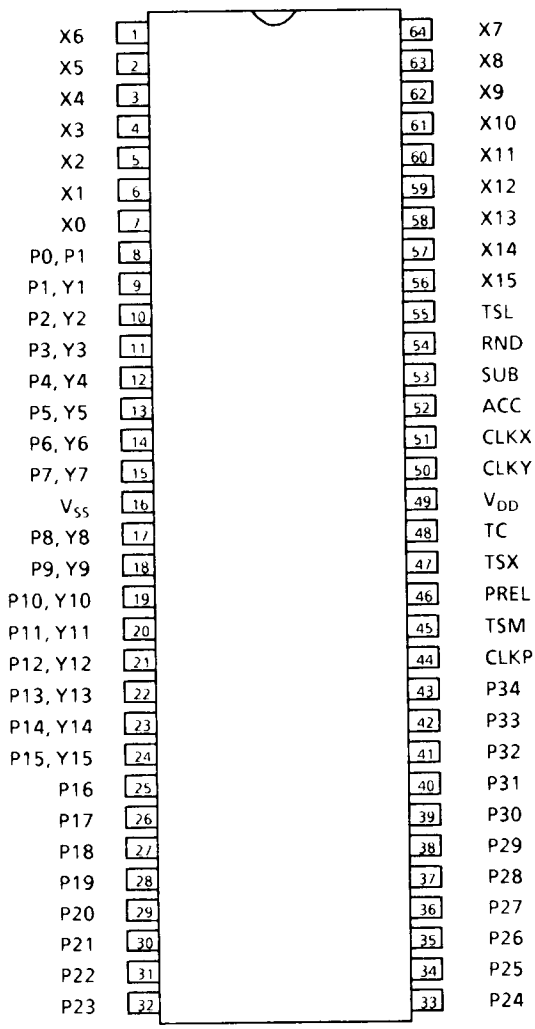
PIN ASSIGNMENTS

64-Pin DIL



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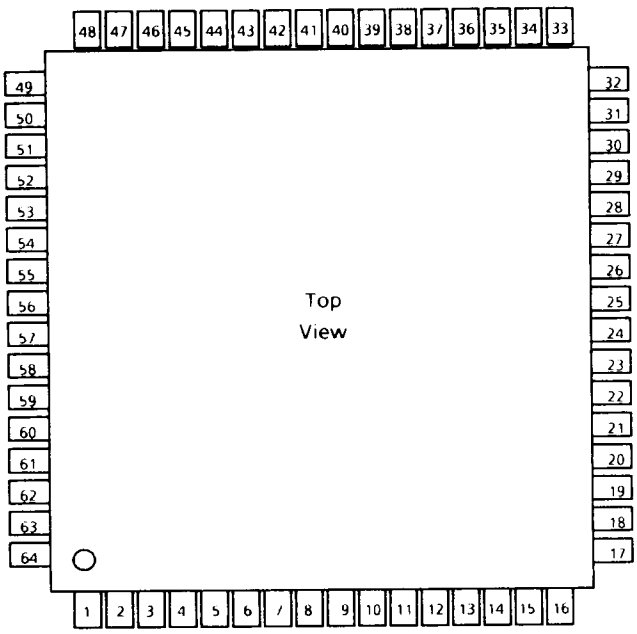
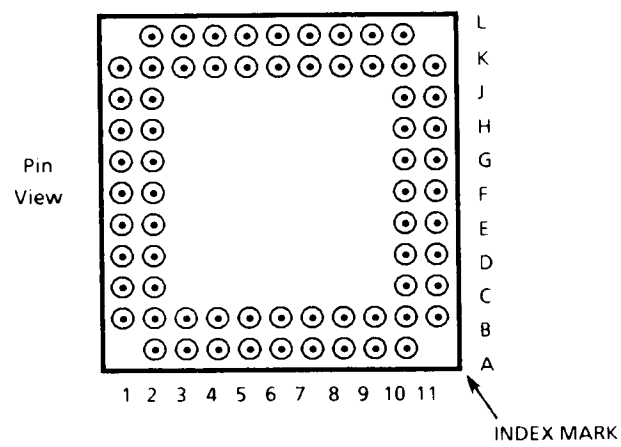
PIN ASSIGNMENTS (cont)

64-PIN LEADED FLATPACK



1	P31	17	P15, Y15	33	P0, Y0	49	X15
2	P30	18	P14, Y14	34	X0	50	TSL
3	P29	19	P13, Y13	35	X1	51	RND
4	P28	20	P12, Y12	36	X2	52	SUB
5	P27	21	P11, Y11	37	X3	53	ACC
6	P26	22	P10, Y10	38	X4	54	CLKX
7	P25	23	P9, Y9	39	X5	55	CLKY
8	P24	24	P8, Y8	40	X6	56	VDD
9	P23	25	VSS	41	X7	57	TC
10	P22	26	P7, Y7	42	X8	58	TSX
11	P21	27	P6, Y6	43	X9	59	PREL
12	P20	28	P5, Y5	44	X10	60	TSW
13	P19	29	P4, Y4	45	X11	61	CLKP
14	P18	30	P3, Y3	46	X12	62	P34
15	P17	31	P2, YY2	47	X13	63	P33
16	P16	32	P1, Y1	48	X14	64	P32

68-Pin Grid Array



E1	X6	L5	V_{DD}	G11	P25	A7	P8, Y8
F2	X7	K6	FT	F10	P24	B6	V_{SS}
F1	X8	L6	$\overline{RST}$	F11	P23	A6	V_{SS}
G2	X9	K7	TC	E10	P22	B5	P7, Y7
G1	X10	L7	TSX	E11	P21	A5	P6, Y6
H2	X11	K8	PREL	D10	P20	B4	P5, Y5
H1	X12	L8	TSM	D11	P19	A4	P4, Y4
J2	X13	K9	CLKP	C10	P18	B3	P3, Y3
J1	X14	L9	P34	C11	P17	A3	P2, Y2
K1	X15	L10	P33	B11	P16	B2	P1, Y1
K2	TSL	K10	P32	B10	P15, Y15	A2	P0, Y0
L2	RND	K11	P31	A10	P14, Y14	B1	X0
K3	SUB	J10	P30	B9	P13, Y13	C2	X1
L3	ACC	J11	P29	A9	P12, Y12	C1	X2
K4	CLKX	H10	P28	B8	P11, Y11	D2	X3
L4	CLKY	H11	P27	A8	P10, Y10	D1	X4
K5	V_{DD}	G10	P26	B7	P9, Y9	E2	X5

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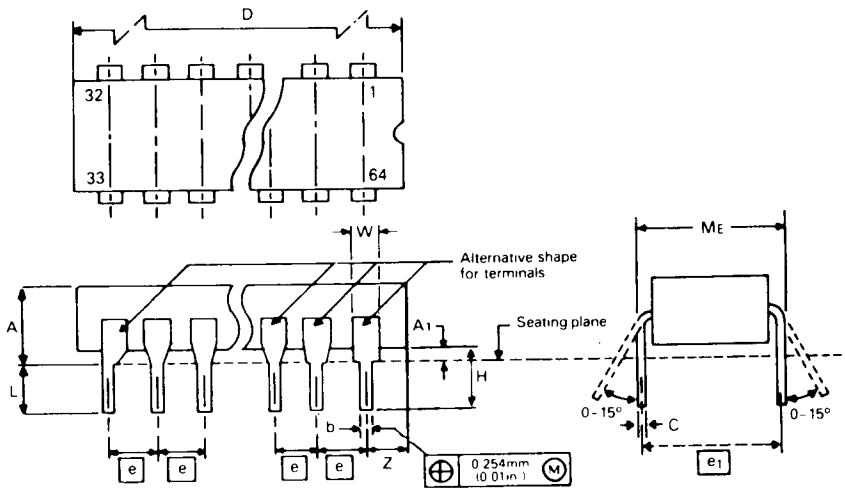
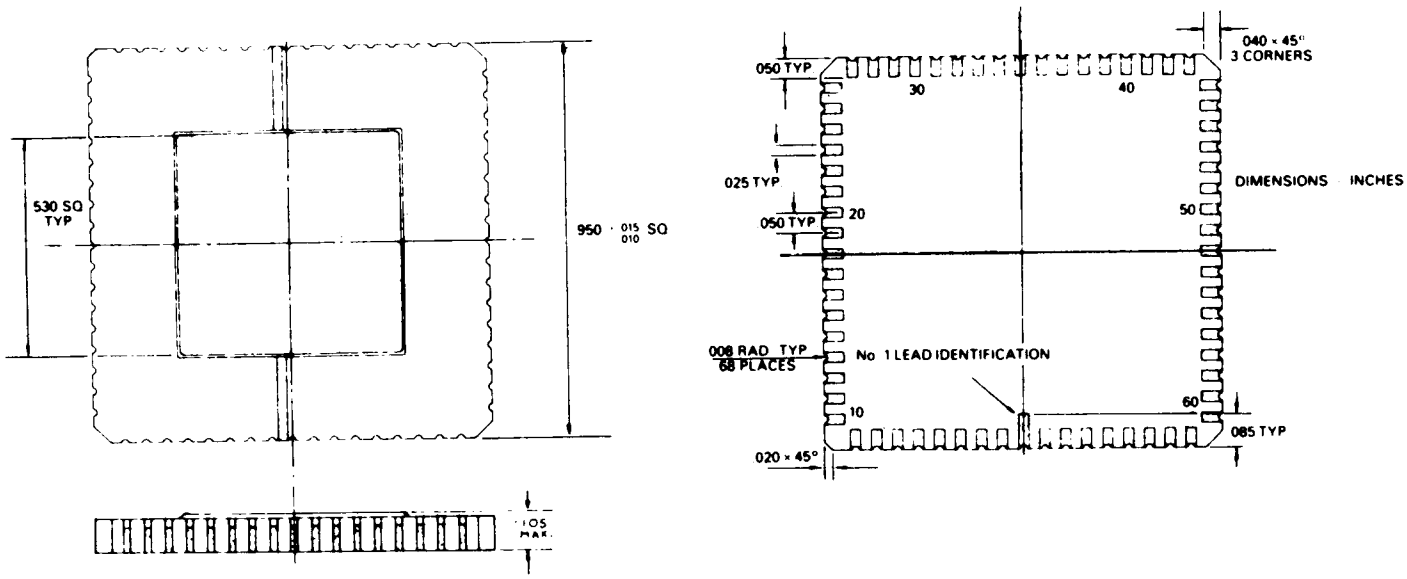
PACKAGE OUTLINE

64 PIN CERAMIC DUAL-IN-LINE



Ref.	Millimetres		
	Min	Nom	Max
A			5.60
A_1	0.38		1.53
b	0.35		0.59
c	0.20		0.36
D			82.10
e		2.54TP	
e_1		23.52TP	
H	4.71		5.38
M_E			23.52
Z			1.27
W			1.53

68 LEADLESS CHIP CARRIER



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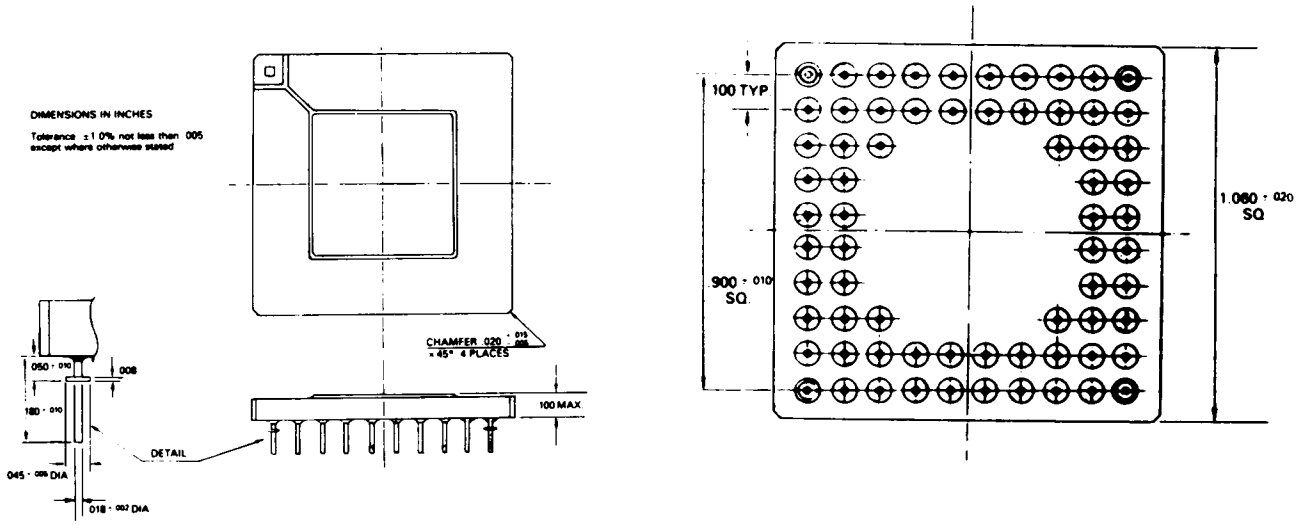
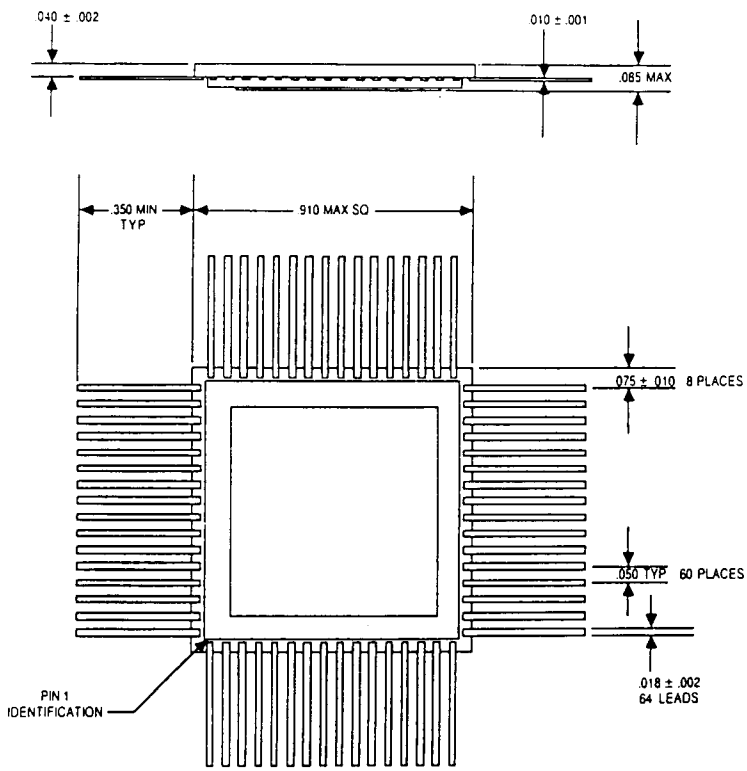
PACKAGE OUTLINE (cont)

68 LEAD PIN GRID PACKAGE



64 PIN LEADED FLATPACK



FLAT PACK

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TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

RADIATION PERFORMANCE

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Total Dose (Function to 1MRad (Si) specification)	$1x10^6$ Rad(Si)
Transient Upset (Stored data loss)	$3x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Latch-up	Not possible

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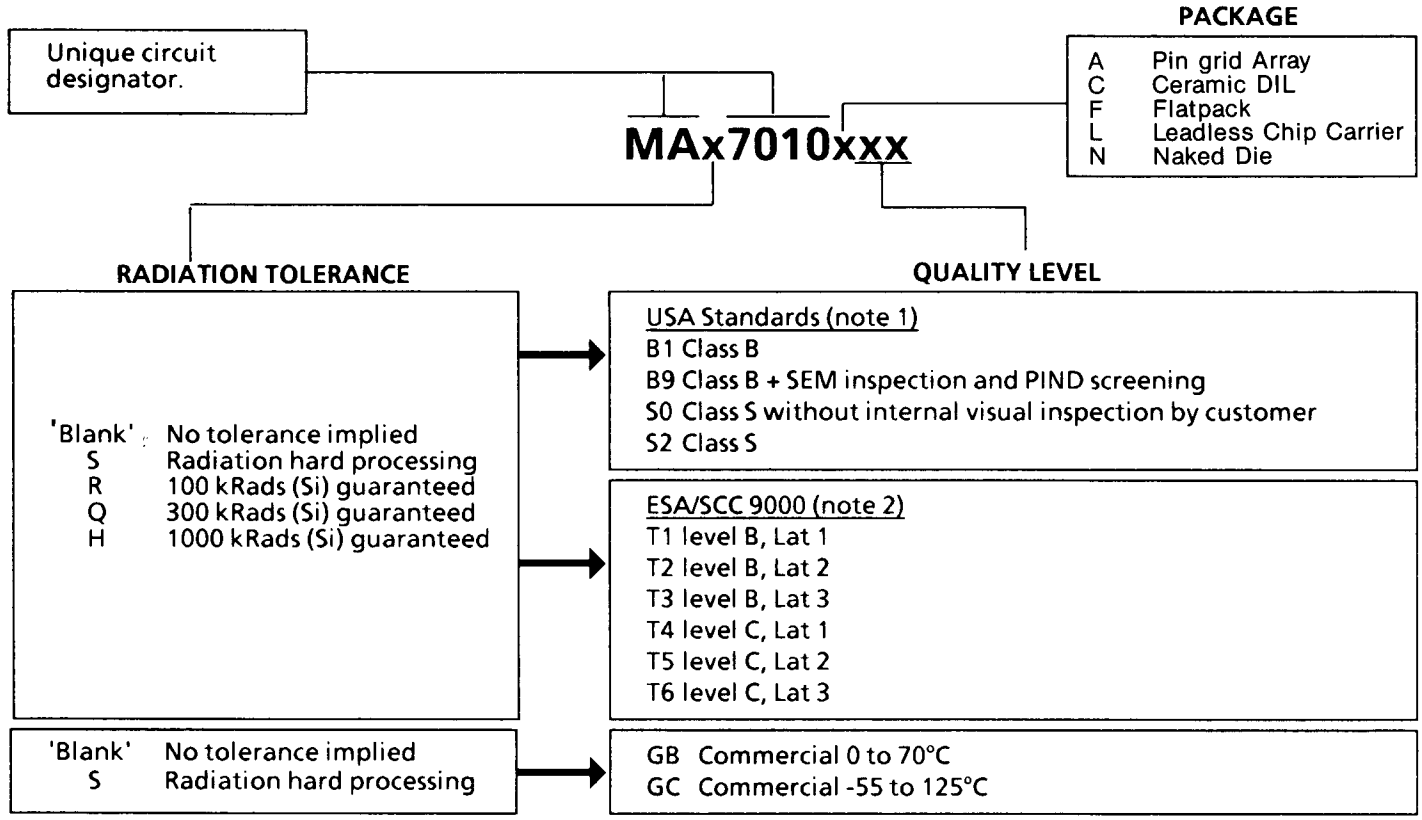
ORDERING INFORMATION



1 Marconi Electronic Devices quality levels conform to MIL STD 883C class B/S, screening method 5004 and Quality Conformance Inspection method 5005 . This does not imply DESC certification, however MIL-M-38510 qualified product listing is being sought.

2 Marconi's specifications for European Space manufacturing flows, including their associated screening procedures, conform to ESA/SCC Generic Specification No.9000. A Process Identification Document, describing the manufacture of these devices, has been approved by the European Space Agency.