

# Fast Logic

# Programmable Pulse Discriminator

SERIES: PPD-56  
(6 BIT) TTL Interfaced



### Description:

The Programmable Discriminator Module, PPD-56 series, is a very powerful and versatile unit. It can be used to discriminate high pulse width or low pulse width or a limited range of pulse widths. It can be used as a programmable delay line with 7-Bit programmability. As an added feature it provides STATUS condition for selector A & B. By tying  $E_A$  &  $E_B$  to ground, the module becomes a programmable delay line and the delayed output signal is given by

$$A_{\text{DELAYED}} = 18 \text{ ns} + (A_0 - A_5) \cdot \text{INCREMENT}$$

$$B_{\text{DELAYED}} = A_{\text{DELAYED}} + (B_0 - B_5) \cdot \text{INCREMENT} + 9 \text{ ns}$$

Tying  $E_B$  to ground and  $E_A$  to positive level, the unit becomes a discriminator passing all pulse widths greater than programmed Selector A in accordance with the formula.

$$PW_{\text{LOWER LIMIT}} = 8 \text{ ns} + (A_0 - A_5) \cdot \text{INCREMENT}$$

Tying  $E_A$  to ground and  $E_B$  to positive level, the unit becomes a discriminator passing all pulse widths less than the programmed Selector B in accordance with the formula.

$$PW_{\text{UPPER LIMIT}} = PW_{\text{LOWER LIMIT}} + (B_0 - B_5) \cdot \text{INCREMENT} - 3 \text{ ns}$$

Tying both  $E_A$  and  $E_B$  to positive level, the unit becomes a discriminator passing only a range of Pulse Widths defined by the equation:

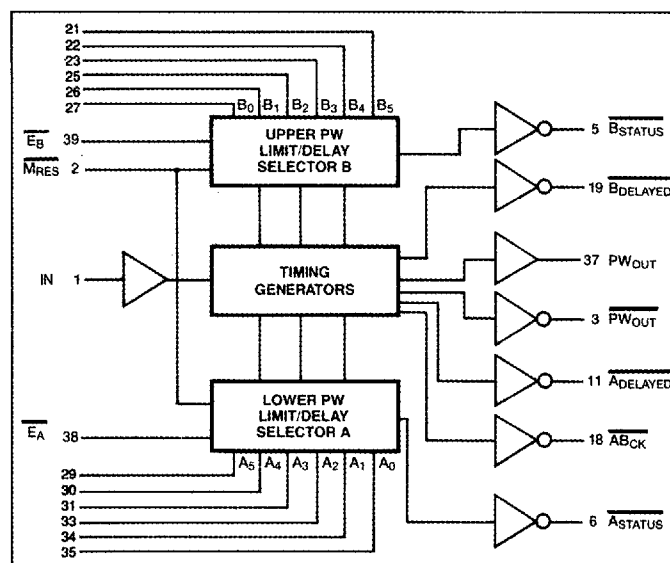
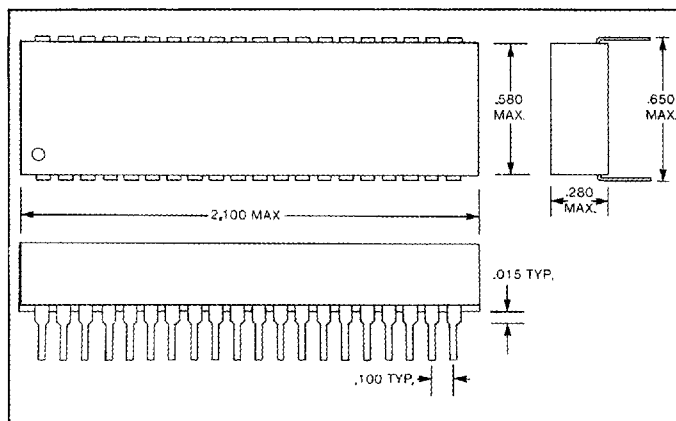
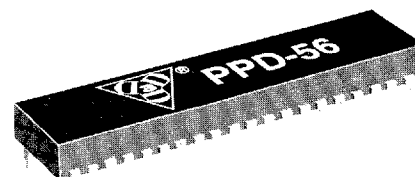
$$PW_{\text{RANGE}} = PW_{\text{UPPER LIMIT}} - PW_{\text{LOWER LIMIT}}$$

### Specifications:

- Discriminator input signal**
  - Minimum Pulse Width High ( $PW_H$ ): 11 ns or  $1/8$  of max. SELECT B, whichever is greater.
  - Minimum Pulse Width Low ( $PW_L$ ): 11 ns or (SELECT B-SELECT A) + 3 ns or  $1/8$  of max. SELECT B, whichever is greater.
  - Minimum Period =  $PW_H + PW_L$
- Programmable delay input signal**
  - Minimum Pulse Width High ( $PW_H$ ): 8 ns or  $1/8$  of max. SELECT B, whichever is greater.
  - Minimum Period:  $2 \times PW_H$
- Supply voltage:** 5 Vdc  $\pm 5\%$
- Supply current:**
  - $I_{CCL} = 80 \text{ ma typ.}$
  - $I_{CCH} = 190 \text{ ma typ.}$
- Operating temperature:** 0°C to 70°C (-55°C to + 125°C on request)\*
- Temperature coefficient:** 100 PPM/°C
- DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.

\*Add "M" after P/N. Ex. PPD-56-5M

Part No.	Incremental Pulse-Width/Delay (Selector A)(ns)	Total Programmed Pulse-Width/Delay (Selector A)(ns)	Incremental Pulse-Width/Delay (Selector B)(ns)	Total Programmed Pulse-Width/Delay (Selector B)(ns)
PPD-56-.5	.5 $\pm$ .3	31.5	.5 $\pm$ .3	31.5
PPD-56-1	1 $\pm$ .5	63	1 $\pm$ .5	63
PPD-56-2	2 $\pm$ .5	126	2 $\pm$ .5	126
PPD-56-3	3 $\pm$ 1.0	189	3 $\pm$ 1.0	189
PPD-56-4	4 $\pm$ 1.0	252	4 $\pm$ 1.0	252
PPD-56-5	5 $\pm$ 1.5	315	5 $\pm$ 1.5	315
PPD-56-6	6 $\pm$ 1.5	376	6 $\pm$ 1.5	376
PPD-56-7	7 $\pm$ 1.5	441	7 $\pm$ 1.5	441
PPD-56-8	8 $\pm$ 2.0	504	8 $\pm$ 2.0	504
PPD-56-9	9 $\pm$ 2.0	567	9 $\pm$ 2.0	567
PPD-56-10	10 $\pm$ 2.0	630	10 $\pm$ 2.0	630

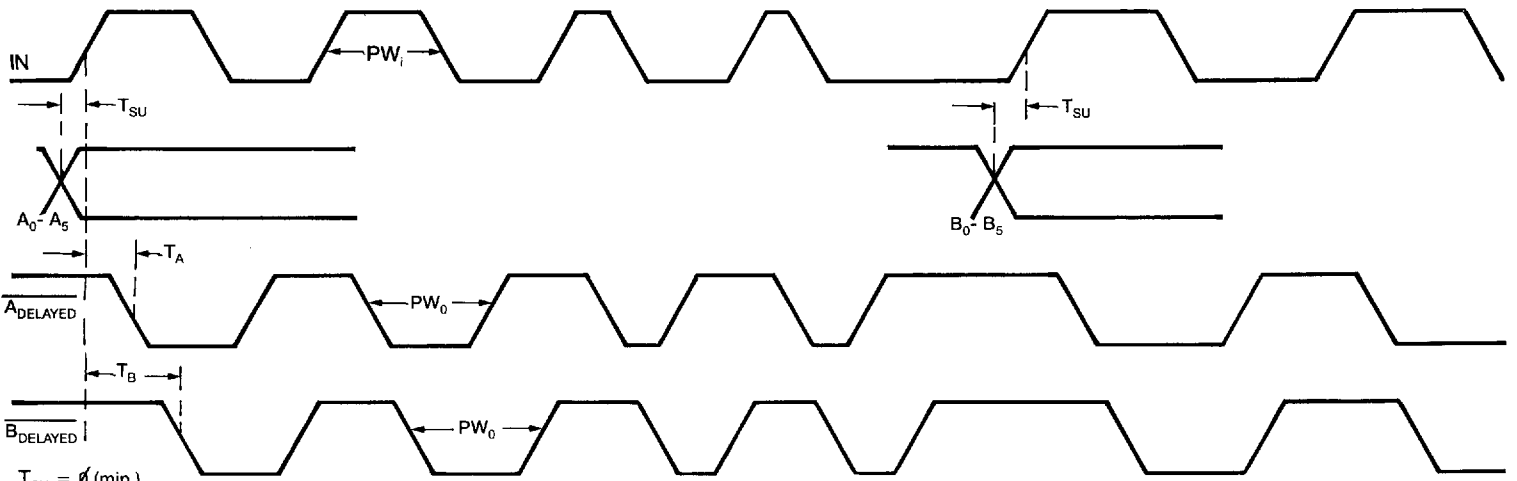


Vcc = 24, 28, 32, 36, 40 GRD = 4, 8, 12, 16, 20

Timing Waveform (see other side)

**Delay Function**

PPD-56 (cont'd)



$T_{SU} = \emptyset$  (min.)

$PW_i = PW_0$

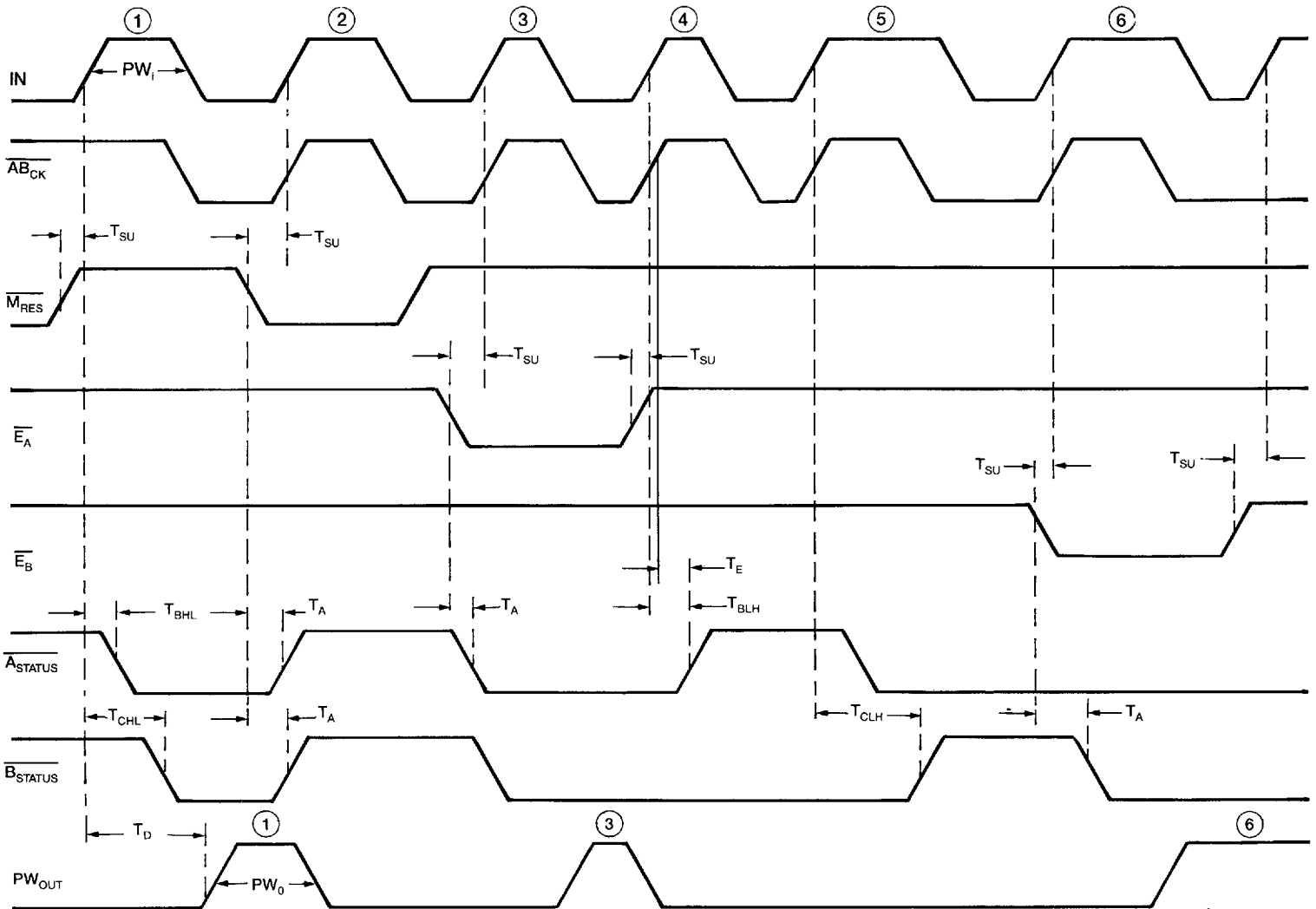
$(A_0 - A_5) = \emptyset$   
 $(A_0 - A_5) \neq \emptyset$

$T_A = 18 \text{ ns}$   
 $T_A = 18 \text{ ns} + (A_0 - A_5) * \text{INCREMENT}$

$(A_0 - A_5), (B_0 - B_5) = \emptyset$   
 $(A_0 - A_5), (B_0 - B_5) \neq \emptyset$

$T_B = 27 \text{ ns}$   
 $T_B = 27 \text{ ns} + (A_0 - A_5) * \text{INCREMENT} + (B_0 - B_5) * \text{INCREMENT}$

**Discriminator Function**



$PW_i = PW_0$   
 $U = \emptyset$

$T_A = 4 \text{ ns typ.}$   
 $T_E = 15 \text{ ns min.}$

$(A_0 - A_5) = \emptyset$   
 $(A_0 - A_5) \neq \emptyset$

$T_{BHL} = 22 \text{ ns}$   
 $T_{BLH} = 21 \text{ ns}$   
 $T_{BHL} = 22 + (A_0 - A_5) * \text{INCREMENT}$   
 $T_{BLH} = 21 + (A_0 - A_5) * \text{INCREMENT}$

$(A_0 - A_5), (B_0 - B_5) = \emptyset$

$T_{CHL} = 30 \text{ ns}$

$(A_0 - A_5), (B_0 - B_5) \neq \emptyset$

$T_{CLH} = 29 \text{ ns}$   
 $T_{CHL} = 30 + [(A_0 - A_5) + (B_0 - B_5)] * \text{INCREMENT}$   
 $T_{CLH} = 29 + [(A_0 - A_5) + (B_0 - B_5)] * \text{INCREMENT}$

$(A_0 - A_5), (B_0 - B_5) = \emptyset$

$(A_0 - A_5), (B_0 - B_5) \neq \emptyset$

$T_D = 35 \text{ ns}$   
 $T_D = 35 + [(A_0 - A_5) + (B_0 - B_5)] * \text{INCREMENT}$

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