

SY0004

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PRELIMINARY

- **INTRODUCTION**

The SY0004 is an accurate time and frequency source that has been designed as a module level subsystem. The module is designed to work within ATM, SONET, SDH, and wireless systems where synchronization is vital. The SY0004 is an excellent synchronization solution for timing, jitter and wander topics specified within ITU-T Recommendations G.812, and Bellcore GR-1244-CORE. The SY0004 is designed for Stratum 3E applications, but also has certain features that can make it useful for other kinds of system clocks.

- **FEATURES**

A synchronization solution for timing, jitter and wander concerns in a single module.

Complies with ITU-T Recommendations G.812 - Type III and Bellcore GR-1244-CORE for Stratum 3E applications.

Supports four modes of operation: Locked to Reference 1, Locked to Reference 2, Holdover and Free-run.

Accepts reference inputs from two independent sources from 8 kHz to 77.76 MHz.

Provides two outputs up to 77.76 MHz and one up to 2.048MHz.

Loop filtering utilizing application specific software in the digital signal processor (DSP).

Continuously monitors and evaluate input reference signals.

Creates a history buffer for Holdover mode operation.

Manual or Automatic selection between timing modes.

Alarm and status signal.

Host interface and JTAG port.

Small dimensions of 3.9 x 2.4 x 0.9 inch.

- **APPLICATION**

The SY0004 performs clock regeneration as a Synchronous Equipment Clock (SEC), or STRATUM 3E in ATM, SDH, PDH, and SONET networks. It is designed for manufacturers of network equipment, especially Access Switches, Core Switches, Cross Connects, Digital Multiplexers-Exchangers, and SDH/SONET equipment. The unit is also suitable for PCS, WLL, and Wireless Base Stations. Wherever a Timing unit with high performance specifications is required, the SY0004 can be integrated into the network system and provide all necessary frequencies and interfaces. The input stage can receive two different input reference signals at various rates from 4 kHz to 77.76 MHz. An optional application can be achieved by integrating the SY0004 with a low cost GPS receiver and locking it to the GPS 1 pps output signal.

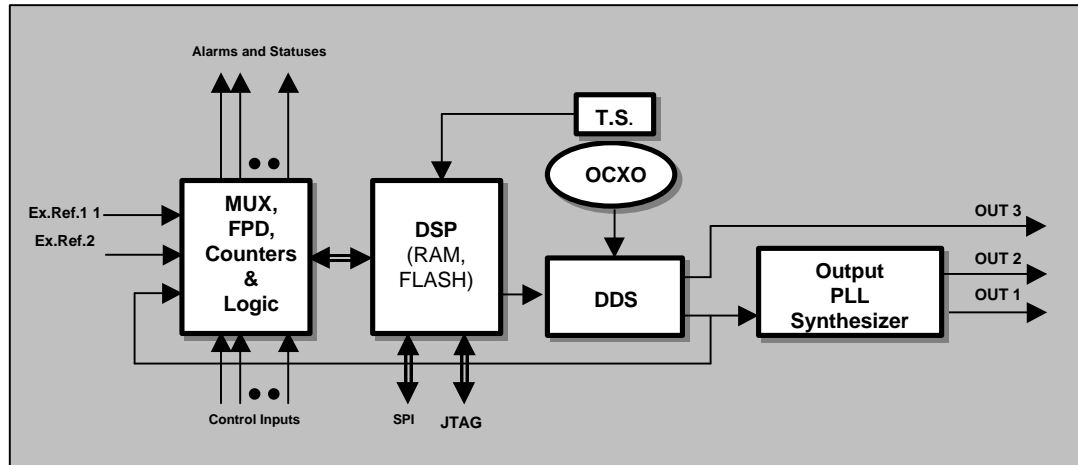


Figure 1. - The functional block diagram of SY0004

• DESCRIPTION

The SY0004 synchronization module is a Digital PLL (DPLL), which utilizes application specific software in the digital signal processor (DSP). The DSP is complemented by fast hardware logic (CPLD) where all multiplexers, counters, dividers, phase detectors, output frequency converters and other control logic circuits are completely implemented. The module uses Direct Digital Synthesis (DDS) technique combine with high stability OCXO in order to provide accurate and fast response in the DPLL and eliminate requirements for an OCXO with high pull. The output of the DDS is connected to an output PLL synthesizer that generates two output signals. The third output comes from DDS. The SY0004 provides several other features such as: switching between the references inputs on the basis of monitoring and estimation of the input signals and internal state diagram; real time calculation of the filtering algorithm for jitter and wander in according to the approved standards; alarm, status and messaging functions; controlling the internal references in regard of frequency vs. temperature (utilizing temperature measurement with T.S.), aging and calibration effects etc. The three wires serial communication interface - SPI provides flow of messages between the module and host computer. The JTAG interface provides an easy way for re-programming the unit with future versions of software without removing from the systems.

✓ The module operates in the following four timing modes:

Free-run

In this mode the unit is unlocked to either of the inputs. The accuracy of the output frequencies in this mode is ± 4.6 ppm. Free-run mode is typically used when a master clock source is required, not valid history of data for the Holdover mode, or immediately following system power-up before network synchronization is achieved. In the Free-run Mode, the SY0004 provides timing and synchronization signals that are based on the accuracy of on-board oscillators only, and are not synchronized to the reference signals.

Holdover

In this mode the module has lost its reference inputs and is utilizing stored timing data, called history, to control the output frequency. Holdover Mode is typically used while network synchronization is temporarily disrupted. In Holdover Mode, the SY0004 provides timing, based on data from the history buffer, while unlocked to an external reference signal. The history data is determined while the device is locked to an external reference signal. The stability of the output signal in holdover mode depends primarily on the stability of on-board oscillator and should be better than 10ppb in the first 24 hours. The SY0004 uses an OCXO as an on-board oscillator but other types of oscillators are available.

Locked to Ref.1

In this mode the output of the module is phase locked to input reference 1.

Locked to Ref.2

In this mode the output of the module is phase locked to input reference 2.

- Input References**

The SY00004 module accepts two input references EX REF1 and EX REF2. End users can specify the frequencies within a range of 8 kHz to 77.76 MHz. The input reference signals are HCMOS/TTL levels with timing characteristic in according to Bellcore GR-1244-core 3.2.1.R3-1 or equivalent standards. Please note that the end user must specify the two input frequencies at the time of order.

- Output Signals**

The SY0004 module provides three output signals OUT1, OUT2 and OUT3. The first two outputs are generated by the output PLL synthesizer and scaled by the output frequency converters and the third one is generated by DDS. The performance of the module significantly depends on the internal oscillator and special care was taken to define its specification. A high stability Oven Controlled Crystal Oscillator (OCXO) is used as the internal oscillator in order to provides stable internal reference in all operating conditions.

- Specifications**

General Specifications	Mechanical	3.9" (D) x 2.4" (W) x 0.9" (H)	Metal box, 24p dual-in-line
	Power	5VDC, 3W after warm up time	
	Environment	Operating Temperature Storage Temperature Humidity	-20°C to 60°C -40° to 85°C 5% to 95% non-condensing
	Internal Oscillator	Ovenized Crystal Oscillator (OCXO)	High Stability SC-cut OCXO
Input Signals	Number of Inputs	2	
	Input reference frequency	8kHz to 77.76MHz	User selectable
	Signal Level	HCMOS/TTL Compatible	
	Time Reference characteristics	Bellcore: GR-1244-core 3.2.1.R3-1	
Output Signal	Number of Outputs	3	
	Output 1	8kHz to 77.76MHz	HCMOS, frequency user define
	Output 2	8kHz to 77.76MHz	HCMOS, frequency user define
	Output 3	8kHz,1.544MHz or2.048MHz	HCMOS, frequency user define
Signal Quality Performance	Jitter Tolerance		Bellcore: GR-1244-core 4.2 ITU-T: G.813
	Phase Transient Tolerance		Bellcore: GR-1244-core 4.4
	Wander Generation		Bellcore: GR-1244-core 5.3 ITU-T: G.812
	Wander Tolerance		Bellcore: GR-1244-core 4.3 ITU-T: G.812
	Jitter Generation and Transfer		Bellcore: GR-1244-core 5.5 ITU-T: G.812
	Wander Transfer		Bellcore: GR-1244-core 5.4 ITU-T: G.812
Frequency Output Performance	Free run accuracy	±4.6ppm	GR-1244-core 5.1 ITU-T: G.812
	Holdover frequency stability	±1x10 ⁻⁸ for 24hours	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Initial Offset	±1x10 ⁻⁹	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Temperature	±8x10 ⁻⁹	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Drift	±1x10 ⁻⁹	Bellcore: GR-1244-core 5.2 ITU-T: G.812
	Phase Build-Out		Bellcore: GR-1244-core 5.7 ITU-T: G.812
	DPLL bandwidth	0.001Hz	
	Lock Time	<700sec	GR-1244-core 3.7
	Lock accuracy	±1x10 ⁻¹¹	

- Pin Assignment**

On the picture below it is shown the pin-out for the SY0004. The design is done in such a way that it can support basically any other pin-out without changes in the hardware. For other pin-out requirements please contact the Raltron.

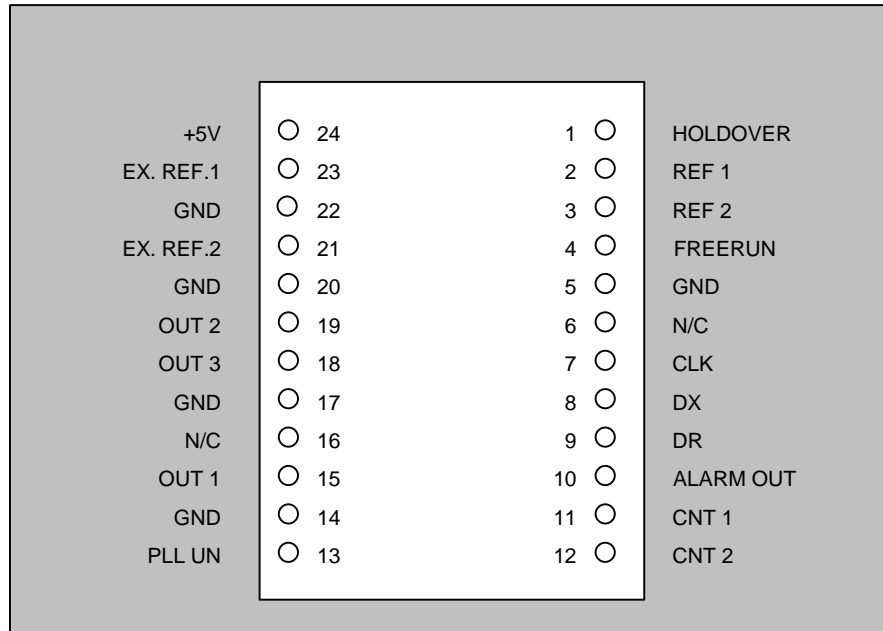
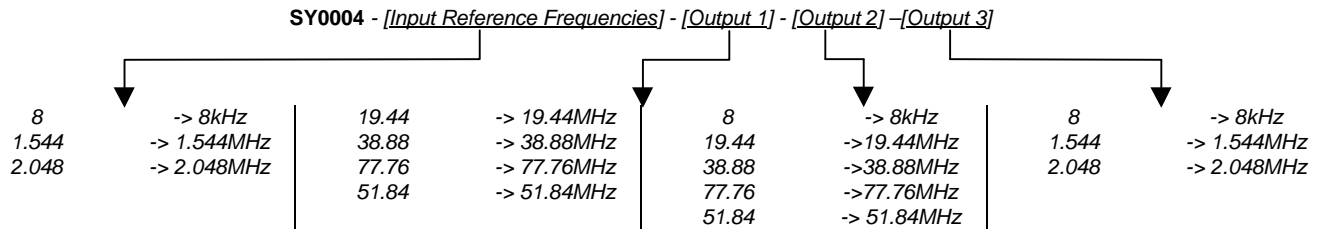


Figure 4 – Bottom view

Pin #	Name	Description
1	HOLDOVER	Holdover Signal -> the unit is in holdover mode, Signal Output
2	REF 1	Reference 1 Signal -> the unit is enslaved to the reference 1, Signal Output
3	REF 2	Reference 2 Signal -> the unit is enslaved to the reference 2, Signal Output
4	FREERUN	Freerun Signal -> the unit is in the free run mode, Signal Output
6, 16	N/C	Not connected
7	CLK	Serial Clock -> host interface, clock pin, Input
8	DX	Data Transmit -> host interface, transmit pin, Output
9	DR	Data Receive -> host interface receive pin, Input
10	ALARM OUT	Alarm signal, Signal Output
11	CNT 1	Control Input 1 -> the external input for selecting mode of the unit, Input
12	CNT 2	Control Input 2 -> the external input for selecting mode of the unit, Input
13	PLL UN	PLL Unlocked Signal -> the PLL is not locked, Signal Output
5,14,16,17,20,22	GND	Ground
24	+5V	Positive Voltage Supply
15	OUT 1	Synchronized Output 1-> the primary output from PLL synthesizer, Output
18	OUT 2	Synchronized Output 2-> the secondary output from PLL synthesizer, Output
19	OUT 3	Synchronized Output 3-> the secondary output from DDS, Output
23	EX REF1	External Reference 1 Input -> the input from reference 1, Input
21	EX REF 2	External Reference 2 Input -> the input from reference 2, Input

For other pin-out configurations contact the factory!

◆ Ordering Information



For other frequencies contact the factory!
Example: SY0004-8-19.44-19.44-8

• Mechanical dimensions

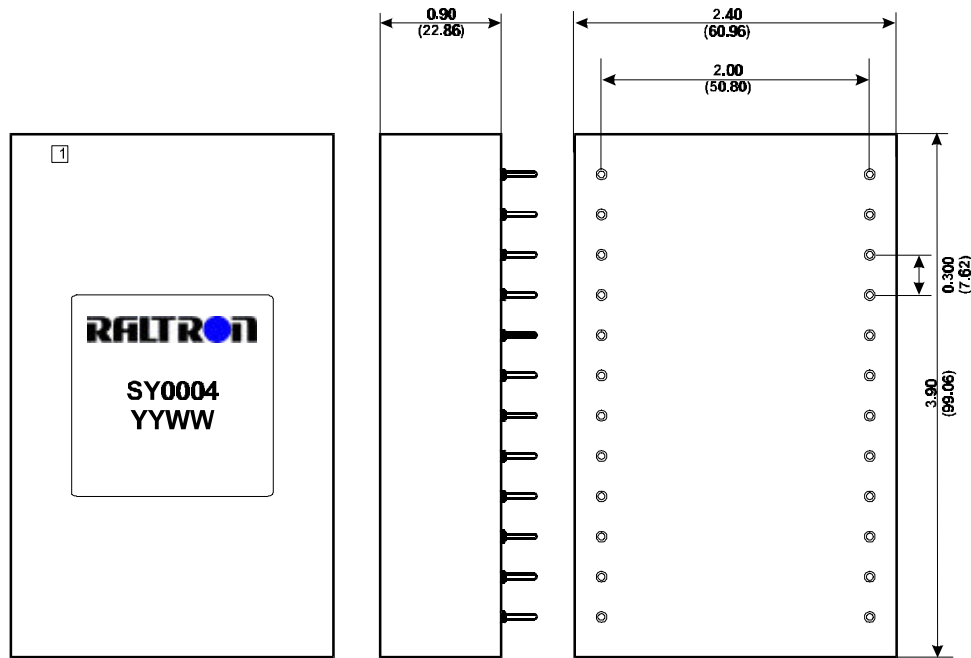


Figure 5 – The mechanical dimensions.

Figure 5 shows the mechanical dimension of the SY0004 module. The module can be supplied in three different types of packaging:

- ✓ Hermetically sealed metal box
- ✓ Metal box
- ✓ Module without packaging

The dimensions shown on the picture are valid for first and second type of packaging, the actual dimensions for the third type are 2.2 x 3.75 x 0.75" keeping the pin-out dimensions the same for all of three. The label on the module shows part number, factory name, week and year of production.

