# 155Mbps Fiber-Optic PIN Pre-Amplifier with AG

## GENERAL DESCRIPTION

The CS6710 is a trans-impedance amplifier with A GC for 155Mbps fiber channel applications. The A GC function allows -39dB to +3dB input dynamic range, thus providing a low cost solution to longer-reach ATM systems.

The CS6710 is fabricated in a standard CMOS process and provided in die form to be assembled with a photodiode into a metal can.

## APPLICATIONS

- Fiber channel
- SDH/SONET
- Ethernet

## FEATURES

- 3.3V or 5V operation.
- 100Ω to 55kΩ single-ended trans-impedance gain with 500Ω termination.
- Minimal 95MHz bandwidth at maximum gain.
- On-chip Automatic Gain Control (AGC).
- Differential outputs drive a high impedance load.
- Available in die form.
- Typical input saturation current of 4.5mA.

## BLOCK DIAGRAM

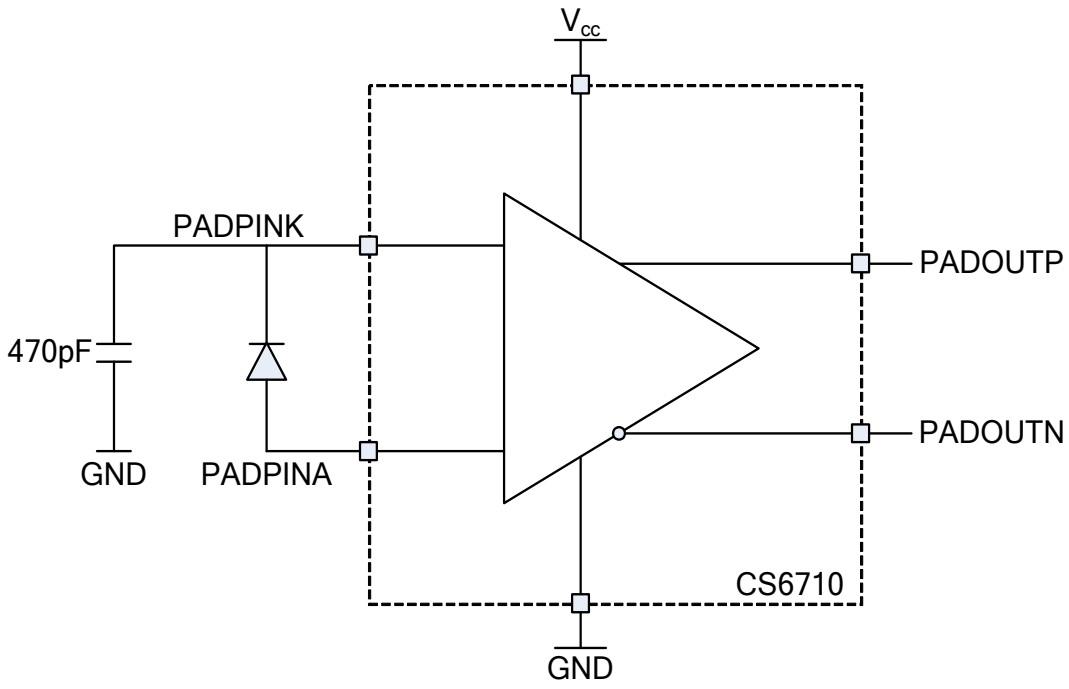



**Figure-1 Block DiagraM**

## DIE CONNECTION DIAGRAM

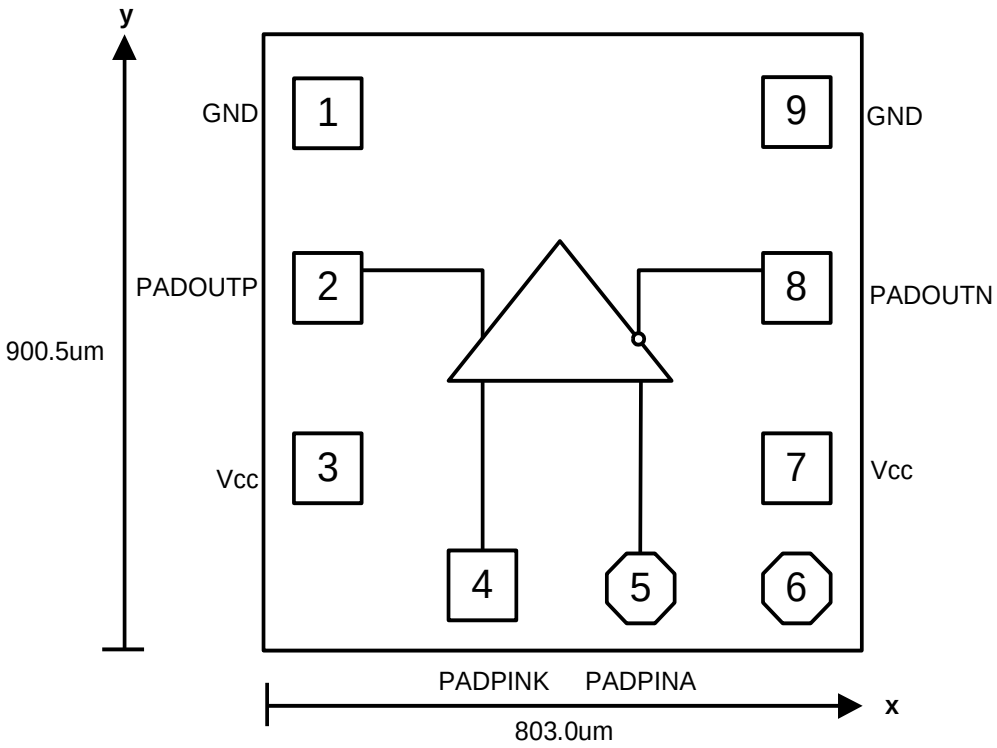



**Figure-2 Die Diagra**

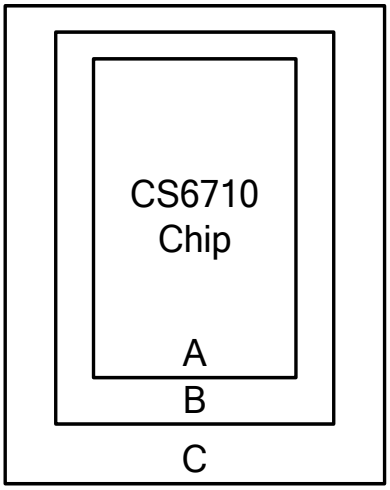
**Bare Die Information**

| Pad No. | Description | X (μm) | Y (μm) |
|---|---|---|---|
| 1 | GND | -352.00 | 261.70 |
| 2 | PADOUTP | -352.00 | 111.70 |
| 3 | Vcc | -352.00 | -261.70 |
| 4 | PADPINK | -135.95 | -352.00 |
| 5 | PADPINA | 153.95 | -360.00 |
| 6 | VH | 352.00 | -361.95 |
| 7 | Vcc | 352.00 | -261.70 |
| 8 | PADOUTN | 352.00 | 111.70 |
| 9 | GND | 352.00 | 261.70 |

*Note: The coordinates start from the center of the die to the center of the pad, and the total die size does not include seal ring and scribe line.*

Area A: total chip size in Figure 2 mentioned 803*900.5 um.
Area B: seal ring, 20um/side
Area C: scribe line residue after die saw,
X=17.5±2.5 um/side, Y=17.5±2.5um/side
Actual size after die-saw,

Max: 883*980.5um, Min: 873*970.5um
Chip thickness: 12mil±1mil



## PIN DESCRIPTION

| Pin Name | Pin No. | Description |
|---|---|---|
| GND | 1.9 | Ground pin. Connect to the most negative supply voltage. |
| PADOUTP | 2 | Differential data output pin. This pin goes high when current follow into pin PADPINA. |
| Vcc | 3,7 | Power pin. Connect to the most positive supply voltage. |
| PADPINK | 4 | Connect to the cathode of the photodiode. |
| PADPINA | 5 | Input pin. Connect to the anode of the photodiode. |
| PADOUTN | 8 | Differential data output pin. Complementary to pin PADOUTP. |
| VH | 6 | Test pin. Measure the voltage of this pin can get the trans-impedance gain. Leave this pin open in typical application circuits. |

## FUNCTIONAL DESCRIPTION

The CS6710 is a trans-impedance pre-amplifier fabricated in a CMOS process. The CS6710 consists of a trans-impedance amplifier, an AGC control block, an output buffer, and a voltage regulator.

**Trans-impedance Amplifier**
The trans-impedance amplifier in CS6710 is a high gain, single ended amplifier with a feedback resistor. The minimum differential output swing is 20mV with high impedance load at -39dBm input. The feedback resistor converts the input current to voltage at the output node.

**AGC Control Block**
The AGC control block changes the feedback resistance in the CS6710 by using a voltage controlled MOS transistor. The AGC control block starts working when the input signal is larger than 1.8μA (-30dBm at 0.9 A/W).

**Output Buffer**
The output of the single-ended amplifier becomes differential signal after going through the output buffer. The output is able to drive a load larger than 500Ω.

**Voltage Regulator**
In order to minimize the influence of power supply on noise performance, a voltage regulator is incorporated in the CS6710. Moreover, the external capacitor also reduces the power supply noise at high frequencies.

## FUNCTIONAL DIAGRAM

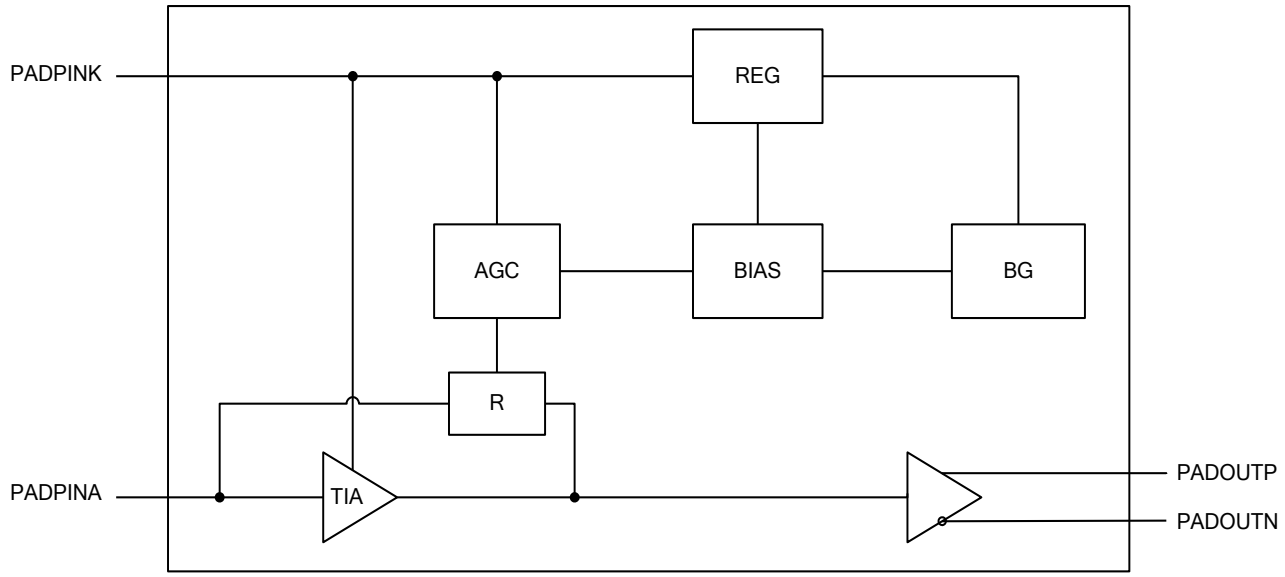
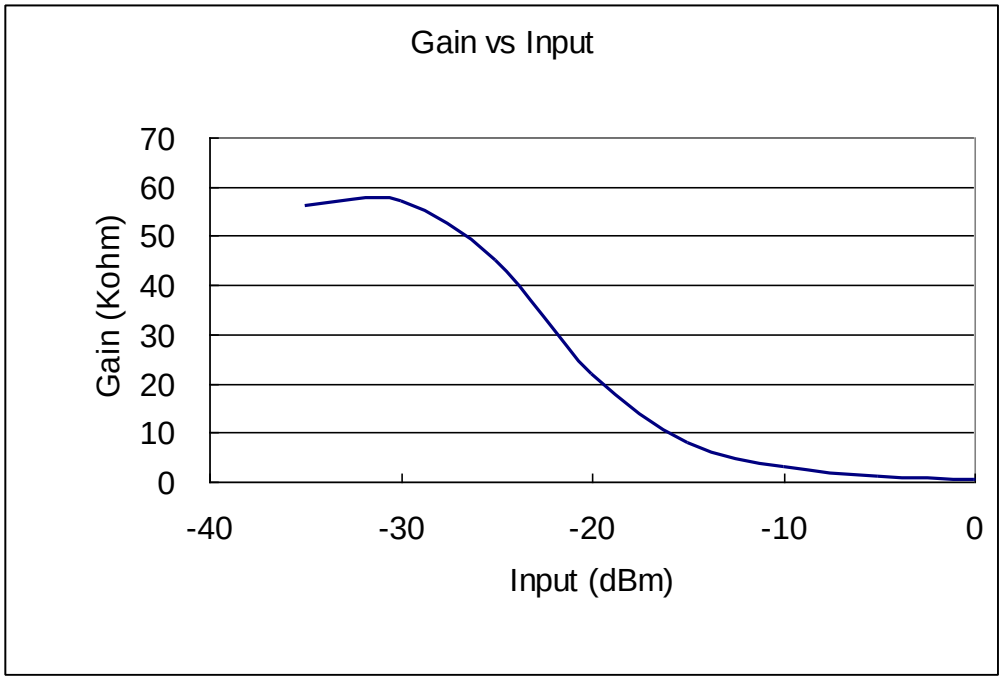
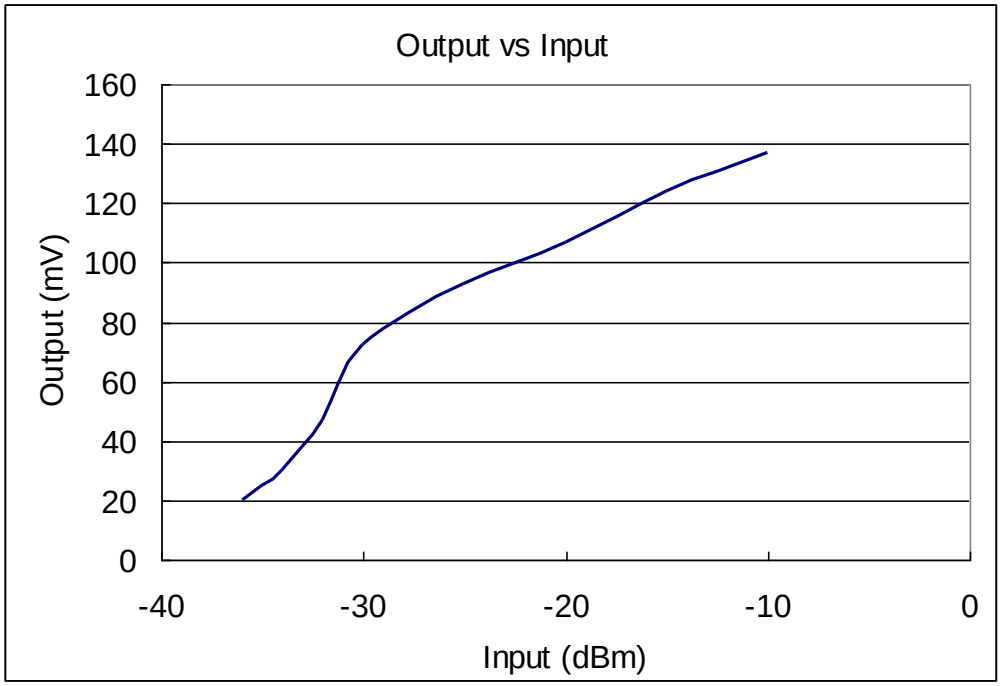


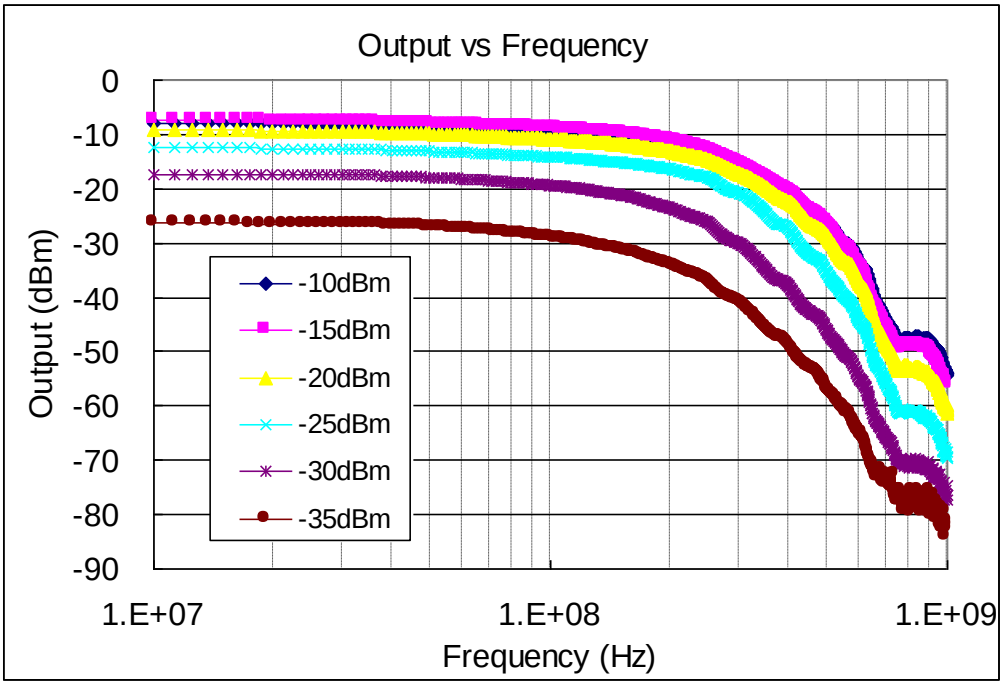

**Figure-3**

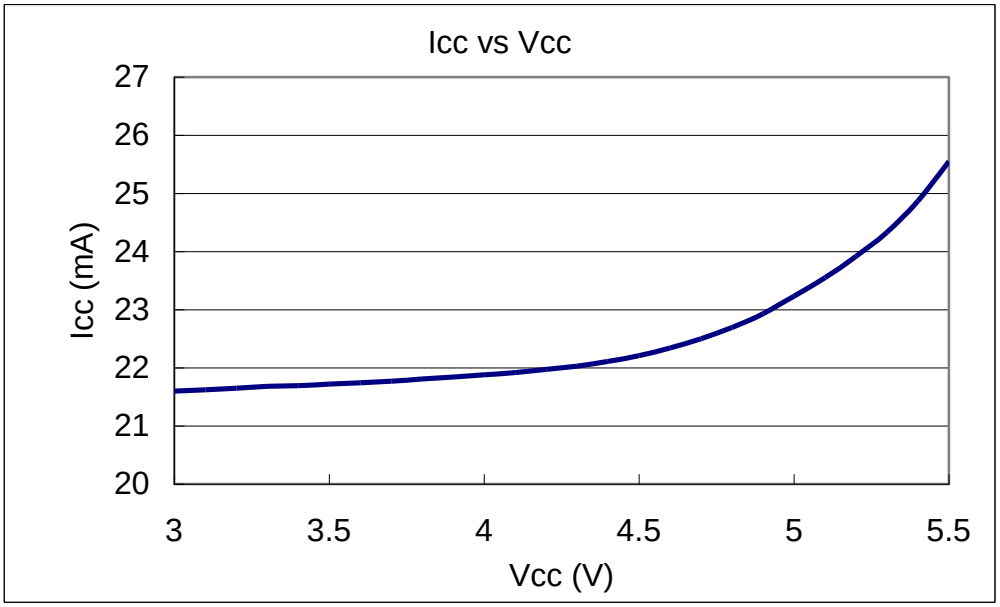
## TYPICAL OPERATING CURVE

(Ta=25°C, $C_{IN}$=1pF, data is collected by single-ended output with 500ohm termination).

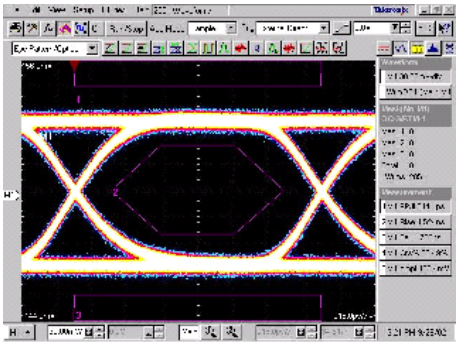


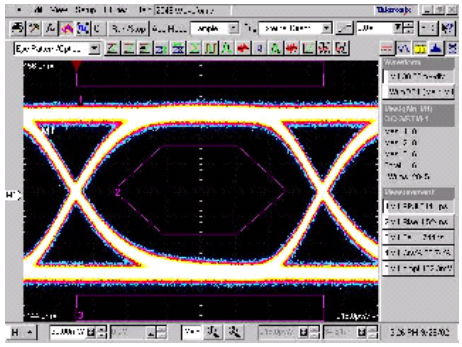

Output vs Frequency
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
Output (dBm)
-10dBm
-15dBm
-20dBm
-25dBm
-30dBm
-35dBm
1.E+07
1.E+08
1.E+09
Frequency (Hz)


Icc vs Vcc
27
26
25
24
23
22
21
20
Icc (mA)
3
3.5
4
4.5
5
5.5
Vcc (V)

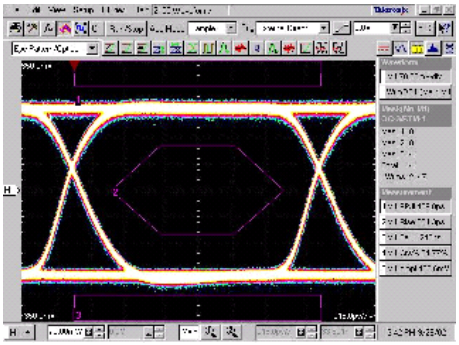
## EYE DIAGRAMS



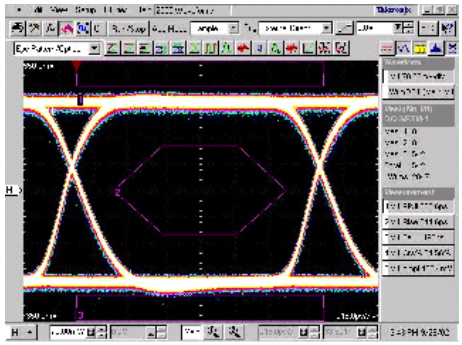
Input 1uA@3.3V



Input 1uA@5V



Input 100uA@3.3V



Input 100uA@5V

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Power supply | 6 | V |
| $T_a$ | Operation ambient temperature range | -40 to +85 | ℃ |
| $T_{STG}$ | Storage temperature range | -65 to +150 | ℃ |

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Power supply range | 3.0 to 5.5 | V |
| $T_a$ | Ambient temperature range | -40 to +85 | ℃ |
| $C_{IN}$ | Total capacitance at the PADPINA pin | 0.7 to 1.0 | pF |

### ELECTRICAL CHARACTERISTICS (DC)

| Symbol | Parameter | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | - | 22 (3.3V)<br>24 (5V) | 32 (3.3V)<br>34 (5V) | mA |
| $V_b$ | PIN bias voltage (PINK-PINA) | 1.5 | 1.65 | 1.8 | V |
| $V_{cm}$ | Common mode output voltage | - | Vcc~2.3 (3.3V)<br>Vcc-2.5 (5V) | - | V |

| | | | | | |
|---|---|---|---|---|---|
| $R_{out}$ | Output impedance (single end) | - | 50 | - | Ω |

**ELECTRICAL CHARACTERISTICS (AC)**

| Symbol | Parameter | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| $I_n$ | Input RMS noise, DC to 100MHz | - | 7.5 | 8.5 | nA |
| PIN, min | Optical sensitivity (note 1) | - | -39 | - | dBm |
| PIN, max | Optical saturation (note 1) | - | 3 | - | dBm |
| $I_{in}$, max | Maximum input current (note 1) | 3.0 | 4.5 | - | mA |
| Gain | Maximum Transimpedance gain with no AGC effect@1MHz(note 3)<br>(single-ended)<br>(differential) | <br><br>45k<br>90k | <br><br>55k<br>110k | <br><br>65k<br>130k | <br><br>Ω<br>Ω |
| | Typical Transimpedancegain over AGC range@1MHz(note 3)<br>(single-ended)<br>(differential) | <br><br>100<br>200 | <br><br>-<br>- | <br><br>55k<br>110k | <br><br>Ω<br>Ω |
| BW | Bandwidth (-3dB)(Note 2) | 95 | - | - | MHz |
| $BW_{(LF)}$ | Small-Signal –3dB Low frequency cutoff | - | - | 30 | kHz |
| $T_r$, $T_f$ | Output rise / fall times (20%~80%) | - | - | 2.2 | ns |
| $T_{pwd}$ | Pulse width distortion | - | - | 10 | % |
| OS | Overshoot | - | - | 10 | % |
| dVout | Differential output voltage (note 3) | - | - | 700 | mV |
| $T_{agc}$ | AGC converging time | - | - | 0.7 | ms |
| PSRR | Power supply rejection ratio | 35 | - | - | dB |

*Note1. With PIN responsivity of 0.9A/W, extinction ratio of 10dB, and BER of 10E-10*
*Note2. With –39dBm input, 0.9A/W, and $C_{IN}$=1.0pF*
*Note3. Output with 500ohm termination*

## TYPICAL APPLICATION CIRCUIT

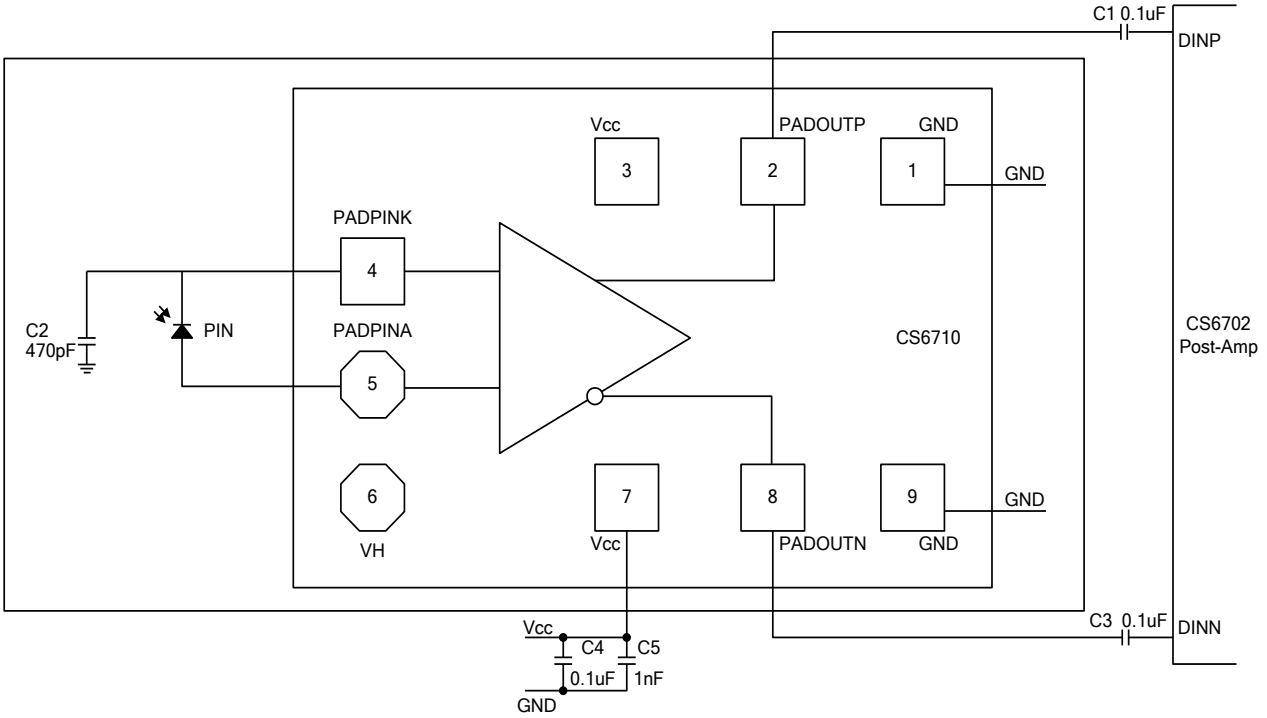



**Figure-4**

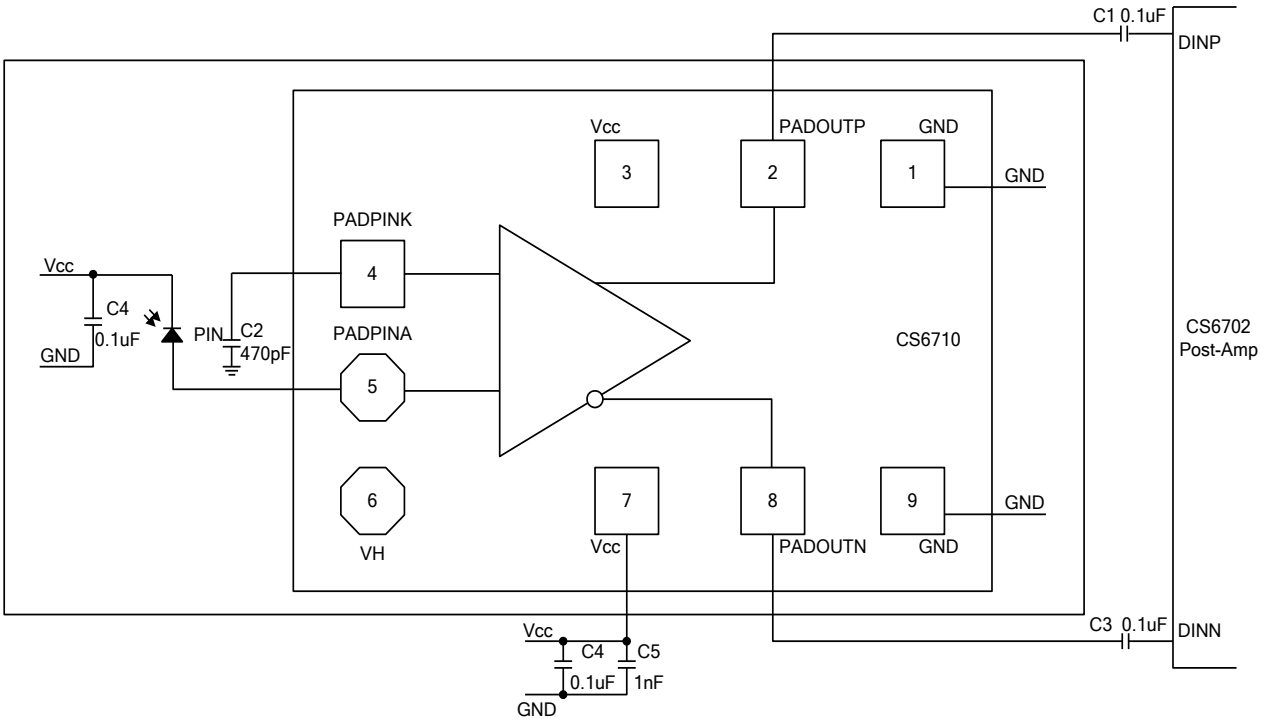
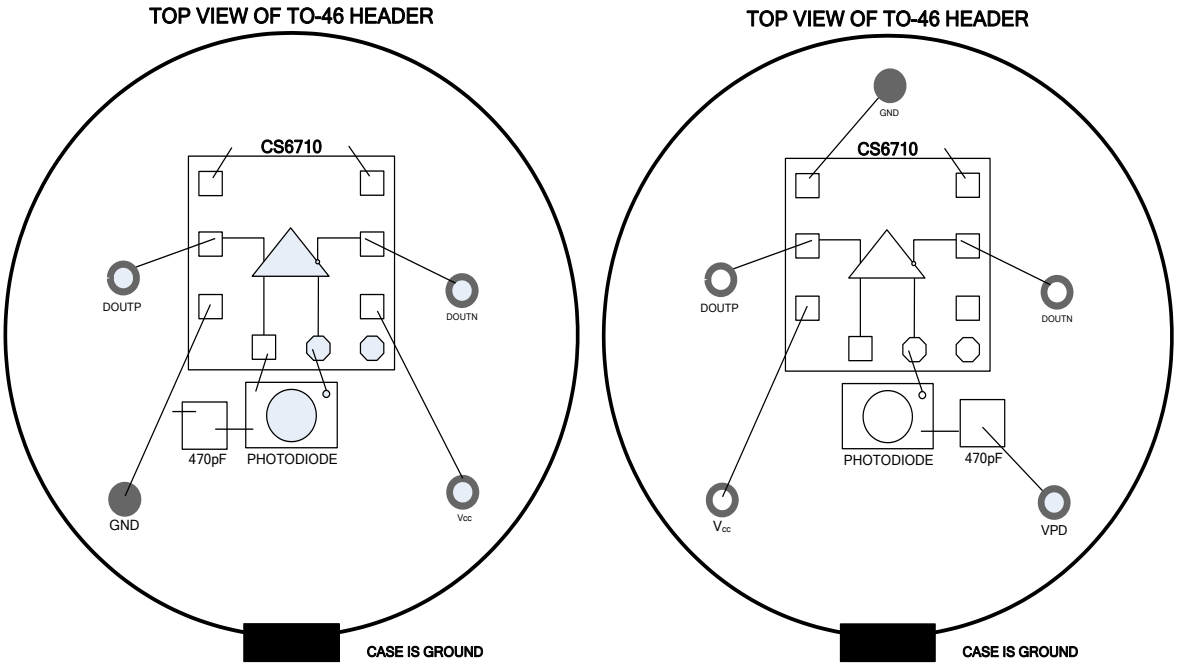



**Figure-5**




## APPLICATION INFORMATION

Typical application circuit is shown in Figure4. An alternative of the PIN diode is to connect the cathode of the PIN diode to VCC with a decoupling capacitor to ground. This configuration requires one more capacitor connected from PADPINK pin to ground, as shown in Figure5.

## LAYOUT CONSIDERATIONS

Noise performance is directly proportional to the total capacitance at the PADDINA pin. Minimise the bond-wire length, and the capacitance of the PIN diode. Figure 6 showns the typical layout of TO-CAN.

## ORDERING INFORMATION

| Prefix | Part Number | Remark |
|---|---|---|
| CS | 6710 | |

## DISCLAIMER AND DECLARATION