MICRO NETWORKS

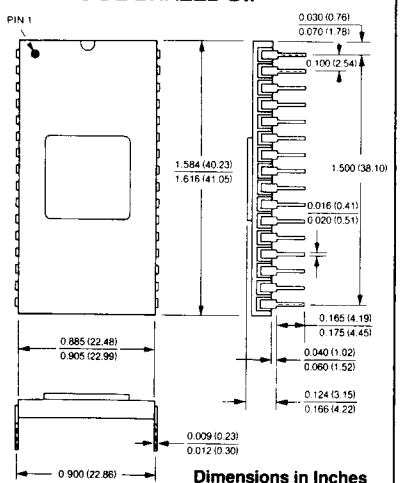
ADC80

LOW-COST, MONOLITHIC
10 and 12-Bit
A/D CONVERTERS

FEATURES

- **Low-Cost Single-Chip Design**
- **Complete with Internal Clock, Comparator and Reference**
- **−25°C to +85°C Operation**
- **± ½ LSB Linearity and No Missing Codes Guaranteed**
- **Maximum Conversion Time: 25μsec 12 Bits 22μsec 10 Bits**
- **5 User-Selectable Input Voltage Ranges**
- **Serial and Parallel Outputs**
- **±12V to ±15V Supplies**
- **705mW Maximum Power Consumption**
- **Standard 32-Pin Hermetic DIP**
- **Multisourced**

32 PIN SIDE BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

Micro Networks ADC80 is a complete, single-chip, 12-bit, successive approximation A/D converter that includes on-chip clock, reference and comparator. 12-bit units (add "-12" suffix to part number) perform a complete conversion in 25μsec. Devices specified for 10-bit performance (add "-10" suffix to part number) perform a short-cycled 10-bit conversion in 22μsec. Both are packaged in standard, 32-pin, side-brazed ceramic dual-in-lines, and both guarantee ± ½ LSB integral linearity and "no missing codes" for their respective resolutions.

These TTL-compatible A/D's feature internal input scaling resistors that provide 5 user-selectable input ranges (0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V). Functionally trimmed thin-film resistors ensure that all published accuracy and linearity specifications are met without the need for additional external adjustments. User-optional gain and offset adjust points are provided, however, for critical applications requiring the highest accuracies. Units may be driven from the internal clock or from an external system clock, and short cycling may be used to reduce conversion times for applications in which fewer than 12 bits are required. Output data is complementary binary coded and appears in both serial and parallel formats.

Low cost, multisource availability and guaranteed performance have made the ADC80 the designer's choice for most 10 or 12-bit commercial and industrial applications. Devices operate from ±12V to ±15V supplies and also require a +5V logic supply. Power consumption is 705mW maximum, and unlike earlier hybrid versions of this device, a +5V analog supply is no longer required. Similarly, the "Z" suffix on the part number is no longer required for ±12V operation as all devices now operate from either ±12V or ±15V supplies.

Model	Integral Linearity (%FSR)	No Missing Codes	Power Supplies
ADC80-12	±0.012	12 Bits	±12V/±15V, +5V
ADC80-10	±0.049	10 Bits	±12V/±15V, +5V

April 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

ADC80 LOW-COST MONOLITHIC 10 and 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+V_{CC}, Pin 17)	−0.5 to +18 Volts
Negative Supply (−V_{CC}, Pin 25)	+0.5 to −18 Volts
Logic Supply (+V_{dd}, Pin 9)	−0.5 to +7 Volts
Analog Inputs (Pins 13 and 14)	±16.5 Volts
Digital Inputs (Pins 18, 19, 20 and 21)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— ADC80-12
Select "-10" for guaranteed 10-bit performance or "-12" for guaranteed 12-bit performance.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±12V or ±15V +Vdd = +5V unless otherwise indicated) (Note 1)

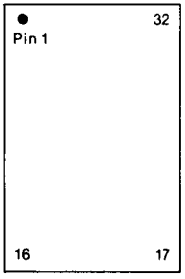
ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: Unipolar Bipolar		0 to +5, 0 to +10 ±2.5, ±5, ±10		Volts Volts
Input Impedance: 0 to +5V, ±2.5V 0 to +10V, ±5V ±10V		2.5 5 10		kΩ kΩ kΩ
DIGITAL INPUTS (Note 2)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V) Logic "0" (V_{IL} = +0.4V)			+20 −20	μA μA
TRANSFER CHARACTERISTICS (Note 4)				
Integral Linearity Error (Note 5): "-12" Devices "-10" Devices		±0.006 ±0.024	±0.012 ±0.049	%FSR %FSR
Integral Linearity Drift		±1	±3	ppm of FSR/°C
Differential Linearity Error (Note 5): "-12" Devices "-10" Devices		±1/2 ±1/2		LSB LSB
Differential Linearity Drift: "-12" Devices "-10" Devices		±2 ±5		ppm of FSR/°C ppm of FSR/°C
No Missing Codes Guaranteed −25°C to +85°C: "-12" Devices "-10" Devices	 12 10			 Bits Bits
Unipolar Offset Error (Notes 6, 7): Initial (+25°C) Drift		±0.05 ±3	±0.2	%FSR ppm of FSR/°C
Bipolar Offset Error (Notes 6, 8): Initial (+25°C) Drift		±0.1 ±7	±0.3 ±15	%FSR ppm of FSR/°C
Gain Error (Notes 6, 9): Initial (+25°C) Drift		±0.1 ±15	±0.3 ±30	% ppm of FSR/°C
DIGITAL OUTPUTS (Note 3)				
Output Coding (Note 10): Unipolar Ranges Bipolar Ranges		CSB COB, CTC		
Logic Levels: Logic "1" ($I_{SOURCE} \leq 80\mu A$) Logic "0" ($I_{SINK} \leq 3.2mA$)	+2.4		 +0.4	Volts Volts
REFERENCE OUTPUT				
Internal Reference: Voltage Accuracy Tempco External Current		+6.3 ±1 ±10	 200	Volts % ppm/°C μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 11): "-12" Devices "-10" Devices		22 19	25 22	μsec μsec
Internal Clock Frequency		556		kHz
Start Convert Positive Pulse Width (Note 11)	0.1		20	μsec

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: $+V_{CC}$ Supply	+11.4	+15	+16.5	Volts
$-V_{CC}$ Supply	−11.4	−15	−16.5	Volts
$+V_{dd}$ Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection: $+V_{CC}$ Supply		±0.003		%FSR/%Supply
$-V_{CC}$ Supply		±0.003		%FSR/% Supply
$+V_{dd}$ Supply		±0.002		%FSR/% Supply
Current Drains: $+V_{CC}$ Supply		+8.5	+11	mA
$-V_{CC}$ Supply		−21	−24	mA
$+V_{dd}$ Supply		+30	+36	mA
Power Consumption		593	705	mW

SPECIFICATION NOTES:

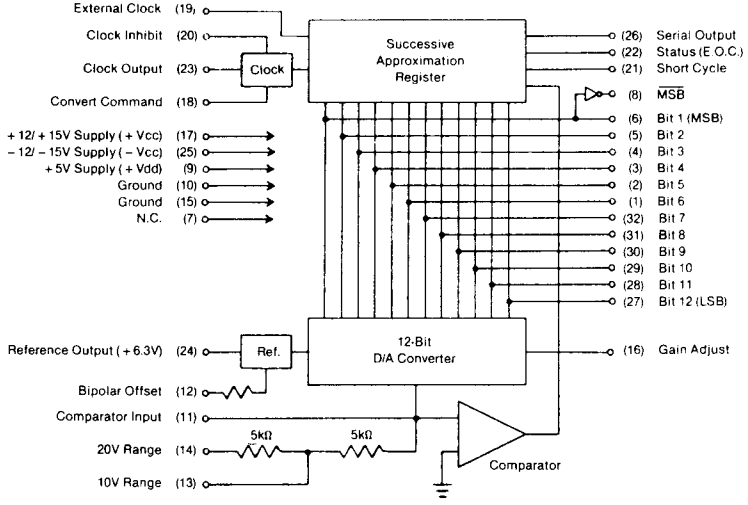
1. Unless otherwise indicated, all specifications apply for both 10-bit and 12-bit versions.
2. Digital inputs include Start Convert, External Clock Input, Clock Inhibit and Short Cycle.
3. Digital outputs include Parallel Data, Serial Data, Status and Clock Output.
4. FSR = full scale range. A unit connected for ±10V operation has a 20V FSR. A unit connected for 0 to +10V or ±5V operation has a 10V FSR etc.
5. For a 12-bit converter, 1LSB = 0.024%FSR and ±0.012%FSR = ± ½LSB. For a 10-bit converter, 1LSB = 0.098%FSR and ±0.049%FSR = ± ½LSB. ADC80 "-10" and "-12" devices both have 12 output data bits. "-12" devices guarantee true 12-bit performance while "-10" devices guarantee the equivalent of 10-bit performance.
6. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
7. Unipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a unipolar input range.
8. Bipolar offset error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition occurs when operating on a bipolar input range.
9. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.
10. CSB = complementary straight binary. COB = complementary offset binary. CTC = complementary two's complement. CTC coding is achieved using the $\overline{\text{MSB}}$ output. Coding applies for both serial and parallel outputs. CTC coding not available for serial output.
11. Conversion time is defined as the width of the Status (End of Conversion) pulse. Conversion time may be shortened, with lower resolution, by short cycling. Conversion is initiated on the rising edge of the Start Convert command. Listed conversion times apply for internal clock. See Timing Diagram.

PIN DESIGNATIONS



1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB)
7	N.C.	26	Serial Output
8	$\overline{\text{Bit 1 (MSB)}}$	25	−12/−15V Supply (−V_{CC})
9	+5V Supply (+V_{dd})	24	Reference Output (+6.3V)
10	Ground	23	Clock Output
11	Comparator Input	22	Status (E.O.C.)
12	Bipolar Offset	21	Short Cycle
13	10V Range	20	Clock Inhibit
14	20V Range	19	External Clock
15	Ground	18	Convert Command
16	Gain Adjust	17	+12/+15V Supply (+V_{CC})

BLOCK DIAGRAM

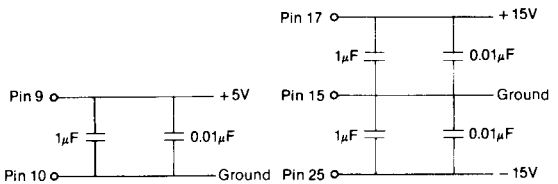


APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the ADC80. The units' two ground pins (pins 15 and 10) are not connected to each other internally and must be tied together as close to the package as possible, preferably to a large analog ground plane underneath the package. If these commons must be run separately, a non-polarized 0.01μF to 0.1μF bypass capacitor should be connected between pins 10 and 15 as close to the unit as possible and wide conductor runs employed.

Coupling between the analog inputs and digital signals should be minimized to avoid noise pickup. Pin 11, the high impedance input to the internal comparator, is particularly susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing the comparator input. In bipolar operation, where pin 11 is connected to pin 12, a short jumper should be used, and for external offset adjustment, the 1.8 megohm resistor should be located as close to the package as possible.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the ADC80. For optimum performance, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be connected as shown below. An additional 0.01μF ceramic bypass capacitor should be located close to the package connecting Gain Adjust (pin 16) to ground.



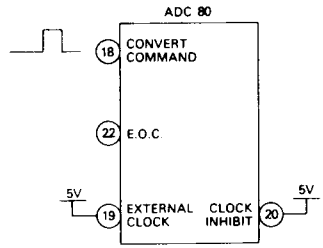
END OF CONVERSION—During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of the clock pulse "n + 1". Therefore, a complete conversion requires 13 clock pulses with the Status (E.O.C.) output dropping from logic "1" to logic "0" shortly after the falling edge of the 13th clock pulse. Parallel data is valid and ready to be read when Status falls. This allows direct use of Status for latching parallel data.

CLOCK OUTPUT—The internal 556kHz clock is brought out (pin 23) and will drive up to two standard TTL loads. The internal clock is stopped at the end of each conversion and remains low until a new conversion is initiated.

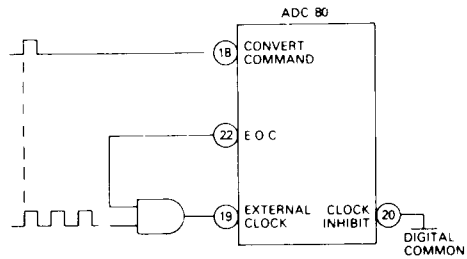
SERIAL DATA OUTPUT—Serial data is available (pin 26) in non-return-to-zero format. Timing for the serial output is shown on the Timing Diagram.

REFERENCE OUTPUT—The internal 6.3V reference (pin 24) will drive loads up to 30k ohms, however it is recommended that this output be buffered before use.

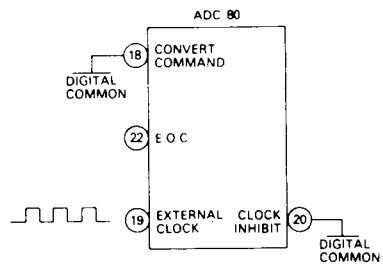
NORMAL OPERATION—For normal operation, a positive input pulse (100nsec minimum, 20μsec maximum pulse width) is applied to the Convert Command input as shown. The rising edge of the Convert Command will start the internal clock and initiate conversion. The Convert Command input must return low before the E.O.C. output returns low indicating the end of the conversion period. The External Clock and Clock Inhibit inputs must be tied high for normal operation.



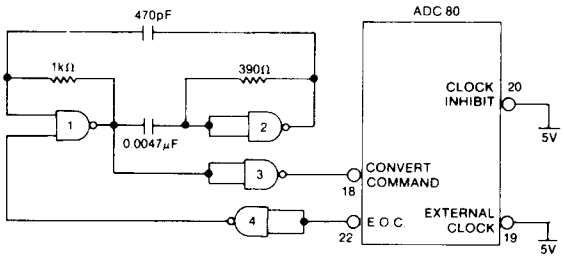
OPERATION WITH EXTERNAL CLOCK—The external clock is connected and gated as shown. The Convert Command input must be synchronized with the external clock signal and the Clock Inhibit input tied low, for proper operation.



CONTINUOUS CONVERSION WITH EXTERNAL CLOCK—For continuous conversion of the input signal, the Convert Command and Clock Inhibit inputs are tied low and an external clock applied to the Clock Input. The converter will then continuously convert, reset and initiate new conversions. The converter will be reset on the 13th clock pulse, and the subsequent conversion will be initiated by the 14th clock pulse. The output data will be valid when E.O.C. goes low and will remain valid until E.O.C. returns high.



CONTINUOUS CONVERSION WITH INTERNAL CLOCK—For continuous conversion of the input signal, the Clock Inhibit and External Clock pins are tied high. The conversion is initiated by the 14th clock pulse and the internal clock runs continuously. The oscillator formed by gates 1 and 2 insures that the conversion will start when logic power is turned on.



SHORT CYCLE FEATURE—The ADC80 may be operated at faster speeds if resolution of less than 12 bits is required. Connections for Short Cycle (pin 21) are shown in the following table:

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 28	Pin 30
Maximum Conversion Time Internal Clock (μsec) (Note 1)	25	22	18
Maximum nonlinearity at +25°C (% of FSR)	±0.012 (Note 2)	±0.048	±0.20

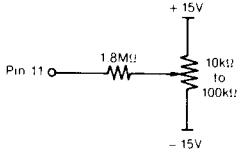
NOTES: (1) Max. conversion time to maintain ± ½LSB linearity error.
(2) ADC80-12 model only.

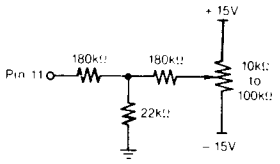
INPUT VOLTAGE CONNECTIONS—The analog input voltage ranges of the ADC80 are user selectable by external pin connections as shown in the adjacent table.

INPUT SIGNAL	CONNECT INPUT SIGNAL TO PIN	CONNECT PIN 12 TO PIN	CONNECT PIN 14 TO PIN
±10V	14	11	Input Sig.
±5V	13	11	Open
±2.5V	13	11	Pin 11
0 to +5V	13	15	Pin 11
0 to +10V	13	15	Open

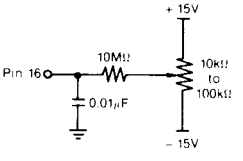
OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS—Initial offset and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warm-up, and to avoid interaction, offset should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100 ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 11 should be connected as described in the Input Voltage Connections section, and pin 16 should be left open.

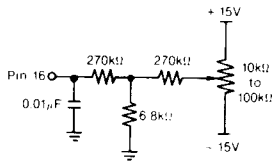
OFFSET ADJUSTMENT—Connect the offset potentiometer as shown, and apply the input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition is idealy supposed to occur (see Output Coding Table). While continuously converting, adjust the offset potentiometer until all the output bits are "1" and the LSB "flickers" on and off.





GAIN ADJUSTMENT—Connect the gain potentiometer as shown, and apply the input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "0" and the LSB "flickers" on and off.





DIGITAL OUTPUT CODING

Analog Input Voltage Range					Digital Outputs
0 to +5V	0 to +10V	±2.5V	±5V	±10V	MSB LSB
+5.0000	+10.0000	+2.5000	+5.0000	+10.0000	0000 0000 0000
+4.9982	+9.9963	+2.4982	+4.9963	+9.9927	0000 0000 000Ø*
+2.5006	+5.0012	+0.0006	+0.0012	+0.0024	0111 1111 111Ø*
+2.4994	+4.9988	−0.0006	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+2.4982	+4.9963	−0.0018	−0.0037	−0.0073	1000 0000 000Ø*
+0.0006	+0.0012	−2.4994	−4.9988	−9.9976	1111 1111 111Ø*
0.0000	0.0000	−2.5000	−5.0000	−10.0000	1111 1111 1111

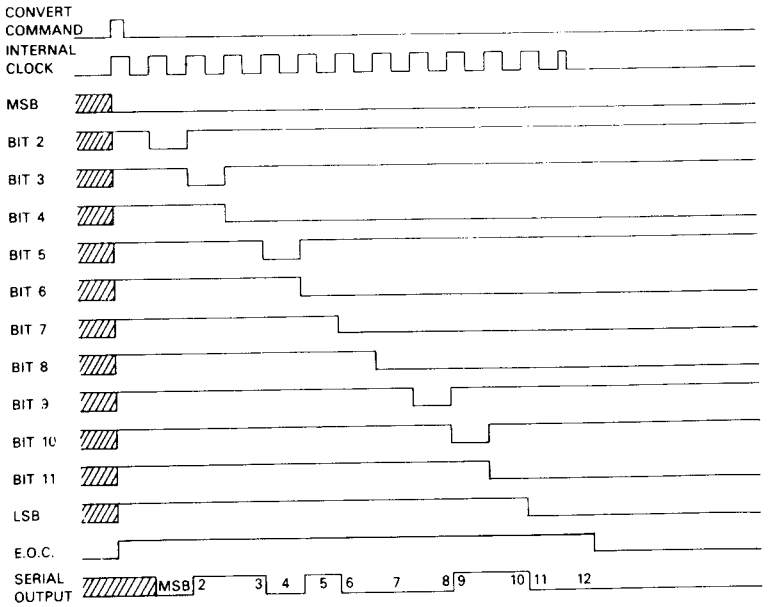
DIGITAL OUTPUT CODING NOTES:

1. For unipolar input ranges, output coding is complementary straight binary.
2. For bipolar input ranges, output coding is complementary offset binary or complementary two's complement if $\overline{\text{MSB}}$ output is used.
3. For 0 to +5V or ±2.5V input ranges, 1LSB for 12 bits = 1.22mV. 1LSB for 10 bits = 4.88mV.
4. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 10 bits = 9.77mV.
5. For 0 to +20V or ±10V input ranges, 1LSB for 12 bits = 4.88mV. 1LSB for 10 bits = 19.53mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADC80-12 operating on its ±10V input range, the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9976 Volts. Subsequently, any input voltage more negative than −9.9976 Volts will give a digital output of all "1's". The transition from digital output 0111 1111 1111 to 1000 0000 0000 will ideally occur at an input of −0.024 Volts, and the 0000 0000 0000 to 0000 0000 0001 transition should occur at +9.9927 Volts. An input more positive than +9.9927 Volts will give all "0's".

TIMING DIAGRAM



DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time: 12-Bits		22	25	μsec
10-Bits		19	22	μsec
Clock Delay from Convert Command		153		nsec
Clock Period		1.81		μsec
Clock Pulse Width (High)		0.87		μsec
Status Delay from Convert Command		186		nsec
All Bits Reset Delay from Convert Command		141		nsec
Data Valid Time from Clock Pulse High		−15		nsec