

# 100398

## Quad Differential ECL/TTL Translating Transceiver with Latch

### General Description

The 100398 is a quad latched transceiver designed to convert TTL logic levels to differential F100K ECL logic levels and vice versa. This device was designed with the capability of driving a differential 25Ω ECL load with cutoff capability, and will sink a 64 mA TTL load. The 100398 is ideal for mixed technology applications utilizing either an ECL or TTL backplane.

The direction of translation is set by the direction control pin (DIR). The DIR pin on the 100398 accepts TTL logic levels. A TTL LOW on DIR sets up the ECL pins as inputs and TTL pins as outputs. A TTL HIGH on DIR sets up the TTL pins as inputs and ECL pins as outputs.

A LOW on the output enable input pin (OE) holds the ECL output in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the latch transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-fol-

lowers to turn off when the termination supply is -2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

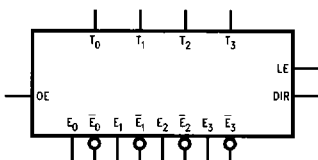
The 100398 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All Inputs have 50 kΩ pull-down resistors.

### Features

- Differential ECL input/output structure
- 64 mA FAST TTL outputs
- 25Ω differential ECL outputs with cut-off
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- TRI-STATE® outputs
- Voltage compensated operating range = -4.2V to -5.7V

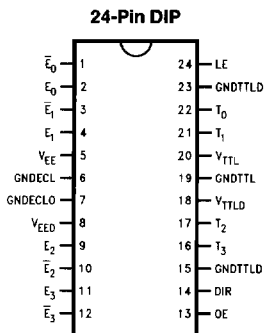
**Ordering Code:** See Section 6

### Logic Symbol

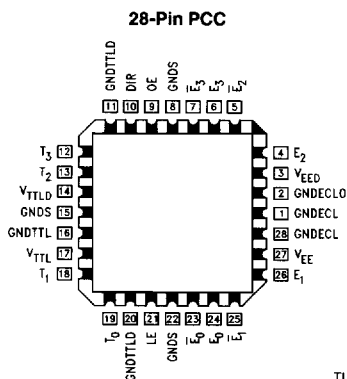


TL/F/10970-1

### Connection Diagrams

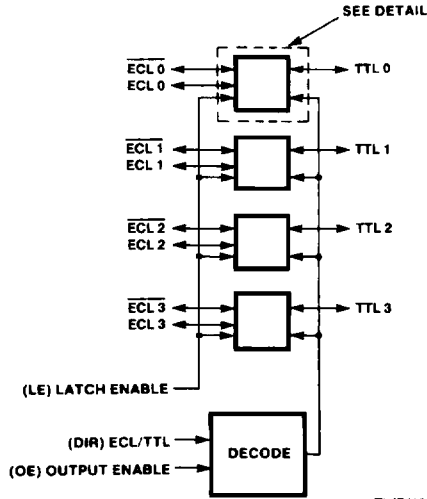


TL/F/10970-2



TL/F/10970-3

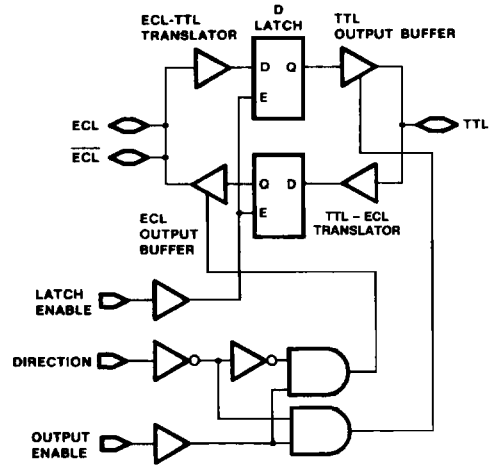
## Functional Diagram



TL/F/10970-5

Note: LE, and OE use TTL logic levels

## Detail



TL/F/10970-6

## Truth Table

Pin Names	Description
E <sub>0</sub> -E <sub>3</sub>	ECL Data I/O
E <sub>0</sub> -E <sub>3</sub>	Complementary ECL Data I/O
T <sub>0</sub> -T <sub>3</sub>	TTL Data I/O
OE	Output Enable Input Levels
LE	Latch Enable Input Levels
DIR	Direction Control Input (TTL levels)
GNDECL	ECL Ground
GNDECLO	ECL Output Ground
GNDS	ECL Ground-to-Substrate
V <sub>EE</sub>	ECL Quiescent Power Supply
V <sub>EED</sub>	ECL Dynamic Power Supply
GNDTTL	TTL Quiescent Ground
GNDTTLD	TTL Dynamic Ground
V <sub>TTL</sub>	TTL Quiescent Power Supply
VTTL	TTL Dynamic Power Supply

LE	DIR	OE	ECL Port	TTL Port	Notes
0	0	0	LOW (Cut-Off)	Z	
0	0	1	Input	Output	1, 4
0	1	0	LOW (Cut-Off)	Z	
0	1	1	Output	Input	2, 4
1	0	0	Input	Z	1, 3
1	0	1	Latched	X	1, 3
1	1	0	Low (Cut-Off)	Input	2, 3
1	1	1	Latched	X	2, 3

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
$V_{TTL}$ Pin Potential to Ground Pin	-0.5V to +6.0V
ECL Input Voltage (DC)	$V_{EE}$ to +0.5V
ECL Output Current (DC Output HIGH)	-50 mA
TTL Input Voltage (Note 4)	-0.5V to +7.0V
TTL Input Current (Note 4)	-30 mA to +5.0 mA

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

Voltage Applied to Output in HIGH State	-0.5V to +5.5V
TRI-STATE Output	
Current Applied to TTL Output in LOW State (Max)	Twice the Rated $I_{OL}$ (mA)
ESD (Note 2)	$\geq 2000V$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
ECL Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V
TTL Supply Voltage ( $V_{TTL}$ )	+4.5V to +5.5V

## Commercial Version

### TTL-to-ECL DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$  (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50 $\Omega$ to -2V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV	
	Cutoff Voltage		-2000	-1950	mV	OE and LE Low, DIR High $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ , Loading with 50 $\Omega$ to -2V
$V_{OHC}$	Output HIGH Voltage Corner Point High	-1035			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50 $\Omega$ to -2V
$V_{OLC}$	Output LOW Voltage Corner Point Low			-1610	mV	
$V_{IH}$	Input HIGH Voltage	2.0		5.0	V	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range
$V_{IL}$	Input LOW Voltage	0		0.8	V	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range
$I_{IH}$	Input HIGH Current			5.0	$\mu A$	$V_{IN} = +2.7V$
	Breakdown Test			0.5	mA	$V_{IN} = +5.5V$
$I_{IL}$	Input LOW Current	-700			$\mu A$	$V_{IN} = +0.5V$
$V_{FCD}$	Input Clamp Diode Voltage	-1.2			V	$I_{IN} = -18$ mA
$I_{EE}$	$V_{EE}$ Supply Current	-99		-50	mA	LE Low, OE and DIR High Inputs Open
$I_{EEZ}$	$V_{EE}$ Supply Current	-159		-90	mA	LE and OE Low, DIR High Inputs Open

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**Commercial Version** (Continued)**ECL-to-TTL DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $C_L = 50$  pF,  $V_{TTL} = +4.5V$  to  $+5.5V$  (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	2.7	3.1		V	$I_{OH} = -3$ mA, $V_{TTL} = 4.75V$ $I_{OH} = -3$ mA, $V_{TTL} = 4.50V$
		2.4	2.9		V	
$V_{OL}$	Output LOW Voltage		0.3	0.5	V	$I_{OL} = 24$ mA, $V_{TTL} = 4.50V$
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$V_{DIFF}$	Input Voltage Differential	150			mV	Required for Full Output Swing
$V_{CM}$	Common Mode Voltage	GNDECL - 2.0		GNDECL - 0.5	V	
$I_{IH}$	Input HIGH Current			30	$\mu A$	$V_{IN} = V_{IH}$ (Max)
$I_{IL}$	Input LOW Current	0.50			$\mu A$	$V_{IN} = V_{IL}$ (Min)
$I_{OZHT}$	TRI-STATE Current Output High			70	$\mu A$	$V_{OUT} = +2.7V$
$I_{OZLT}$	TRI-STATE Current Output Low	-650			$\mu A$	$V_{OUT} = +0.5V$
$I_{OS}$	Output Short-Circuit Current	-100		-225	mA	$V_{OUT} = 0.0V$ , $V_{TTL} = +5.5V$
$I_{CEX}$	Output HIGH Leakage Current			50	$\mu A$	$V_{OUT} = 5.5V$
$I_{ZZ}$	Bus Drainage Test			500	$\mu A$	$V_{OUT} = 5.25V$
$I_{TTL}$	$V_{TTL}$ Supply Current			39	mA	TTL Outputs LOW
				27	mA	TTL Outputs HIGH
				39	mA	TTL Outputs in TRI-STATE

**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**DIP and PCC TTL-to-ECL AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = 25^\circ C$		$T_C = 85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$F_{max}$	Toggle Frequency	180		180		180		MHz	
$t_{PLH}$ $t_{PHL}$	$T_n$ to $E_n$ , $\bar{E}_n$ (Transparent)	0.90	2.10	0.80	2.20	0.70	2.50	ns	Figures 1, 3
$t_{PLH}$ $t_{PHL}$	LE to $E_n$ , $\bar{E}_n$	1.40	2.70	1.50	2.70	1.80	3.10	ns	Figures 1, 3
$t_{PZH}$	OE to $E_n$ , $\bar{E}_n$ (Cutoff to High)	2.90	8.00	2.80	6.90	2.80	5.80	ns	Figures 1, 3
$t_{PHZ}$	OE to $E_n$ , $\bar{E}_n$ (High to Cutoff)	1.30	2.70	1.40	2.90	1.70	3.40	ns	Figures 1, 3
$t_{PHZ}$	DIR to $E_n$ , $\bar{E}_n$ (High to Cutoff)	1.30	2.70	1.40	2.90	1.80	3.50	ns	Figures 1, 3
$t_S$	$T_n$ to LE	0.70		0.70		0.70		ns	Figures 1, 3
$t_H$	$T_n$ to LE	0.90		0.80		0.70		ns	Figures 1, 3
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	Figures 1, 3

**Commercial Version** (Continued)**DIP and PCC ECL-to-TTL AC Electrical Characteristics** $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ ,  $C_L = 50$  pF

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = 25^\circ C$		$T_C = 85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$F_{max}$	Toggle Frequency	75		75		75		MHz	
$t_{PLH}$ $t_{PHL}$	$E_n, \bar{E}_n$ to $T_n$ (Transparent)	1.70	4.90	1.70	5.10	1.80	5.80	ns	Figures 2, 4
$t_{PLH}$ $t_{PHL}$	LE to $T_n$	2.30	4.60	2.40	4.70	2.60	4.90	ns	Figures 2, 4
$t_{PZH}$ $t_{PZL}$	OE to $T_n$ (Enable Time)	2.30	4.90	2.10	4.70	2.00	4.30	ns	Figures 2, 5
$t_{PHZ}$ $t_{PLZ}$	OE to $T_n$ (Disable Time)	3.30	7.90	3.30	7.50	3.70	7.90	ns	Figures 2, 5
$t_{PHZ}$ $t_{PLZ}$	DIR to $T_n$ (Disable Time)	2.00	6.00	1.90	5.70	1.70	5.20	ns	Figures 2, 6
$t_S$	$E_n, \bar{E}_n$ to LE	0.50		0.50		0.50		ns	Figures 2, 4
$t_H$	$E_n, \bar{E}_n$ to LE	1.00		1.00		1.00		ns	Figures 2, 4

**Industrial Version****TTL-to-ECL DC Electrical Characteristics** $V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$  (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1085	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with $50\Omega$ to $-2V$
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1575	mV	
	Cutoff Voltage		-2000	-1900	mV	OE and LE Low, DIR High $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ , Loading with $50\Omega$ to $-2V$
$V_{OHC}$	Output HIGH Voltage Corner Point High	-1095			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with $50\Omega$ to $-2V$
$V_{OLC}$	Output LOW Voltage Corner Point Low			-1565	mV	
$V_{IH}$	Input HIGH Voltage	2.0		5.0	V	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range
$V_{IL}$	Input LOW Voltage	0		0.8	V	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range
$I_{IH}$	Input HIGH Current			5.0	$\mu A$	$V_{IN} = +2.7V$
	Breakdown Test			0.5	mA	$V_{IN} = +5.5V$
$I_{IL}$	Input LOW Current	-700			$\mu A$	$V_{IN} = +0.5V$
$V_{FCD}$	Input Clamp Diode Voltage	-1.2			V	$I_{IN} = -18$ mA
$I_{EE}$	$V_{EE}$ Supply Current	-99	-40		mA	LE Low, OE and DIR High Inputs Open

**Note 1:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**Industrial Version** (Continued)**ECL-to-TTL DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ ,  $C_L = 50$  pF,  $V_{TTL} = +4.5V$  to  $+5.5V$  (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.1		V	I <sub>OH</sub> = -3 mA, V <sub>TTL</sub> = 4.75V
		2.4	2.9		V	I <sub>OH</sub> = -3 mA, V <sub>TTL</sub> = 4.50V
V <sub>OL</sub>	Output LOW Voltage		0.3	0.5	V	I <sub>OL</sub> = 24 mA, V <sub>TTL</sub> = 4.50V
V <sub>IH</sub>	Input HIGH Voltage	-1170		-870	mV	Guaranteed HIGH Signal for All Inputs
V <sub>IL</sub>	Input LOW Voltage	-1830		-1480	mV	Guaranteed LOW Signal for All Inputs
V <sub>DIFF</sub>	Input Voltage Differential	150			mV	Required for Full Output Swing
V <sub>CM</sub>	Common Mode Voltage	GNDECL - 2.0		GNDECL - 0.5	V	
I <sub>IH</sub>	Input HIGH Current			35	μA	V <sub>IN</sub> = V <sub>IH(Max)</sub>
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IH(Min)</sub>
I <sub>OZHT</sub>	TRI-STATE Current Output High			70	μA	V <sub>OUT</sub> = +2.7V
I <sub>OZLT</sub>	TRI-STATE Current Output Low	-650			μA	V <sub>OUT</sub> = +0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	V <sub>OUT</sub> = 0.0V, V <sub>TTL</sub> = +5.5V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	V <sub>OUT</sub> = 5.5V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	V <sub>OUT</sub> = 5.25V
I <sub>TTL</sub>	V <sub>TTL</sub> Supply Current			39	mA	TTL Outputs LOW
				27	mA	TTL Outputs HIGH
				39	mA	TTL Outputs in TRI-STATE

**Note 1:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**PCC TTL-to-ECL AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	T <sub>C</sub> = -40°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
F <sub>max</sub>	Toggle Frequency	180		180		180		MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	T <sub>n</sub> to E <sub>n</sub> , $\bar{E}_n$ (Transparent)	0.90	2.40	0.80	2.20	0.70	2.50	ns	Figures 1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	LE to E <sub>n</sub> , $\bar{E}_n$	1.30	2.70	1.50	2.70	1.80	3.10	ns	Figures 1, 3
t <sub>PZH</sub>	OE to E <sub>n</sub> , $\bar{E}_n$ (Cutoff to High)	2.90	9.00	2.80	6.90	2.80	5.80	ns	Figures 1, 3
t <sub>PHZ</sub>	OE to E <sub>n</sub> , $\bar{E}_n$ (High to Cutoff)	1.10	2.70	1.40	2.90	1.70	3.40	ns	Figures 1, 3
t <sub>PHZ</sub>	DIR to E <sub>n</sub> , $\bar{E}_n$ (High to Cutoff)	1.10	2.70	1.40	2.90	1.80	3.50	ns	Figures 1, 3
t <sub>S</sub>	T <sub>n</sub> to LE	0.70		0.70		0.70		ns	Figures 1, 3
t <sub>H</sub>	T <sub>n</sub> to LE	0.90		0.90		0.90		ns	Figures 1, 3
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	0.45	2.20	0.45	1.50	0.45	1.50	ns	Figures 1, 3

**Industrial Version** (Continued)**PCC ECL-to-TTL AC Electrical Characteristics** $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ ,  $C_L = 50$  pF

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$F_{max}$	Toggle Frequency	75		75		75		MHz	
$t_{PLH}$ $t_{PHL}$	$E_n, \bar{E}_n$ to $T_n$ (Transparent)	1.70	4.90	1.70	5.10	1.80	5.80	ns	Figures 2, 4
$t_{PLH}$ $t_{PHL}$	LE to $T_n$	2.30 3.30	4.80 5.50	2.40 3.50	4.70 5.70	2.60 4.00	4.90 6.70	ns	Figures 2, 4
$t_{PZH}$ $t_{PZL}$	OE to $T_n$ (Enable Time)	2.30 4.10	5.50 8.20	2.10 4.10	4.70 7.80	2.00 4.20	4.30 7.80	ns	Figures 2, 5
$t_{PHZ}$ $t_{PLZ}$	OE to $T_n$ (Disable Time)	3.20 4.00	7.90 7.40	3.30 4.30	7.50 7.80	3.70 5.30	7.90 9.40	ns	Figures 2, 5
$t_{PHZ}$ $t_{PLZ}$	DIR to $T_n$ (Disable Time)	2.00 2.10	6.60 4.70	1.90 2.00	5.70 3.70	1.70 1.90	5.20 3.70	ns	Figures 2, 6
$t_S$	$E_n, \bar{E}_n$ to LE	0.50		0.50		0.50		ns	Figures 2, 4
$t_H$	$E_n, \bar{E}_n$ to LE	1.00		1.00		1.00		ns	Figures 2, 4

## Military Version—Preliminary

### TTL-to-ECL DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with $50\Omega$ to $-2.0V$
		-1085	-870	mV	$-55^\circ C$		
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$		
		-1830	-1555	mV	$-55^\circ C$		
	Cutoff Voltage		-1950	mV	$0^\circ C$ to $+125^\circ C$	OE or DIR Low	
			-1850	mV	$-55^\circ C$		
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$
		-1085		mV	$-55^\circ C$		
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$		
			-1555	mV	$-55^\circ C$		
$V_{IH}$	Input HIGH Voltage	2.0		V	$-55^\circ C$ to $+125^\circ C$	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range	1, 2, 3, 4
$V_{IL}$	Input LOW Voltage		0.8	V	$-55^\circ C$ to $+125^\circ C$	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range	1, 2, 3, 4
$I_{IH}$	Input HIGH Current		70	$\mu A$	$-55^\circ C$ to $125^\circ C$	$V_{IN} = +2.7V$	1, 2, 3
	Breakdown Test		1.0	mA	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +5.5V$	
$I_{IL}$	Input LOW Current	-1.0		mA	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +0.5V$	1, 2, 3
$V_{FCD}$	Input Clamp Diode Voltage	-1.2		V	$-55^\circ C$ to $+125^\circ C$	$I_{IN} = -18 mA$	1, 2, 3
$I_{EE}$	$V_{EE}$ Supply Current	-165 -175	-65 -65	mA	$-55^\circ C$ to $+125^\circ C$	LE Low, OE and DIR High Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	1, 2, 3

**Military Version—Preliminary** (Continued)**ECL-to-TTL DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $GND = 0V$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$ ,  $C_L = 50$  pF,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$V_{OH}$	Output HIGH Voltage	2.5 2.4		mV	$0^\circ C$ to $+125^\circ C$ $-55^\circ C$	$I_{OH} = -1$ mA, $V_{TTL} = 4.50V$ $I_{OH} = -3$ mA, $V_{TTL} = 4.50V$	1, 2, 3
$V_{OL}$	Output LOW Voltage		0.5	mV	$-55^\circ C$ to $+125^\circ C$	$I_{OL} = 24$ mA, $V_{TTL} = 4.50V$	
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
$I_{IH}$	Input HIGH Current		350 500	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH(Max)}$	1, 2, 3
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL(Min)}$	1, 2, 3
$I_{OZHT}$	TRI-STATE Current Output High		70	$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{OUT} = +2.7V$	1, 2, 3
$I_{OZLT}$	TRI-STATE Current Output Low	-1.0		mA	$-55^\circ C$ to $+125^\circ C$	$V_{OUT} = +0.5V$	1, 2, 3
$I_{OS}$	Output Short-Circuit Current	-150	-60	mA	$-55^\circ C$ to $+125^\circ C$	$V_{OUT} = 0.0V$ , $V_{TTL} = +5.5V$	1, 2, 3
$I_{TTL}$	$V_{TTL}$ Supply Current		75 50 70	mA mA mA	$-55^\circ C$ to $+125^\circ C$	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	1, 2, 3

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ . Subgroups, 1, 2, 3, 7, and 8.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ . Subgroups A1, 2, 3, 7, and 8.

**Note 4:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

**TTL-to-ECL AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ ,  $GND = 0V$ 

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	$T_n$ to $E_n$ , $\bar{E}_n$ (Transparent)	1.0	3.9	1.1	3.6	1.1	4.0	ns	Figures 1, 2	1, 2, 3
$t_{PLH}$ $t_{PHL}$	LE to $E_n$ , $\bar{E}_n$	1.2	3.8	1.4	3.7	1.6	4.2	ns	Figures 1, 2	
$t_{PZH}$	OE to $E_n$ , $\bar{E}_n$ (Cutoff to HIGH)	1.0	4.3	1.5	4.4	1.7	5.2	ns	Figures 1, 2	
$t_{PHZ}$	OE to $E_n$ , $\bar{E}_n$ (HIGH to Cutoff)	1.5	5.1	1.6	4.5	1.6	5.1	ns	Figures 1, 2	1, 2, 3
$t_{PHZ}$	DIR to $E_n$ , $\bar{E}_n$ (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.9	ns	Figures 1, 2	
$t_S$	$T_n$ to LE	2.5		2.0		2.5		ns	Figures 1, 2	4
$t_H$	$T_n$ to LE	2.5		2.0		2.5		ns	Figures 1, 2	
$t_{PW(H)}$	Pulse Width LE	2.5		2.0		2.5		ns	Figures 1, 2	4
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	Figures 1, 2	4

# Military Version—Preliminary (Continued)

## ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ ,  $GND = 0V$ ,  $C_L = 50$  pF

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	$E_n, \bar{E}_n$ to $T_n$ (Transparent)	2.3	6.4	2.4	5.6	2.6	6.3	ns	Figures 3, 4	1, 2, 3
$t_{PLH}$ $t_{PHL}$	LE to $T_n$	3.1	8.0	3.1	7.3	3.3	8.0	ns	Figures 3, 4	
$t_{PZH}$ $t_{PZL}$	OE to $T_n$ (Enable Time)	3.2	8.9	3.7	9.0	4.0	10.2	ns	Figures 3, 5	1, 2, 3
$t_{PHZ}$ $t_{PLZ}$	OE to $T_n$ (Disable Time)	3.2	9.9	3.3	9.0	3.5	9.4	ns	Figures 3, 5	
$t_{PHZ}$ $t_{PLZ}$	DIR to $T_n$ (Disable Time)	2.6	9.4	2.8	8.8	2.9	9.1	ns	Figures 3, 6	
$t_{PLZ}$	DIR to $T_n$ (Disable Time)	2.7	8.5	3.1	8.0	4.0	9.7	ns	Figures 3, 6	
$t_S$	$E_n, \bar{E}_n$ to LE	2.5		2.0		2.5		ns	Figures 3, 4	4
$t_H$	$E_n, \bar{E}_n$ to LE	3.0		2.5		3.0		ns	Figures 3, 4	
$t_{PW(H)}$	Pulse Width LE	2.5		2.0		5.0		ns	Figures 3, 4	4

### Test Circuitry

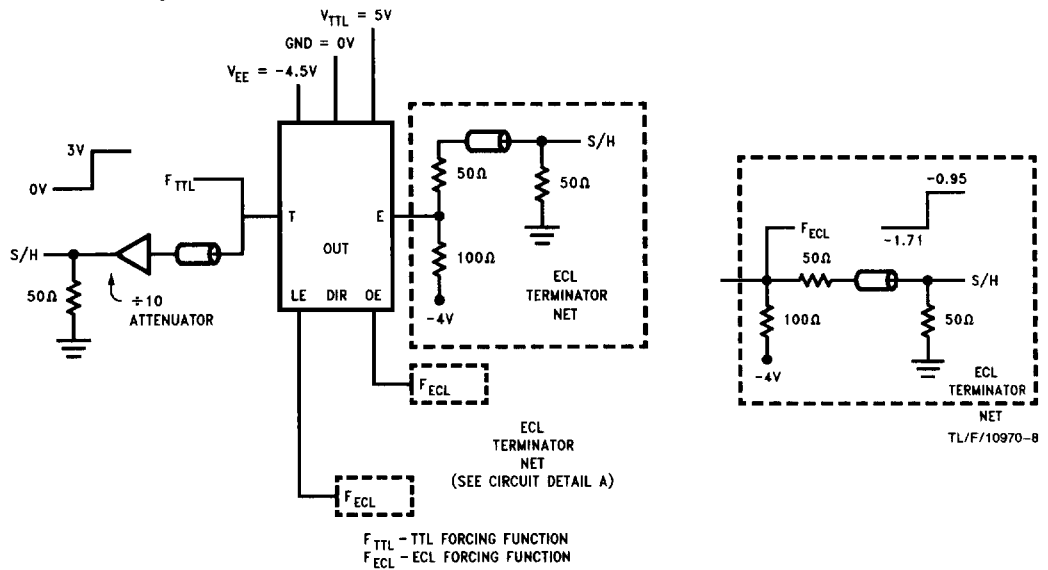
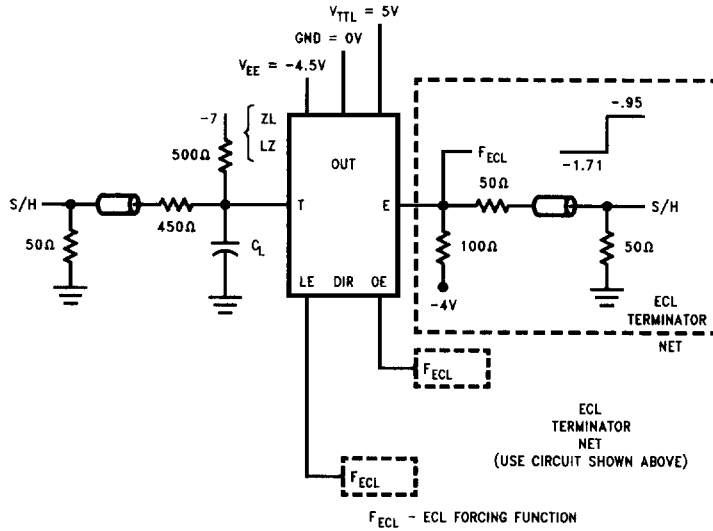


FIGURE 1. TTL-to-ECL AC Test Circuit

Test Circuitry (Continued)



$C_L = 50$  pF including stray and jig capacitance.

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**Note:** 50Ω to ground termination **must be included** on ECL I/O pins **not** monitored by a 50Ω scope to prevent oscillatory feedback.

FIGURE 2. ECL-to-TTL AC Test Circuit

Switching Waveforms

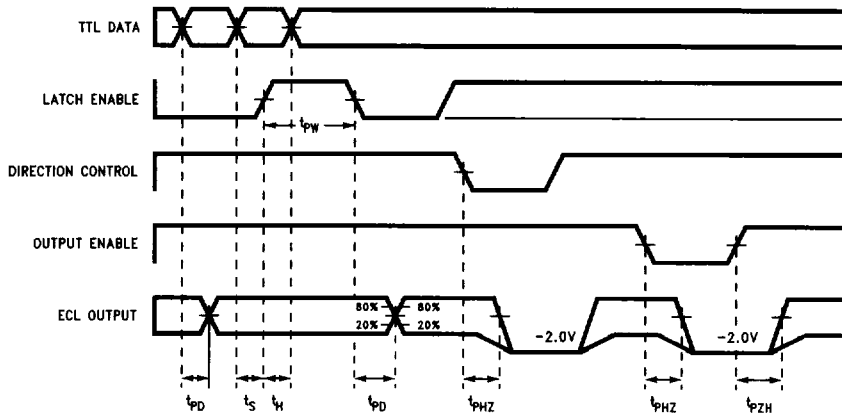
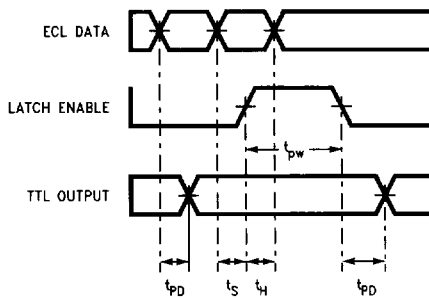


FIGURE 3. TTL-to-ECL Transition—Propagation Delay and Transition Times

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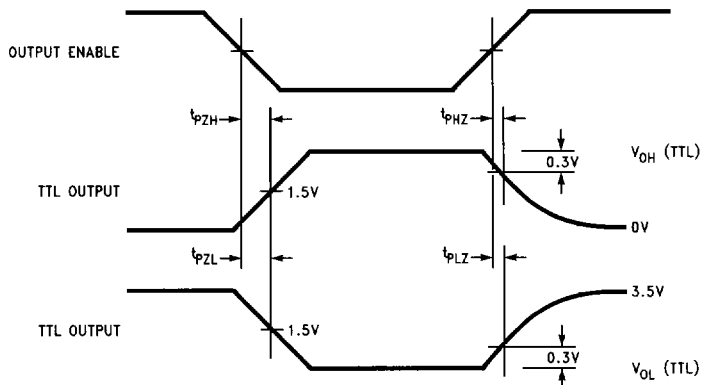
# Switching Waveforms (Continued)



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Note: DIR is LOW, and OE is HIGH

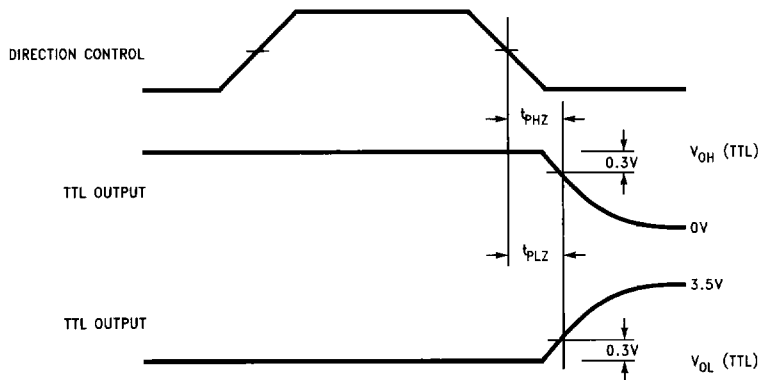
**FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times**



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Note: DIR is LOW, LE is HIGH

**FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times**

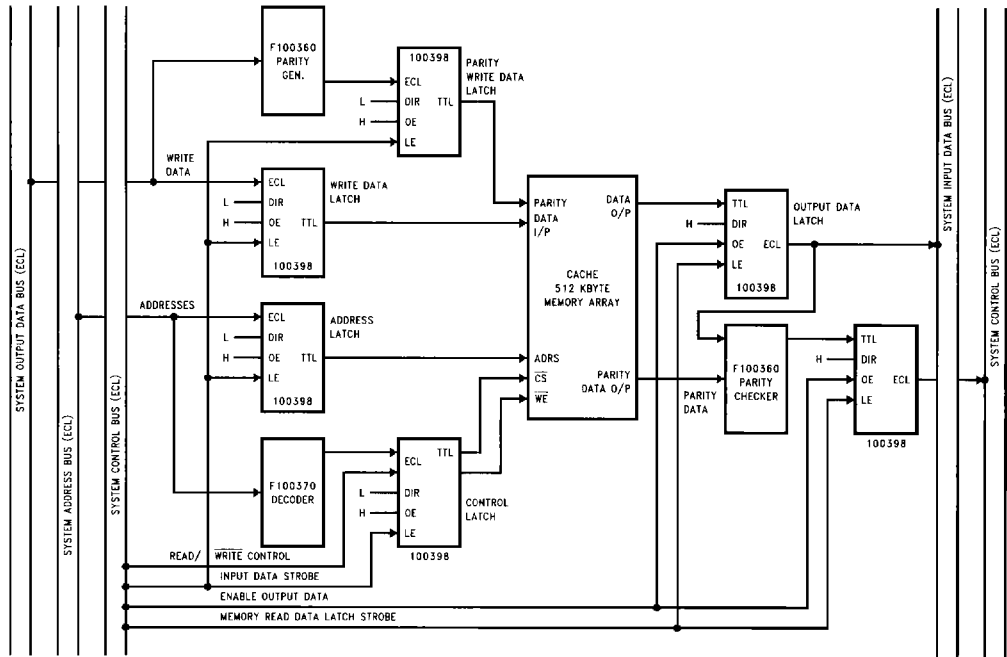


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Note: OE is HIGH, LE is HIGH

**FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time**

# Applications



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FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100398 ECL-TTL Latched Translator