2D Discrete Cosine Transform Circuit

Introduction

The 29C80F is a dedicated two-dimensional discrete cosine transform circuit. The two-dimensional forward transform (FDCT) or inverse transform (IDCT) is performed on fixed 8 × 8 pixel or coefficient blocks (64 samples).

These blocks can be scanned from left to right, line by line, or up to down, column by column, or in zig-zag order for coefficient blocks only. If the input matrix is scanned line by line and if the zig-zag order is not used, then the output matrix will appear column by column (line/column transposition between inputs and outputs).

For FDCT, the input bus receives pixels coded with 8 or 9 bit in two's complement format and the 29C80F output coefficients are coded with 12 bit in two's complement format..

For IDCT, the input bus receives coefficients coded with 12 bit in two's complement format and the 29C80F output pixels are coded with 8 or 9 bit in two's complement format.

A parallel architecture and a DCT based on modified CHEN algorithm are used allowing high precision compatible with the CCITT H261 requirements for accuracy and fast operation up to 20 Mpixels/s.

Except for clock circuitry, the 29C80F is composed of 5 blocks :

– 2 identical 1D DCT processors (line DCT and column DCT).

– 1 memory for line/column transposition (between the 2 DCT processors).

– 1 memory for zig-zag scanning.

– 1 clipping operator (following the column DCT processor).

All the internal sequencers are reset then started by a pipelined signal, BLKIN (Block Input), and stopped after a fixed number of cycles. The BLKOUT (Block Output) signal indicates the beginning of a block on the output data bus DO[0..11].

The latent period (the time between input data and its corresponding output result) is 128 CLK cycles (regardless of zig-zag scanning selection). The 29C80F has been designed to process contiguous blocks. However, it is possible to introduce a gap period between two blocks and/or to mix FDCT/IDCT by respecting some recommendations.

The 29C80F is designed to cover a wide range of real time DCT coding/decoding applications up to 20 MSamples/s.

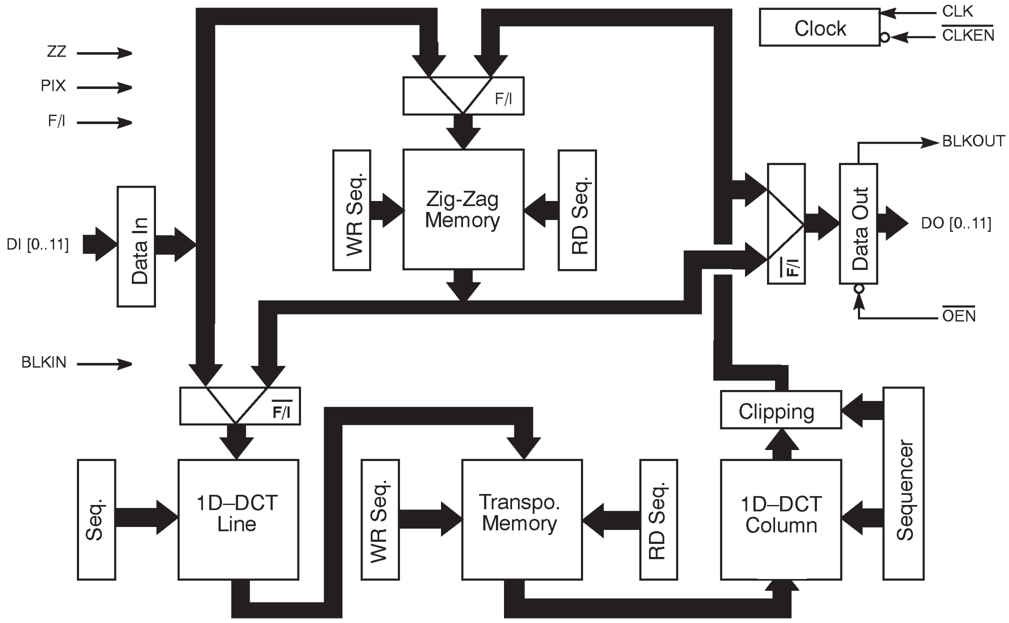
	Input Data Bus[1]	Output Data Bus[1]
FDCT	Pixels 8-bit : DI [11..4][2] Pixels 9-bit : DI[11..3][3]	Coefficients : DO[11..0]
IDCT	Coefficients : DO[11..0]	Pixels 8-bit : DI[11..4][4] Pixels 9-bit : DI[11..3][5]

Notes :
1. Data coded with 2's complement
2. DI[3..0] must be tied to VIL
3. DI[2..0] must be tied to VIL
4. DO[3..0] forced to VOL
5. DO[2..0] forced to VOL

Features

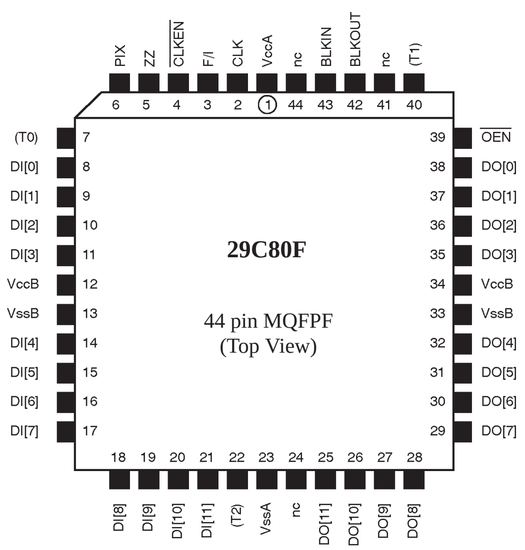
- Forward and inverse 8 × 8 data transform
- DC to 20 MHz pixel rate (20 MHz clock)
- 9 bit two's complement pixel format
- 8 bit two's complement pixel format with optimised accuracy
- 12 bit two's complement coefficient format
- Fully compliant with CCITT H261 accuracy
- Selectable zig-zag scanning for coefficient blocks
- Full parallel architecture
- Radiation tolerant for space application
- Fully synchronous interface
- 128 block cycles latency
- Power down mode
- Tristate control output
- TTL compatible inputs and outputs
- Single 5 V ± 10 % power supply
- 44 pin MQFPJ
- Advanced 0.8 µm CMOS technology

Functional Block Diagram



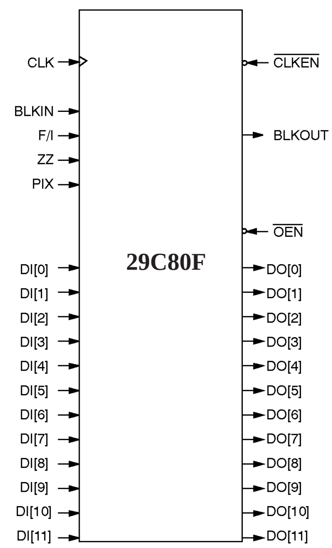
Interface

Pin Configuration



T0, T1 & T2 must be tied to VSS.
Diagrams are for pin reference only.
Package sizes are not to scale

Logic Symbol



Pin Description

Power

VCCA : Array Positive Supply . . . . pin 1
VCCB : Input/Output Buffers Positive Supply . . . . pin 12 & 34
VSSA : Array Negative Supply (0 Volt) . . . . pin 23
VSSB : Input/Output Buffers Negative Supply (0 Volt) . . . . pin 13 & 33

Several power supply pins are provided to minimise inductance within package. All supplies must be connected. The supply must be decoupled close to the chip by at least one 100 nF ceramic capacitor between each couple VCC/VSS (pin 1 & 23, pin 12 & 13, pin 34 & 33). Four layer boards are recommended (cf figure 13). If two layer boards are used, a special care should be taken in decoupling.

System Services

CLK : Input Clock . . . . pin 2
/CLKEN : Clock Enable (active low) . . . . pin 4
/OEN : Output Enable (active low) . . . . pin 39

CLK : The input clock controls the 29C80F timing. The falling edge of CLK samples the input data (DI[..]) and the input commands (BLKIN, F/I, PIX, ZZ & /CLKEN). The rising edge of CLK drives the output latches which provide computed data (DO[..]) and output control (BLKOUT).

/CLKEN : The clock enable allows to stop (/CLKEN = VIH) the internal clock. Sampled on the falling edge of CLK, this command is taken into account in the next cycle, this means from the next rising edge. Then, the internal clocks are stoped and the output data (DI[..]) and the output control (BLKIN) are in high impedance regardless output enable command (/OEN). So, /CLKEN can be used to reduce the power consumption.

/OEN : When output enable in high, all the outputs (/BLKOUT and DO [..]) are forced in the high impedance state.

Synchronous Controls

BLKIN : Block Input Synchronization . . . . pin 43
BLKOUT : Block Output Synchronization . . . . pin 42
F/I : FDCT/IDCT Selection . . . . pin 3
ZZ : Coefficient Scanning Selection . . . . pin 5
PIX : 8 or 9 Pixel Data Selection . . . . pin 6

BLKIN : BLKIN defines the beginning of a new input block. It is sampled on the falling edge of CLK. When BLKIN has been sampled high, the next CLK cycle corresponds to the first data of the new input block (if the blocks to be computed are contiguous, the BLKIN signal must be generated during the 64th input data of the previous block).

BLKOUT : BLKOUT defines the beginning of a new output block. It is the pipelined BLKIN signal (1 latent period) provided by the output latch driven by the rising edge of CLK. It is active (high level) one CLK cycle in advance compared to the first data of corresponding output block (if the blocks computed were contiguous, the BLKOUT signal is provided during the 64^{th} output data of the previous block).

F/I : F/I input defines the type of transform for the entire block, F/I = VIH for FCDT and F/I = VIL for IDCT. This selection is sampled on the falling edge of CLK during the BKLIN period (cf BLKIN definition). In order to mixt FDCT and IDCT together, a minimum gap of 128 CLK periods is needed between blocks. This means, if a BKLIN is placed in cycle “-1” for one type of block (cf figure 10), the BLKIN for the other type of block must be placed in cycle "191".

ZZ : ZZ input defines the block scanning to be used (cf figure 1) for the input or the output of coefficients, according to the CCITT H261 requirements. ZZ signal is sampled on the falling edge of CLK during the BKLIN period (cf BLKIN definition).

PIX : This input allows to choose input/output pixel format, 9 bit 2's complement format (PIX=VIL) or 8 bit 2's complement format (PIX = VIH). The chosen format is sampled by the falling edge of CLK during the BKLIN period (cf BLKIN definition). The JPEG 8 bit mode can be obtained by inverting MSB on pixel data (bias +128).

Figure 1. Function of Synchronous Controls.

Control	State	Function
BLKIN	VIL VIH	No action. Block input synchronisation
BLKOUT	VOL VOH	No action. Block output synchronisation.
F/I	VIL VIH	(valid during "BLKIN period") Inverse DCT. Forward DCT.
ZZ	VIL VIH	(valid during "BLKIN period") Normal scanning for coefficient block. Zig–Zag scanning for coefficient block.
PIX	VIL VIH	(valid during "BLKIN period") 9 bit 2's complement pixel format. 8 bit 2's complement pixel format.

Synchronous data

DI[..] : Data Input Port . . . . pin 8 to 11 and 14 to 21
DO[..] : Data Output Port . . . . pin 38 to 35 and 32 to 25
DI[..] : The data input port is sampled on falling edge of CLK.

Figure 2. 9 bit 2's Complement Pixel Format for FDCT.

* FDCT : The input data, for FDCT, is a 9 (8)-bit 2's complement number (pixel) in the range –256, 257 (–128, 127).

Pin	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Weight	– 256	128	64	32	16	8	4	2	1	–	–	–
Digital value	-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	(*)	(*)	(*)

(*) Must be fixed to VIL

Figure 3. 8 bit 2's Complement Pixel Format for FDCT.

Pin	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Weight	– 128	65	32	16	8	4	2	1	–	–	–	–
Digital value	-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	(*)	(*)	(*)	(*)

(*) Must be fixed to VIL

Figure 4. 12 bit 2's Complement Coefficient Format for IDCT.

* IDCT : The input data, for IDCT, is a 12-bit 2's complement number (coefficient) in the range –2048, 2047.

Pin	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Weight	– 2048	1024	512	256	128	64	32	16	8	4	2	1
Digital value	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

DO[...] : The data output port is updated on each rising edge of CLK.

*FDCT : The output data, for FDCT, is a 12 bit 2's complement number (coefficient) in the range (–2048, 2047). Note that an inside clipping is performed before outputting the data onto this range.

Figure 5. 12 bit 2's Complement Coefficient Format for FDCT.

Pin	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Weight	– 2048	1024	512	256	128	64	32	16	8	4	2	1
Digital value	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

*IDCT : The output data, for IDCT, is a 9 (8)-bit 2's complement number (pixel) in the range –256, 257 (–128, 127). Note that an inside clipping is performed before outputting the data onto this range.

Figure 6. 12 bit 2's Complement Coefficient Format for FDCT.

Pin	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Weight	– 256	128	64	32	16	8	4	2	1	–	–	–
Digital value	-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	(*)	(*)	(*)

(*) Forced to VOL

Figure 7.8 bit 2's Complement Pixel Format for IDCT.

Pin	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Weight	– 128	65	32	16	8	4	2	1	–	–	–	–
Digital value	-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	(*)	(*)	(*)	(*)

(*) Forced to VOL

The 29C80F processes data blocks including 64 samples and representing an 8×8 pixel or coefficient matrix. The input blocks can be scanned :

– line by line or column by column for pixels
– line by line, column by column or in zig-zag mode (cf H261) for coefficients.

Figure 8 shows the relation between input blocks scanning order and output blocks scanning order.

Figure 8. 29C80F – Scanning Order.

	Pixel/Coefficient Order		**Coefficient/Pixel Order**
Normal Mode	01 09 17 25 33 41 49 57	<=>	01 02 03 04 05 06 07 08
	02 10 18 26 34 42 50 58		09 10 11 12 13 14 15 16
	03 11 19 27 35 43 51 59		17 18 19 20 21 22 23 24
	04 12 20 28 36 44 52 60		25 26 27 28 29 30 31 32
	05 13 21 29 37 45 53 61		33 34 35 36 37 38 39 40
	06 14 22 30 38 46 54 62		41 42 43 44 45 46 47 48
	07 15 23 31 39 47 55 63		49 50 51 52 53 54 55 56
	08 16 24 32 40 48 56 64		57 58 59 60 61 62 63 64
	Pixel Order		**Coefficient Order**
Zig-Zag Mode	01 02 03 04 05 06 07 08	<=>	01 03 04 10 11 21 22 36
	09 10 11 12 13 14 15 16		02 05 09 12 20 23 35 37
	17 18 19 20 21 22 23 24		06 08 13 19 24 34 38 49
	25 26 27 28 29 30 31 32		07 14 18 25 33 39 48 50
	33 34 35 36 37 38 39 40		15 17 26 32 40 47 51 58
	41 42 43 44 45 46 47 48		16 27 31 41 46 52 57 59
	49 50 51 52 53 54 55 56		28 30 42 45 53 56 60 63
	57 58 59 60 61 62 63 64		29 43 44 54 55 61 62 64
	01 09 17 25 33 41 49 57	<=>	01 02 06 07 15 16 28 29
	02 10 18 26 34 42 50 58		03 05 08 14 17 27 30 43
	03 11 19 27 35 43 51 59		04 09 13 18 26 31 42 44
	04 12 20 28 36 44 52 60		10 12 19 25 32 41 45 54
	05 13 21 29 37 45 53 61		11 20 24 33 40 46 53 55
	06 14 22 30 38 46 54 62		21 23 34 39 47 52 56 61
	07 15 23 31 39 47 55 63		22 35 38 48 51 57 60 62
	08 16 24 32 40 48 56 64		36 37 49 50 58 59 63 64

The 29C80F has synchronous input and output interfaces. The input data (DI[..]) and input commands (BLKIN, F/I, PIX, ZZ & /CLKEN) are sampled on the falling edge of CLK. The rising edge of CLK drives the output latches which provide computed data (DO[..]) and output control (BLKOUT). An asynchronous command (/OEN) puts the output latched buffers in high impedance.

BLKIN command must be activated one clock cycle before the first data of the input block. All input commands are taken into account on the falling edge of the CLK period defined by BLKIN. In accordance with the pipelined architecture, the 29C80F provides the output control signal BLKOUT one clock cycle before the first data of the output block.

A clock disable mode (/CLKEN) allows to stop internal clocks. This command can be used to reduce the power consumption or to adapt the flow rate (input/output data - gap cycles -...).

Mathematical Equations

Mathematical equation for FDCT

(nb - the FDCT is selected by setting F/I In at VIH)
Let A (i, j) be a pixel matrix where 0 < i (line) < 7 and 0 < j (column) < 7, the transformed matrix B (k, l) where 0 < k (line) < 7 and 0 < l (column) < 7 is defined by :

FCDT

$$B(k,l) = 1/4\ c(k)\ c(l) \sum_{i=0}^{7} \sum_{j=0}^{7} A(i,j)\ \cos\left[(2i+1)\frac{k\pi}{16}\right] \cos\left[(2j+1)\frac{l\pi}{16}\right]$$

where : $c(k) = 1/\sqrt{2}$ if k = 0 otherwise, c(k) = 1
$c(l) = 1/\sqrt{2}$ if l = 0 otherwise, c(l) = 1

The forward transform equation can be written :

$$B(k,l) = 1/2\ c(k) \sum_{i=0}^{7} \underbrace{\left[1/2\ c(l) \sum_{j=0}^{7} A(i,j) \cos\left[(2j+1)\frac{l\pi}{16}\right]\right]}_{1 \times D \text{ forward transform of i line of A (i, j)}} \cos\left[(2i+1)\frac{k\pi}{16}\right]$$

Mathematical Equation for IDCT

(nb - the IDCT is selected by setting F/I In at VIL)
Let B (k, l) be a coefficient matrix where 0 < k (line) < 7 and 7 < l (column) < 7, the transformed matrix A (i, j) where 0 < i (line) < 7 and 0 < j (column) < 7 is defined by :

IDCT

$$A(i,j) = 1/4 \sum_{k=0}^{7} \sum_{l=0}^{7} c(k)\ c(l)\ B(k,l)\ \cos\left[(2i+1)\frac{k\pi}{16}\right] \cos\left[(2j+1)\frac{l\pi}{16}\right]$$

where : $c(k) = 1/\sqrt{2}$ if k = 0 otherwise, c(k) = 1
$c(l) = 1/\sqrt{2}$ if l = 0 otherwise, c(l) = 1

The inverse transform equation can be written :

$$A(i,j) = 1/2 \sum_{i=0}^{7} c(l) \underbrace{\left[1/2 \sum_{k=0}^{7} c(k)\ B(k,l) \cos\left[(2i+1)\frac{k\pi}{16}\right]\right]}_{1 \times D \text{ inverse transform of 1 line of B (k, l)}} \cos\left[(2j+1)\frac{k\pi}{16}\right]$$

Figure 9. Block Period – Latent Period – DCT Period.

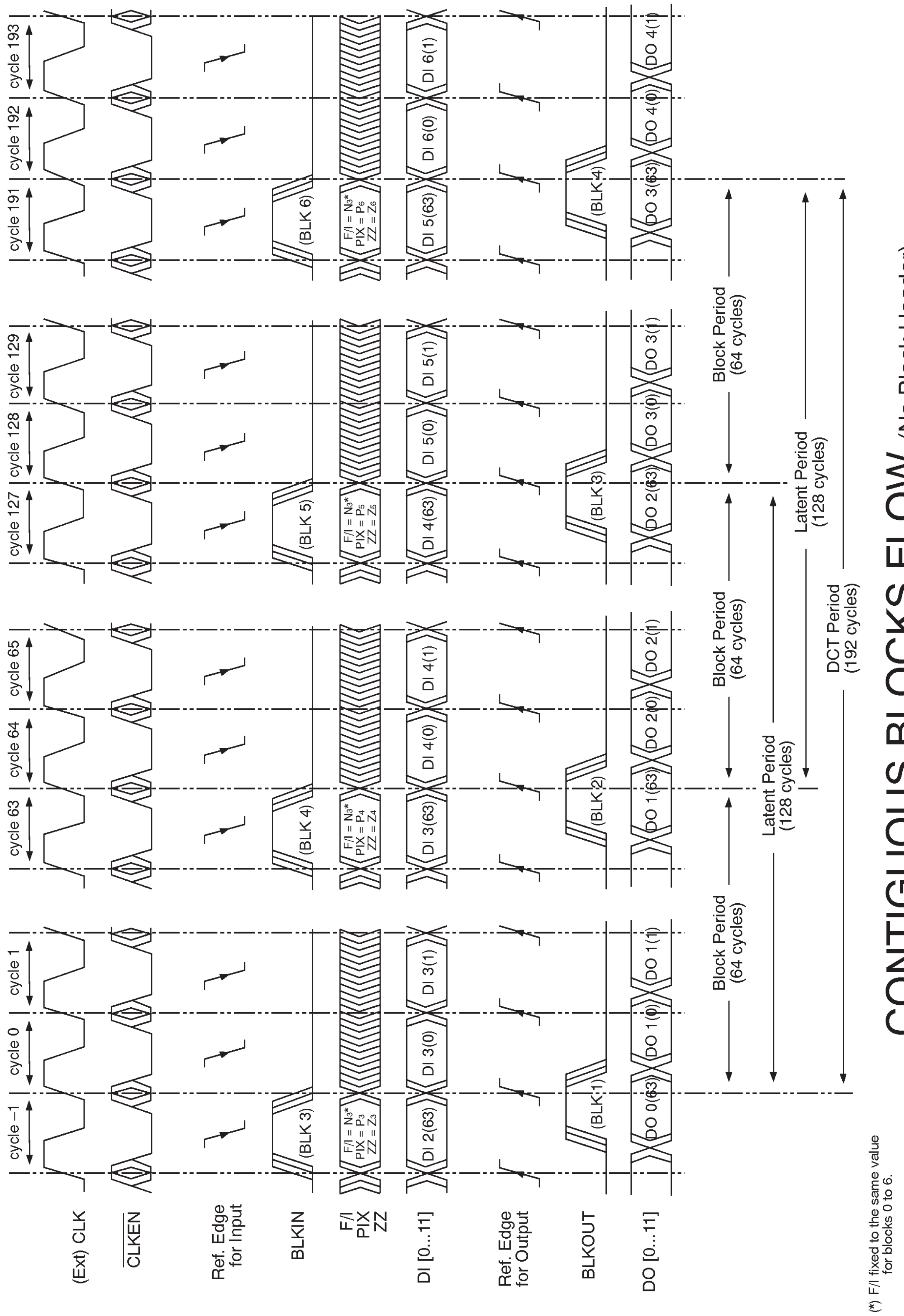
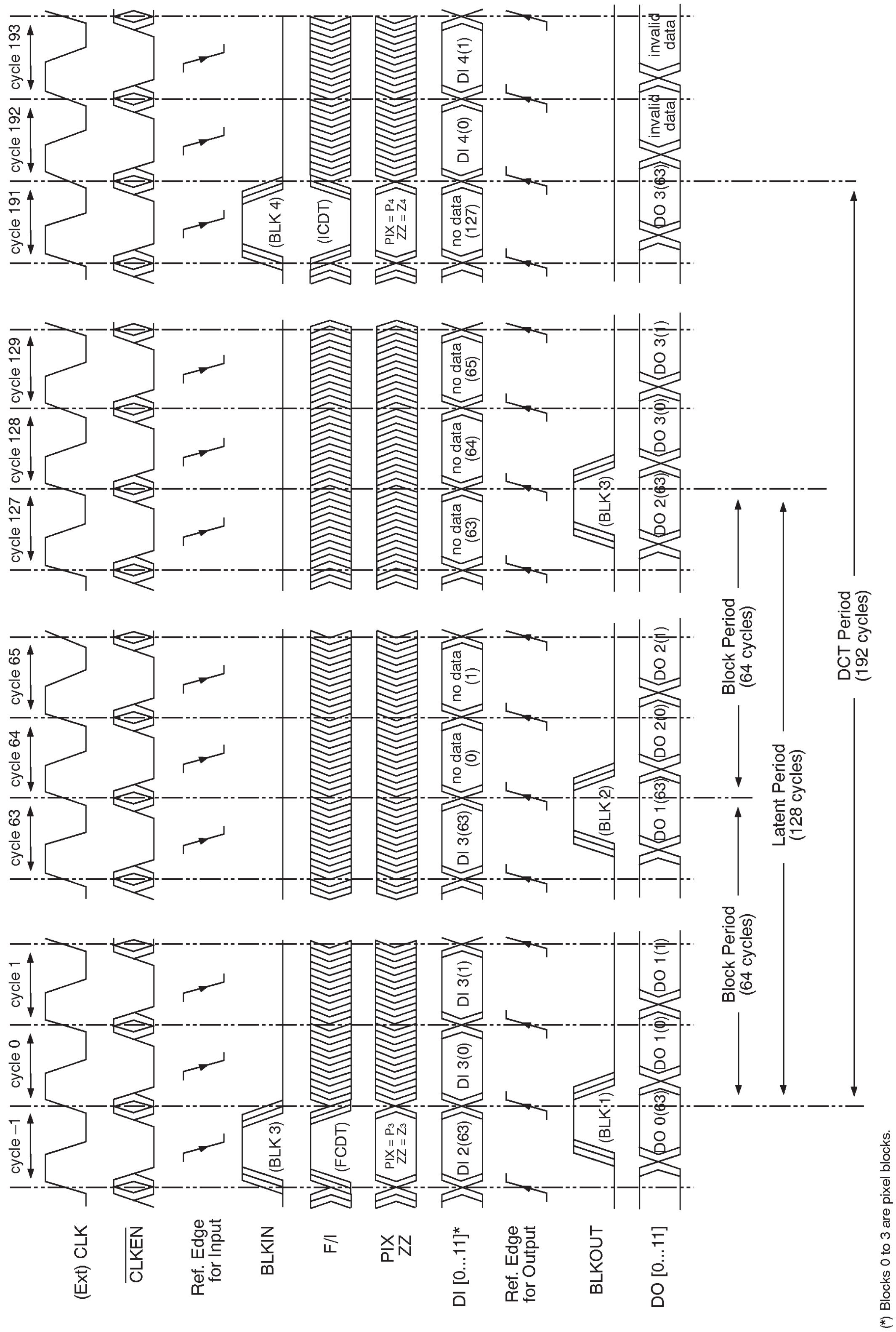


Figure 10. Mixing FDCT and IDCT.



Signaling Flow

Block Period

The block period is the time needed to input or output the 64 data of one block (cf figure 9). The 29C80F has a block period of 64 CLK cycles (1 cycle is defined by two contiguous rising edges of CLK). This means that the CLK period defines the FDCT/IDCT rate.

Latent Period

The latent period is the time between input data and its corresponding output result (cf figure 13). The 29C80F has a latent period of 128 CLK cycles (1 cycle is defined by two contiguous rising edges of CLK) using or not the internal zig-zag memory.

DCT Period

The DCT period is the time between the first input data of a block and the last output data of the resulting block (cf figure 9). The 29C80F has a DCT period of 192 CLK cycles (1 latent period + 1 block period).

GAP Cycles

The gap cycles are the CLK cycles between the 64^{th} data of a block and the 1^{st} data of the following block (cf figure 11). These cycles can fit a block header or simply an inactive period. The 29C80F authorizes 0, 8 or > 16 internal clock cycles as input gap cycles, else the following computed block will be corrupted. Driving /CLKEN can solve rapidly a possible application problem due to the presence of 1 to 7 or 9 to 15 input gap cycles (cf figure 10). The input gap cycles are fully retransmited on the output bus one latent period later. During an effective input gap cycle, the 29C80F does not pipeline data, so the input data is lost.

Block Abortion

The data input phase for a block only can be aborted by the BLKIN of a new block (cf figure 12). The aborttion is authorized if 8 or > 16 data of the wanted aborted block has been inputed before, else data output are corrupted. In case of 8 (16) data, the new BLKIN is placed into the cycle of the 8 $(16)^{th}$ data of the aborted block.

Figure 11. Gap Cycles.

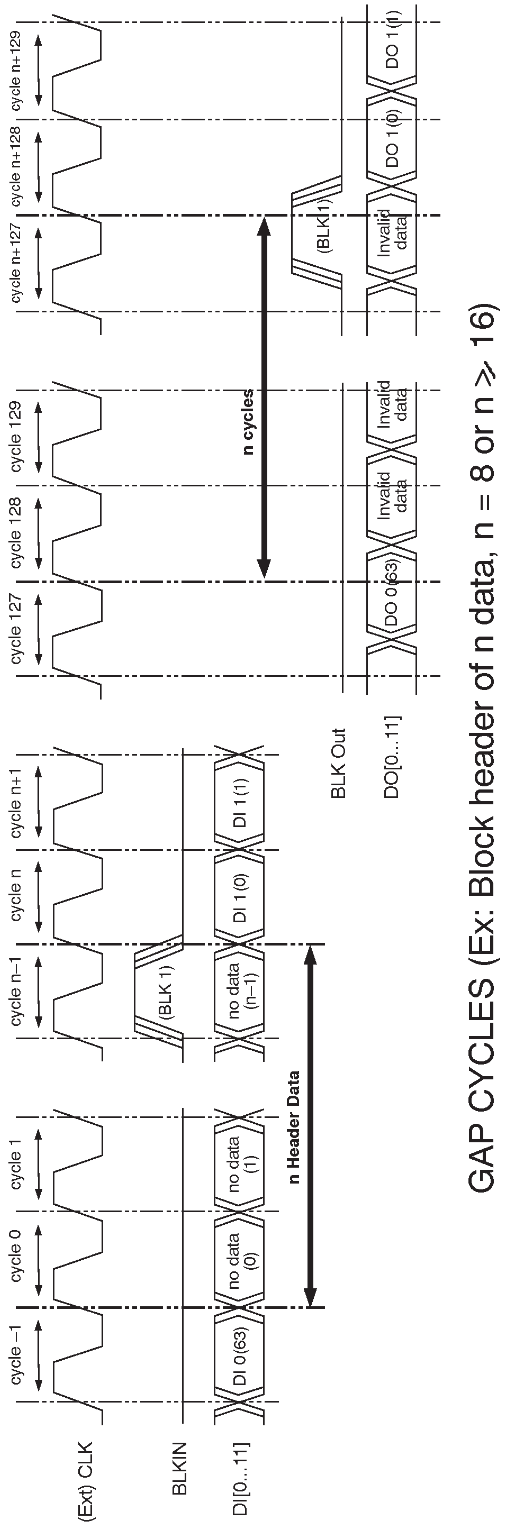
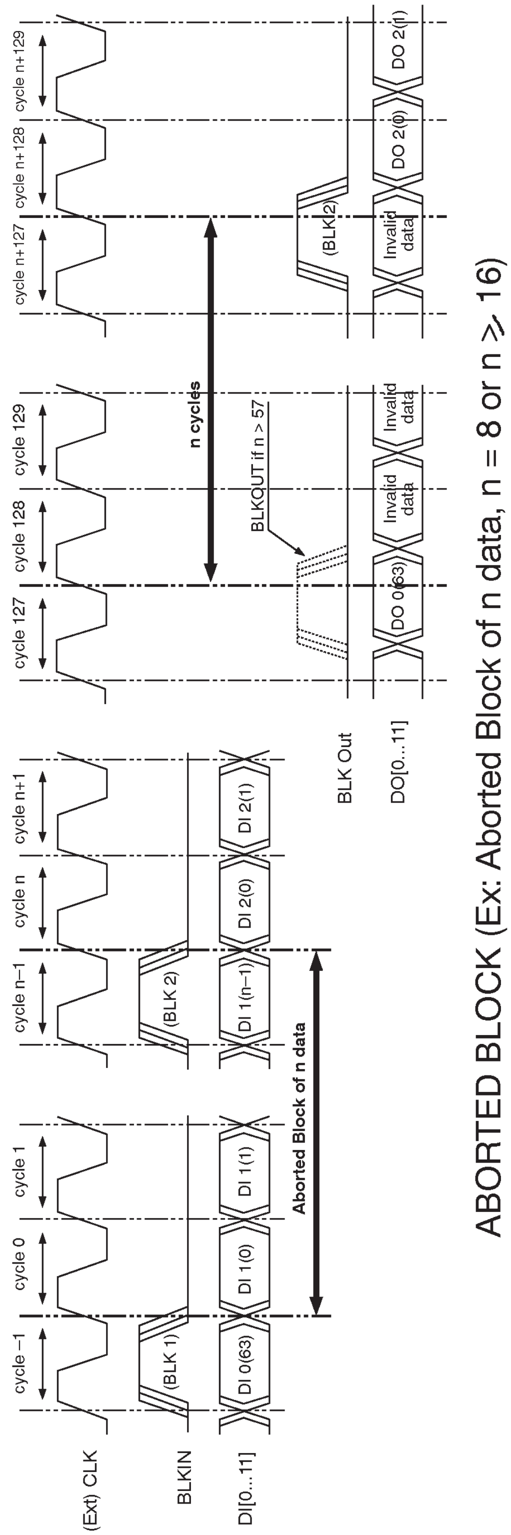


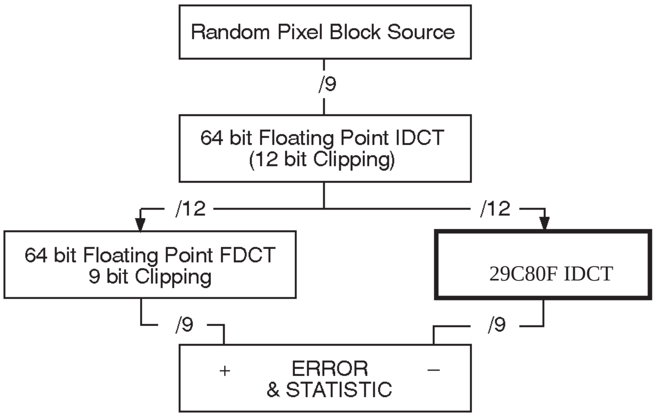
Figure 12. Aborted Block.



Accuracy / Reversibility

IDCT Accuracy

The accuracy characteristics for IDCT, specified by the CCITT H261 requirements, have been measured according to the following scheme :



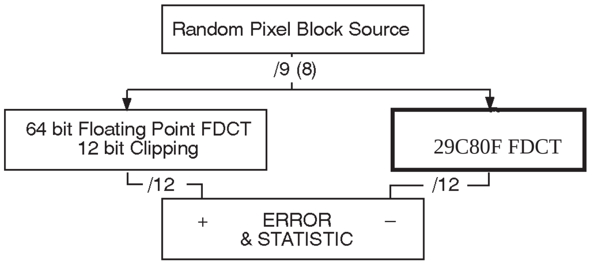
	29C80F IDCT	CCITT H261 Requirements
Peak error	1 LSB	1 LSB
Peak Mean Square Error	2.4 %	< 6 %
Overall Mean Square Error	1.7 %	< 2 %
Peak Mean Error	1.2 %	< 1.5 %
Overall Mean Error	.14 %	< .15 %

The same scheme is used for measurements of 8 bit IDCT, so an 8 bit clipping is made after 64 bit floating point calculations and the 29C80F is programmed in PIX mode (PIX = VIH).

	29C80F 8-bit IDCT
Peak error	1 LSB
Peak Mean Square Error	.09 %
Overall Mean Square Error	.02 %
Peak Mean Error	.05 %
Overall Mean Error	.004 %

FDCT Accuracy

The accuracy characteristics for FDCT have been measured according the following scheme :

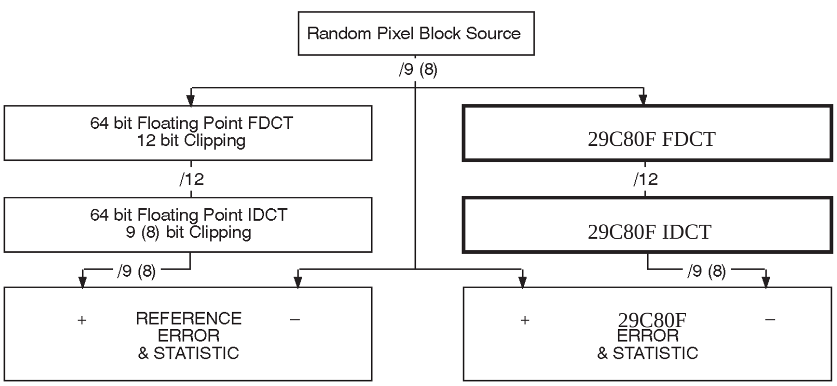


	29C80F 9 bit FDCT	29C80F 8 bit FDCT
Peak error	1 LSB	1 LSB
Peak Mean Square Error	8.3 %	8.4 %
Overall Mean Square Error	3.6 %	3.6 %
Peak Mean Error	1.9 %	2.0 %
Overall Mean Error	.31 %	.28 %

Note : The two result columns are nearly equivalent because the 29C80F computes 9 or 8 bit FDCT in the same internal configuration.

Reversibility

The 29C80F reversibility (FDCT then IDCT) is calculated according to the following scheme :



	9 BIT (FDCT → IDCT)		8 BIT (FDCT → IDCT)	
	29C80F	FLOAT. REF.	29C80F	FLOAT. REF.
Reversibility	91.3 %	91.7 %	99.94 %	99.95 %
1 LSB Error	8.7 %	8.3 %	.06 %	.05 %
2 LSB Error	.00 %	.00 %	.00 %	.00 %

Reseting / Power Up

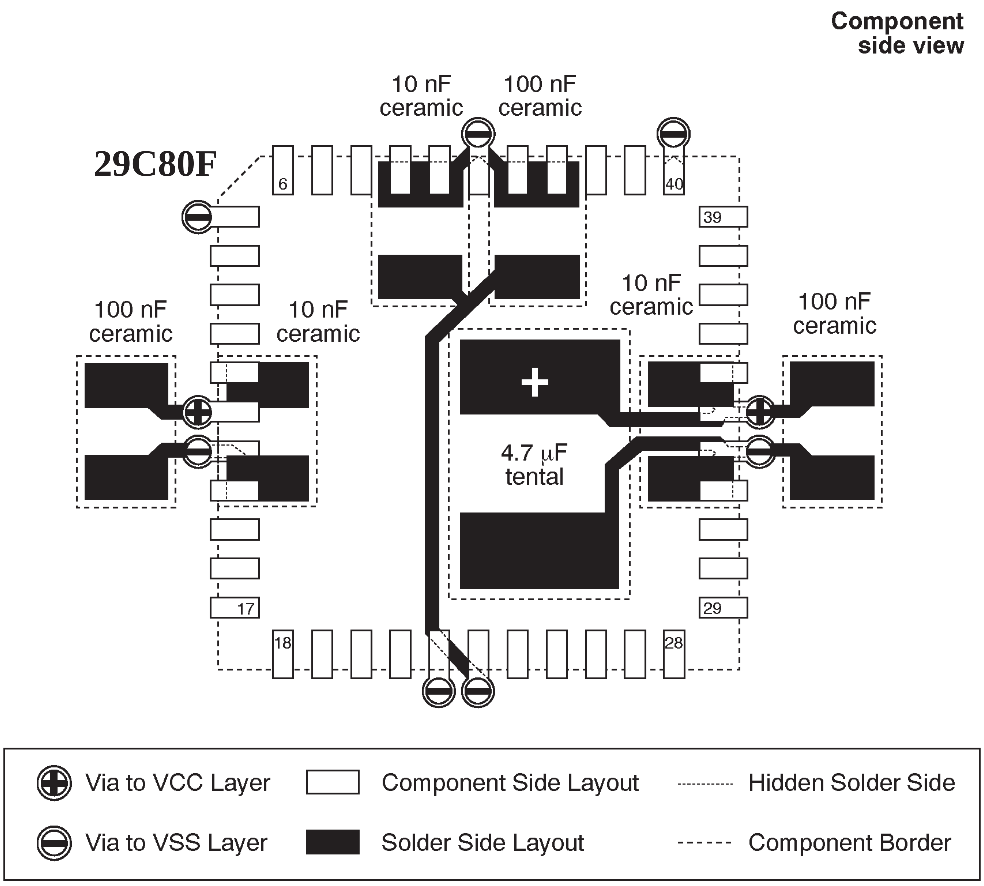
There is no general reset for 29C80F. Nevertheless, each internal sequencer has its own reset input. BLKIN resets the first sequencer and each sequencer resets the following one. Each sequencer starts after reseting and stops after a determinated number of cycles. Note that 192 cycles after the last BLKIN, all the sequencers are stopped, but the input/output latches and clock circuitery (/CLKEN = VIL) always are running.

When the 29C80F is powered on, some internal values are positionned to undefined value. After 8 cycles, the first BLKIN can be send.

Decoupling Proposal

Figure 13 proposes a 29C80F decoupling using SMC capacitors on a four layers PCB.

Figure 13.29C80F Decoupling Proposal.



Electrical Characteristics

DC Characteristics

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit	Note
Supply Voltage to VSS Potential	– 0.5	+ 7.0	V	1
Input or Output Voltage Applied	VSS – 0.3	VCC + 0.3	V	1
Storage temperature	– 65	+ 150	°C	1

Note : 1. Stresses greater than those listed may cause permanent damage to the 29C80F.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	DC Supply Voltage	+ 4.5	+ 5.0	+ 5.5	V
VIL	Input Low Voltage	– 0.3	0.0	+ 0.8	V
VIH	Input High Voltage	+ 2.2	/	VCC + 0.3	V

Symbol	Parameter	Min.	Typ.	Max	Unit
ICCPD	Power-Down Supply Current(2)		0.5	2	mA
ICCOP	Operating Supply Current(3)		50	100	mA
VOL	Output Low Voltage(4)	0		+ 0.4	V
VOH	Output High Voltage(4)	+ 2.4		VCC	V
IIX	Input Leakage Current(5)	– 5.0		+ 5.0	µA
IOZ	Output Leakage Current(5)	– 5.0		+ 5.0	µA
Cin	Input Capacitance(6)		8	8	pF
Cout	Output Capacitance(6)		8	8	pF

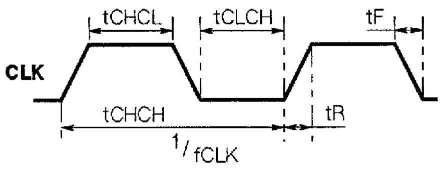
Notes :
1. Commercial operating range (0°C to 70°C)
2. VCC Max, f_{CLK} = 10 MHz, /CLKEN = F/I = ZZ = VIH, BLKIN = PIX = /OEN = VIL
   (/OEN without effect because /CLKEN = VIH)
   Min value : DI[0..11] = VIL & Max value : DI[0..11] = Random Pattern
3. VCC Max, f_{CLK} = 10 MHz, F/I = ZZ = VIH, PIX = /OEN = /CLKEN = VIL
   DI[0..11] = Random Pattern
   Min value : BLKIN = VIL & Max value : BLKIN active every block
4. IOL = 4 mA, IOH = –1 mA.
5. VCC max, Vin = VCC to VSS, Vout = VCC to VSS
6. These parameters are sampled and not 100 % tested – Amb. temp. = + 25°C.

AC Characteristics

AC Test Conditions

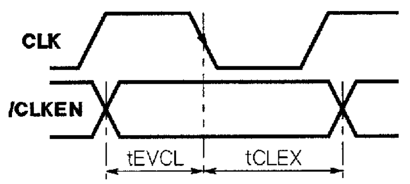
V_{CC} = + 5 V ± 10 %
Input pulse levels : 0 to + 3.0 V
Input timing reference level : + 1.5 V
Input rise : 5 ns
Output load : 1 TTL gate and CL = 50 pF
(including scope and jig)

CLK Timing



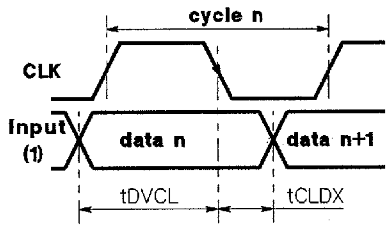
Symbol	Parameter	Min.	Max.	Unit
tCHCL/ tCLCH	Pulse High/Low Width	20	/	ns
tR/tF	Rise/Fall Time	/	20	ns
fCLK	CLK Frequency (1/tCHCH)	D.C	20	MHz

/CLKEN Timing



Symbol	Parameter	Min.	Max.	Unit
tEVCL	/CLKEN Set-Up Time	7	tCHCH – tCLEX min	ns
tCLEX	/CLKEN Hold Time	10	tCHCH – tEVCL min	ns

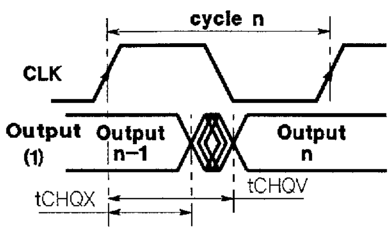
Input Timing



Symbol	Parameter	Min.	Max.	Unit
tDVCL	Data-In[1] set-Up Time	3	TCHCH – tCLDX min	ns
tCLDX	Data-In[1] Hold Time	10	tCHCH – tDVCL min	ns

Note : 1. The Inputs are : DI[0..11], BLKIN, F/I, PIX & ZZ.

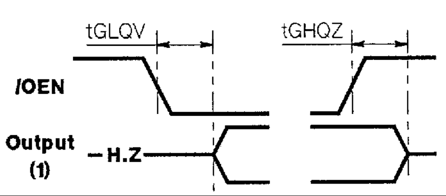
Output Timing



Symbol	Parameter	Min.	Max.	Unit
tCHQX	CLK High to Output n–1 Disable[1]	3	/	ns
tCHQV	CLK High to Output n Enable[1 & 2]	/	30	ns

Notes : 1. The Outputs are : DO[0..11] & BLKOUT
2. Including internal CLK restarting after /CLKEN activation

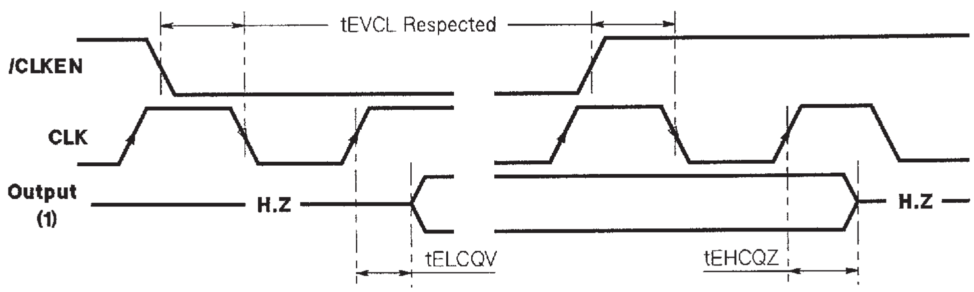
Output Enable Timing



Symbol	Parameter	Min.	Max.	Unit
tGHQZ	/EON High to H.Z Output[1]	/	30	ns
tGLQV	/OEN Low to L.Z Output[1]	0	/	ns

Note : 1. The Outputs are : DO[0..11] & BLKOUT
Iout = 10 mA, VOH = 2.4 V, VOL = 1.4 V.

/CLKEN to Output Timing



Symbol	Parameter	Min.	Max.	Unit
tEHCQZ	CLK High to High Z Output[1] (After Latching /CLKEN = VIH)	/	20	ns
tELCQV	CLK Low to Low Z Output[1] (After Latching /CLKEN = VIL)	0	/	ns

Note : 1. The Outputs are : DO[0..11] & BLKOUT
Iout = 10 mA,
VOH = 2.4 V, VOL = 1.4 V.

Ordering Information

S	M	JL	–	29C80F	SB
M: Mil S: Space		JL: MQFPJ44			Blank: Std Mil /883: MIL–STD–883 class B or S P883: /883+PIND Test SB: SCC9000 B SC: SCC9000 C Hxxx: Custom spec