2.5 Gbit/s 16:1 Multiplexer GD16507

Preliminary

General Information

The GD16507 is a high performance 2.5 Gbit/s 16:1 Multiplexer with on-chip VCO and PLL – sytem. Designed for use in ITU-T STM16 or SONET OC-48 fiber optic communication systems.

The GD16507 multiplexes sixteen 155 Mbit/s data streams into a single 2.5 Gbit/s data stream output using an external reference clock at 155.52 MHz or 77.6 MHz.

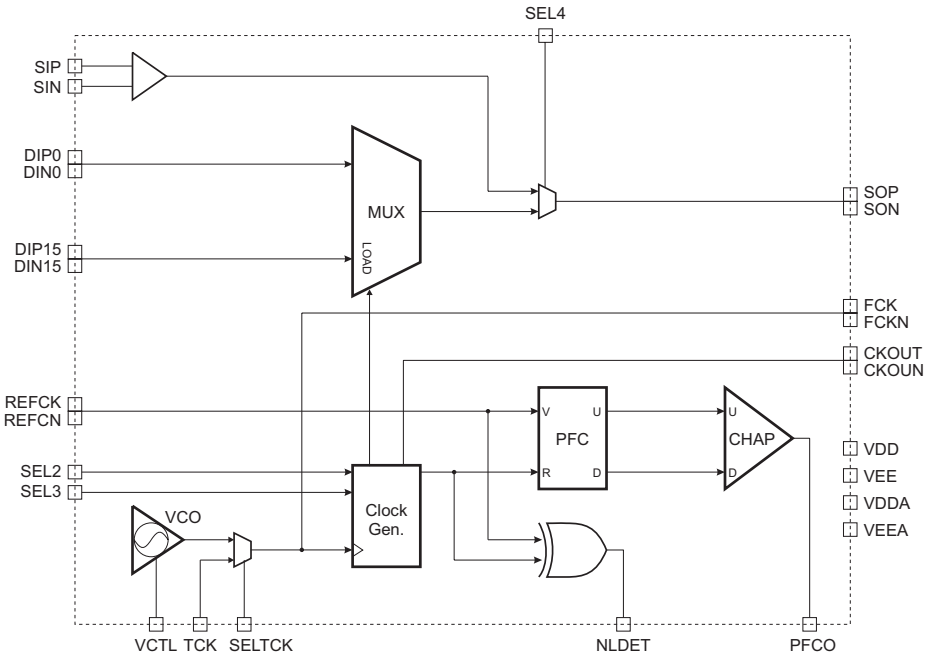
The output bit rate of the GD16507 covers the frequency range 2.3-2.7 GHz depending on the reference clock frequency.

A selecable high-speed data input allows direct 2.5 Gbit/s input to the 2.5 Gbit output (no retiming).

Internal clock synchronisation is provided by an on-chip PLL circuit requiring a simple passive external loop filter. The PLL circuit features an NLDET pin output for simple implementation of a lock detect function, as shown overleaf.

The GD16507 is manufactured in a Silicon Process .

The GD16507 requires a single -5.2 V supply.



Features

- SDH STM-16, SONET OC-48 compatible.
- On-chip PLL containing low jitter 2.5 GHz VCO, phase/frequency detector and charge pump.
- PLL lock detect output.
- Single -5.2 V supply operation.
- Differential ECL 2.5 GHz clock and 2.5 Gbit data output.
- Differential ECL compatible data and clock inputs.
- Power dissipation: 1.0 W (typ.).
- Packaged in:
  - 144 ld fpBGA
  - 68 pin MLC

Applications

- Tele Communications systems:
  - SDH STM-16
  - SONET OC-48
- Data Communications

Application Details

PLL Loop Filter and PLL Reset

Based on GIGA's experience with the PLL in the GD16507, GIGA recommends use of a loop filter, as shown in the figure below. This loop filter is used in the AC production test set-up and has been found to ensure that the jitter performance of GD16507 is within ITU specifications. Loop filter component values TBD.

Resistor (R1) connected between the pins PFCO and VCTL, helps to linearise the current source in the charge pump.

Resistor (R2) and capacitor (C1) comprise the loop filter. These components have been shown to give optimum PLL performance under test, with jitter well within the specifications. The optimum choice of component values with regard to jitter is affected by the reference clock phase-noise performance.

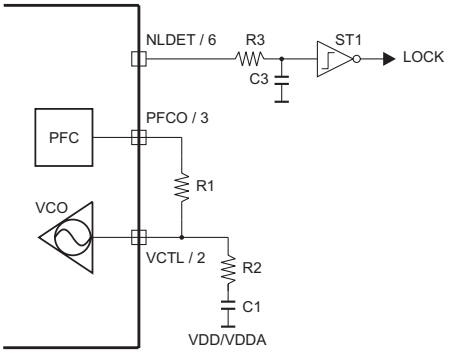


Figure 1. *PLL Loop Filter*

For noise and jitter reasons it is very important that C1 is connected to VDD/VDDA in close proximity of the VCTL pin.

Lock Detect Circuit

A simple PLL lock detect function can be implemented by 3 external components (R3, C3 and ST1), comprising a low-pass filter followed by a Schmitt trigger, as shown in the figure below.

Pin List

Mnemonic:	Pin Number 144EA	Pin Number 68BA	Pin Type:	Description:
DIP0, DIN0 DIP1, DIN1 DIP2, DIN2 DIP3, DIN3 DIP4, DIN4 DIP5, DIN5 DIP6, DIN6 DIP7, DIN7 DIP8, DIN8 DIP9, DIN9 DIP10, DIN10 DIP11, DIN11 DIP12, DIN12 DIP13, DIN13 DIP14, DIN14 DIP15, DIN15	A7, B7 A8, B8 A9, B9 A10, B10 A12, B12 C12, D11 D12, E11 E12, F11 H12, J12 L12, K12 M11, M12 M10, L10 M9, L9 M8, L9 M7, L7 M6, L6	8, 7 11, 10 13, 12 16, 15 20, 19 23, 22 25, 24 28, 27 33, 32 37, 36 40, 39 42, 41 45, 44 47, 46 50, 49 54, 53	ECL IN	Differential data inputs. Shifted to the serial output starting with DI15, followed by DI14, DI13....
SIP, SIN	C1, D1	63, 62	CML IN	Differential serial input. High speed self-terminating input to be used in conjunction with GD16504 for remote/line loop back.
REFCK, REFCN	A1, A2	67, 66	ECL IN	Reference clock differential input for PLL.
SEL1	G1	N/A	ECL IN	Select signal for reference clock frequency. When high, 155.52 MHz is selected; when low, 77.76 MHz. Bonded high for 155.52 MHz option in 68BA version.
SEL2 SEL3	B2 H11	6 N/A	ECL IN	Phase relation select between positive going edge of CKOUT and sample time of input data: SEL3, SEL2 1 1 T_{DEL} = 0° 1 0 T_{DEL} = 90° 0 1 T_{DEL} = 180° 0 0 T_{DEL} = 270° SEL3 is bounded high in 68BA version.
SEL4	M4	35	ECL IN	Select between MUX or Serial Input as source for the output buffer. When high, MUX is selected; low, Serial Input.
VCTL	A4	2	Anl. IN	VCO voltage control input.
TCK		64	ECL IN	Test clock input. Replaces the VCO as clock source when SELTCK is set to high.
SOP, SON	J1, K1	57, 56	ECL OUT	Differential Serial Output, 2.488 Gbit/s.
FCK, FCKN	F1, G1	58, 59	ECL OUT	Differential Serial Clock Output, 2.5 GHz.
CKOUT, CKOUN	F12, G12	29, 30	ECL OUT	155.52 MHz subdivided VCO-clock. Phase relation between this output and sample point of input data configurable by SEL2, 3.
PFCO	A5	3	Anl. OUT	Phase/ frequency comparator output. Changes between Drive High - Tristate - Drive Low according to VCO phase and freq. with respect to REFCK.
NLDET	B6	6	Anl. OUT	Inverted Lock Detect output. Refer to Figure 1on page 2 for connection.
SELTCK	J11	17	ECL IN	Select TCK for Clock input. For DC test only. Connect to VEE for normal operation.
VDD	B1, C2, D2, D4..D9, E1, E2, E4..9, F2, F4..9, G2, G4..9, H1, H2, H4..H9, J2, J4..9, K2, L1	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V Power for core and ECL I/O.

Mnemonic:	Pin Number 144EA	68BA	Pin Type:	Description:
VEE	C3..9, D3, D10, E3, E10, F3, F10, G3, G10, H3, H10, J3, J10, K3..9, M3	34, 52	PWR	-5 V Power for core and ECL I/O.
VDDA	B4, B5	1	PWR	0 V Power for VCO.
VEEA	A3, A6	18, 68	PWR	-5 V Power for VCO.
NC	A11, B11, C11, K10, K11, L2..5, L11, M1, M2	5, 51	NC	Not connected.

Package Pinout

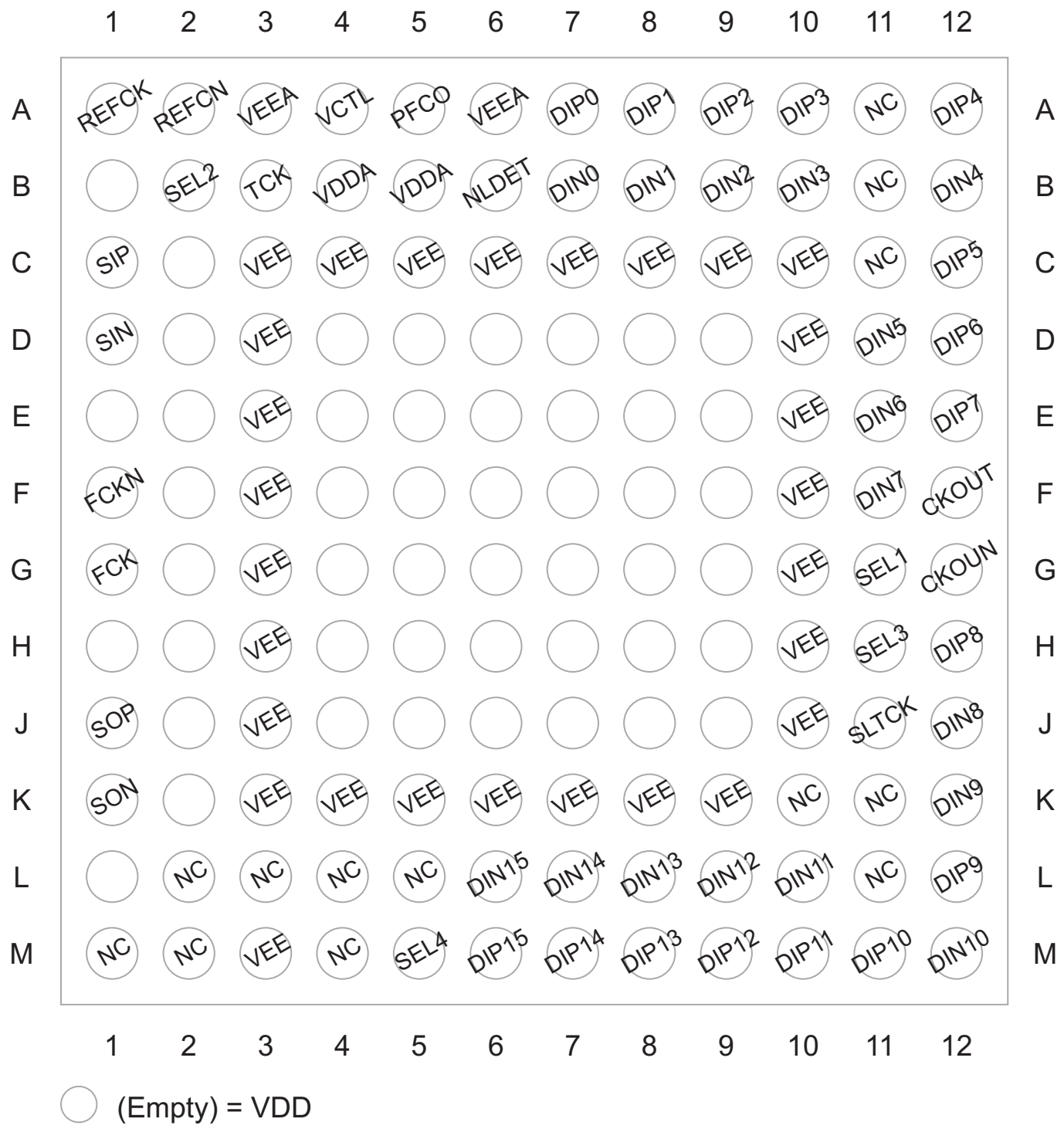


Figure 2. *Package Pinout - 144EA, Top View*

Note: Please note that this pinout is under design and can be changed.

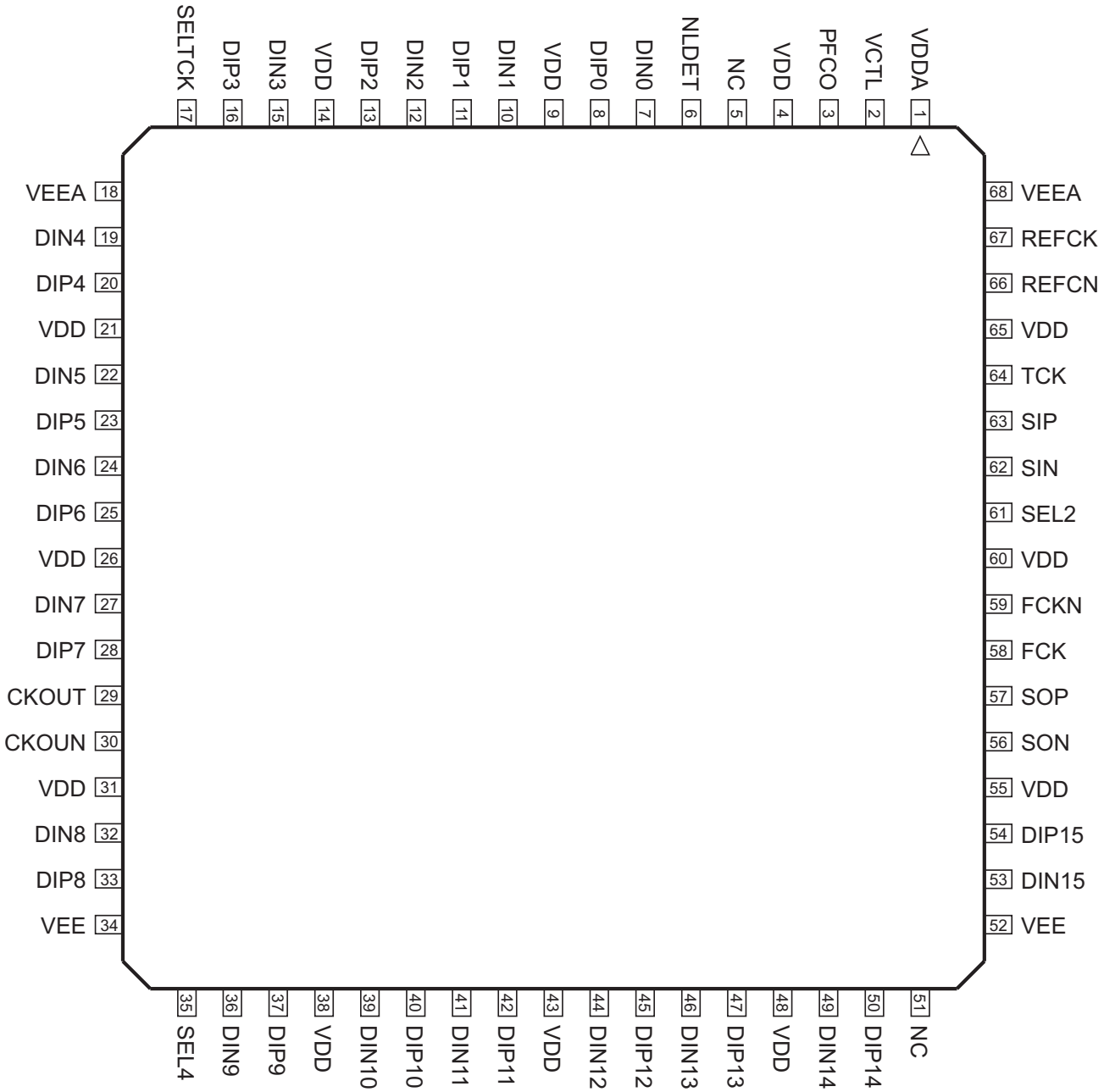


Figure 3. *Package Pinout - 68BA, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD (Ground).
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}, V_{EEA}	Power Supply		-7		0	V
V_O	Applied Voltage (all outputs)		V_{EE} -0.5		0.5	V
$I_{O\ ECL}$	Output Current ECL		-10		40	mA
$I_{O\ NLDET}$	Output Current NLDET		-3		8	mA
V_I	Applied Voltage		V_{EE} -0.5		0.5	V
$V_{IO\ ESD}$	ESD I/O Sensitivity	Note 1		±500		V
$I_{I\ ECL}$	Input Current ECL		-1		1	mA
T_O	Operating Temperature	Channel	-55		+150	°C
T_S	Storage Tempeature		-65		+175	°C

Note 1: Human body model (100 pF, 1500 Ω) MIL 883 standard. Actual ESD level TBD.

DC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -5.4 V to -5.0 V
All voltages in the table are referred to VDD.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Supply Voltage		-5.4	-5.2	-5.0	V
I_{EE}	Supply Current			200	250	mA
P_{DISS}	Power Dissipation			1000		mW
$V_{IH\,ECL}$	ECL Input HI Voltage		-1.1		-0.7	V
$V_{IL\,ECL}$	ECL Input LO Voltage	Note 2	V_{EE}		-1.5	V
$V_{IH\,SEL4}$	ECL SEL4 input HI Voltage		-1.1		0	V
$V_{IL\,SEL4}$	ECL SEL4 input LO Voltage	Note 1	V_{EE}		-1.5	V
$I_{IH\,ECL}$	ECL Input HI Current	$V_{IH\,max}$			10	mA
$I_{IL\,ECL}$	ECL input LO Current	$V_{IL\,min}$			-10	mA
$V_{OH\,ECL}$	ECL Output HI Voltage	Note 2, 3	-1.0		-0.5	V
$V_{OL\,ECL}$	ECL Output LO Voltage	Note 2, 3	V_{TT}		-1.6	V
$I_{OH\,ECL}$	ECL Output HI Current	Note 4	20	23	30	mA
$I_{OL\,ECL}$	ECL Output LO Current	Note 4	-2	5	8	mA
$V_{OH\,NLDET}$	NLDET Output HI Voltage		-1.2		0	V
$V_{OL\,NLDET}$	NLDET Output LO Voltage		V_{EE}		V_{EE}+1.2	V
$I_{OH\,NLDET}$	NLDET Output HI Current		1			mA
$I_{OL\,NLDET}$	NLDET Output LO Current		-1			mA
V_{CTL}	VCO Control Voltage	I_{VCTL}< 30 µA	V_{EE}		-0.5	V
$I_{OH\,PFCO}$	PFCO	Note 5	100	500		µA
$I_{OL\,PFCO}$	PFCO	Note 5		-500	-100	µA

Note 1: V_{EE} = -5.0 V.
Note 2: V_{TT} = -2.0 V ± 5 %.
Note 3: R_{load} = 50 Ω to V_{TT}.
Note 4: Not tested, consistent with V_{OH} and V_{OL} tests.
Note 5: Output terminated to -2.5 V during test.

AC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -5.5 V to -4.95 V.

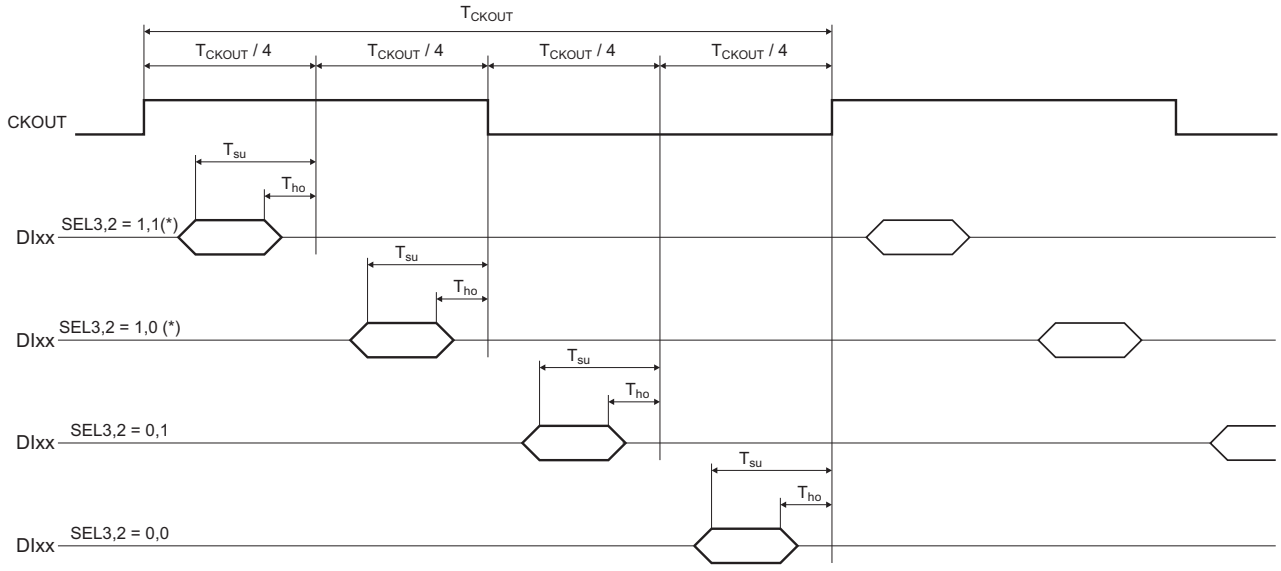
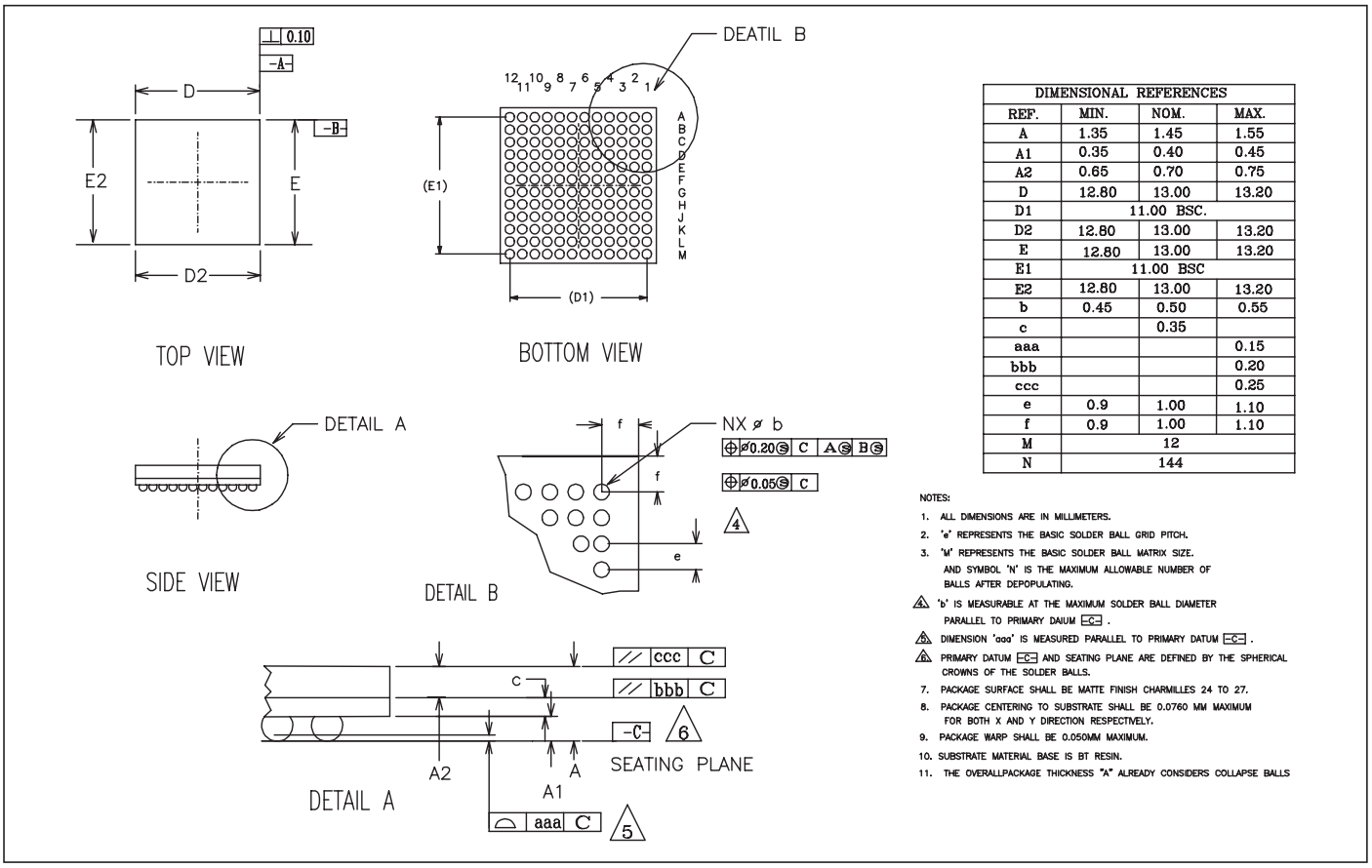


Figure 4. *DI0..DI15 Data Input Set-up and Hold with Respect to CKOUT. Only options 1,1 and 1,0 (*) are available in 68BA.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Gen}	Jitter Generation	12 kHz < f_C < 20 MHz (Note 1)			0.5	$UI_{16, p-p}$
J_{Trf}	Jitter Transfer	12 kHz < f_C < 2 MHz (Note 2)		0.08	0.1	dB
J_{Clk}	Output Clock Intrinsic Jitter	5 kHz < f < 1 MHz (Note 3) 1 MHz< f < 20 MHz (Note 3)			0.125 0.05	$UI_{16, p-p}$ $UI_{16, p-p}$
$T_{LH\ OD}$	High speed ECL output rise time 50 Ω	20 – 80 % (Note 4)				ps
$T_{HL\ OD}$	High speed ECL output fall time 50 Ω	80 – 20 % (Note 4)				ps
$T_{LH\ Clock}$	CKOUT/ CKOUN rise time	20 – 80 %, 25 Ω to -2 V		350	700	ps
$T_{THL\ Clock}$	CKOUT/ CKOUN fall time	80 – 20 %, 25 Ω to -2 V		350	700	ps
$T_{LH\ ECL}$	ECL Output rise time	20 – 80 %, 50 Ω to -2 V		350	700	ps
$T_{THL\ ECL}$	ECL Output fall time	80 – 20 %, 50 Ω to -2 V		350	700	ps
$C_{DUTY\ REFCK}$	REFCK clock duty cycle	$V_{Thresh.}$ = -1.3 V	40		60	%
$C_{DUTY\ CKOUT}$	Output clock duty cycle	$V_{Thresh.}$ = -1.3 V, 25 Ω to -2 V	45		55	%
$C_{DUTY\ CKOUT}$	Differential output clock duty cycle	Note 5	49.0	50.0	51.0	%
T_{su}	DIN set-up from CKOUT	SEL3/2: 1,1	-1600			ps
T_{ho}	DIN hold from CKOUT	SEL3/2: 1,1			-400	ps
F_{REFCK}	REFCK, REFCN input freq.	SEL1 = 1 SEL1 = 0	144 72	155.5 77.76	163 81.5	MHz MHz
$F_{SOP,\ SON}$	Open Collector Output Bit Rate		2.3	2.488	2.6	Gbit/s
F_{VCO}	VCO Frequency Range		2.3		2.6	GHz
K_{VCO}	VCO Gain Constant	Measured at operating point		250		MHz/V
$N_{Parallel\ -\ Serial}$	no. of bits stored in pipe-lines				40	bits

Note 1: UI_{16} = 402ps.
Note 2: Transfer Jitter = 20log J_{SOP}/J_{REFCK} within freq. range. f_C is loop filter dependant, see figure. The choice of f_C is a trade off between Jitter Transfer reduction and VCO Phase Noise Suppression. Through careful filter design, loop peaking may be controlled, which is the major contribute to Jitter Transfer.
Note 3: In the absence of input jitter, the intrinsic jitter at CKOUT as measured over a 60 seconds interval shall not exceed these limits.
Note 4: R_{load} = 50 Ω to *VDD*. I_{LD} = 20 mA.
Note 5: Measuret in a “perfect” differential environment.

Package Outline



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.35	1.45	1.55
A1	0.35	0.40	0.45
A2	0.65	0.70	0.75
D	12.80	13.00	13.20
D1		11.00 BSC.	
D2	12.80	13.00	13.20
E	12.80	13.00	13.20
E1		11.00 BSC	
E2	12.80	13.00	13.20
b	0.45	0.50	0.55
c		0.35	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.9	1.00	1.10
f	0.9	1.00	1.10
M		12	
N		144	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'N' IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DAIUM -C- .
5. DIMENSION 'aaa' IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. PACKAGE CENTERING TO SUBSTRATE SHALL BE 0.0760 MM MAXIMUM FOR BOTH X AND Y DIRECTION RESPECTIVELY.
9. PACKAGE WARP SHALL BE 0.050MM MAXIMUM.
10. SUBSTRATE MATERIAL BASE IS BT RESIN.
11. THE OVERALLPACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS

Figure 5. *Package outline - 144EA. All dimensions are in mm.*

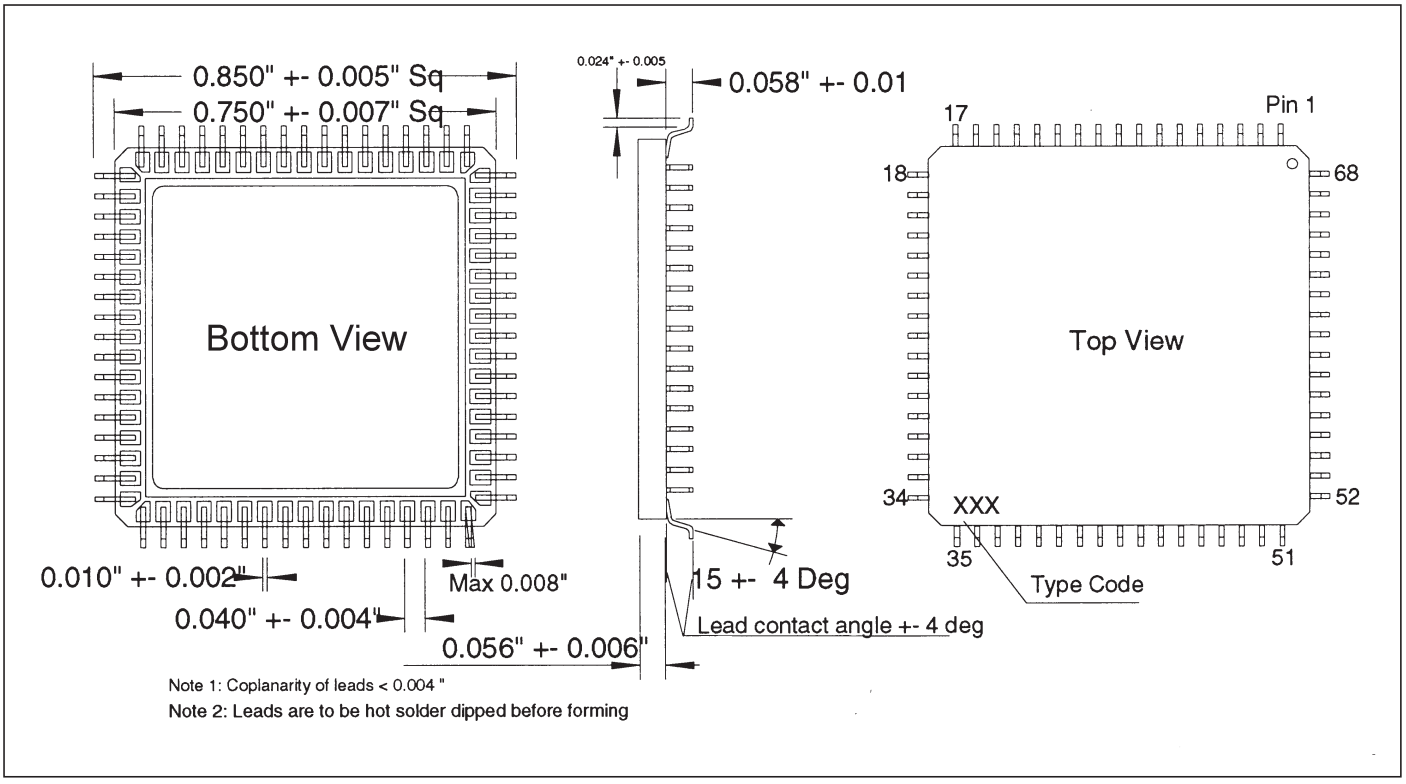


Figure 6. *Package outline - 68BA. All dimensions are in mm.*

Device Marking

Figure 7. *Device marking - 68BA, Top view.*

Ordering Information

Product Name:	Package Type:	Case Temperature Range:	Options:
GD16507-144EA	144 fpBGA	0..85 °C	
GD16507-68BA	68 pin MLC	0..85 °C	

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