17 TELEDYNE COMPONENTS

4736

HIGH-RELIABILITY HYBRID FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- Wide Power Supply Range±12V to ±18V
- Nonlinearity±0.008% FS Max
- **Accepts Any Input Waveshape**
- **High Noise Immunity**
- Low Full-Scale Drift
- Low Offset-Voltage Drift

APPLICATIONS

- Measure Flow, RPM, Frequency
- Demodulate FM
- **Use With V-to-F Converter**
- **Low-Cost FM Telemetry**
- **DC Response Magnetic Tape Recording**
- Multi-Decade Range Phase Lock Loops
- Fiber-Optic Data Link

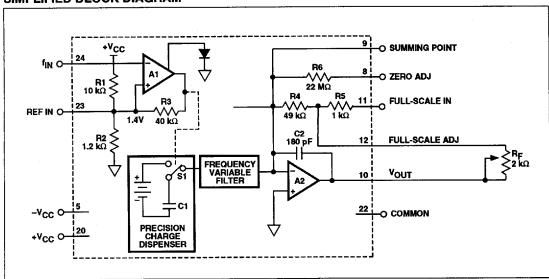
GENERAL DESCRIPTION

The 4736 is an ultra-linear, low-drift frequency-to-voltage (F-to-V) converter which produces an output voltage linearly proportional to input frequency, regardless of input waveshape. Designed to satisfy a multitude of precision system requirements, the 4736 represents an invaluable tool for the advancement of data acquisition and signal processing technology.

The superior specifications of the 4736 allow it to be used in the most critical frequency conversion applications. Common tasks include monitoring/controlling the pulsed output of a motor or flowmeter.

The standard 4736 is packaged in a 24-pin dual-in-line metal package and is specified for 0°C to +70°C operation. For high-reliability applications, the 4736-HR is specified for -55°C to +125°C operation.

SIMPLIFIED BLOCK DIAGRAM



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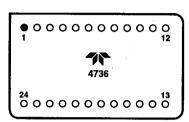
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PIN CONFIGURATION



Pin No.	Designation	Pin No.	Designation
1	NC	24	fin
2	NC	23	REF INPUT
3	NC	22	COMMON
4	NC	21	NC
5	-V _{cc}	20	+V _{CC}
6	NC	19	NC
7	NC	18	NC
8	ZERO ADJUST	17	NC
9	SUMMING POINT	16	NC
10	OUTPUT	15	NC
11	FULL-SCALE INPUT	14	NC
12	FULL-SCALE ADJ.	13	NC

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Power Supplies±22V
V_{IN}	Input Voltage±V _{CC} to ±15V
V_{ID}	Differential Input Voltage±12V
V_{REF}	Reference Voltage±12V
Tc	Specified Temperature Range (Case)
	47360°C to +70°C
	4736-HR55°C to +125°C
T _{STG}	Storage Temperature Range65°C to +150°C
T_S	Lead Temperature
	(Soldering, 0.06" from pkg., < 10 sec) 260°C
	Unit Weight11,2g Tvp

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ELECTRICAL CHARACTERISTICS: $T_C = +25$ °C, $\pm V_{CC} = \pm 15$ V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Input						
f _{IN}	Frequency Input Range		0	1	1.3	MHz
	Input Waveform			Any		
t _{PW}	Input Pulse Width	V _{IH} = 2V	75			ns
V _{IH}	Input High Voltage		.2		12	٧
VIL	Input Low Voltage		-12	-	0.8	V
V _{INT+}	Threshold, Positive-Going Pulses	Typically 1.4V ±200 mV	8.0	1.4	2.2	V
	Threshold, External Set Range				±12	ν .
	Hysteresis		300	400	500°	mV
	Hysteresis, External Set Range		0	400		mV
R _{IN}	Input Impedance			100ll4		GΩllpF
Output		1				
Vo	Full-Scale Output Voltage	Pin 10 Shorted to Pin 11	9.99	10	10.01	<u>v</u>
VOADJ	Vo Adjustable Full-Scale Voltage	Pin 10 Shorted to Pin 12	9.97	9.9	10.03	V
V _O /TC	Vo Full Scale vs Temperature	0°C to +70°C (Standard)	_	±40	±50	ppm/°C
	<u> </u>	-55°C to +125°C (HR)		±70	±100	ppm/°C
Vos	Output Offset Voltage	f _{IN} = 0 Hz		±1	±5	mV
V _{OS} /TC	Vos Voltage vs Temperature	0°C to +70°C (Standard)	_	±20	±50	μV/°C
		-55°C to +125°C (HR)		±30	±80	μV/°C
Vole	V _O Linearity Error	1.1 kHz to 1 MHz		±0.003	±0.008	
V _{OLE} /TC	V _{OLE} Over Temperature	1.1 kHz to 1 MHz,	_	±0.005	±0.015	%FS
		0°C to +70°C (Standard)		±0.008	±0.05	%FS
		1.1 kHz to 1 MHz, -55°C to +125°C (HR)	_	10.000	10.03	761 3
	V _O Ripple Voltage	f _{IN} = 100 Hz		80	200	mV _{P-P}
	AO Libbie Agirade	f _{iN} = 100 kHz	_	450	700	mV _{P-P}
		f _{IN} = 1 MHz		80	150	mV _{P-P}
	V _O vs Time	Per Day		±20	_	μV/D
		Per Week		±60	_	μV/W
PSRR ₁	Vo Zero vs Power Supplies }	±Vps from ±13V to ±17V referred	_	±10	±20	μV%ΔVps
PSRR ₂	Vo Full Scale vs Power Supplies }	to Vps = ±15V	_	±40	±80	ppm/%∆Vps
lo	Output Current	Not Short-Circuit Protected	-2/+20		_	mA
Ro	Output Impedance		_	<u>L – </u>	0.05	Ω
Transfer						
	Ideal Transfer Function	fA = 1 MHz	[f _{IN}	+ fA] × 1	oV	V
Dynamic					:	
RC	Response Time, Internal Filter			9	ļ <u>-</u>	μs
t _{SR}	Step Response Time to 0.5 %FS	0 Hz to 1 MHz Step, R _L = 500Ω	_	60	-	μѕ
		1 MHz to 200 kHz Step, R _L = 500Ω	_	70 95	-	μs
		1 MHz to 0 Hz Step, $R_L = 500\Omega$		95	 _	μs
Power Sup	•		±13	±15	±17	V
V _{CC}	Voltage Range	<u> </u>	113	±28	±35	mA .
lcc	Quiescent Current		<u> </u>	1050	135	mW
PD	Power Dissipation			1000		11184

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested at +25°C. HR versions have I_O, V_{OLE}/TC, V_O, V_{OS} and V_{OS}/TC tested at -55°C, +25°C and +125°C. Standard parts are tested at room temperature only. Other min/max parameters are guaranteed by design.

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THEORY OF OPERATION

The 4736 F-to-V converter is an example of a sophisticated concept implemented in a low-cost, highly reliable device (see block diagram). The input is a comparator (A1) whose output switches between +1V and -14V each time the voltage between f_{IN} (pin 24) and REF IN (pin 23) reverses polarity. Two consecutive reversals are interpreted as one cycle (or pulse) of input frequency.

Each reversal causes a solid-state switch (S1) to alternately connect capacitor C1 to a precision reference voltage and then, through a frequency-variable filter, to the summing point of op-amp A2. Each time C1 is connected to the reference voltage, a fixed amount of charge (Q) is dumped into C1 according to the equation Q = CV.

When C1 is connected to the summing point of A2, it discharges and the resulting current is converted to a voltage. The higher the input frequency, the greater the average current into the summing point. A2 is a current-to-voltage converter, where:

$$V_{OUT} = -(I \times R_F)$$

Therefore, V_{OUT} is a function of the discharge current from C1, the frequency of discharge, and the feedback resistor. C2 filters the current pulses from C1 to minimize output voltage ripple.

When used as shown in Figure 1, the 4736 operates as specified with no additional components.

Input Threshold

The f_{IN} (A1) input comparator's threshold is preset at +1.4V to provide maximum noise immunity when operating with TTL levels and has approximately 400 mV of hysteresis. It can operate with signals of any waveshape which vary about this threshold; for example, a 0V to 2V square wave or a ± 5 V_{P-P} sine wave. Each alternate threshold crossing is recognized as one cycle (or pulse) of input frequency.

The threshold level at which comparator A1 switches is set to 1.4V by resistors R1, R2 and R3. The threshold level can be modified by inputting a voltage to REF IN. The threshold will be equal to the voltage input to pin 23. This voltage should not exceed 12V, or internal damage will occur.

The comparator hysteresis (400 mV) can be reduced by connecting REF IN to COMMON (pin 22) with a resistor (see "Operation with HNIL or CMOS Logic" following).

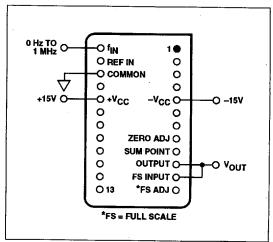


Figure 1. Basic Operational Connections

Output Circuit

The 4736 output is an inverting op amp. The output voltage is set by connecting the OUTPUT (pin 10) to FULL-SCALE IN (pin 11) or FULL-SCALE ADJ (pin 12). These are the gain-setting inputs, feedback paths, for amplifier A2.

Pin 11 is the nominal feedback connection. The internal resistor is factory trimmed to approximately 49.5 k Ω and produces a +10V \pm 0.1% output for a 1 MHz input frequency. Use this input when accuracy to \pm 0.1% full scale is sufficient or when external components cannot be tolerated. Use pin 12 when greater accuracy is required, as it allows use of an external trim (see Figure 2).

The feedback resistor from pin 12 is approximately 495Ω (or 1%) less than nominal. Connecting a 1 k Ω potentiometer between the output and pin 12 allows the user to fine-tune the output accuracy over a $\pm 1\%$ range.

Trim Procedure

Referring to Figure 2:

- 1. Connect fin to COMMON and adjust R1 for 0V output.
- Connect f_{IN} to a frequency source set at 1 MHz and adjust R2 for 10V output.
- 3. Repeat steps (1) and (2) until zero and full scale are set.

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0 Hz TO 1 MHz O IN O REF IN 0 O COMMON 0 -15V O 0 O+Vcc -vcc O +15V O 0 0 O O **R1*** O ZERO ADJ O 50 kΩ O SUM POINT O OUTPUT O O VOUT **FS INPUT O** O O 13 FS ADJ O 2 kΩ *R1 and R2 should have low temperature coefficient.

Figure 2. Zero and Full-Scale Trim

Output Offsetting

Many frequency-to-voltage applications measure a range of frequencies that do not include zero, but require zero volts out for a particular frequency input. For example, the pulse train from a tachometer in a motor speed-control circuit might range between 500,000 and 1,000,000 pulses per second which would normally generate +5V to +10V from the 4736.

To obtain a 0V to +5V output range the 4736 must be offset by -5V. This is done by injecting a current of approximately +50 μ A into the SUMMING POINT (pin 9).

The offset-adjust scale factor is $-10\,\mu\text{A/V}\pm25\%$. Offset adjust can be implemented, as shown in Figure 3, by connecting a potentiometer or fixed resistor between the SUMMING POINT and +V_{CC} (pin 20). The resistor value can be calculated:

R =
$$V_{CC}$$
 + [V_{OFF} × Offset Scale Factor]
= 15 + [5 × 0.00001]
= 300 k Ω

If a bipolar output voltage of -2.5V to +2.5V is required for a 500 kHz to 1 MHz input, the output may be offset a total of -7.5V by the same method.

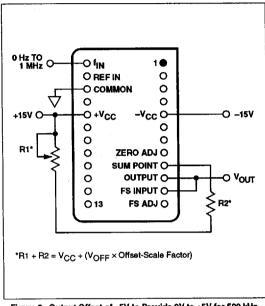


Figure 3. Output Offset of --5V to Provide 0V to +5V for 500 kHz to 1 MHz Input Frequency

Scale Expansion and Output Offset

If an application requires a full-scale (0V to +10V) output for a less than full-scale range of input frequencies, the full-scale factor can be expanded by increasing the feedback resistor for A2. This is done by adding a series resistor to the internal feedback resistors. Another method is not to use the internal resistors and to add an external resistor between the SUMMING POINT and the OUTPUT (see Figure 4). The value for the total feedback resistance needed, regardless of which method you choose, is:

$$\begin{split} R_F &= G \times 100,000 \\ &= [\Delta V_{OUT} + \Delta f_{\text{IN}} \text{ (in kHz)]} \times 100,000 \\ &= [10 + 500] \times 100,000 \\ &= 2 \text{ k}\Omega \text{ ($\pm 25\%$)} \end{split}$$

If this technique is used, be sure to account for the 4736's output compliance range. For example, at G=2, a 500 kHz input produces +10V output, and a 1 MHz input demands a +20V output which will overrange the output of the 4736. The output must be offset by -10V.

Be aware that the offset scale factor must be divided by the gain factor (G) that you have determined. Therefore, to offset the output by –10V you must drive ([–10 μ A/V + Gain of 2] × –10V) = +50 μ A/V into the summing point.

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11 kO

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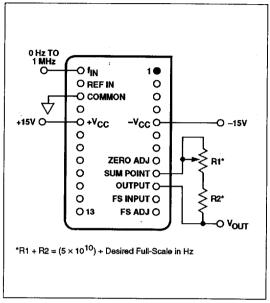


Figure 4. Custom Full-Scale Factor

O fin 0.1 μF OREFIN 0 O COMMON 0 1 MO O 0 O+Vcc -Vcc O ±500 -15V O Q O 0 0 DC OFFSET 0 ZERO ADJ O O SUM POINT () O **OUTPUT O** О∨оит O FS INPUT O O 13 FS ADJ O

Figure 5. Input Conditioned for Small AC Signal with DC Offset

Operation With HNIL or CMOS Logic

To obtain maximum noise immunity with a particular logic type, the threshold should be set approximately half-way between the upper and lower logic levels. For example, a 2 k Ω , 5% resistor connected between REF IN and +15V provides a threshold of +6V (a typical CMOS or HNIL threshold level). Adjusting the threshold voltage in this manner has no impact on the zero and full-scale trim techniques discussed earlier.

Operation With Signals Less Than +2V Peak

Connecting an 11 k Ω , 5% resistor between REF IN and –15V will set the threshold at 0V with hysteresis of approximately 340 mV. Now the input signal only needs to be larger than 340 mV. However, input signals less than 500 mV should be used with care. They may produce erroneous output voltage due to the uncertainty of the hysteresis level.

For input signals less than 500 mV, hysteresis should be reduced by connecting a 200Ω resistor between REF IN and COMMON. This will lower the hysteresis and noise immunity to approximately 60 mV (see Figure 5). A 100Ω resistor provides 30 mV of hysteresis, which is the minimum recommended value. When operating in this mode the 4736 is virtually a zero-crossing detector.

Operation With DC Common Mode

When the input signal is small and impressed on a DC voltage (i.e., +9V DC ± 500 mV AC), it should be capacitively coupled to the 4736, as shown in Figure 5. If the DC voltage is large, greater than $\pm V_{CC}$, the input should be protected against transients with diodes, as shown in Figure 6.

Signals greater than $\pm V_{CC}$ peak-to-peak may also be attenuated with a simple resistive divider and the appropriate threshold level, as discussed earlier.

Scale Expansion and Bipolar Output

If an output voltage of –5V to +5V is required for 500 kHz to 1 MHz input, the same technique described in "Scale Expansion and Output Offset" is used. The scale is doubled and the output is offset a total of –15V (from +10V to –5V) by additional current into the SUMMING POINT (pin 9).

Output Ripple Filtering and Response Time

By definition, frequency-to-voltage conversion is converting an AC signal to a DC level. Therefore, there must be ripple on the output. This ripple is filtered by a frequency variable filter and by an internal RC network consisting of Re and a capacitor (C2) (see block diagram). Additional filtering

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is obtained by adding an external capacitance between the summing point and output.

The response time of the F-to-V converter (how fast the output voltage changes for a step change in the input frequency) is the RC time constant of the ripple filter. If

external capacitance is added, response time is increased. If faster response with reduced ripple voltage is required, a higher frequency-to-voltage should be used or a multipole (i.e., sharp cutoff) low-pass filter should follow the frequencyto-voltage.

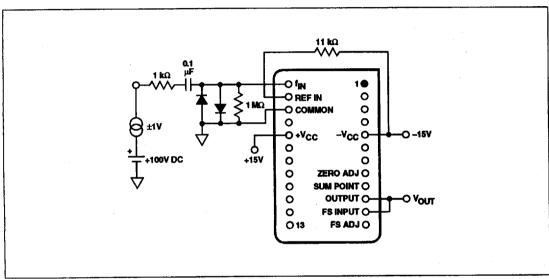


Figure 6. Input Conditioned for Small AC Signal Impressed on Large DC Voltage