
HD66752

(132 x 168-dot Graphics LCD Controller/Driver with
Bit-operation Functions)

HITACHI

ADE-207-326(Z)

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Description

The HD66752, dot-matrix graphics LCD controller and driver LSI, displays 132-by-168-dot graphics for four monochrome grayscales. When 12-by-13-dot size fonts are used, up to 13 lines x 11 characters (143 characters) can be simultaneously displayed. Since the HD66752 incorporates bit-operation functions and a 16-bit high-speed bus interface, it enables efficient data transfer and high-speed rewriting of data in the graphics RAM.

The HD66752 has various functions for reducing the power consumption of an LCD system, such as low-voltage operation of 2.0 V/min., a step-up circuit to generate a maximum of seven-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66752 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bidirectional pagers, and small PDAs.

Features

- 132 × 168-dot graphics display LCD controller/driver for four monochrome grayscales (1/132 duty)
- 16-/8-bit high-speed bus interface
- Bit-operation functions for graphics processing:
 - Write-data mask function in bit units
 - Bit rotation function
 - Bit logic-operation function
- Low-power operation supports:
 - $V_{CC} = 2.0$ to 3.6 V (low voltage)
 - $V_{LCD} = 5$ to 15.5 V (liquid crystal drive voltage)
 - Two-, five-, six-, or seven-times step-up circuit for liquid crystal drive voltage
 - 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
 - Power-save functions such as the standby mode and sleep mode
 - Programmable drive duty ratios and bias values displayed on LCD

HD66752

- 168-segment × 132-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Duty ratio and drive bias (selectable by program)
- Window cursor display supported by hardware
- Black-and-white reversed display
- Internal oscillation and hardware reset
- Shift change of segment and common driver

Table 1 Programmable Display Sizes and Duty Ratios

Duty Ratio	Optimum Drive Bias	Bit-map Display Area	Graphics Display				
			12 x 13-dot Font Width	12 x 14-dot Font Width	16 x 16-dot Font Width	16 x 17-dot Font Width	8 x 10-dot Font Width
1/96	1/10	96 x 168 dots	13 lines x 8 characters	12 lines x 8 characters	10 lines x 6 characters	9 lines x 6 characters	16 lines x 12 characters
1/104	1/11	104 x 168 dots	13 lines x 8 characters	12 lines x 8 characters	10 lines x 6 characters	9 lines x 6 characters	16 lines x 13 characters
1/112	1/11	112 x 168 dots	13 lines x 9 characters	12 lines x 9 characters	10 lines x 7 characters	9 lines x 7 characters	16 lines x 14 characters
1/120	1/11	120 x 168 dots	13 lines x 10 characters	12 lines x 10 characters	10 lines x 7 characters	9 lines x 7 characters	16 lines x 15 characters
1/128	1/11	128 x 168 dots	13 lines x 10 characters	12 lines x 10 characters	10 lines x 8 characters	9 lines x 8 characters	16 lines x 16 characters
1/132	1/11	132 x 168 dots	13 lines x 11 characters	12 lines x 11 characters	10 lines x 8 characters	9 lines x 8 characters	16 lines x 16 characters

Note: When 12 x 13-dot fonts are used for display, the spaces between characters on the last line are not displayed.

<Target values>

Total Current Consumption Characteristics (V_{cc} = 3 V, TYP Conditions, LCD Drive Power Current Included)

Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Total Power Consumption				
				Normal Display Operation				
				Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
96 x 168 dots	1/96	100 kHz	69 Hz	(60 µA)	(20 µA)	Five-times (160 µA)	(12 µA)	0.1 µA
104 x 168 dots	1/104	100 kHz	69 Hz	(60 µA)	(20 µA)	Five-times (160 µA)	(12 µA)	
112 x 168 dots	1/112	100 kHz	69 Hz	(70 µA)	(25 µA)	Six-times (220 µA)	(12 µA)	
120 x 168 dots	1/120	100 kHz	69 Hz	(70 µA)	(25 µA)	Six-times (220 µA)	(12 µA)	
128 x 168 dots	1/128	100 kHz	71 Hz	(80 µA)	(25 µA)	Six-times (230 µA)	(12 µA)	
132 x 168 dots	1/132	100 kHz	69 Hz	(80 µA)	(25 µA)	Six-times (230 µA)	(12 µA)	

Note: When a two-, five-, six-, or seven-times step-up is used:
the total current consumption = internal logic current + LCD power current x 2 (two-times step-up),
the total current consumption = internal logic current + LCD power current x 5 (five-times step-up),
the total current consumption = internal logic current + LCD power current x 6 (six-times step-up), and
the total current consumption = internal logic current + LCD power current x 7 (seven-times step-up)

Type Name

Types	External Dimensions	COM Driver Arrangement	Display
HCD66752BP	Au-bump chip	One side of COM (Output from one side of the chip)	Four monochrome grayscale

HD66752

LCD Family Comparison

Items	HD66705U	HD66717	HD66727
Character display sizes	12 characters x 2 lines	12 characters x 4 lines	12 characters x 4 lines
Graphic display sizes	—	—	—
Grayscale display	—	—	—
Multiplexing icons	40	40	40
Annunciator	Static: 10	Static: 10	Static: 12
Key scan control	—	—	4 x 8
LED control ports	—	—	3
General output ports	—	—	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 9 V	3 V to 13 V	3 V to 13 V
Serial bus	Clock-synchronized serial	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	—
Liquid crystal drive duty ratios	1/10, 18	1/10, 18, 26, 34	1/10, 18, 26, 34
Liquid crystal drive biases	1/4	1/4, 1/6	1/4, 1/6
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage step-up	Two- or three-times	Two- or three-times	Two- or three-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (16 steps)	Incorporated (16 steps)	Incorporated (16 steps)
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	60 x 8
CGROM	9,600	9,600	11,520
CGRAM	32 x 5	32 x 5	32 x 6
SEGRAM	8 x 5	8 x 5	8 x 6
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	4	4	4
Font sizes	5 x 8	5 x 8	5 x 8, 6 x 8
Bit map area	—	—	—
R-C oscillation resistor/ oscillation frequency	External resistor (40, 80 kHz)	External resistor (40-160 kHz)	External resistor (40-160 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG only	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-153	TCP-153	TCP-158
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	153	153	158
Chip sizes	9.69 x 2.73	10.88 x 2.89	11.39 x 2.89
Pad intervals	120 μm	120 μm	120 μm

LCD Family Comparison (cont)

Items	HD66724	HD66725	HD66726
Character display sizes	12 characters x 3 lines	16 characters x 3 lines	16 characters x 5 lines
Graphic display sizes	72 x 26 dots	96 x 26 dots	96 x 42 dots
Grayscale display	—	—	—
Multiplexing icons	144	192	192
Annunciator	1/2 duty: 144	1/2 duty: 192	1/2 duty: 192
Key scan control	8 x 4	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6.5 V	3 V to 6.5 V	4.5 V to 11 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42
Liquid crystal drive biases	1/4 to 1/6.5	1/4 to 1/6.5	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage step-up	Single, two-, or three-times	Single, two-, or three-times	Single, two-, three-, or four-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (32 steps)	Incorporated (32 steps)	Incorporated (32 steps)
Horizontal smooth scroll	3-dot unit	3-dot unit	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	20,736
CGRAM	384 x 8	384 x 8	480 x 8
SEGRAM	72 x 8	96 x 8	96 x 8
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
Bit map areas	72 x 26	96 x 26	96 x 42
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor (50 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-146	TCP-170	TCP-188
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	146	170	188
Chip sizes	10.34 x 2.51	10.97 x 2.51	13.13 x 2.51
Pad intervals	80 μm	80 μm	100 μm

HD66752

LCD Family Comparison (cont)

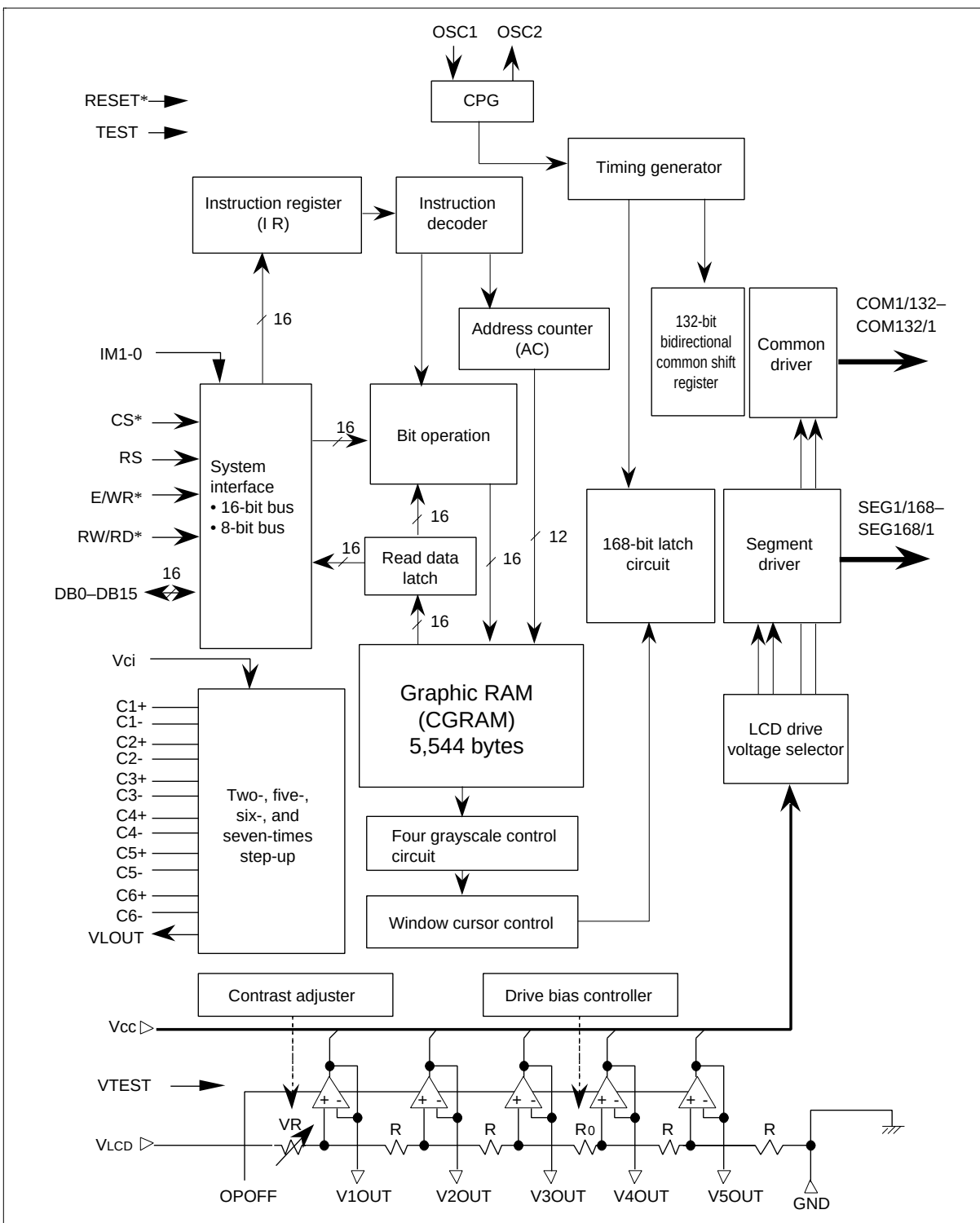
Items	HD66728	HD66729	HD66741
Character display sizes	16 characters x 10 lines	—	—
Graphic display sizes	112 x 80 dots	105 x 68 dots	128 x 80 dots
Grayscale display	—	—	—
Multiplexing icons	—	—	—
Annunciator	—	—	—
Key scan control	8 x 4	—	—
LED control ports	—	—	—
General output ports	3	—	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	4.5 V to 15 V	4.0 V to 13 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80	1/8, 16, 24, 32, 40, 48, 56, 64, 68	1/8, 16, 24, 32, 40, 48, 56, 64, 72, 80
Liquid crystal drive biases	1/4 to 1/10	1/4 to 1/9	1/4 to 1/10
Liquid crystal drive waveforms	B, C	B, C	B, C
Liquid crystal voltage step-up	Three-, four-, or five-times	Two-, three-, four-, or five-times	Three-, four-, or five-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (64 steps)	Incorporated (64 steps)	Incorporated (64 steps)
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	160 x 8	—	—
CGROM	20,736	—	—
CGRAM	1,120 x 8	1,050 x 8	1,280 x 8
SEGRAM	—	—	—
No. of CGROM fonts	240 + 192	—	—
No. of CGRAM fonts	64	—	—
Font sizes	6 x 8	—	—
Bit map areas	112 x 80	105 x 68	128 x 80
R-C oscillation resistor/oscillation frequency	External resistor (70–90 kHz)	External resistor (75 kHz)	External resistor (70–90 kHz)
Reset function	External	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off, Key wake-up interrupt	Partial display off, Oscillation off, Liquid crystal power off	Partial display off, Oscillation off, Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-243	TCP-213	TCP-254
Bare chip	—	—	—
Bumped chip	Yes	Yes	Yes
No. of pins	243	213	243
Chip sizes	13.67 x 2.78	12.23 x 2.52	14.30 x 2.78
Pad intervals	70 µm	70 µm	70 µm

LCD Family Comparison (cont)

Items	HD66750/751	HD66752
Character display sizes	—	—
Graphic display sizes	128 x 128 dots	168 x 132 dots
Grayscale display	Four monochrome grayscales (5 levels)	Four monochrome grayscales (7 levels)
Multiplexing icons	—	—
Annunciator	—	—
Key scan control	—	—
LED control ports	—	—
General output ports	—	—
Operating power voltages	2.0 V to 3.6 V	2.0 V to 3.6 V
Liquid crystal drive voltages	5.0 V to 15.5V	5.0 V to 15.5V
Serial bus	—	—
Parallel bus	8 bits, 16 bits	8 bits, 16 bits
Liquid crystal drive duty ratios	1/16, 24, 72, 80, 88, 96, 104, 112, 120, 128	1/80, 88, 96, 104, 112, 120, 128, 132
Liquid crystal drive biases	1/4 to 1/11	1/4 to 1/11
Liquid crystal drive waveforms	B, C	B, C
Liquid crystal voltage step-up	Two-, five-, six-, or seven-times	Two-, five-, six-, or seven-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated (64 steps)	Incorporated (128 steps)
Horizontal smooth scroll	—	—
Vertical smooth scroll	Line unit	—
Double-height display	Yes	—
DDRAM	—	—
CGROM	—	—
CGRAM	4,096 x 8	5,544 x 8
SEGRAM	—	—
No. of CGROM fonts	—	—
No. of CGRAM fonts	—	—
Font sizes	—	—
Bit map areas	128 x 128	168 x 132, 132 x 168
R-C oscillation resistor/oscillation frequency	External resistor (70 kHz)	External resistor (100 kHz)
Reset function	External	External
Low power control	Partial display off, Oscillation off, Liquid crystal power off	2-screen division partial drive, Partial display off, Oscillation off, Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM
QFP package	—	—
TQFP package	—	—
TCP package	TCP-300 (HD66750)	—
Bare chip	—	—
Bumped chip	Yes	Yes
No. of pins	300	344
Chip sizes	10.97 x 4.13	12.68x 4.31
Pad intervals	60 μ m	60 μ m

HD66752

HD66752 Block Diagram





HD66752

HD66752 Pad Coordinates

Unit (μm)

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	DUMMY1	-6170	-1985	46	C5+	-2647	-1985	91	DB1	817	-1985	136	DUMMY9	4607	-1985
2	DUMMY2	-5990	-1985	47	C5+	-2586	-1985	92	DB1	877	-1985	137	DUMMY10	4667	-1985
3	DUMMY3	-5929	-1985	48	C6-	-2466	-1985	93	DB2	1001	-1985	138	DUMMY11	4727	-1985
4	DUMMY4	-5869	-1985	49	C6-	-2406	-1985	94	DB2	1061	-1985	139	DUMMY12	4787	-1985
5	VTEST	-5773	-1985	50	C6-	-2346	-1985	95	DB3	1185	-1985	140	DUMMY13	4847	-1985
6	V5OUT	-5713	-1985	51	C6+	-2226	-1985	96	DB3	1245	-1985	141	DUMMY14	4907	-1985
7	V4OUT	-5653	-1985	52	C6+	-2166	-1985	97	DB4	1369	-1985	142	DUMMY15	4967	-1985
8	V3OUT	-5592	-1985	53	C6+	-2105	-1985	98	DB4	1429	-1985	143	DUMMY16	5028	-1985
9	V2OUT	-5532	-1985	54	VCI	-1985	-1985	99	DB5	1553	-1985	144	DUMMY17	5088	-1985
10	V1OUT	-5472	-1985	55	VCI	-1925	-1985	100	DB5	1613	-1985	145	DUMMY18	5148	-1985
11	VLCD	-5366	-1985	56	VCI	-1865	-1985	101	DB6	1737	-1985	146	DUMMY19	5208	-1985
12	VLCD	-5306	-1985	57	VCI	-1805	-1985	102	DB6	1797	-1985	147	DUMMY20	5268	-1985
13	VLCD	-5245	-1985	58	Vcc	-1685	-1985	103	DB7	1921	-1985	148	DUMMY21	5328	-1985
14	VLCD	-5185	-1985	59	Vcc	-1625	-1985	104	DB7	1981	-1985	149	DUMMY22	5388	-1985
15	VLOUT	-5088	-1985	60	Vcc	-1564	-1985	105	DB8	2105	-1985	150	DUMMY23	5448	-1985
16	VLOUT	-5028	-1985	61	Vcc	-1504	-1985	106	DB8	2165	-1985	151	DUMMY24	5509	-1985
17	GNDDUM4	-4931	-1985	62	Vcc	-1444	-1985	107	DB9	2289	-1985	152	DUMMY25	5569	-1985
18	C1-	-4871	-1985	63	Vcc	-1384	-1985	108	DB9	2349	-1985	153	DUMMY26	5629	-1985
19	C1-	-4811	-1985	64	Vcc	-1324	-1985	109	DB10	2473	-1985	154	DUMMY27	5689	-1985
20	C1-	-4751	-1985	65	OSC1	-1151	-1985	110	DB10	2533	-1985	155	DUMMY28	5749	-1985
21	C1+	-4631	-1985	66	OSC1	-1091	-1985	111	DB11	2657	-1985	156	DUMMY29	5809	-1985
22	C1+	-4570	-1985	67	OSC2	-968	-1985	112	DB11	2717	-1985	157	DUMMY30	5869	-1985
23	C1+	-4510	-1985	68	OSC2	-907	-1985	113	DB12	2841	-1985	158	DUMMY31	5929	-1985
24	C2-	-4390	-1985	69	GND	-838	-1985	114	DB12	2901	-1985	159	DUMMY32	5990	-1985
25	C2-	-4330	-1985	70	GND	-777	-1985	115	DB13	3025	-1985	160	DUMMY33	6170	-1985
26	C2-	-4270	-1985	71	GND	-717	-1985	116	DB13	3085	-1985	161	SEG168/1	6170	-1804
27	C2+	-4150	-1985	72	GND	-657	-1985	117	DB14	3209	-1985	162	SEG167/2	6170	-1743
28	C2+	-4089	-1985	73	GND	-597	-1985	118	DB14	3269	-1985	163	SEG166/3	6170	-1683
29	C2+	-4029	-1985	74	GND	-537	-1985	119	DB15	3392	-1985	164	SEG165/4	6170	-1623
30	C3-	-3909	-1985	75	GND	-477	-1985	120	DB15	3453	-1985	165	SEG164/5	6170	-1563
31	C3-	-3849	-1985	76	GND	-417	-1985	121	GNDDUM2	3516	-1985	166	SEG163/6	6170	-1503
32	C3-	-3789	-1985	77	GND	-357	-1985	122	TEST	3576	-1985	167	SEG162/7	6170	-1443
33	C3+	-3669	-1985	78	RW/RD*	-287	-1985	123	TEST	3637	-1985	168	SEG161/8	6170	-1383
34	C3+	-3608	-1985	79	RW/RD*	-227	-1985	124	OPOFF	3760	-1985	169	SEG160/9	6170	-1323
35	C3+	-3548	-1985	80	E/WR*	-103	-1985	125	OPOFF	3821	-1985	170	SEG159/10	6170	-1263
36	C4-	-3428	-1985	81	E/WR*	-43	-1985	126	VCCDUM1	3881	-1985	171	SEG158/11	6170	-1202
37	C4-	-3368	-1985	82	RS	81	-1985	127	IM0	3944	-1985	172	SEG157/12	6170	-1142
38	C4-	-3308	-1985	83	RS	141	-1985	128	IM0	4004	-1985	173	SEG156/13	6170	-1082
39	C4+	-3188	-1985	84	CS*	265	-1985	129	IM1	4128	-1985	174	SEG155/14	6170	-1022
40	C4+	-3128	-1985	85	CS*	325	-1985	130	IM1	4188	-1985	175	SEG154/15	6170	-962
41	C4+	-3067	-1985	86	RESET*	449	-1985	131	GNDDUM1	4249	-1985	176	SEG153/16	6170	-902
42	C5-	-2947	-1985	87	RESET*	509	-1985	132	DUMMY5	4366	-1985	177	SEG152/17	6170	-842
43	C5-	-2887	-1985	88	GNDDUM3	569	-1985	133	DUMMY6	4426	-1985	178	SEG151/18	6170	-782
44	C5-	-2827	-1985	89	DB0	633	-1985	134	DUMMY7	4487	-1985	179	SEG150/19	6170	-721
45	C5+	-2707	-1985	90	DB0	693	-1985	135	DUMMY8	4547	-1985	180	SEG149/20	6170	-661

HD66752

Unit (μm)

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
181	SEG148/21	6170	-601	226	DUMMY43	5749	1985	271	SEG68/101	2976	1985	316	SEG23/146	271	1985
182	SEG147/22	6170	-541	227	SEG112/57	5621	1985	272	SEG67/102	2916	1985	317	SEG22/147	210	1985
183	SEG146/23	6170	-481	228	SEG111/58	5561	1985	273	SEG66/103	2856	1985	318	SEG21/148	150	1985
184	SEG145/24	6170	-421	229	SEG110/59	5501	1985	274	SEG65/104	2796	1985	319	SEG20/149	90	1985
185	SEG144/25	6170	-361	230	SEG109/60	5441	1985	275	SEG64/105	2735	1985	320	SEG19/150	30	1985
186	SEG143/26	6170	-301	231	SEG108/61	5381	1985	276	SEG63/106	2675	1985	321	SEG18/151	-30	1985
187	SEG142/27	6170	-240	232	SEG107/62	5321	1985	277	SEG62/107	2615	1985	322	SEG17/152	-90	1985
188	SEG141/28	6170	-180	233	SEG106/63	5261	1985	278	SEG61/108	2555	1985	323	SEG16/153	-150	1985
189	SEG140/29	6170	-120	234	SEG105/64	5200	1985	279	SEG60/109	2495	1985	324	SEG15/154	-210	1985
190	SEG139/30	6170	-60	235	SEG104/65	5140	1985	280	SEG59/110	2435	1985	325	SEG14/155	-271	1985
191	SEG138/31	6170	0	236	SEG103/66	5080	1985	281	SEG58/111	2375	1985	326	SEG13/156	-331	1985
192	SEG137/32	6170	60	237	SEG102/67	5020	1985	282	SEG57/112	2315	1985	327	SEG12/157	-391	1985
193	SEG136/33	6170	120	238	SEG101/68	4960	1985	283	SEG56/113	2255	1985	328	SEG11/158	-451	1985
194	SEG135/34	6170	180	239	SEG100/69	4900	1985	284	SEG55/114	2194	1985	329	SEG10/159	-511	1985
195	SEG134/35	6170	240	240	SEG99/70	4840	1985	285	SEG54/115	2134	1985	330	SEG9/160	-571	1985
196	SEG133/36	6170	301	241	SEG98/71	4780	1985	286	SEG53/116	2074	1985	331	SEG8/161	-631	1985
197	SEG132/37	6170	361	242	SEG97/72	4719	1985	287	SEG52/117	2014	1985	332	SEG7/162	-691	1985
198	SEG131/38	6170	421	243	SEG96/73	4659	1985	288	SEG51/118	1954	1985	333	SEG6/163	-752	1985
199	SEG130/39	6170	481	244	SEG95/74	4599	1985	289	SEG50/119	1894	1985	334	SEG5/164	-812	1985
200	SEG129/40	6170	541	245	SEG94/75	4539	1985	290	SEG49/120	1834	1985	335	SEG4/165	-872	1985
201	SEG128/41	6170	601	246	SEG93/76	4479	1985	291	SEG48/121	1774	1985	336	SEG3/166	-932	1985
202	SEG127/42	6170	661	247	SEG92/77	4419	1985	292	SEG47/122	1713	1985	337	SEG2/167	-992	1985
203	SEG126/43	6170	721	248	SEG91/78	4359	1985	293	SEG46/123	1653	1985	338	SEG1/168	-1052	1985
204	SEG125/44	6170	782	249	SEG90/79	4299	1985	294	SEG45/124	1593	1985	339	COM132/1	-1112	1985
205	SEG124/45	6170	842	250	SEG89/80	4238	1985	295	SEG44/125	1533	1985	340	COM131/2	-1172	1985
206	SEG123/46	6170	902	251	SEG88/81	4178	1985	296	SEG43/126	1473	1985	341	COM130/3	-1232	1985
207	SEG122/47	6170	962	252	SEG87/82	4118	1985	297	SEG42/127	1413	1985	342	COM129/4	-1293	1985
208	SEG121/48	6170	1022	253	SEG86/83	4058	1985	298	SEG41/128	1353	1985	343	COM128/5	-1353	1985
209	SEG120/49	6170	1082	254	SEG85/84	3998	1985	299	SEG40/129	1293	1985	344	COM127/6	-1413	1985
210	SEG119/50	6170	1142	255	SEG84/85	3938	1985	300	SEG39/130	1232	1985	345	COM126/7	-1473	1985
211	SEG118/51	6170	1202	256	SEG83/86	3878	1985	301	SEG38/131	1172	1985	346	COM125/8	-1533	1985
212	SEG117/52	6170	1263	257	SEG82/87	3818	1985	302	SEG37/132	1112	1985	347	COM124/9	-1593	1985
213	SEG116/53	6170	1323	258	SEG81/88	3758	1985	303	SEG36/133	1052	1985	348	COM123/10	-1653	1985
214	SEG115/54	6170	1383	259	SEG80/89	3697	1985	304	SEG35/134	992	1985	349	COM122/11	-1713	1985
215	SEG114/55	6170	1443	260	SEG79/90	3637	1985	305	SEG34/135	932	1985	350	COM121/12	-1774	1985
216	SEG113/56	6170	1503	261	SEG78/91	3577	1985	306	SEG33/136	872	1985	351	COM120/13	-1834	1985
217	DUMMY34	6170	1623	262	SEG77/92	3517	1985	307	SEG32/137	812	1985	352	COM119/14	-1894	1985
218	DUMMY35	6170	1683	263	SEG76/93	3457	1985	308	SEG31/138	752	1985	353	COM118/15	-1954	1985
219	DUMMY36	6170	1743	264	SEG75/94	3397	1985	309	SEG30/139	691	1985	354	COM117/16	-2014	1985
220	DUMMY37	6170	1804	265	SEG74/95	3337	1985	310	SEG29/140	631	1985	355	COM116/17	-2074	1985
221	DUMMY38	6170	1985	266	SEG73/96	3277	1985	311	SEG28/141	571	1985	356	COM115/18	-2134	1985
222	DUMMY39	5990	1985	267	SEG72/97	3216	1985	312	SEG27/142	511	1985	357	COM114/19	-2194	1985
223	DUMMY40	5929	1985	268	SEG71/98	3156	1985	313	SEG26/143	451	1985	358	COM113/20	-2255	1985
224	DUMMY41	5869	1985	269	SEG70/99	3096	1985	314	SEG25/144	391	1985	359	COM112/21	-2315	1985
225	DUMMY42	5809	1985	270	SEG69/100	3036	1985	315	SEG24/145	331	1985	360	COM111/22	-2375	1985

HD66752

Unit (μm)

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
361	COM110/23	-2435	1985	391	COM80/53	-4238	1985	421	DUMMY50	-6170	1804	451	COM30/103	-6170	-60
362	COM109/24	-2495	1985	392	COM79/54	-4299	1985	422	DUMMY51	-6170	1743	452	COM29/104	-6170	-120
363	COM108/25	-2555	1985	393	COM78/55	-4359	1985	423	DUMMY52	-6170	1683	453	COM28/105	-6170	-180
364	COM107/26	-2615	1985	394	COM77/56	-4419	1985	424	DUMMY53	-6170	1623	454	COM27/106	-6170	-240
365	COM106/27	-2675	1985	395	COM76/57	-4479	1985	425	COM56/77	-6170	1503	455	COM26/107	-6170	-301
366	COM105/28	-2735	1985	396	COM75/58	-4539	1985	426	COM55/78	-6170	1443	456	COM25/108	-6170	-361
367	COM104/29	-2796	1985	397	COM74/59	-4599	1985	427	COM54/79	-6170	1383	457	COM24/109	-6170	-421
368	COM103/30	-2856	1985	398	COM73/60	-4659	1985	428	COM53/80	-6170	1323	458	COM23/110	-6170	-481
369	COM102/31	-2916	1985	399	COM72/61	-4719	1985	429	COM52/81	-6170	1263	459	COM22/111	-6170	-541
370	COM101/32	-2976	1985	400	COM71/62	-4780	1985	430	COM51/82	-6170	1202	460	COM21/112	-6170	-601
371	COM100/33	-3036	1985	401	COM70/63	-4840	1985	431	COM50/83	-6170	1142	461	COM20/113	-6170	-661
372	COM99/34	-3096	1985	402	COM69/64	-4900	1985	432	COM49/84	-6170	1082	462	COM19/114	-6170	-721
373	COM98/35	-3156	1985	403	COM68/65	-4960	1985	433	COM48/85	-6170	1022	463	COM18/115	-6170	-782
374	COM97/36	-3216	1985	404	COM67/66	-5020	1985	434	COM47/86	-6170	962	464	COM17/116	-6170	-842
375	COM96/37	-3277	1985	405	COM66/67	-5080	1985	435	COM46/87	-6170	902	465	COM16/117	-6170	-902
376	COM95/38	-3337	1985	406	COM65/68	-5140	1985	436	COM45/88	-6170	842	466	COM15/118	-6170	-962
377	COM94/39	-3397	1985	407	COM64/69	-5200	1985	437	COM44/89	-6170	782	467	COM14/119	-6170	-1022
378	COM93/40	-3457	1985	408	COM63/70	-5261	1985	438	COM43/90	-6170	721	468	COM13/120	-6170	-1082
379	COM92/41	-3517	1985	409	COM62/71	-5321	1985	439	COM42/91	-6170	661	469	COM12/121	-6170	-1142
380	COM91/42	-3577	1985	410	COM61/72	-5381	1985	440	COM41/92	-6170	601	470	COM11/122	-6170	-1202
381	COM90/43	-3637	1985	411	COM60/73	-5441	1985	441	COM40/93	-6170	541	471	COM10/123	-6170	-1263
382	COM89/44	-3697	1985	412	COM59/74	-5501	1985	442	COM39/94	-6170	481	472	COM9/124	-6170	-1323
383	COM88/45	-3758	1985	413	COM58/75	-5561	1985	443	COM38/95	-6170	421	473	COM8/125	-6170	-1383
384	COM87/46	-3818	1985	414	COM57/76	-5621	1985	444	COM37/96	-6170	361	474	COM7/126	-6170	-1443
385	COM86/47	-3878	1985	415	DUMMY44	-5749	1985	445	COM36/97	-6170	301	475	COM6/127	-6170	-1503
386	COM85/48	-3938	1985	416	DUMMY45	-5809	1985	446	COM35/98	-6170	240	476	COM5/128	-6170	-1563
387	COM84/49	-3998	1985	417	DUMMY46	-5869	1985	447	COM34/99	-6170	180	477	COM4/129	-6170	-1623
388	COM83/50	-4058	1985	418	DUMMY47	-5929	1985	448	COM33/100	-6170	120	478	COM3/130	-6170	-1683
389	COM82/51	-4118	1985	419	DUMMY48	-5990	1985	449	COM32/101	-6170	60	479	COM2/131	-6170	-1743
390	COM81/52	-4178	1985	420	DUMMY49	-6170	1985	450	COM31/102	-6170	0	480	COM1/132	-6170	-1804

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HD66752

Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions		
IM1, IM0	2	I	GND or V _{cc}	Selects the MPU interface mode:		
				IM1	IM0	MPU interface mode
				GND	GND	68-system 16-bit bus interface
				GND	V _{cc}	68-system 8-bit bus interface
				V _{cc}	GND	80-system 16-bit bus interface
				V _{cc}	V _{cc}	80-system 8-bit bus interface
CS*	1	I	MPU	Selects the HD66752: Low: HD66752 is selected and can be accessed High: HD66752 is not selected and cannot be accessed Must be fixed at GND level when not in use.		
RS	1	I	MPU	Selects the register. Low: Index/status High: Control		
E/WR*	1	I	MPU	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.		
RW/RD*	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.		
DB0–DB15	16	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the V _{cc} or GND level.		
COM1/132–COM132/1	132	O	LCD	Output signals for common drive: All the unused pins output unselected waveforms. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/132 is COM1, and COM132/1 is COM132. If CMS = 1, COM1/132 is COM132, and COM132/1 is COM1.		
SEG1/168–SEG168/1	168	O	LCD	Output signals for segment drive. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/168 is SEG1. If SGS = 1, SEG1/168 is SEG168.		

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
V1OUT–V5 OUT	5	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	1	—	Power supply	Power supply for LCD drive. $V_{LCD} - GND = 15.5\text{ V max.}$
V_{CC} , GND	2	—	Power supply	V_{CC} : +2.0 V to + 3.6 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, input clock pulses to OSC1.
Vci	1	I	Power supply	Inputs a reference voltage and supplies power to the step-up circuit; generates the liquid crystal display drive voltage from the operating voltage. The step-up output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the step-up circuit is not used.
VLOUT	1	O	V_{LCD} pin/step-up capacitance	Potential difference between Vci and GND is two- to seven-times-stepped up and then output. Magnitude of step-up is selected by instruction.
C1+, C1–	2	—	Step-up capacitance	External capacitance should be connected here for five-times step-up.
C2+, C2–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C3+, C3–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C4+, C4–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C5+, C5–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
C6+, C6–	2	—	Step-up capacitance	External capacitance should be connected here when using the five-times or more step-up.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC} , and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	2	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.

HD66752

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
GNDDUM	4	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	4	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST	1	—	—	Test pin. Must be left disconnected. When internal operational amplifier is used and Vcc is below 2.5 V condition, VTEST pin 1.2 to 1.3 needs to be supplied.

Block Function Description

System Interface

The HD66752 has four high-speed system interfaces: an 80-system 16-bit/8-bit bus and a 68-system 16-bit/8-bit bus. The interface mode is selected by the IM1-0 pins.

The HD66752 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the CGRAM. The WDR temporarily stores data to be written into control registers and the CGRAM, and the RDR temporarily stores data read from the CGRAM. Data written into the CGRAM from the MPU is first written into the WDR and then is automatically written into the CGRAM by internal operation. Data is read through the RDR when reading from the CGRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66752 by using the display data set in the CGRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection

80-series Bus		68-series Bus		Operations
WR Bits	RD Bits	R/W Bits	RS Bits	
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads status
0	1	0	1	Writes into control registers and CGRAM through WDR
1	0	1	1	Reads from CGRAM through RDR

Bit Operation

The HD66752 supports the following functions: a bit rotation function that writes the data written from the MPU into the CGRAM by moving the display position in bit units, a write data mask function that selects and writes data into the CGRAM in bit units, and a logic operation function that performs logic operations on the display data set in the CGRAM and writes into the CGRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the CGRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

HD66752

After writing into the CGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the RDM bit automatically updates or does not update the AC.

Graphic RAM (CGRAM)

The graphic RAM (CGRAM) stores bit-pattern data of 168 x 132 dots. It has two bits/pixel and 5544-byte capacity.

Grayscale Control Circuit

The grayscale control circuit performs four-grayscale control with the frame rate control (FRC) method for four-monochrome grayscale display. For details, see the Four Grayscale Display Function section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66752 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 132 common signal drivers (COM1 to COM132) and 168 segment signal drivers (SEG1 to SEG168). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is latched when 132-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 132-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Step-up Circuit (DC-DC Converter)

The step-up generates two-, five-, six-, or seven-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Step-up output level from three-

times to seven-times step-up can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/11 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 128 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

HD66752

CGRAM Address Map (HD66752)

Table 4 Relationship between Display Position and CGRAM Address

Common Driver		Segment Driver	SEG1/168	SEG2/167	SEG3/166	SEG4/165	SEG5/164	SEG6/163	SEG7/162	SEG8/161	SEG9/160	... SEG16/153	SEG17/152	... SEG24/145		SEG161/8	... SEG168/1															
CMS="1"	CMS="0"	Bit	SGS="0"	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	...	D15	D0	D1	...	D15		D0	D1	...	D15
			SGS="1"	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	...	D0	D15	D14	...	D0		D15	D14	...	D0
COM132/1	COM1/132	COM1	Address: "0000"H																		"0001"H	"0002"H		"0014"H								
COM131/2	COM2/131	COM2	Address: "0020"H																		"0021"H	"0022"H		"0034"H								
COM130/3	COM3/130	COM3	Address: "0040"H																		"0041"H	"0042"H		"0054"H								
COM129/4	COM4/129	COM4	Address: "0060"H																		"0061"H	"0062"H		"0074"H								
COM128/5	COM5/128	COM5	Address: "0080"H																		"0081"H	"0082"H		"0094"H								
COM127/6	COM6/127	COM6	Address: "00A0"H																		"00A1"H	"00A2"H		"00B4"H								
COM126/7	COM7/126	COM7	Address: "00C0"H																		"00C1"H	"00C2"H		"00D4"H								
COM125/8	COM8/125	COM8	Address: "00E0"H																		"00E1"H	"00E2"H		"00F4"H								
COM124/9	COM9/124	COM9	Address: "0100"H																		"0101"H	"0102"H		"0114"H								
COM123/10	COM10/123	COM10	Address: "0120"H																		"0121"H	"0122"H		"0134"H								
COM122/11	COM11/122	COM11	Address: "0140"H																		"0141"H	"0142"H		"0154"H								
COM121/12	COM12/121	COM12	Address: "0160"H																		"0161"H	"0162"H		"0174"H								
COM120/13	COM13/120	COM13	Address: "0180"H																		"0181"H	"0182"H		"0194"H								
COM119/14	COM14/119	COM14	Address: "01A0"H																		"01A1"H	"01A2"H		"01B4"H								
COM118/15	COM15/118	COM15	Address: "01C0"H																		"01C1"H	"01C2"H		"01D4"H								
COM117/16	COM16/117	COM16	Address: "01E0"H																		"01E1"H	"01E2"H		"01F4"H								
COM116/17	COM17/116	COM17	Address: "0200"H																		"0201"H	"0202"H		"0214"H								
COM115/18	COM18/115	COM18	Address: "0220"H																		"0221"H	"0222"H		"0234"H								
COM114/19	COM19/114	COM19	Address: "0240"H																		"0241"H	"0242"H		"0254"H								
COM113/20	COM20/113	COM20	Address: "0260"H																		"0261"H	"0262"H		"0274"H								
⋮	⋮	⋮	⋮																		⋮	⋮		⋮								
COM8/125	COM125/8	COM125	Address: "0F80"H																		"0F81"H	"0F82"H		"0F94"H								
COM7/126	COM126/7	COM126	Address: "0FA0"H																		"0FA1"H	"0FA2"H		"0FB4"H								
COM6/127	COM127/6	COM127	Address: "0FC0"H																		"0FC1"H	"0FC2"H		"0FD4"H								
COM5/128	COM128/5	COM128	Address: "0FE0"H																		"0FE1"H	"0FE2"H		"0FF4"H								
COM4/129	COM129/4	COM129	Address: "1000"H																		"1001"H	"1002"H		"1014"H								
COM3/130	COM130/3	COM130	Address: "1020"H																		"1021"H	"1022"H		"1034"H								
COM2/131	COM131/2	COM131	Address: "1040"H																		"1041"H	"1042"H		"1054"H								
COM1/132	COM132/1	COM132	Address: "1060"H																		"1061"H	"1062"H		"1074"H								

Table 5 Relationship between CGRAM Data and Display Contents

User Bit	Lower Bit	LCD
0	0	Non-selection display (unlit)
0	1	1/4-, 1/3- or 2/4-level grayscale display (selected by the GSL1-0 bits)
1	0	2/4-, 2/3-, or 3/4-level grayscale display (selected by the GSH1-0 bits)
1	1	Selection display (lit)

Note: Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, DB1

Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, DB0

HD66752

Instructions

Outline

The HD66752 uses the 16-bit bus architecture. Before the internal operation of the HD66752 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66752 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB7), make up the HD66752 instructions. There are seven categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal CGRAM addresses
- Transfer data to and from the internal CGRAM

Normally, instructions that write data are used the most. However, an auto-update of internal CGRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00 to R12). It sets the register number in the range of 00000 to 10010 in binary form.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	*	*	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66752.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, 0752H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0

Figure 3 Start Oscillation Instruction

HD66752

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/132 shifts to COM1, and COM132/1 to COM132. When CMS = 1, COM1/132 shifts to COM132, and COM132/1 to COM1.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/168 shifts to SEG1, and SEG168/1 to SEG168. When SGS = 1, SEG1/168 shifts to SEG168, and SEG168/1 to SEG1.

NL4-0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. CGRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	CMS	SGS	*	*	*	NL4	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

Table 6 NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	0	168 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	0	1	168 x 16 dots	1/16 Duty	COM1–COM16
0	0	0	1	0	168 x 24 dots	1/24 Duty	COM1–COM24
0	0	0	1	1	168 x 32 dots	1/32 Duty	COM1–COM32
0	0	1	0	0	168 x 40 dots	1/40 Duty	COM1–COM40
0	0	1	0	1	168 x 48 dots	1/48 Duty	COM1–COM48
0	0	1	1	0	168 x 56 dots	1/56 Duty	COM1–COM56
0	0	1	1	1	168 x 64 dots	1/64 Duty	COM1–COM64
0	1	0	0	0	168 x 72 dots	1/72 Duty	COM1–COM72
0	1	0	0	1	168 x 80 dots	1/80 Duty	COM1–COM80
0	1	0	1	0	168 x 88 dots	1/88 Duty	COM1–COM88
0	1	0	1	1	168 x 96 dots	1/96 Duty	COM1–COM96
0	1	1	0	0	168 x 104 dots	1/104 Duty	COM1–COM104
0	1	1	0	1	168 x 112 dots	1/112 Duty	COM1–COM112
0	1	1	1	0	168 x 120 dots	1/120 Duty	COM1–COM120
0	1	1	1	1	168 x 128 dots	1/128 Duty	COM1–COM128
1	0	0	0	0	168 x 132 dots	1/132 Duty	COM1–COM132

LCD-Driving-Waveform Control

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORED for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	B/C	EOR	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

Power Control

BS2–0: The LCD drive bias value is set within the range of a 1/4 to 1/11 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

BT1–0: The output factor of V5OUT between two-times, three-times, four-times, five-times, six-times, and seven-times step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

DC1–0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1–0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

HD66752

Table 7 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	1/11 bias drive
0	0	1	1/10 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Table 8 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Two-times step-up
0	1	Five-times step-up
1	0	Six-times step-up
1	1	Seven-times step-up

Table 9 DC Bits and Operating Clock Frequency

DC1	DC0	Operating Clock Frequency in the Step-up Circuit
0	0	32-divided clock
0	1	16-divided clock
1	0	8-divided clock
1	1	4-divided clock

Table 10 AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

SLP: When SLP = 1, the HD66752 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66752 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

- a. Standby mode cancel (STB = 0)
- b. Start oscillation
- c. Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	BS2	BS1	BS0	BT1	BT0	*	*	DC1	DC0	AP1	AP0	SLP	STB

Figure 6 Power Control Instruction

Contrast Control

CT6–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 128-step contrast. For details, see the Contrast Adjuster section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 7 Contrast Control Instruction

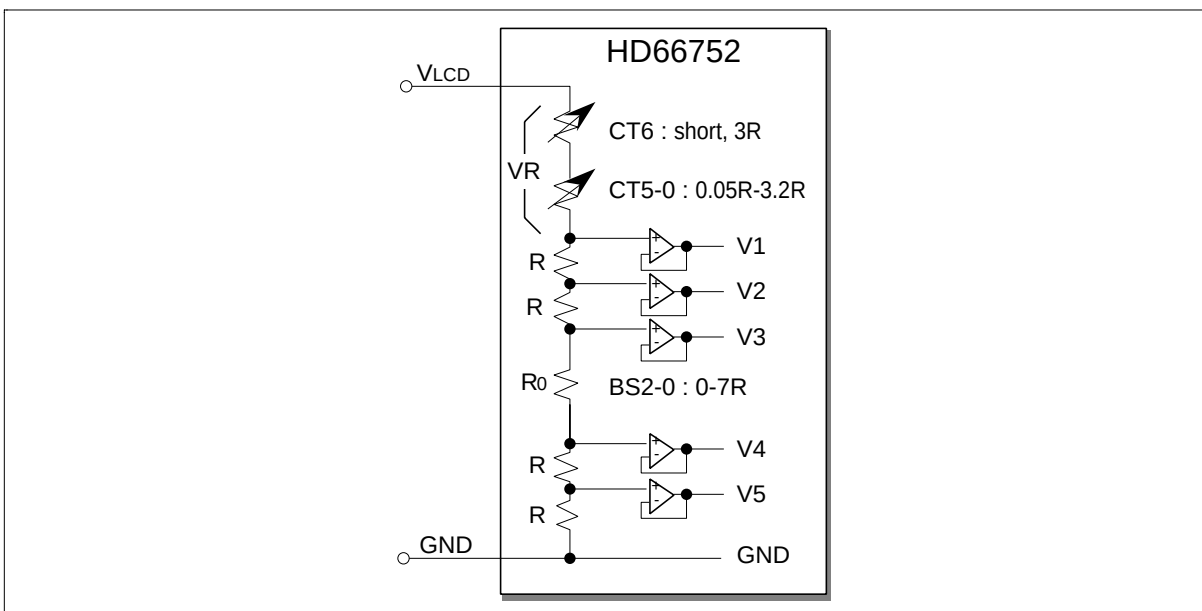


Figure 8 Contrast Adjuster

Table 12 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						Variable Resistor (VR)	
CT5	CT4	CT3	CT2	CT1	CT0	CT6 = 0	CT6 = 1
0	0	0	0	0	0	6.20 x R	3.20 x R
0	0	0	0	0	1	6.15 x R	3.15 x R
0	0	0	0	1	0	6.10 x R	3.10 x R
0	0	0	0	1	1	6.05 x R	3.05 x R
0	0	0	1	0	0	6.00 x R	3.00 x R
			.			.	.
			.			.	.
1	1	1	1	0	1	3.15 x R	0.15 x R
1	1	1	1	1	0	3.10 x R	0.10 x R
1	1	1	1	1	1	3.05 x R	0.05 x R

Entry Mode

Rotation

The write data sent from the microcomputer is modified in the HD66752 and written to the CGRAM. The display data in the CGRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the CGRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the CGRAM.

AM1–0: Set the automatic update method of the AC after the data is written to the CGRAM. When AM1–0 = 00, the data is continuously written in parallel. When AM1–0 = 01, the data is continuously written vertically. When AM1–0 = 10, the data is continuously written vertically with two-word width (32-bit length).

LG1–0: Write again the data read from the CGRAM and the data written from the microcomputer to the CGRAM by a logical operation. When LG1–0 = 00, replace (no logical operation) is done. ORed when LG1–0 = 01, ANDed when LG1–0 = 10, and EORed when LG1–0 = 11.

RT2–0: Write the data sent from the microcomputer to the CGRAM by rotating in a bit unit. RT3–0 specify rotation. For example, when RT2–0 = 001, the data is rotated in the upper side by two bits. When RT2–0 = 111, the data is rotated in the upper side by 14 bits. The upper bit overflown in the most significant bit (MSB) side is rotated in the least significant bit (LSB) side.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	I/D	AM1	AM0	LG1	LG0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	RT2	RT1	RT0

Figure 9 Entry Mode and Rotation Instructions

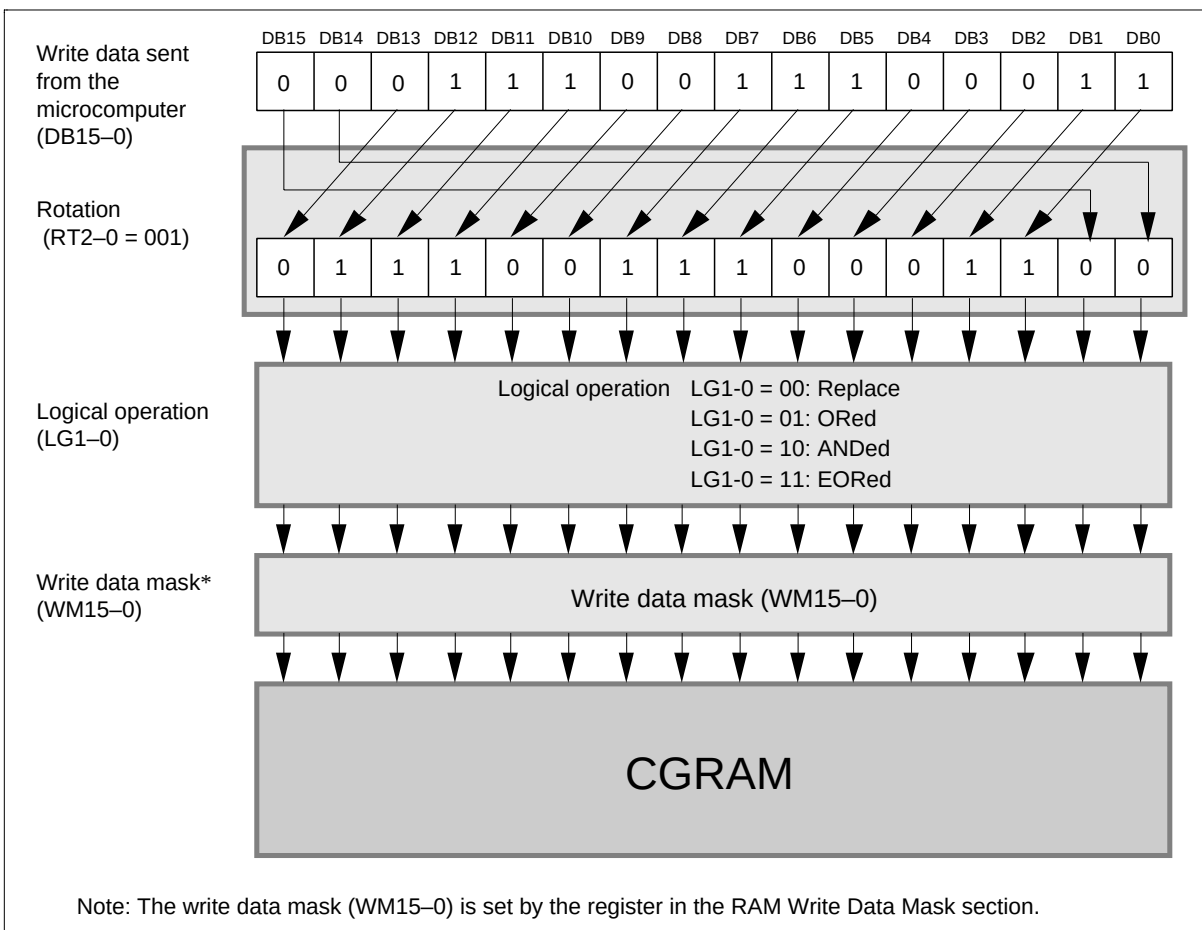


Figure 10 Logical Operation and Rotation for the CGRAM

Display Control

SPT: When SPT = 01, the 2-division LCD drive is performed. For details, see the Division Screen Drive section.

GSH1-0: When GS = 0, the grayscale level at a brightly-colored display (when DB = 10) is selected. For details, see the 4-Grayscale Display Function section.

GSL1-0: The grayscale level at a weakly-colored display (when DB = 01) is selected.

Table 12 GSH Bits and Output Level

GSH1	GSH0	Grayscale Output Level (DB = 10)
0	0	3/4 level grayscale control
0	1	2/3 level grayscale control
1	0	2/4 level grayscale control
1	1	Lit (No grayscale control)

Table 13 GSL Bits and Output Level

GSL1	GSL0	Grayscale Output Level (DB = 01)
0	0	1/4 level grayscale control
0	1	1/3 level grayscale control
1	0	2/4 level grayscale control
1	1	Lit (No grayscale control)

REV: Displays all character and graphics display sections with black-and-white reversal when REV = 1. For details, see the Reversed Display Function section.

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG168 outputs and COM1 to COM132 outputs set to the GND level. Because of this, the HD66752 can control the charging current for the LCD with AC driving.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	SPT	*	*	GS H1	GS H0	GS L1	GS L0	REV	D

Figure 11 Display Control Instruction

Cursor Control

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1–0 bits, and the display area is specified in a dot unit by the horizontal cursor position register (HS7–0 and HE7–0 bits) and vertical cursor position register (VS7–0 and VE7–0 bits). For details, see the Window Cursor Display section.

CM1–0: The display mode of the window cursor is selected. These bits can display a white-blink cursor, black-blink cursor, black-and-white reversed cursor, and black-and-white-reversed blink cursor.

HD66752

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	C	CM1	CM0

Figure 12 Cursor Control Instruction

Table 14 CM Bits and Window Cursor Display Mode

CM1	CM0	Window Cursor Display Mode
0	0	White-blink cursor (alternately blinking between the normal display and an all-white display (all unlit))
0	1	Black-blink cursor (alternately blinking between the normal display and an all-black display (all lit))
1	0	Black-and-white reversed cursor (black-and-white-reversed normal display (no blinking))
1	1	Black-and-white-reversed blink cursor (alternately blinking the black-and-white-reversed normal display)

Horizontal Cursor Position

Vertical Cursor Position

HS7-0: Specify the start position for horizontally displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that $HS7-0 \leq HE7-0$.

HE7-0: Specify the end position for horizontally displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that $HS7-0 \leq HE7-0$.

VS7-0: Specify the start position for vertically displaying the window cursor in a dot unit. The cursor is displayed from the 'set value + 1' dot. Ensure that $VS7-0 \leq VE7-0$.

VE7-0: Specify the end position for vertically displaying the window cursor in a dot unit. The cursor is displayed to the 'set value + 1' dot. Ensure that $VS7-0 \leq VE7-0$.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
W	1	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Figure 13 Horizontal Cursor Position and Vertical Cursor Position Instructions

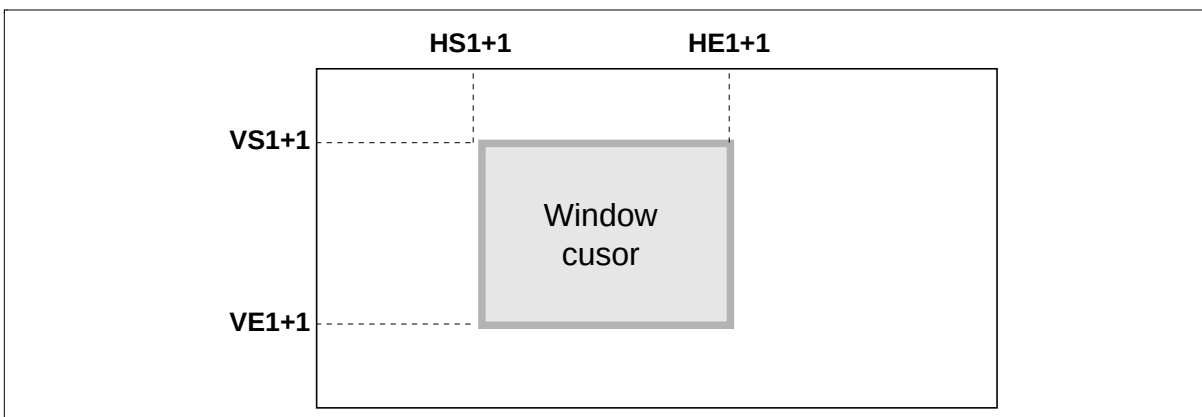


Figure 14 Window Cursor Position

1st Screen Driving Position**2nd Screen Driving Position**

SS17-0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE17-0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17-10 = 07H and SE17-10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that $SS17-10 \leq SE17-10 \leq 83H$. For details, see the Screen Division Driving Function section.

SS27-0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE27-0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS27-20 = 20H, and SE27-20 = 5FH are set, the LCD driving is performed from COM33 to COM96. Ensure that $SS17-10 \leq SE17-10 < SS27-20 \leq SE27-20 \leq 83H$. For details, see the Screen Division Driving Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 15 1st Screen Driving Position and 2nd Screen Driving Position

RAM Write Data Mask

WM15-0: In writing to the CGRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the CGRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. However, when AM = 10, the write data is masked with the set values of VM15–0 for the odd-times CGRAM write. It is also masked automatically with the reversed set values of VM15–0 for the even-times CGRAM write. For details, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VM15	VM14	VM13	VM12	VM11	VM10	VM9	VM8	VM7	VM6	VM5	VM4	VM3	VM2	VM1	VM0

Figure 16 RAM Write Data Mask Instruction

RAM Address Set

AD12-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the AM1-0 and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is not automatically updated. CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 17 RAM Address Set Instruction

Table 15 AD Bits and CGRAM Settings

AD12-AD0	CGRAM Setting
"0000"H-"0014"H	Bitmap data for COM1
"0020"H-"0034"H	Bitmap data for COM2
"0040"H-"0054"H	Bitmap data for COM3
"0060"H-"0074"H	Bitmap data for COM4
"0080"H-"0094"H	Bitmap data for COM5
"00A0"H-"00B4"H	Bitmap data for COM6
:	:
"0FC0"H-"0FD4"H	Bitmap data for COM127
"0FE0"H-"0FF4"H	Bitmap data for COM128
"1000"H-"1014"H	Bitmap data for COM129
"1020"H-"1034"H	Bitmap data for COM130
"1040"H-"1054"H	Bitmap data for COM131
"1060"H-"1074"H	Bitmap data for COM132

Write Data to CGRAM

WD15-0 : Write 16-bit data to the CGRAM. After a write, the address is automatically updated according to the AM1-0 and I/D bit settings. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 18 Write Data to CGRAM Instruction

Read Data from CGRAM

RD15-0 : Read 16-bit data from the CGRAM. When the data is read to the microcomputer, the first-word read immediately after the CGRAM address setting is latched from the CGRAM to the internal read-data latch. The data on the data bus (DB15-0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66752, only one read can be processed since the latched data in the first word is used.

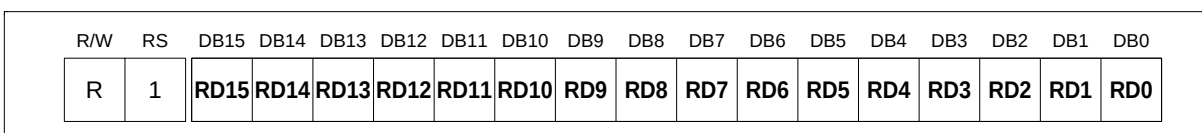


Figure 19 Read Data from CGRAM Instruction

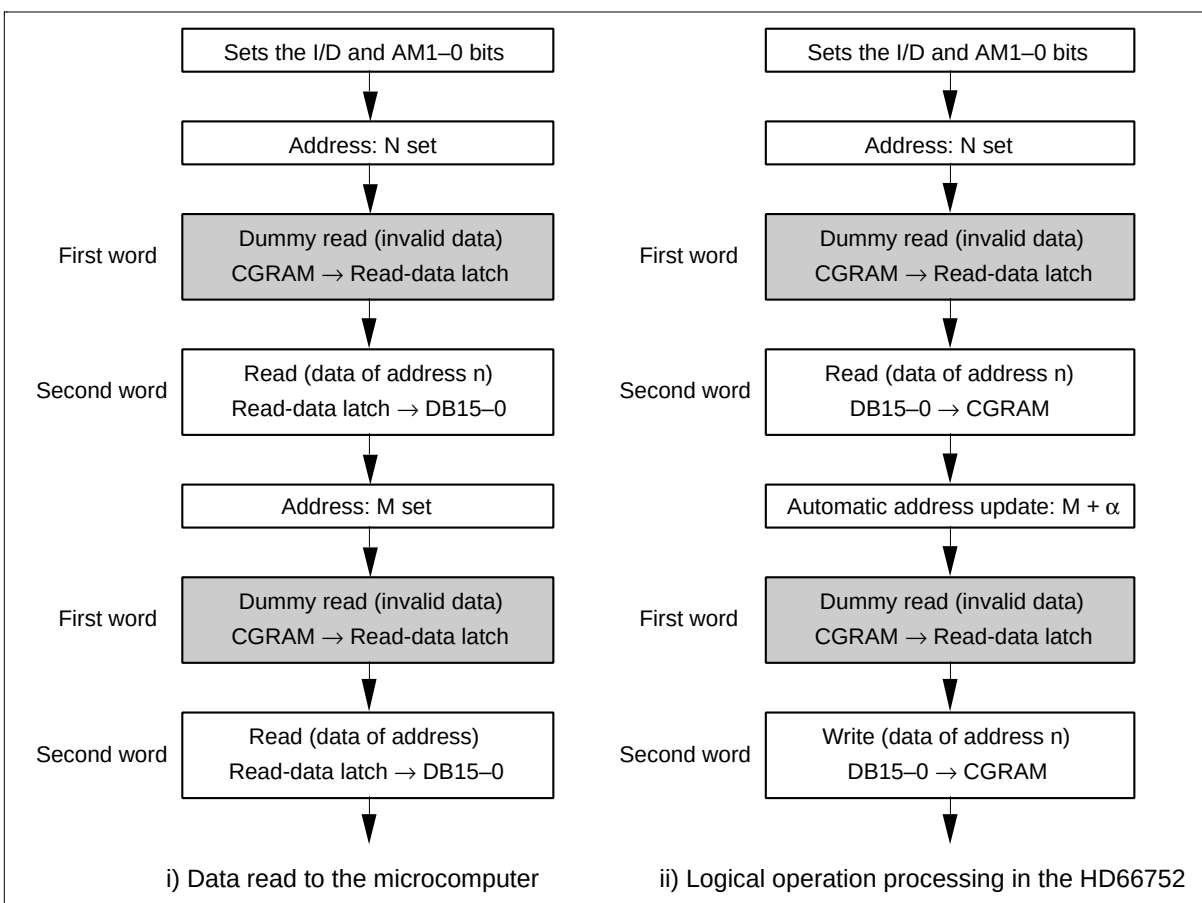


Figure 20 CGRAM Read Sequence

Table 16 Instruction List

				Upper Code								Lower Code														Execution Cycle
Reg. No.	Register Name	R/W	RS	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Description						
IR	Index	0	0	*	*	*	*	*	*	*	*	*	*	*	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0					
SR	Status read	1	0	0	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L6–0) and contrast setting (C6–0).	0					
R00	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms					
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0	Reads 0752H.	0					
R01	Driver output control	0	1	*	*	*	*	*	*	CMS	SGS	*	*	*	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS) and driving duty ratio (NL4–0).	0					
R02	LCD-driving-waveform control	0	1	*	*	*	*	*	*	*	*	*	B/C	EOR	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), and EOR output (EOR) or the number of n-raster-rows (NW4–0) at C-pattern AC drive.	0					
R03	Power control	0	1	*	*	*	BS2	BS1	BS0	BT1	BT0	*	*	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1–0), boosting cycle (DC1–0), boosting output multiplying factor (BT1–0), and LCD drive bias value (BS2–0).	0					
R04	Contrast control	0	1	*	*	*	*	*	*	*	*	*	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the contrast adjustment (CT6–0).	0					
R05	Entry mode	0	1	*	*	*	*	*	*	*	*	*	*	*	I/D	AM1	AM0	LG1	LG0	Specifies the logical operation (LG1–0), AC counter mode (AM1–0), and increment/decrement mode (I/D).	0					
R06	Rotation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	RT2	RT1	RT0	Specifies the amount of write-data rotation (RT2–0).	0					
R07	Display control	0	1	*	*	*	*	*	*	*	SPT	*	*	GSH 1	GSH 0	GSL 1	GSL 0	REV	D	Specifies display on (D), black-and-white reversed display (REV), grayscale mode (GSL1-0, GSH1-0) and screen division driving (SPT).	0					
R08	Cursor control	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	C	CM1	CM0	Specifies cursor display on (C) and cursor display mode (CM1–0).	0					
R09	NOOP	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	No operation	0					
R0A	NOOP	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	No operation	0					
R0B	Horizontal cursor position	0	1	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0	Sets horizontal cursor start (HS7–0) and end (HE7–0).	0					
R0C	Vertical cursor position	0	1	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	Sets vertical cursor start (VS7–0) and end (VE7–0).	0					
R0D	Horizontal cursor position	0	1	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	SS 17	SS 16	SS 15	SS 14	SS 13	SS 12	SS 11	SS 10	Sets 1 st screen division start position (SS17–10) and 1 st screen division end position (SE17–10).	0					
R0E	Vertical cursor position	0	1	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	SS 27	SS 26	SS 25	SS 24	SS 23	SS 22	SS 21	SS 20	Sets 2 nd screen division start position (SS27–20) and 2 nd screen division end position (SE27–20).	0					
R10	RAM write data mask	0	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0	Specifies write data mask (WM15–0) at RAM write.	0					
R11	RAM address set	0	1	*	*	*	AD12–8 (upper)								AD7–0 (lower)								Initially set the RAM address to the counter (AC).		0	
R12	RAM data write	0	1	Write data (upper)								Write data (lower)								Writes data to the RAM.				0		
	RAM data read	1	1	Read data (upper)								Read data (lower)								Reads data to the RAM.				0		

Reset Function

The HD66752 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period, no instruction or CGRAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Do not access the CGRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4-0 = 10000, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW4-0 = 00000)
4. Power control (DC1-0 = 00, AP1-0 = 00: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. 1/11 bias drive (BS2-0 = 000), Two-times step-up (BT1-0 = 00), Weak contrast (CT6-0 = 0000000)
6. Entry mode set (I/D = 1: Increment by 1, AM1-0 = 00: Horizontal move, LG1-0 = 00: Replace mode)
7. Rotation (RT2-0 = 000: No shift)
8. Display control (SPT = 0: GSH1-0 = GSL1-0 = 00, REV = 0, D = 0: Display off)
9. Cursor control (C = 0: Cursor display off, CM1-0 = 00)
10. 1st screen division (SS17-10 = 00000000, SE17-10 = 11111111)
11. 2nd screen division (SS27-20 = 00000000, SE27-20 = 11111111)
12. Window cursor display position (HS7-0 = HE7-0 = VS7-0 = VE7-0 = 00000000)
13. RAM write data mask (WM15-0 = 0000H: No mask)
14. RAM address set (AD12-0 = 0000H)

CGRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Step-up circuit output pins (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2=0 (interface mode) to the GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM1/0 to the Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

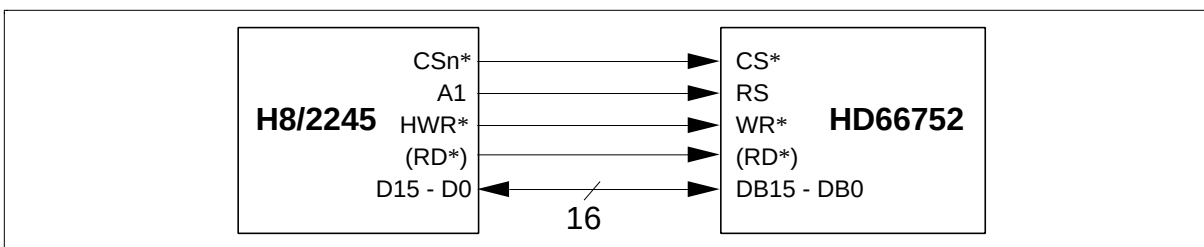


Figure 21 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM1/0 (interface mode) to the GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

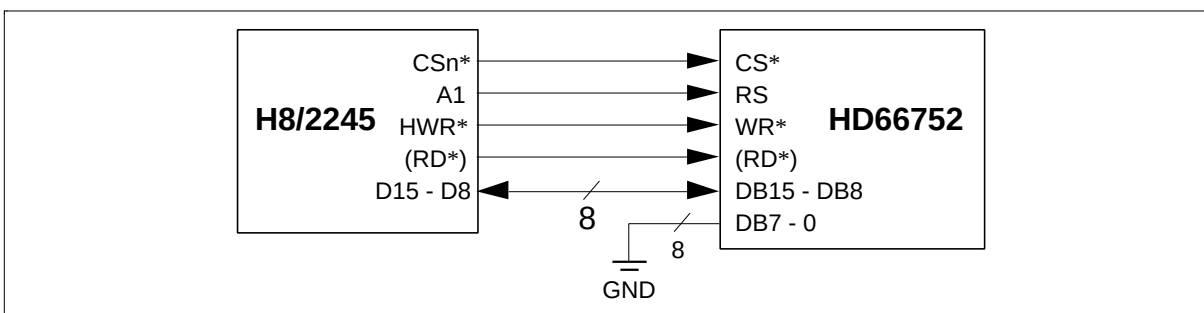


Figure 22 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface

The HD66752 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

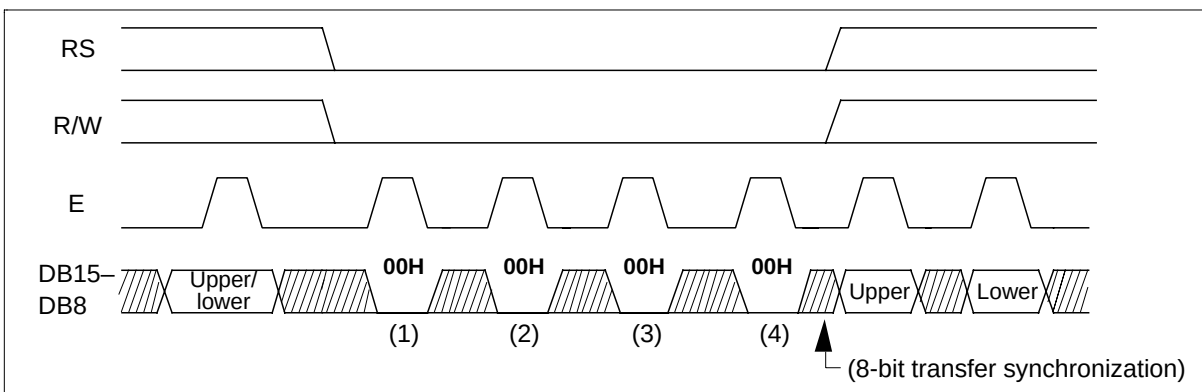


Figure 23 8-bit Transfer Synchronization

Graphics Operation Function

The HD66752 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A bit rotation function that shifts and writes the data sent from the microcomputer in a bit unit.
3. A logical operation function that writes the data sent from the microcomputer and the original RAM data by a logical operation.

Since the display data in the graphics RAM (CGRAM) can be quickly rewritten, the load of the microcomputer processing can be reduced in the large display screen when a font pattern, such as kanji characters, is developed for any position (BiTBLT processing).

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 17 Graphics Operation

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG	
Write mode 1	0/1	00	00	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	01	00	Vertical data replacement, font development, vertical-border drawing
Write mode 3	0/1	10	00	Vertical data replacement with two-word width, kanji-font development
Read/write mode 1	0/1	00	01 10 11	Horizontal data replacement with logical operation, horizontal-border drawing
Read/write mode 2	0/1	01	01 10 11	Vertical data replacement with logical operation, vertical-border drawing
Read/write mode 3	0/1	10	01 10 11	Horizontal data replacement with two-word-width logical operation

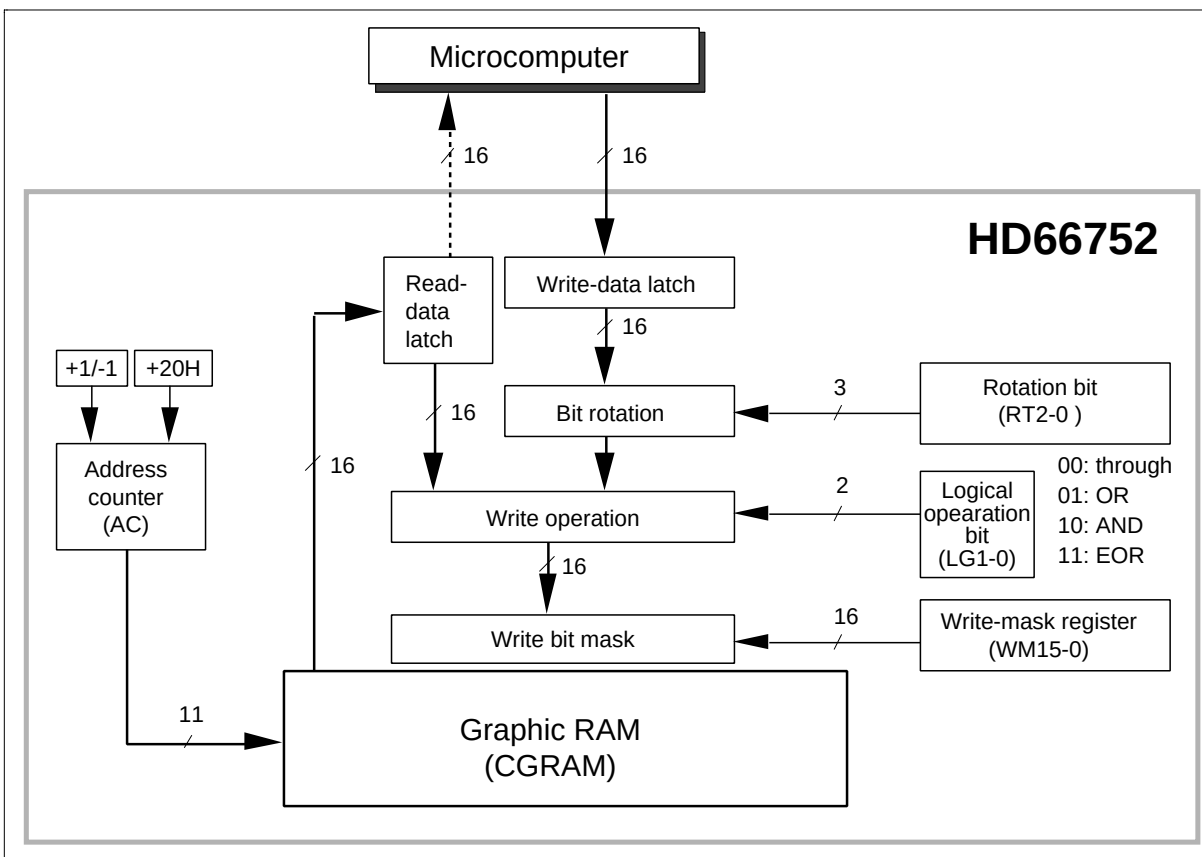


Figure 24 Data Processing Flow of the Graphics Bit Operation

1. Write mode 1: AM1-0 = 00, LG1-0 = 00

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (CGRAM) or to draw borders. The rotation function (RT2-0) or write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the graphics RAM.

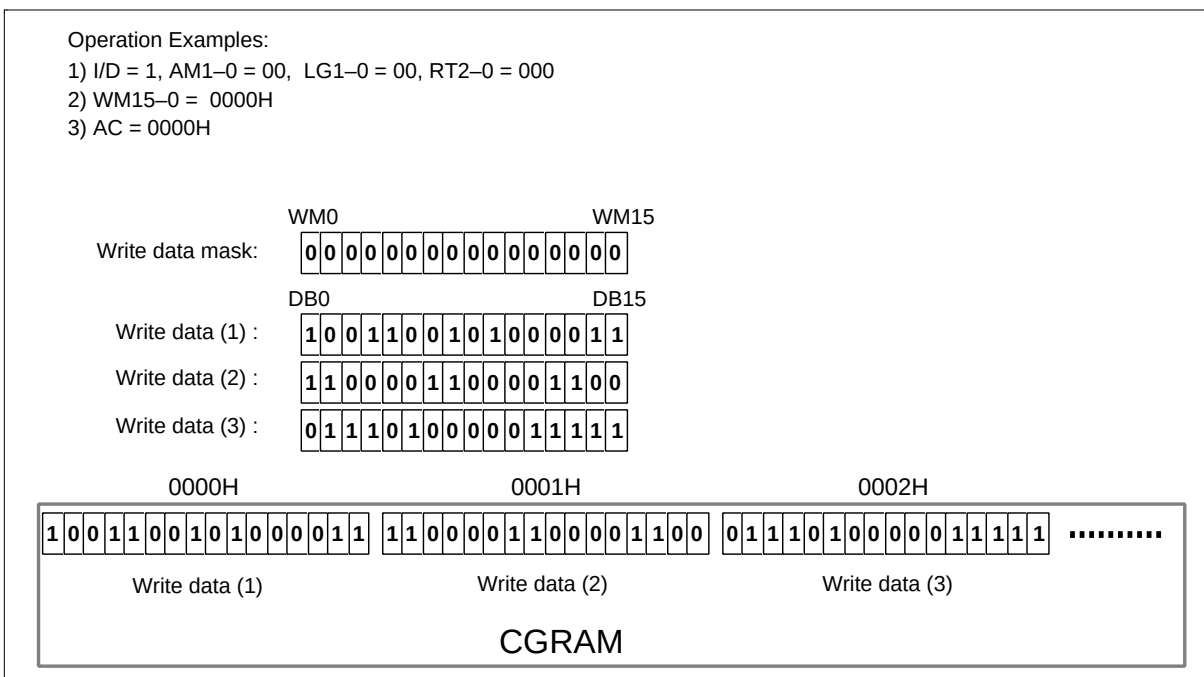


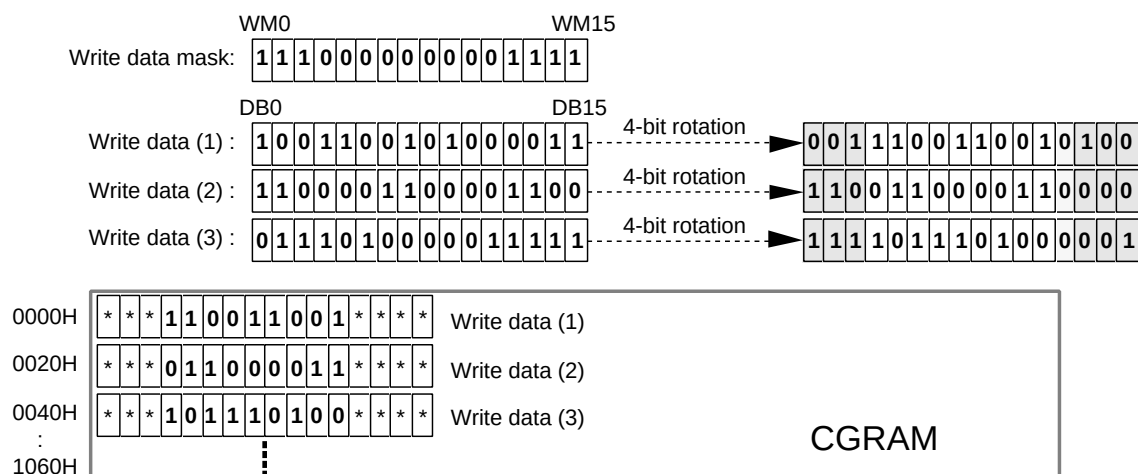
Figure 25 Writing Operation of Write Mode 1

2. Write mode 2: AM1-0 = 01, LG1-0 = 00

This mode is used when the data is vertically written at high speed. It can also be used to initialize the graphics RAM (CGRAM), develop the font pattern in the vertical direction, or draw borders. The rotation function (RT2-0) or write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 20H, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.

Operation Examples:

- 1) I/D = 1, AM1-0 = 01, LG1-0 = 00, RT2-0 = 010
- 2) WM15-0 = F007H
- 3) AC = 0000H

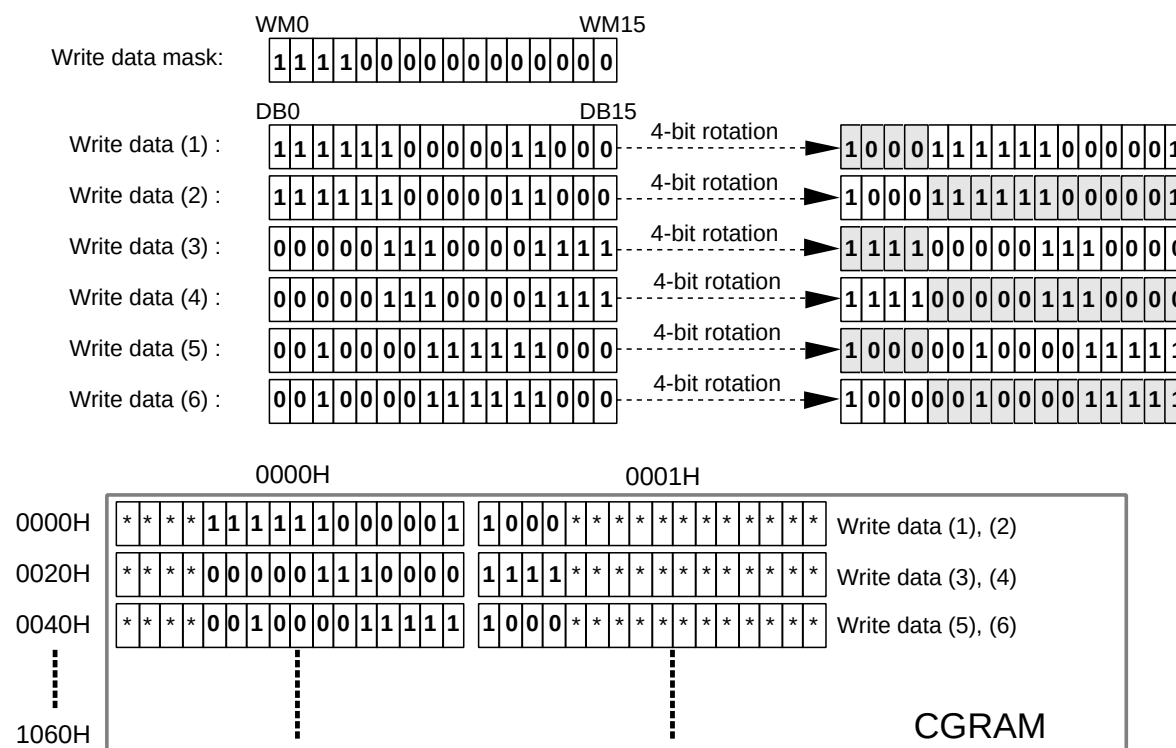


- Notes:
1. The bit area data in the RAM indicated by '*' is not changed.
 2. After writing to address 1060H, the AC jumps to 0001H.

Figure 26 Writing Operation of Write Mode 2

Operation Examples:

- 1) I/D = 1, AM1—0 = 10, LG1—0 = 00, RT2—0 = 010
- 2) WM15—0 = 000FH
- 3) AC = 0000H



- Notes: 1. The bit area data in the RAM indicated by '*' is not changed.
2. After writing to address 1061H, the AC jumps to 0002H.

Figure 27 Writing Operation of Write Mode 3

4. Read/Write mode 1: AM1-0 = 00, LG1-0 = 01/10/11

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same pulse width as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. (However, the bus cycle must be the same as the read cycle.) The rotation function (RT2-0) or write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the graphics RAM.

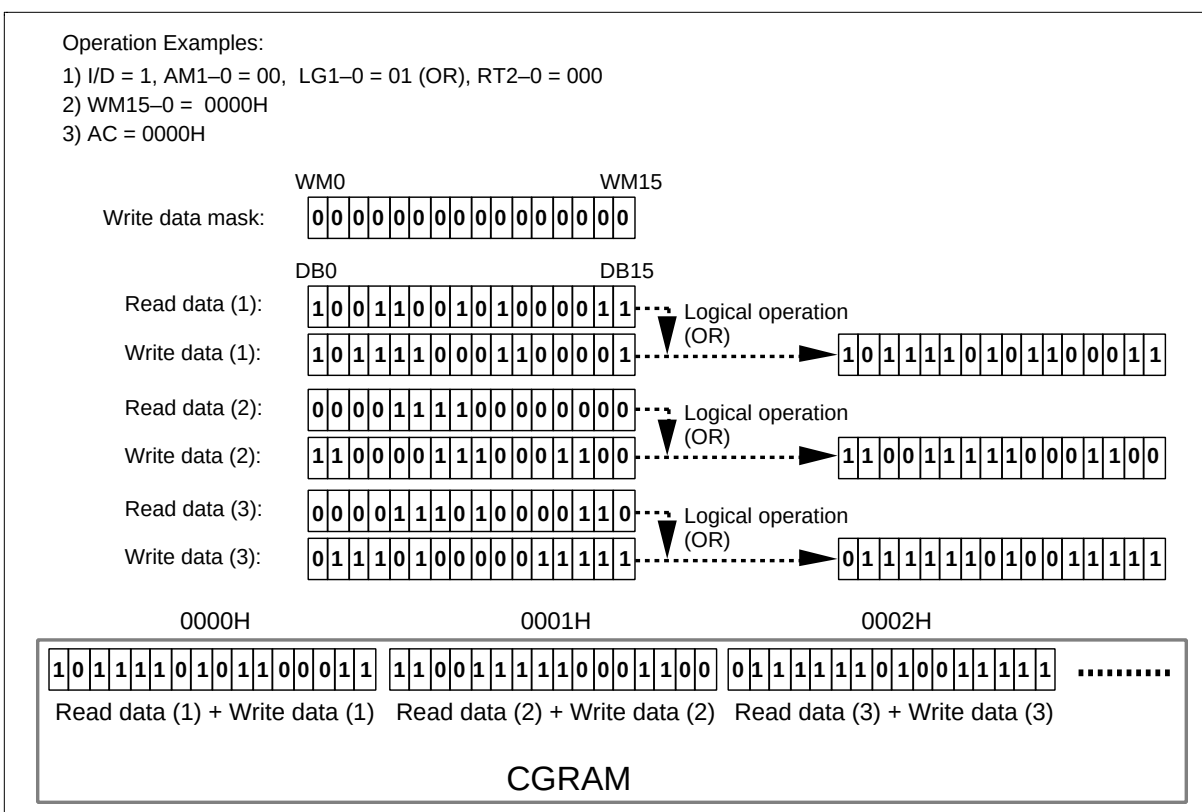


Figure 28 Writing Operation of Read/Write Mode 1

5. Read/Write mode 2: AM1-0 = 01, LG1-0 = 01/10/11

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the graphics RAM (CGRAM), performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the CGRAM. This mode can read the data during the same pulse width as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. (However, the bus cycle must be the same as the read cycle.) The rotation function (RT2-0) or write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 20H, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the graphics RAM.

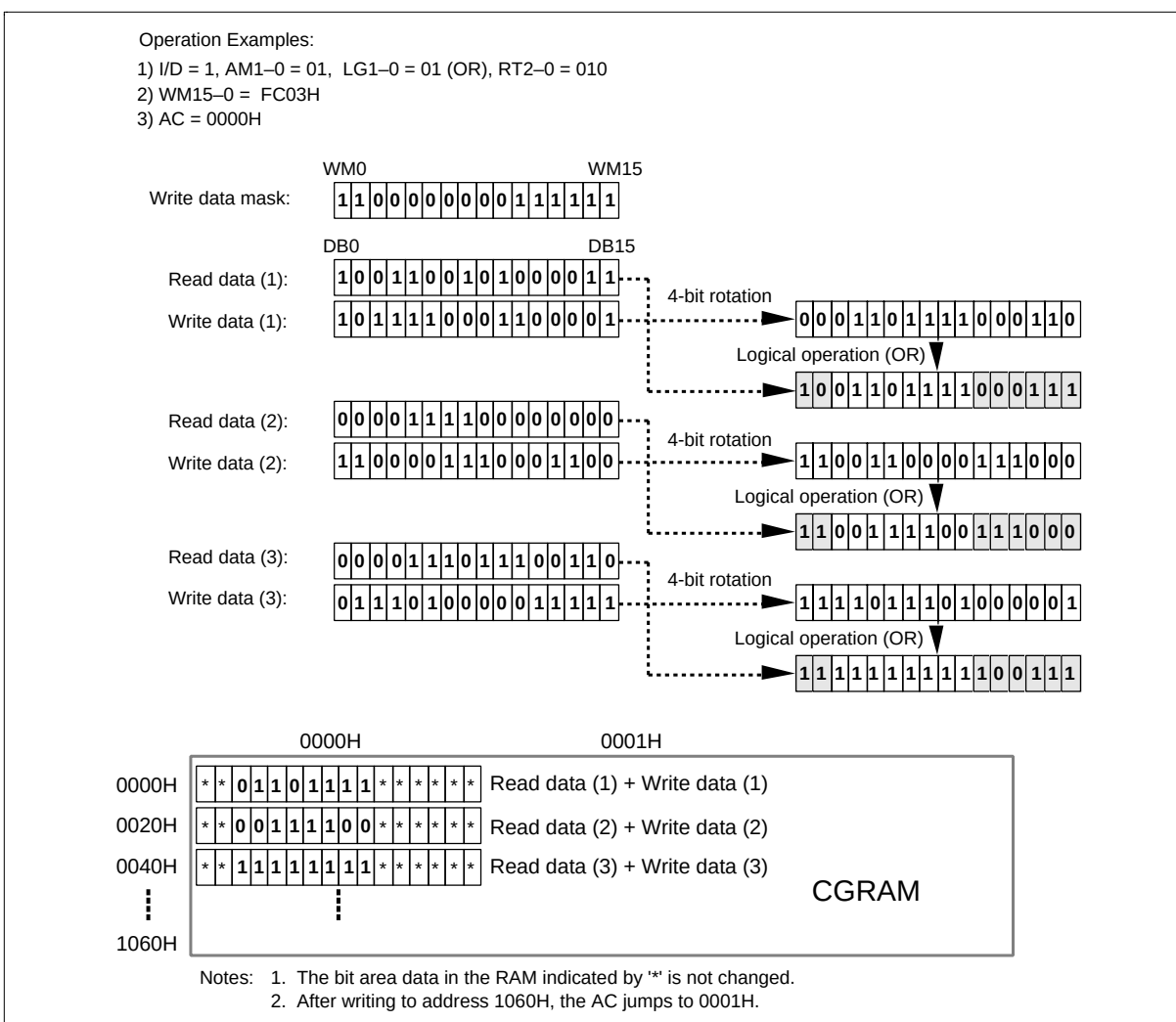


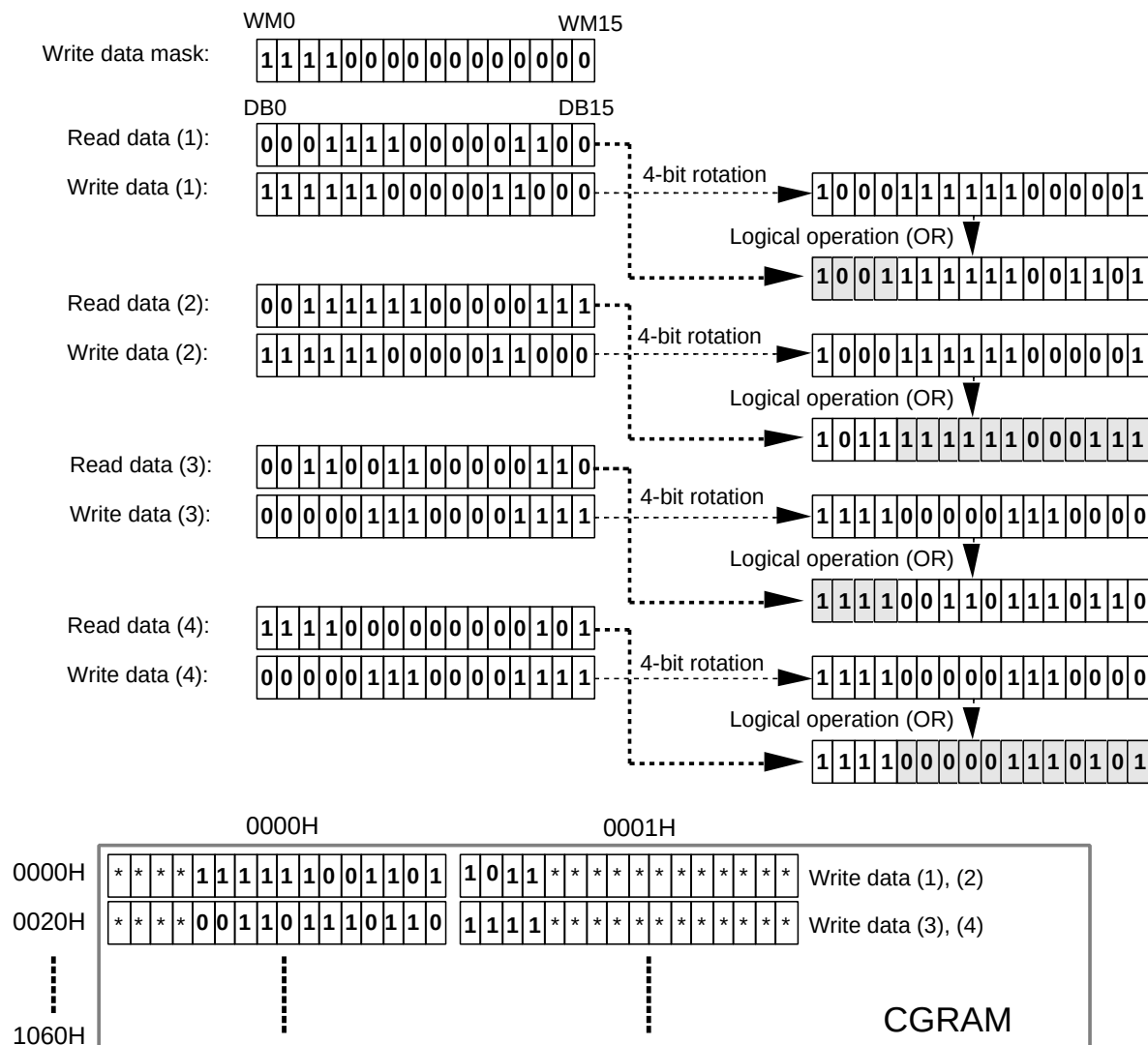
Figure 29 Writing Operation of Read/Write Mode 2

6. Read/Write mode 3: AM1–0 = 10, LG1–0 = 01/10/11

This mode is used when the data is written with high speed by vertically shifting bits and by performing logical operation with the original data. It can be also used to write the 16-bit data for two words into the graphics RAM (CGRAM), develop the font pattern, or transfer the BiTBLT as a bit unit. This mode can read the data during the same pulse width as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. (However, the bus cycle must be the same as the read cycle.) The rotation function (RT2–0) or write-data mask function (WM15–0) are also enabled in these operations. However, although the write-data mask function masks the bit position set with the write-data mask register (WM15–0) at the odd-times (such as the first or third) write, the function masks the bit position which reversed the setting value of the write-data mask register (WM15–0) at the even-times (such as the second or fourth) write. After the odd-times writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0). After the even-times writing, the AC automatically increments or decrements by $-1 + 20H$ (I/D=1) or $+1 + 20H$ (I/D=0). The AC automatically jumps to the upper edge after it has reached the lower edge of the graphics RAM.

Operation Examples:

- 1) I/D = 1, AM1—0 = 10, LG1—0 = 01, RT2—0 = 010
- 2) WM15—0 = 000FH
- 3) AC = 0000H



- Notes:
1. The bit area data in the RAM indicated by '*' is not changed.
 2. After writing to address 1061H, the AC jumps to 0002H.

Figure 30 Writing Operation of Read/Write Mode 3

HD66752

Oscillation Circuit

The HD66752 can either be supplied with operating pulses externally (external clock mode) or oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode). Note that in R-C oscillation, the oscillation frequency is changed according to the internal capacitance value, the external resistance value, or operating power-supply voltage.

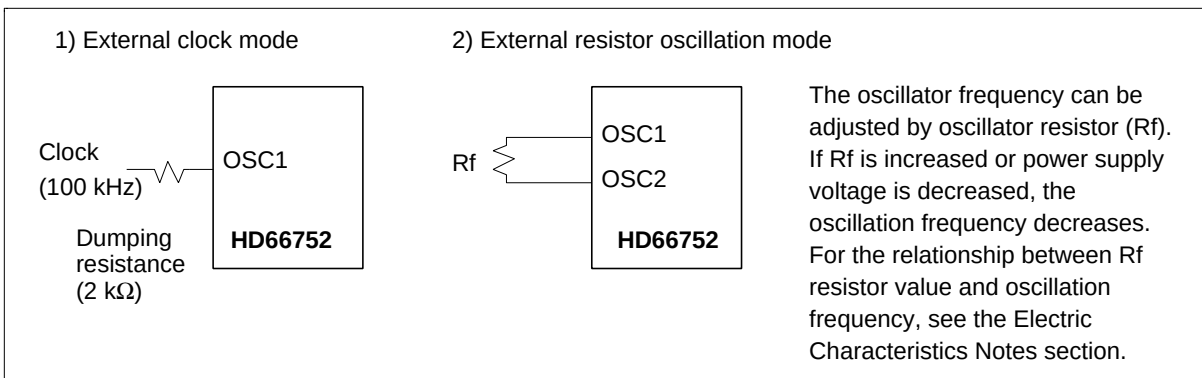


Figure 31 Oscillation Circuits

Table 18 Relationship between Liquid Crystal Drive Duty Ratio and Frame Frequency

LCD Duty	NL4-0 Set Value	Recommended Drive Bias Value	Frame Frequency	One-frame Clock
1/24	02H	1/6	72 Hz	1392
1/32	03H	1/6	71 Hz	1408
1/40	04H	1/7	71 Hz	1400
1/48	05H	1/8	72 Hz	1392
1/56	06H	1/8	71 Hz	1400
1/64	07H	1/9	71 Hz	1408
1/72	08H	1/9.5	69 Hz	1440
1/80	09H	1/10	69 Hz	1440
1/88	0AH	1/10	71 Hz	1408
1/96	0BH	1/10	69 Hz	1440
1/104	0CH	1/11	69 Hz	1456
1/112	0DH	1/11	69 Hz	1456
1/120	0EH	1/11	69 Hz	1440
1/128	0FH	1/11	71 Hz	1408
1/132	10H	1/11	69 Hz	1452

Note: The frame frequency above is for 100-kHz operation and proportions the oscillation frequency (f_{osc}).

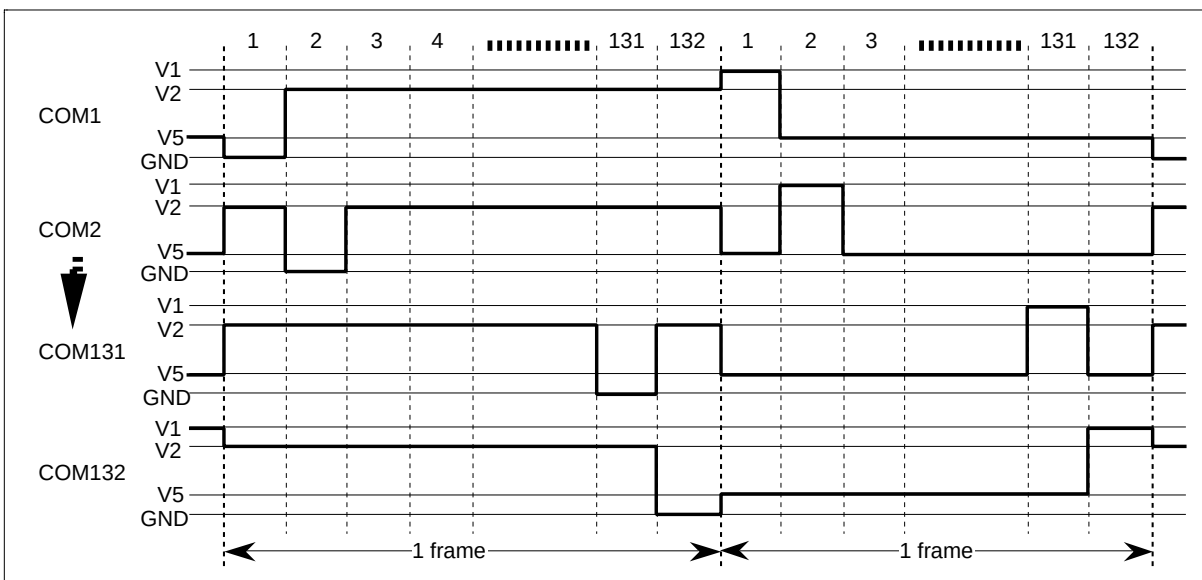


Figure 32 LCD Drive Output Waveform (B-pattern AC Drive with 1/132 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66752 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

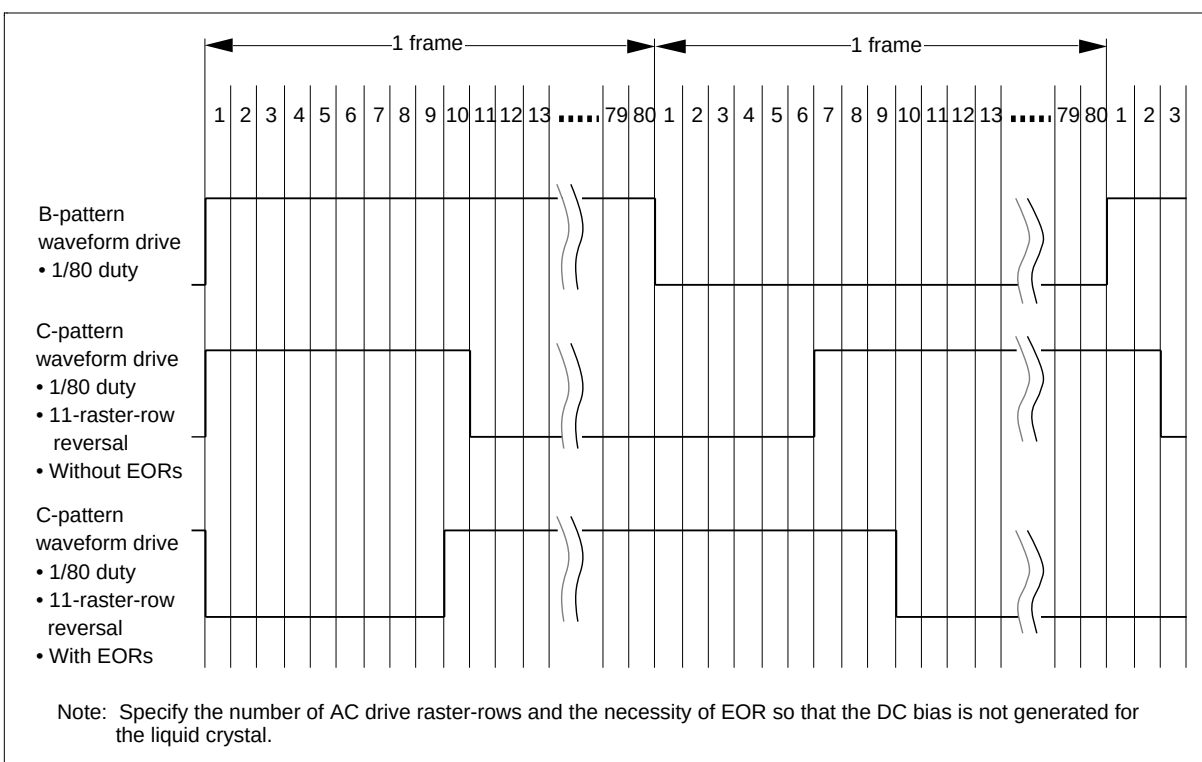


Figure 33 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal step-up circuit, circuits should be connected as shown in figure 34. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66752 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.47 μ F (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.

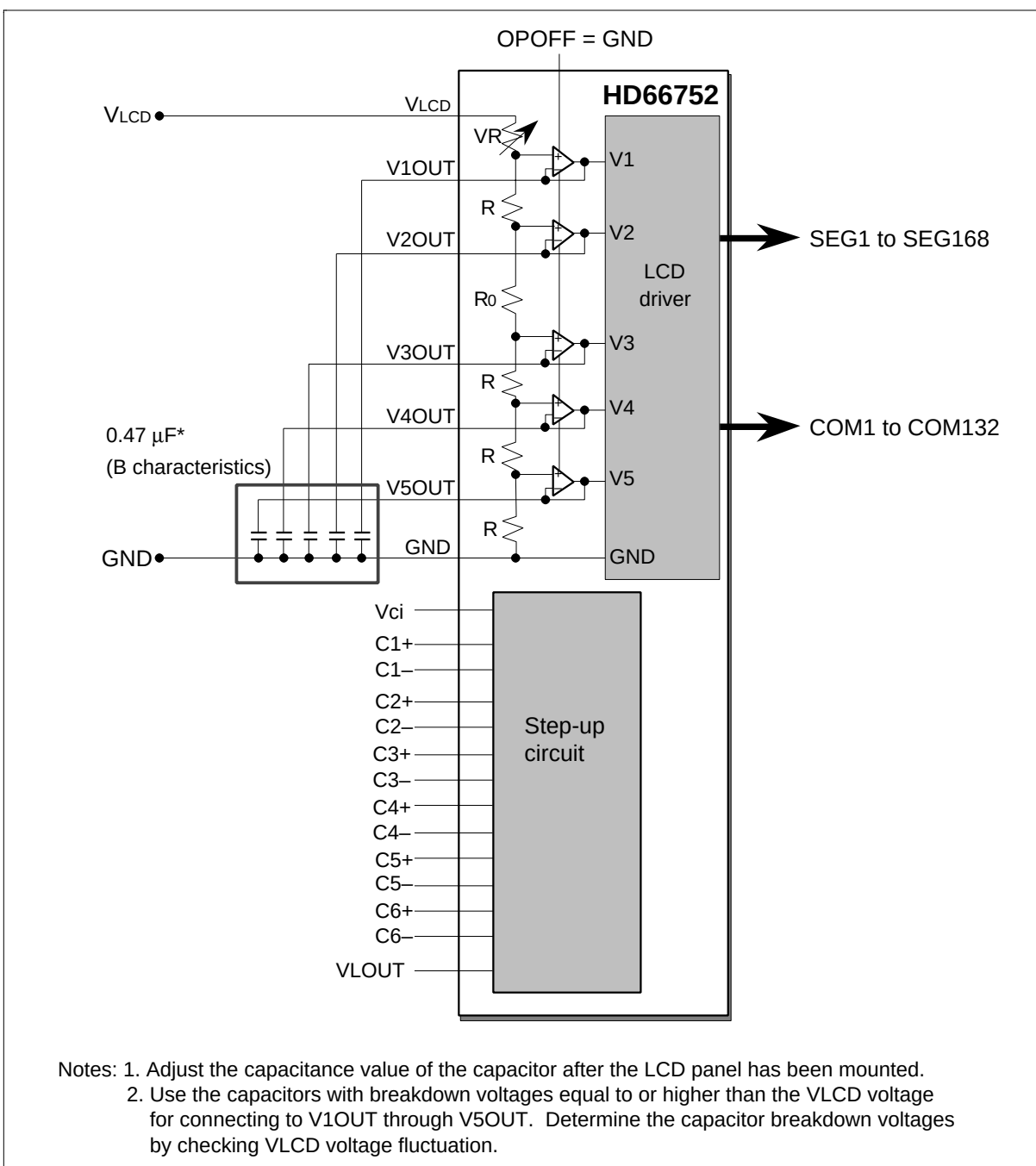


Figure 34 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal step-up circuit, circuits should be connected as shown in figure 35. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits, by controlling the reference voltage for the step-up circuit (Vci pin) using a thermistor, or by controlling the output voltage of the step-up circuit (VLCD pin).

Note that Vci is both a reference voltage and power supply for the step-up circuit, and the VLCD pin is the power source for LCD driving system. These voltages must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied.

The HD66752 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.47 μ F (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.

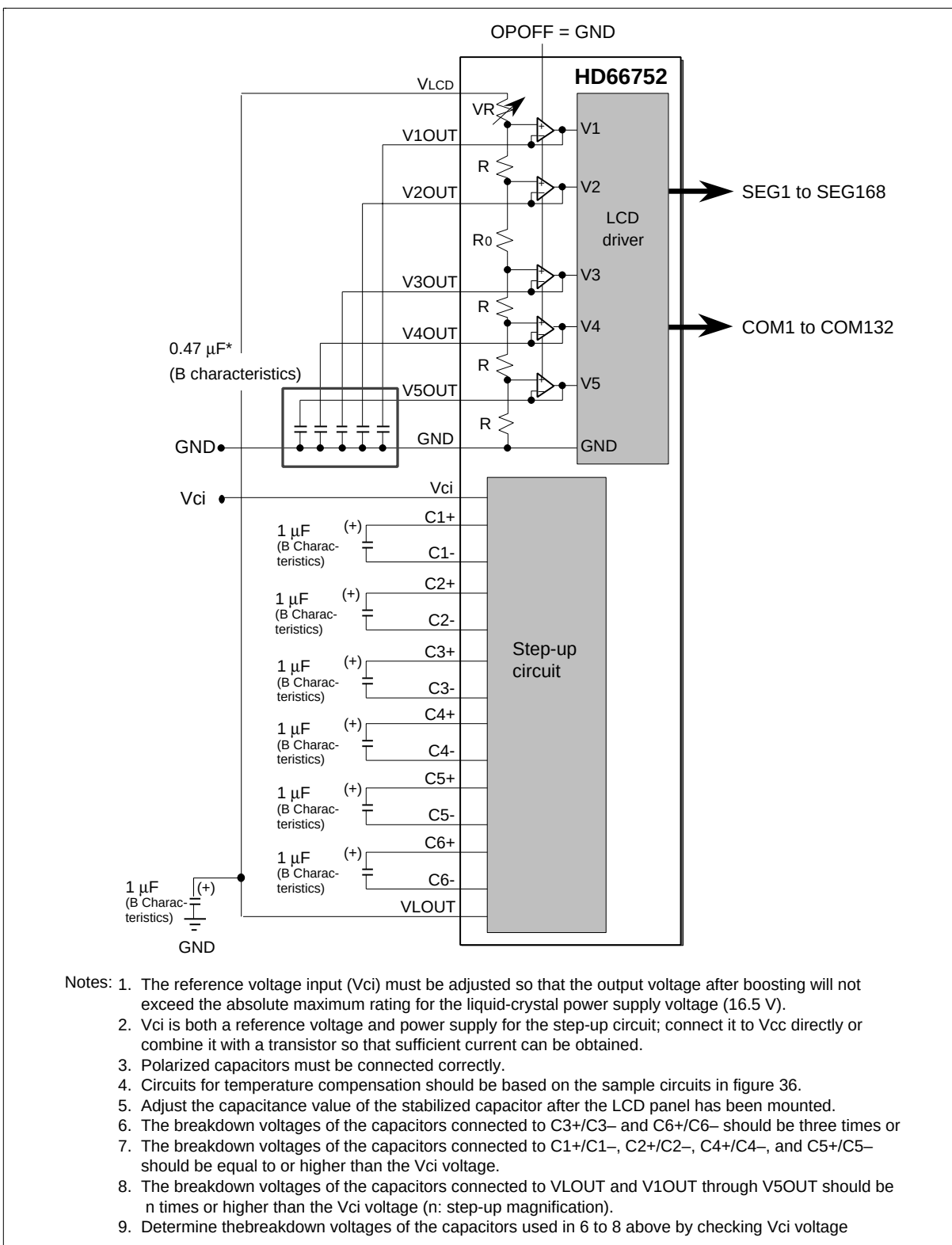


Figure 35 Internal Step-up Circuit for LCD Drive Voltage Generation

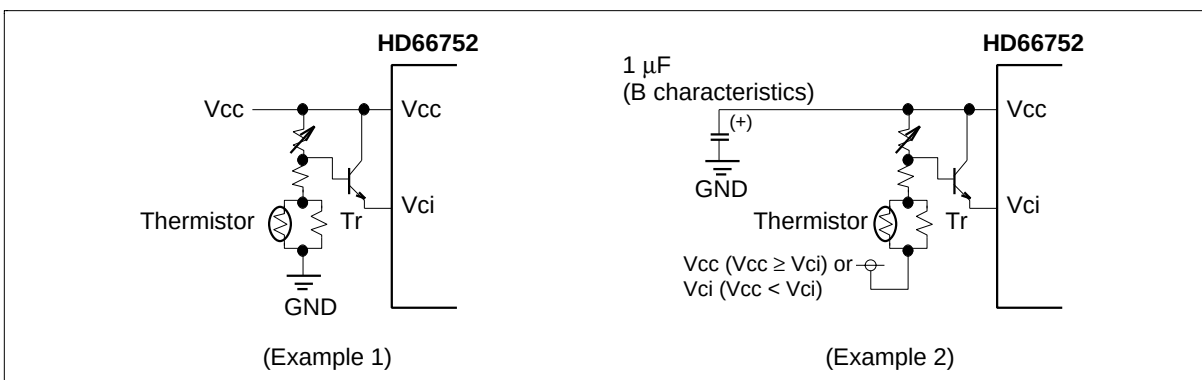


Figure 36 Temperature Compensation Circuits

Using internal Operational Amplifiers

The HD66752's internal operational amplifiers have a low current consumption type circuit to save total power consumption. Enough current may not be supplied by this operation amplifiers with low voltage (e.g. less 2.5 V) and low temperature (e.g. below -20°C). This may affect display quality to be worse by actual displayed pattern.

When specification of LCD panel and peripheral circuit are designed, please refer following information to be better display quality.

Pin condition (VTEST pin)

(1) Power supply voltage; $V_{cc} \geq 2.5 \text{ V}$ (Operational amplifier circuit obtains sufficient operation current.)

VTEST pin = open (NC)

(2) Power supply voltage; $V_{cc} < 2.5 \text{ V}$ (Operational amplifier circuit operates with low current under low temperature.)

VTEST pin = 1.2 to 1.3 V needs to be supplied

Note) Figure and table show circuit example to supply 1.2 to 1.3 V to the VTEST pin. In case of operational amplifiers circuit needs more operation current, VTEST voltage level should be increased to change R1 and R2 resistance, confirming display quality current consumption.

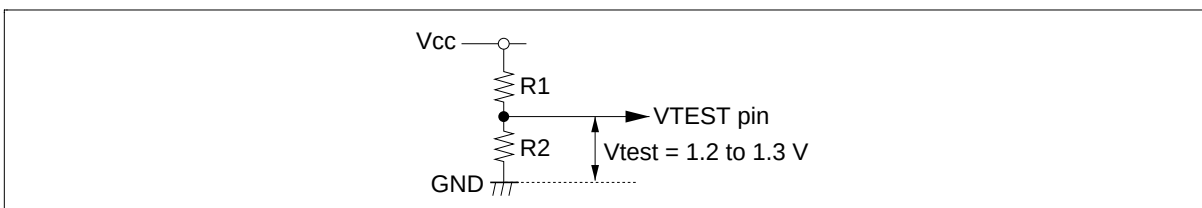


Figure 37 Input voltage to VTEST pin

HD66752

Table 19 Value of R1, R2

Vcc	R1	R2	Vtest (VTEST pin voltage)
2.4 V	270 k Ω	330 k Ω	1.23 V
2.0 V	220 k Ω	360 k Ω	1.22 V
1.8 V	180 k Ω	390 k Ω	1.22 V

Switching the Step-up Factor

Instruction bits (BT1/0 bits) can optionally select the step-up factor of the internal step-up circuit. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the step-up factor for the minimum requirements. For details, see the Partial-display-on Function section.

According to the maximum step-up factor, external capacitors need to be connected. For example, when the maximum step-up is six times or five times, capacitors between C6+ and C6– or between C5+ and C5– are needed as in the case of the seven-times step-up. When the step-up is two-times, capacitors between C1+ and C1– or between C4+ and C4– are not needed.

Place a capacitor with a breakdown voltage of three times or more the Vci-GND voltage between C6+ and C6– and between C3+ and C3–, a capacitor with a breakdown voltage larger than the Vci-GND voltage between C1+ and C1–, C2+ and C2–, C4+ and C4–, and C5+ and C5–, and a capacitor with a breakdown voltage of n times or more the Vci-GND voltage to VLOUT (n: step-up factor) (see figure 37).

Note: Determine the capacitor breakdown voltages by checking Vci voltage fluctuation.

Table 20 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Two-times step-up output
0	1	Five-times step-up output
1	0	Six-times step-up output
1	1	Seven-times step-up output

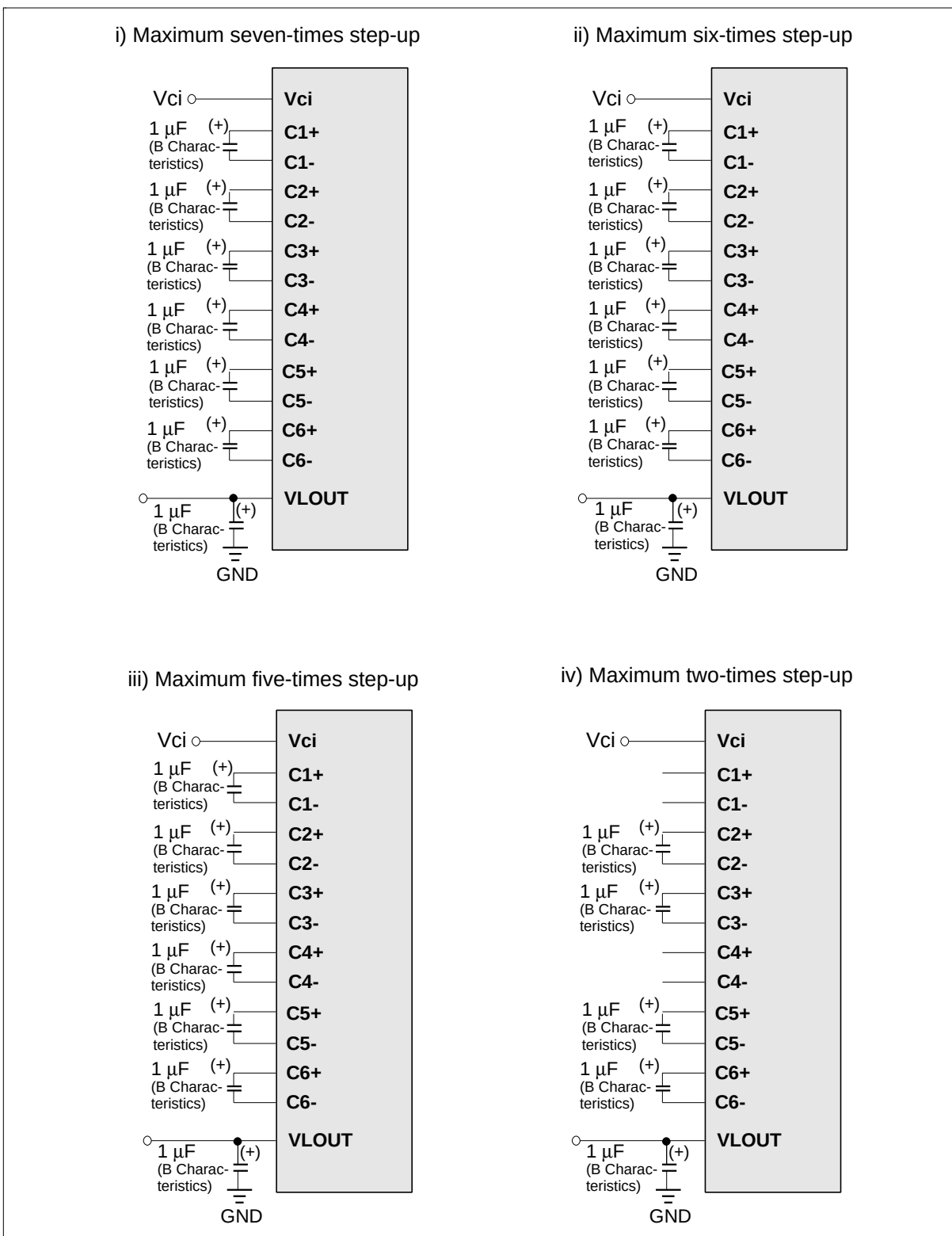


Figure 38 Step-up Circuit Output Factor Switching

Example of Power-supply Voltage Generator for More Than Seven-times Step-up Output

The HD66752 incorporates a step-up circuit for up to seven-times step-up. However, the LCD drive voltage (VLCD) will not be enough for seven-times step-up from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for step-up can be set higher than the power-supply voltage of Vcc.

When the step-up factor is high, the current driving ability is lowered and insufficient display quality may result. In this case, the step-up ability can be improved by decreasing the step-up factor as shown in the step-up circuit in figure 38.

Set the Vci input voltage for the step-up circuit to 3.6 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the step-up output voltage (VLOUT) should be less than the absolute maximum ratings (16.5 V).

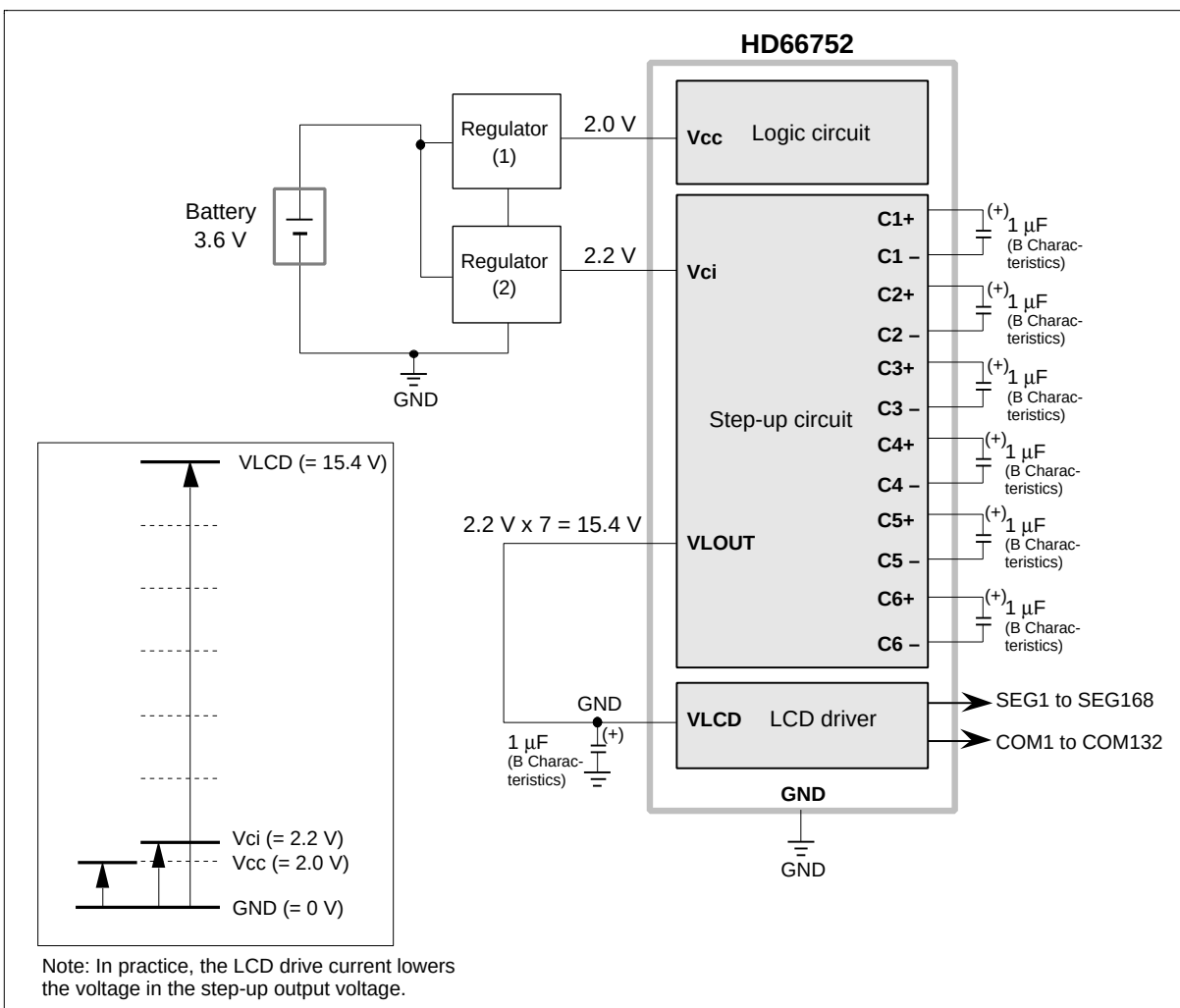


Figure 39 Usage Example of Step-up Circuit at Vci > Vcc

Contrast Adjuster

Software can adjust 128-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and $V1$) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LCD} and $V1$ (VR) can be precisely adjusted by selecting $3 \times R$ or short using the CT6 bit and in a $0.05 \times R$ unit within a range from $0.05 \times R$ through $3.20 \times R$ using the CT5-0 bits, where R is a reference resistance obtained by dividing the total resistance.

The HD66752 incorporates a voltage-follower operational amplifier for each of $V1$ to $V5$ to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT6-0 bits must be adjusted so that potential difference between V_{LCD} and $V1$ is 0.1 V or higher and that between $V4$ and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.

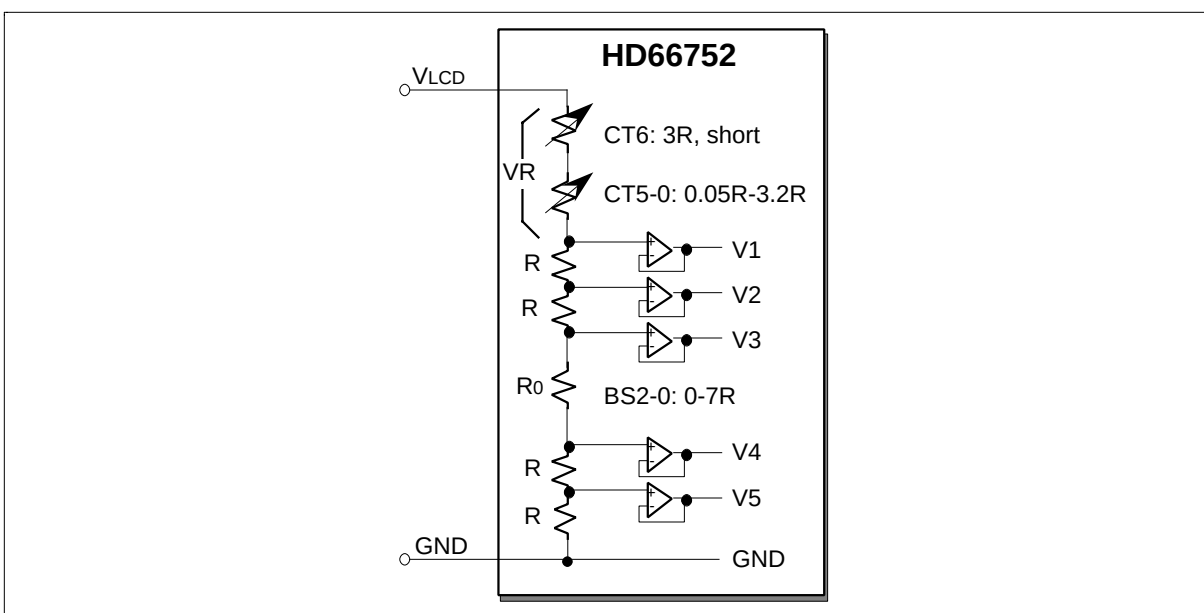


Figure 40 Contrast Adjuster

Table 21 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value						Variable Resistor Value (VR)		Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0	CT6 = "0"	CT6 = "1"		
0	0	0	0	0	0	6.20 x R	3.20 x R	(Small) (Large)	(Weak) (Bright)
0	0	0	0	0	1	6.15 x R	3.15 x R		
0	0	0	0	1	0	6.10 x R	3.10 x R		
0	0	0	0	1	1	6.05 x R	3.05 x R		
0	0	0	1	0	0	6.00 x R	3.00 x R		
0	0	0	1	0	1	5.95 x R	2.95 x R		
0	0	0	1	1	0	5.90 x R	2.90 x R		
0	0	0	1	1	1	5.85 x R	2.85 x R		
0	0	1	0	0	0	5.80 x R	2.80 x R		
0	0	1	0	0	1	5.75 x R	2.75 x R		
0	0	1	0	1	0	5.70 x R	2.70 x R		
0	0	1	0	1	1	5.65 x R	2.65 x R		
0	0	1	1	0	0	5.60 x R	2.60 x R		
1	1	1	1	0	0	3.20 x R	0.20 x R		
1	1	1	1	0	1	3.15 x R	0.15 x R		
1	1	1	1	1	0	3.10 x R	0.10 x R		
1	1	1	1	1	1	3.05 x R	0.05 x R		

Table 22 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/11 bias drive	$\frac{11 \times R}{11 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.775 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.995 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{11 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{11 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/10 bias drive	$\frac{10 \times R}{10 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.757 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.995 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{10 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{10 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/9 bias drive	$\frac{9 \times R}{9 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.737 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.994 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{9 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{9 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.714 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{8 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{8 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.686 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{7 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{7 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.992 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{6 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.990 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{5 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.988 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{4 \times R + VR} \times (V_{LCD}-GND) \geq 1.4 [V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.1 [V]$

Liquid-crystal-display Drive-bias Selector

An optimum liquid-crystal-display bias value can be selected using the BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3-0 bits). The liquid-crystal-display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is a logical optimum value. Driving by using a lower value than the optimum bias value provides lower logical contrast and lower liquid-crystal-display voltage (the potential difference between V1 and GND), which results in better image quality. When the liquid-crystal-display voltage is insufficient even if a seven-times step-up circuit is used, when the step-up driving ability is lowered by setting a high factor for the step-up circuit, or when the output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid-crystal-display bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT5-0 bits) and selecting the step-up output level (BT1/0 bits).

$$\text{Optimum bias value for } 1/N \text{ duty ratio drive voltage} = \frac{1}{\sqrt{N+1}}$$

Table 22 Optimum Drive Bias Values

LCD drive duty ratio	1/128	1/120	1/112	1/104	1/96	1/88	1/80	1/72	1/64	1/32	1/24	1/16
(NL3-0 set value)	1111	1110	1101	1100	1011	1010	1001	1000	0111	0100	0011	0010
Optimum drive bias value	1/11	1/11	1/11	1/11	1/10	1/10	1/10	1/9	1/9	1/6	1/6	1/5
(BS2-0 set value)	000	000	000	000	001	001	001	010	010	101	101	100

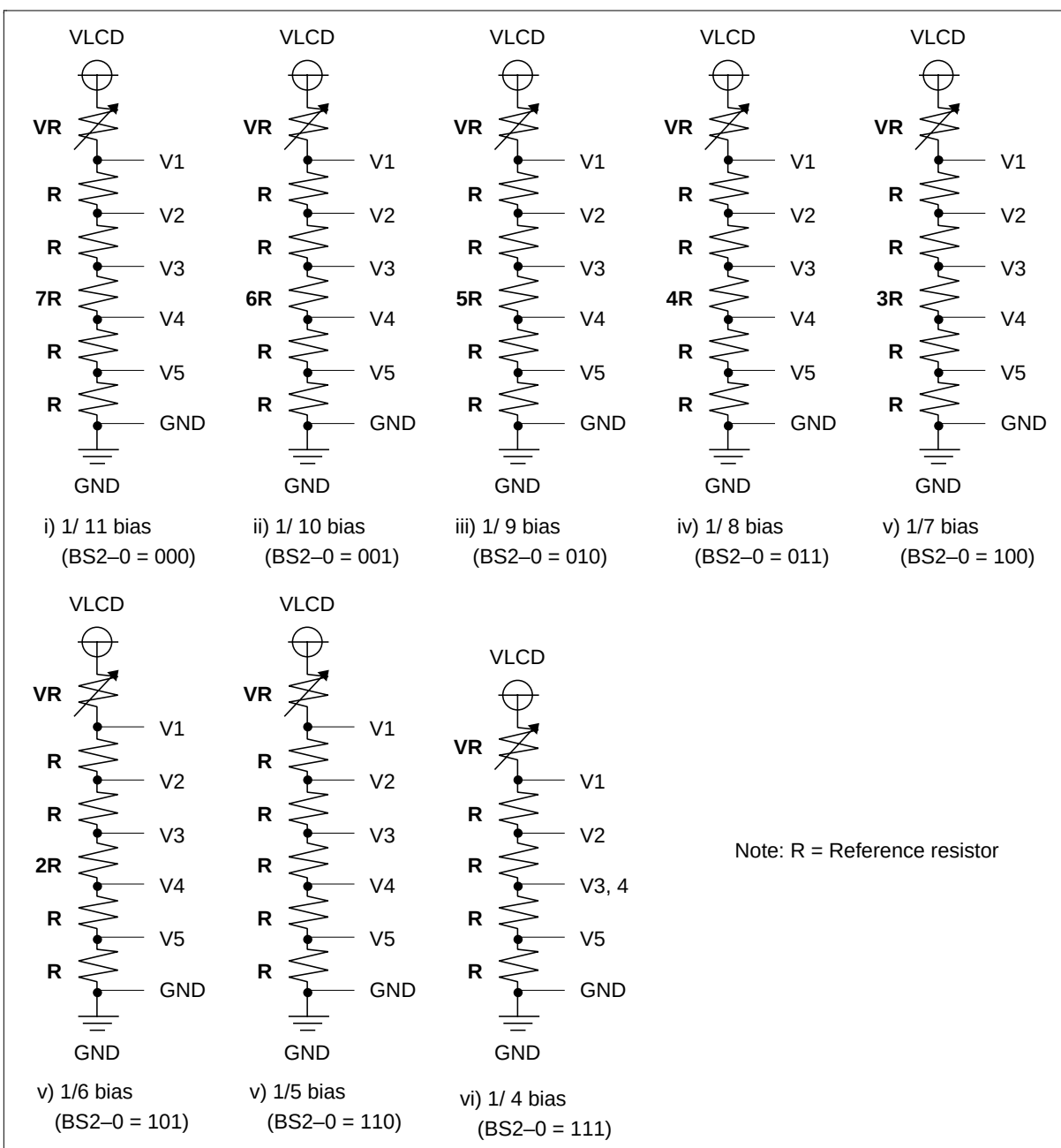


Figure 41 Liquid Crystal Display Drive Bias Circuit

Four-grayscale Display Function

The HD66752 supports the four-grayscale monochrome display function. The four-grayscale monochrome display is used for the display data of the two-bit pixel set sent to the CGRAM. There are four grayscale levels: always unlit, weak middle level, bright middle level, and always lit. In the bright and weak middle-level grayscale displays, the GSL1-0 and GSH1-0 bits can select the grayscale level, respectively.

The frame rate control (FRC) method, which is used for grayscale control, can reduce charge/discharge current in the LCD glass during grayscale display.

Table 23 Relationships between the CGRAM Data and the Display Contents

Upper Bit	Lower Bit	Liquid Crystal Display
0	0	Non-selected (unlit)
0	1	GSL1-0 = 00: 1/4-level grayscale (one frame lit during a four-frame period) GSL1-0 = 01: 1/3-level grayscale (one frame lit during a three-frame period) GSL1-0 = 10: 2/4-level grayscale (two frames lit during a four-frame period) GSL1-0 = 11: Lit (no grayscale control)
1	0	GSH1-0 = 00: 3/4-level grayscale (three frames lit during a four-frame period) GSH1-0 = 01: 2/3-level grayscale (two frames lit during a three-frame period) GSH1-0 = 10: 2/4-level grayscale (two frames lit during a four-frame period) GSH1-0 = 11: Lit (no grayscale control)
1	1	Selected (lit)

Note: Upper bits: DB15, DB13, DB11, DB9, DB7, DB5, DB3, and DB1
Lower bits: DB14, DB12, DB10, DB8, DB6, DB4, DB2, and DB0

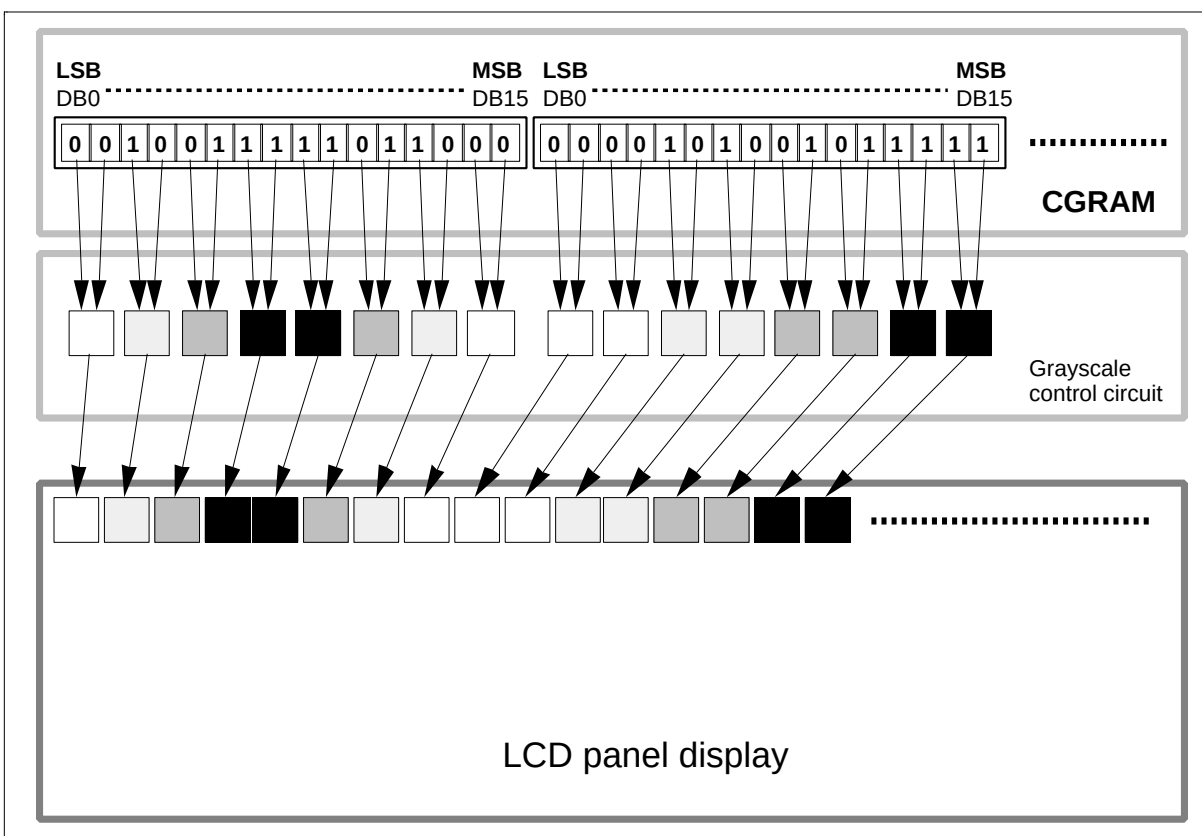


Figure 42 Four-grayscale Monochrome Display

Window Cursor Display Function

The HD66750 displays the window cursor by specifying a window area. The horizontal display position of the window cursor is specified with the horizontal cursor position register (HS7–0 to HE7–0), and the vertical display position is specified with the vertical cursor position register (VS7–0 or VE7–0). In these display position setting registers, ensure that $HS7-0 \leq HE7-0$ and $VS7-0 \leq VE7-0$. If these relationships are not satisfied, normal display cannot be attained. In addition, if the setting is $VS7-0 = VE7-0 = 00H$, a cursor is displayed on a raster-row at the most-upper edge of the screen.

This window cursor can automatically display the hardware-supported block cursor, highlight window, or menu bar. The CM1–0 bits select the following four displays in each window cursor:

1. White-blink cursor (CM1–0 = 00): Alternately blinks between the normal display and an all-white (unlit) display
2. Black-blink cursor (CM1–0 = 01): Alternately blinks between the normal display and an all-black (all lit) display
3. Black-and-white reversed cursor (CM1–0 = 10): Black-and-white-reversed normal display (no blinking)
4. Black-and-white-reversed blink cursor (CM1–0 = 11): Alternately blinks between the normal display and a black-and-white-reversed display

The above blinking display is switched in a 32-frame unit.

In vertical scrolling, note that this window cursor does not automatically move vertically.

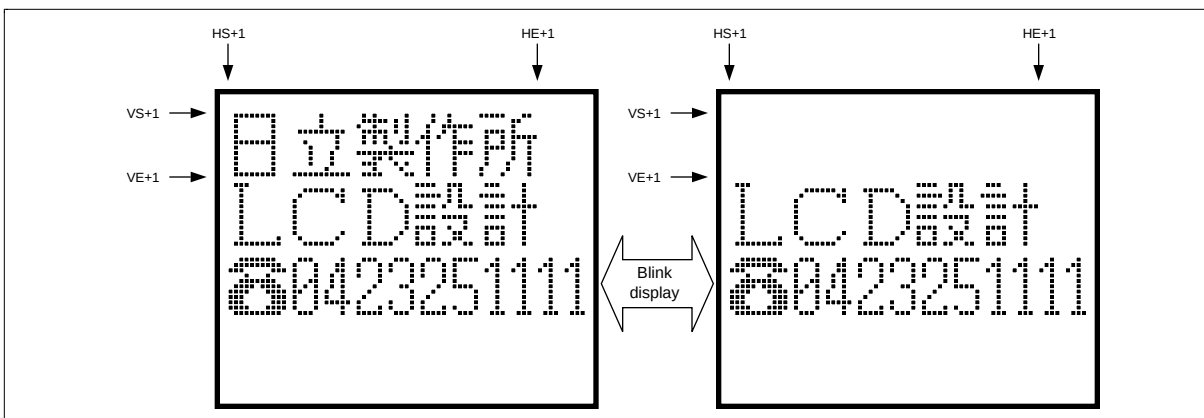


Figure 43 White Blink Cursor Display

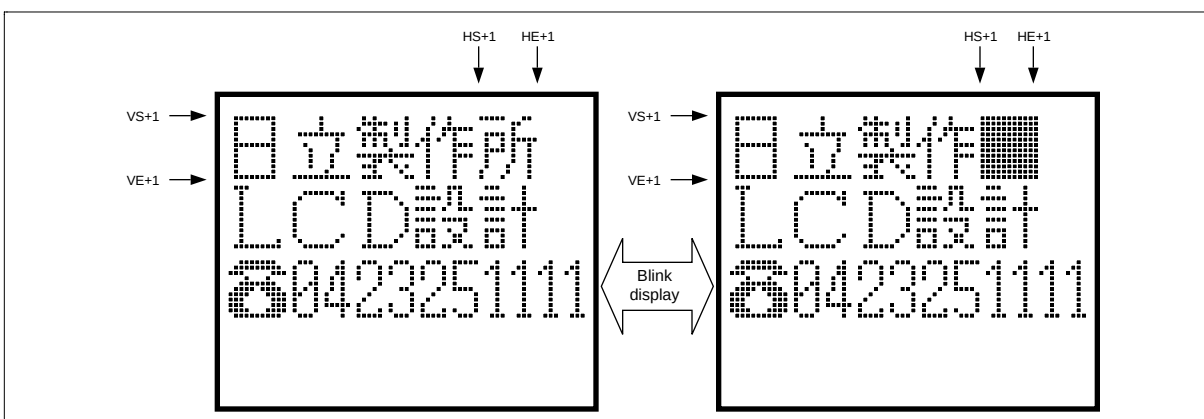


Figure 44 Black Blink Cursor Display

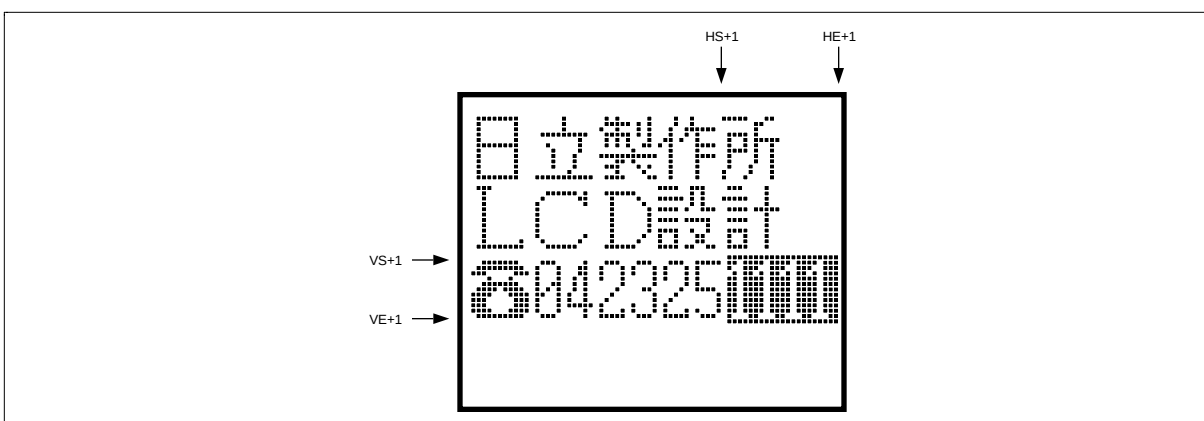


Figure 45 Black-and-white Reversed Cursor Display

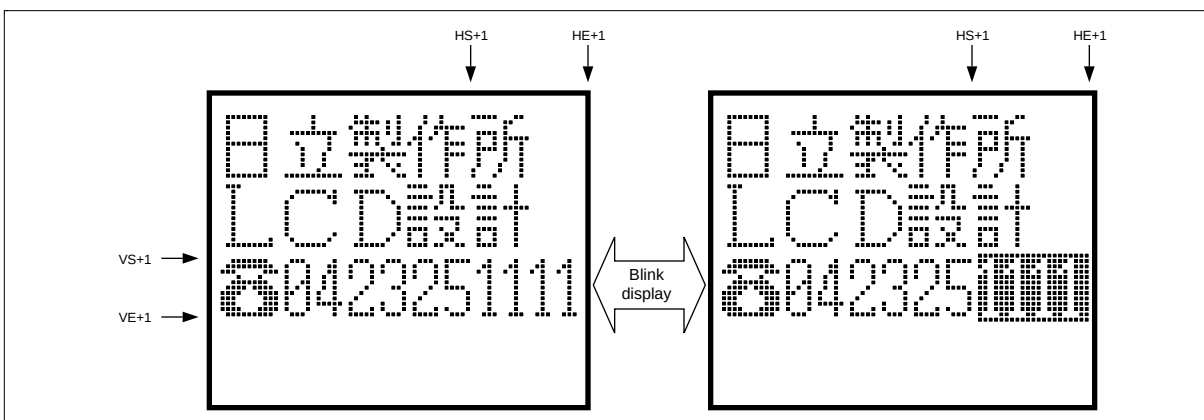


Figure 46 Black-and-white Reversed Blink Cursor Display

Reversed Display Function

The HD66752 can display graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when the REV bit in the display control register is set to 1.

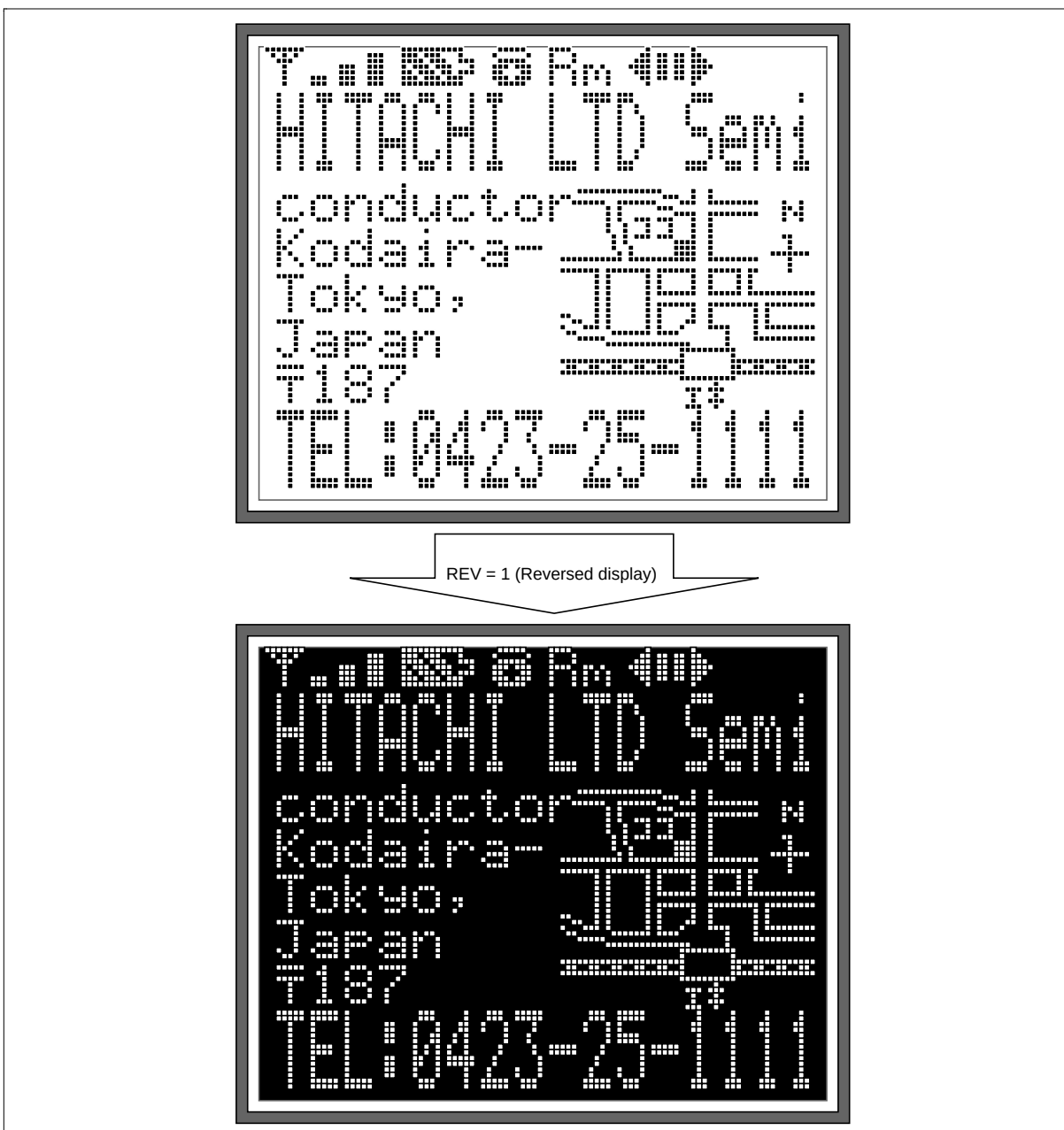


Figure 47 Reversed Display

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R0D) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R0D) for the HD66752. Note that incorrect display may occur if the restrictions are not satisfied.

Table 24 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (STP = 0)	2nd Screen Driving (STP = 1)
Register setting	SS17-10 ≤ SE17-0 ≤ 83H	SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ 83H
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

- Notes:
1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
 2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
 3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

Screen-division Driving Function

The HD66752 can select and drive two screens at any position with the screen-driving position registers (R0D and R0E). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL3-0), thus reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R0D). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R0E). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

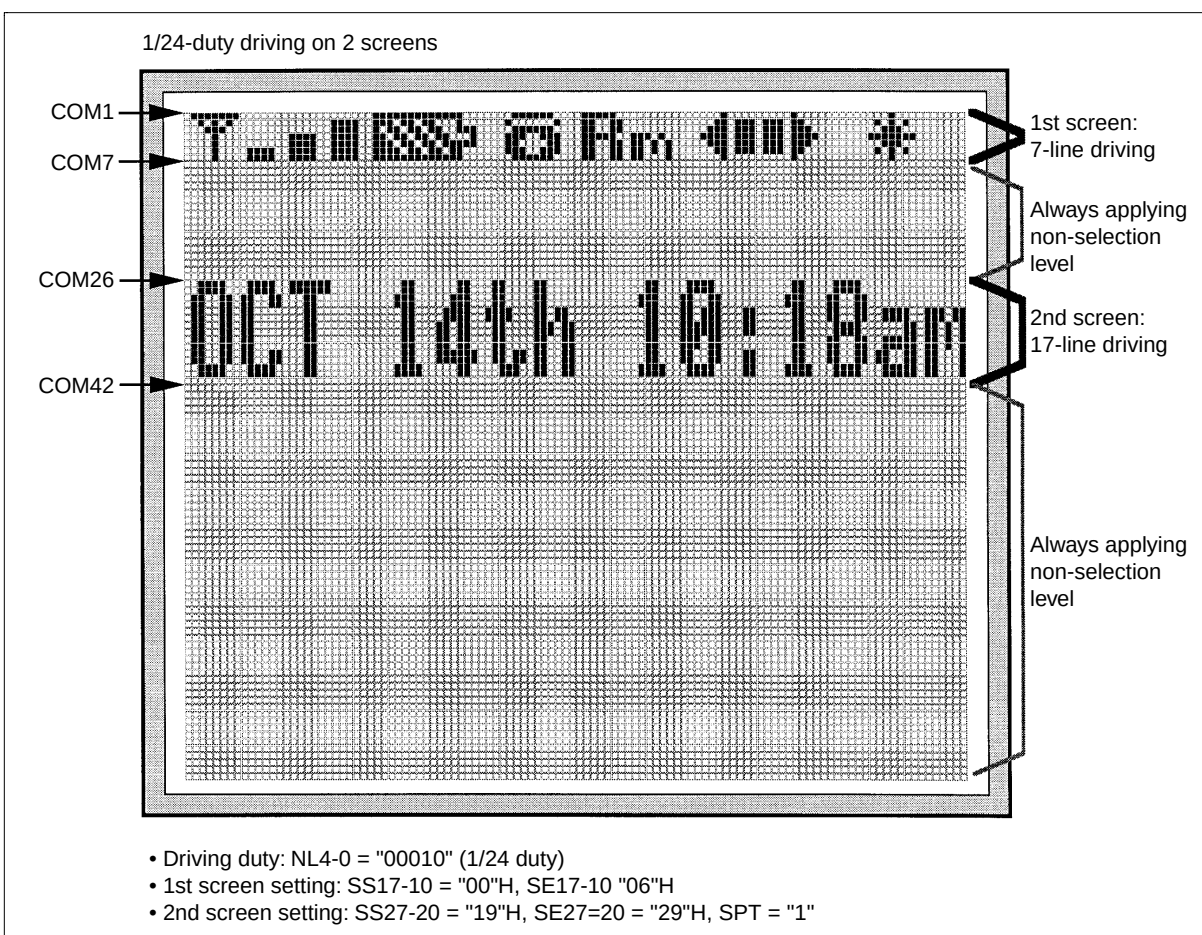


Figure 48 Display Example in 2-screen Division Driving

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66752 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG168) and COM (COM1 to COM132) pins output the GND level, resulting in no display. If the AP1-0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 27 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66752 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG168) and COM (COM1 to COM132) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1-0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

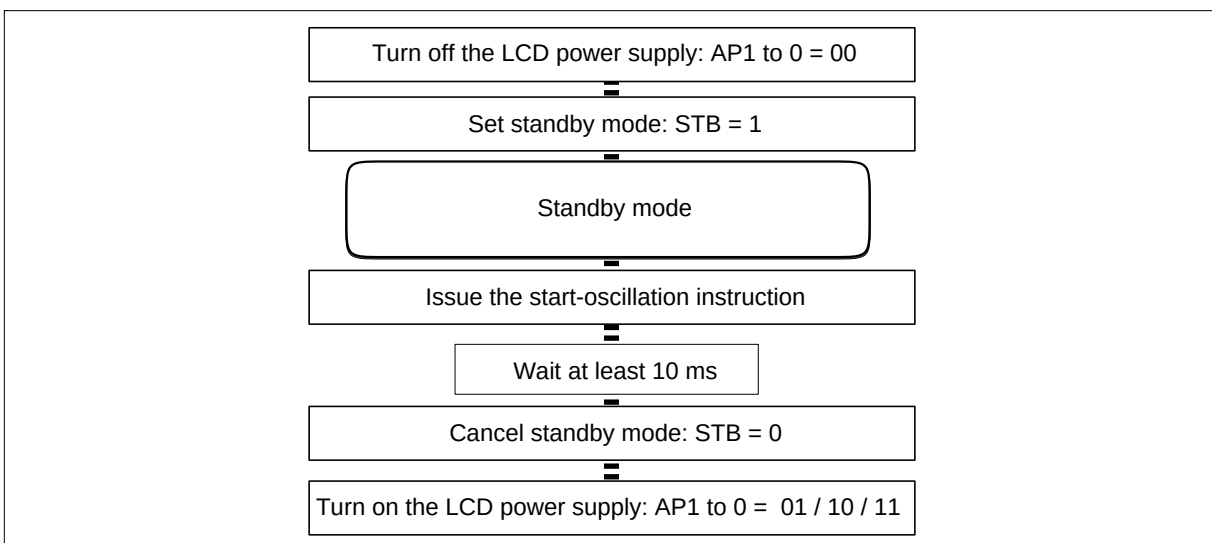


Figure 49 Procedure for Setting and Canceling Standby Mode

HD66752

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	−0.3 to +4.6	1, 2
Power supply voltage (2)	$V_{LCD} - GND$	V	−0.3 to +16.5	1, 3
Input voltage	V_t	V	−0.3 to $V_{CC} + 0.3$	1
Operating temperature	T_{opr}	°C	−40 to +85	1, 4
Storage temperature	T_{stg}	°C	−55 to +110	1, 5

- Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. $V_{CC} > GND$ must be maintained.
 3. $V_{LCD} > GND$ must be maintained.
 4. For bare die and wafer products, specified up to 85°C.
 5. This temperature specifications apply to the TCP package.

DC Characteristics ($V_{CC} = 2.0$ to 3.6 V, $T_a = -40$ to $+85^\circ\text{C}^{*1}$)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$0.7 V_{CC}$	—	V_{CC}	V	$V_{CC} = 2.0$ to 3.6 V	2, 3
Input low voltage	V_{IL}	-0.3	—	$0.15 V_{CC}$	V	$V_{CC} = 2.0$ to 3.6 V	2, 3
Output high voltage (1) (DB0-15 pins)	V_{OH1}	$0.75 V_{CC}$	—	—	V	$I_{OH} = -0.1$ mA	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	—	—	$0.2 V_{CC}$	V	$V_{CC} = 2.0$ to 2.4 V, $I_{OL} = 0.1$ mA	2
		—	—	$0.15 V_{CC}$	V	$V_{CC} = 2.4$ to 3.6 V, $I_{OL} = 0.1$ mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	10	k Ω	$\pm I_d = 0.05$ mA, $V_{LCD} = 10$ V	4
Driver ON resistance (SEG pins)	R_{SEG}	—	3	10	k Ω	$\pm I_d = 0.05$ mA, $V_{LCD} = 10$ V	4
I/O leakage current	I_{Li}	-1	—	1	μA	$V_{in} = 0$ to V_{CC}	5
Current consumption during normal operation ($V_{CC} - \text{GND}$)	I_{OP}	—	70	100	μA	R-C oscillation, $V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$, $f_{osc} = 100$ kHz (1/120 duty)	6, 7
Current consumption during sleep mode ($V_{CC} - \text{GND}$)	I_{SL}	—	12	—	μA	R-C oscillation, $V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$, $f_{osc} = 100$ kHz (1/120 duty)	6, 7
Current consumption during standby mode ($V_{CC} - \text{GND}$)	I_{ST}	—	0.1	5	μA	$V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$	6, 7
LCD drive power supply current ($V_{LCD} - \text{GND}$)	I_{LCD}	—	28	40	μA	$V_{LCD} = 15$ V, 1/11 bias, $T_a = 25^\circ\text{C}$, $f_{osc} = 100$ kHz AP1/0 = 01, $V_{CC} = 3$ V	7
LCD drive voltage ($V_{LCD} - \text{GND}$)	V_{LCD}	5.0	—	15.5	V		8

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

HD66752

Step-up Circuit Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Two-times step-up output voltage (VLOUT pin)	V_{UP2}	4.9	5.3	5.4	V	$V_{CC} = V_{Ci} = 2.7\text{ V}$, $I_o = 30\text{ }\mu\text{A}$, $C = 1\text{ }\mu\text{F}$, $f_{osc} = 100\text{ kHz}$, $T_a = 25^\circ\text{C}$	11
Five-times step-up output voltage (VLOUT pin)	V_{UP5}	13	13.3	13.5	V	$V_{CC} = V_{Ci} = 2.7\text{ V}$, $I_o = 30\text{ }\mu\text{A}$, $C = 1\text{ }\mu\text{F}$, $f_{osc} = 100\text{ kHz}$, $T_a = 25^\circ\text{C}$	11
Six-times step-up output voltage (VLOUT pin)	V_{UP6}	12.7	12.9	13.2	V	$V_{CC} = V_{Ci} = 2.2\text{ V}$, $I_o = 30\text{ }\mu\text{A}$, $C = 1\text{ }\mu\text{F}$, $f_{osc} = 100\text{ kHz}$, $T_a = 25^\circ\text{C}$	11
Seven-times step-up output voltage (VLOUT pin)	V_{UP7}	13.9	15.1	15.4	V	$V_{CC} = V_{Ci} = 2.2\text{ V}$, $I_o = 30\text{ }\mu\text{A}$, $C = 1\text{ }\mu\text{F}$, $f_{osc} = 100\text{ kHz}$, $T_a = 25^\circ\text{C}$	11
Use range of step-up output voltages	V_{UP2} V_{UP5} V_{UP6} V_{UP7}	V_{CC}	—	15.5	V	For two- to seven-times step-up	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics ($V_{CC} = 2.0$ to 3.6 V, $T_a = -40$ to $+85^\circ\text{C}^{*1}$)
Clock Characteristics ($V_{CC} = 2.0$ to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	f _{cp}	70	100	150	kHz	$V_{CC} = 2.0$ to 3.6 V	9
External clock duty ratio	Duty	45	50	55	%	$V_{CC} = 2.0$ to 3.6 V	9
External clock rise time	trcp	—	—	0.2	μs	$V_{CC} = 2.0$ to 3.6 V	9
External clock fall time	tfcp	—	—	0.2	μs	$V_{CC} = 2.0$ to 3.6 V	9
R-C oscillation clock	f _{osc}	80	100	120	kHz	Rf = 270 kΩ, $V_{CC} = 3$ V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

($V_{CC} = 2.0$ to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t _{CYCE}	600	—	—	ns	Figure 57
	Read	t _{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW _{EH}	120	—	—	ns	Figure 57
	Read	PW _{EH}	350	—	—		
Enable low-level pulse width	Write	PW _{EL}	300	—	—	ns	Figure 57
	Read	PW _{EL}	400	—	—		
Enable rise/fall time		t _{Er} , t _{Ef}	—	—	25	ns	Figure 57
Setup time (RS, R/W to E, CS*)		t _{ASE}	50	—	—	ns	Figure 57
Address hold time		t _{AHE}	20	—	—	ns	Figure 57
Write data setup time		t _{DSWE}	60	—	—	ns	Figure 57
Write data hold time		t _{HE}	20	—	—	ns	Figure 57
Read data delay time		t _{DDRE}	—	—	300	ns	Figure 57
Read data hold time		t _{DHRE}	5	—	—	ns	Figure 57

HD66752

(V_{CC} = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t _{CYCE}	300	—	—	ns	Figure 57
	Read	t _{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW _{EH}	70	—	—	ns	Figure 57
	Read	PW _{EH}	250	—	—		
Enable low-level pulse width	Write	PW _{EL}	100	—	—	ns	Figure 57
	Read	PW _{EL}	200	—	—		
Enable rise/fall time		t _{Er} , t _{Ef}	—	—	25	ns	Figure 57
Setup time (RS, R/W to E, CS*)		t _{ASE}	50	—	—	ns	Figure 57
Address hold time		t _{AHE}	5	—	—	ns	Figure 57
Write data setup time		t _{DSWE}	60	—	—	ns	Figure 57
Write data hold time		t _{HE}	15	—	—	ns	Figure 57
Read data delay time		t _{DDRE}	—	—	200	ns	Figure 57
Read data hold time		t _{DHRE}	5	—	—	ns	Figure 57

80-system Bus Interface Timing Characteristics

(V_{CC} = 2.0 to 2.4 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write t_{CYCW}	600	—	—	ns	Figure 58
	Read t_{CYCR}	800	—	—	ns	Figure 58
Write low-level pulse width	PW_{LW}	120	—	—	ns	Figure 58
Read low-level pulse width	PW_{LR}	350	—	—	ns	Figure 58
Write high-level pulse width	PW_{HW}	300	—	—	ns	Figure 58
Read high-level pulse width	PW_{HR}	400	—	—	ns	Figure 58
Write/Read rise/fall time	t_{WRr}, WRf	—	—	25	ns	Figure 58
Setup time (RS to CS*, WR*, RD*)	t_{AS}	50	—	—	ns	Figure 58
Address hold time	t_{AH}	20	—	—	ns	Figure 58
Write data setup time	t_{DSW}	60	—	—	ns	Figure 58
Write data hold time	t_H	20	—	—	ns	Figure 58
Read data delay time	t_{DDR}	—	—	300	ns	Figure 58
Read data hold time	t_{DHR}	5	—	—	ns	Figure 58

(V_{CC} = 2.4 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write t_{CYCW}	300	—	—	ns	Figure 58
	Read t_{CYCR}	500	—	—	ns	Figure 58
Write low-level pulse width	PW_{LW}	70	—	—	ns	Figure 58
Read low-level pulse width	PW_{LR}	250	—	—	ns	Figure 58
Write high-level pulse width	PW_{HW}	100	—	—	ns	Figure 58
Read high-level pulse width	PW_{HR}	200	—	—	ns	Figure 58
Write/Read rise/fall time	t_{WRr}, WRf	—	—	25	ns	Figure 58
Setup time (RS to CS*, WR*, RD*)	t_{AS}	50	—	—	ns	Figure 58
Address hold time	t_{AH}	5	—	—	ns	Figure 58
Write data setup time	t_{DSW}	60	—	—	ns	Figure 58
Write data hold time	t_H	15	—	—	ns	Figure 58
Read data delay time	t_{DDR}	—	—	200	ns	Figure 58
Read data hold time	t_{DHR}	5	—	—	ns	Figure 58

HD66752

Reset Timing Characteristics ($V_{CC} = 2.0$ to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 59

Electrical Characteristics Notes

1. For bare die products, specified up to 85°C.
2. The following three circuits are I/O pin configurations (figure 50).

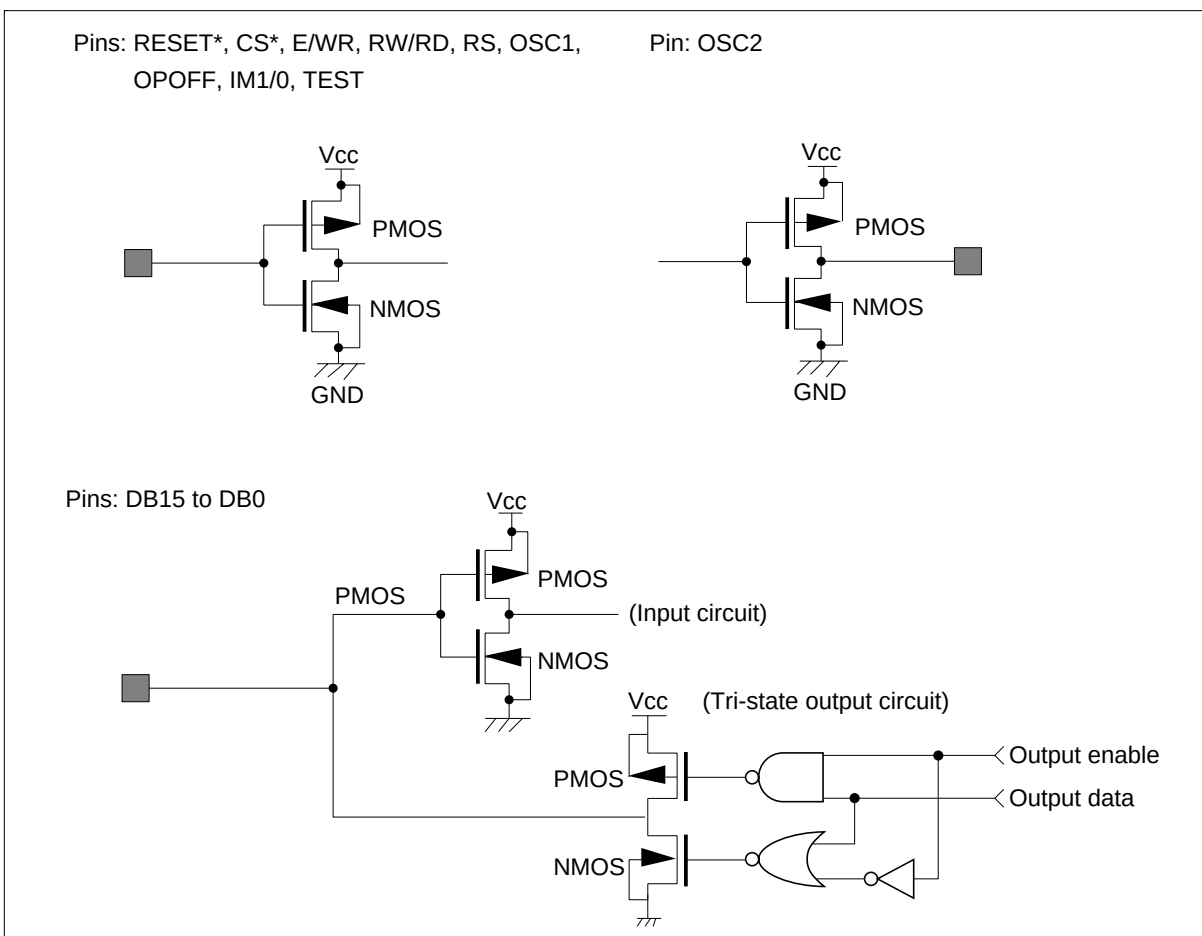


Figure 50 I/O Pin Configuration

HD66752

3. The TEST pin must be grounded and the IM1/0 and OPOFF pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.
7. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 51).

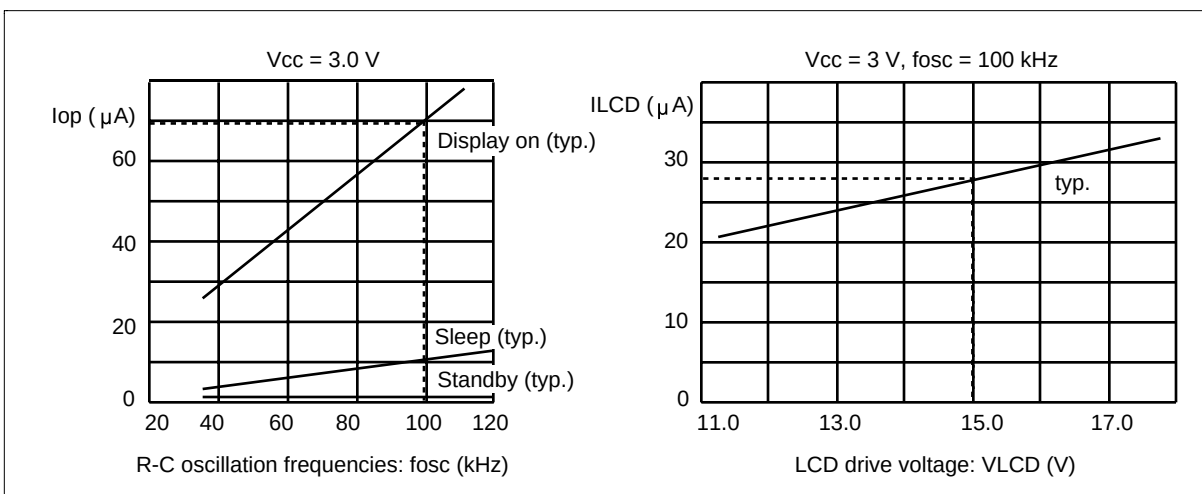


Figure 51 Relationship between the Operation Frequency and Current Consumption

8. Each COM and SEG output voltage is within ± 0.15 V of the LCD voltage (V_{cc}, V1, V2, V3, V4, V5) when there is no load.
9. Applies to the external clock input (figure 52).

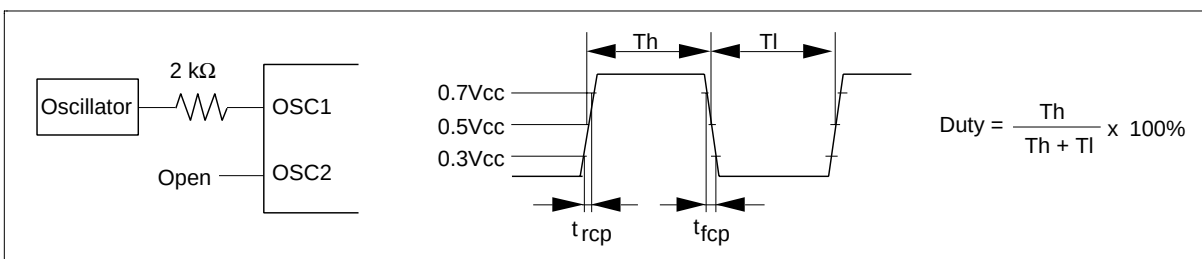


Figure 52 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor R_f (figure 53 and table 26).

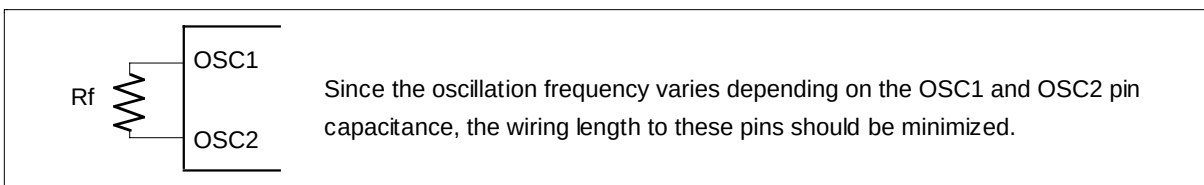


Figure 53 Internal Oscillation

Table 26 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (R_f)	R-C Oscillation Frequency: f_{osc}	
	$V_{cc} = 2.2\text{ V}$	$V_{cc} = 3.0\text{ V}$
200 k Ω	111 kHz	130 kHz
270 k Ω	86 kHz	100 kHz
300 k Ω	79 kHz	92 kHz
330 k Ω	74 kHz	86 kHz
360 k Ω	69 kHz	79 kHz
390 k Ω	64 kHz	74 kHz
430 k Ω	59 kHz	67 kHz
470 k Ω	54 kHz	61 kHz

11. The step-up characteristics test circuit is shown in figure 54.

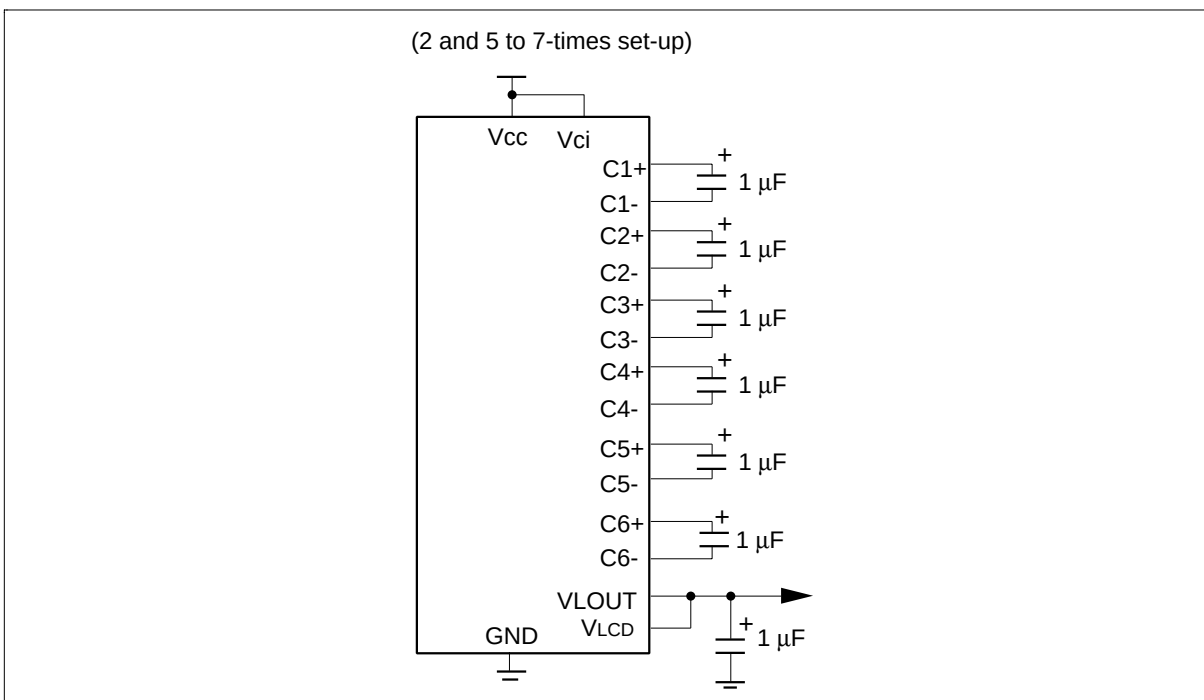
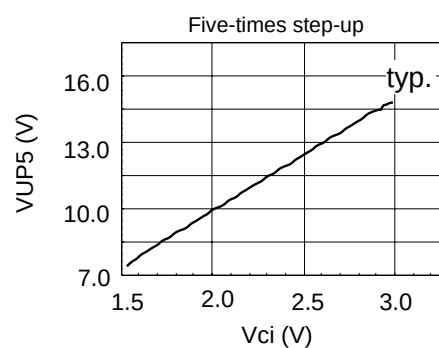


Figure 54 Step-up Characteristics Test Circuit

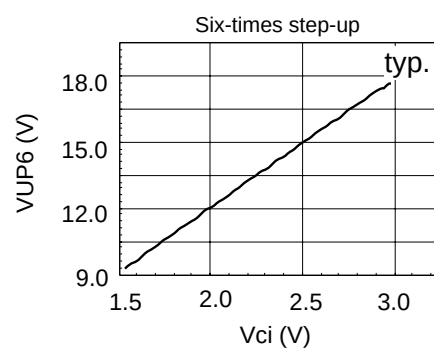
Reference data

VUP6 = VLCD - GND, VUP7 = VLCD - GND

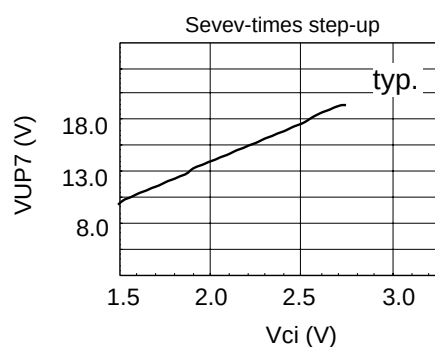
(i) Relation between the obtained voltage and input voltage



Vci = Vcc, fosc = 100 kHz, Ta = 25°C, DC1 to 0 = 00



Vci = Vcc, fosc = 100 kHz, Ta = 25°C, DC1 to 0 = 00



Vci = Vcc, fosc = 100 kHz, Ta = 25°C, DC1 to 0 = 00

Figure 55 Step-up

(ii) Relation between the obtained voltage and temperature

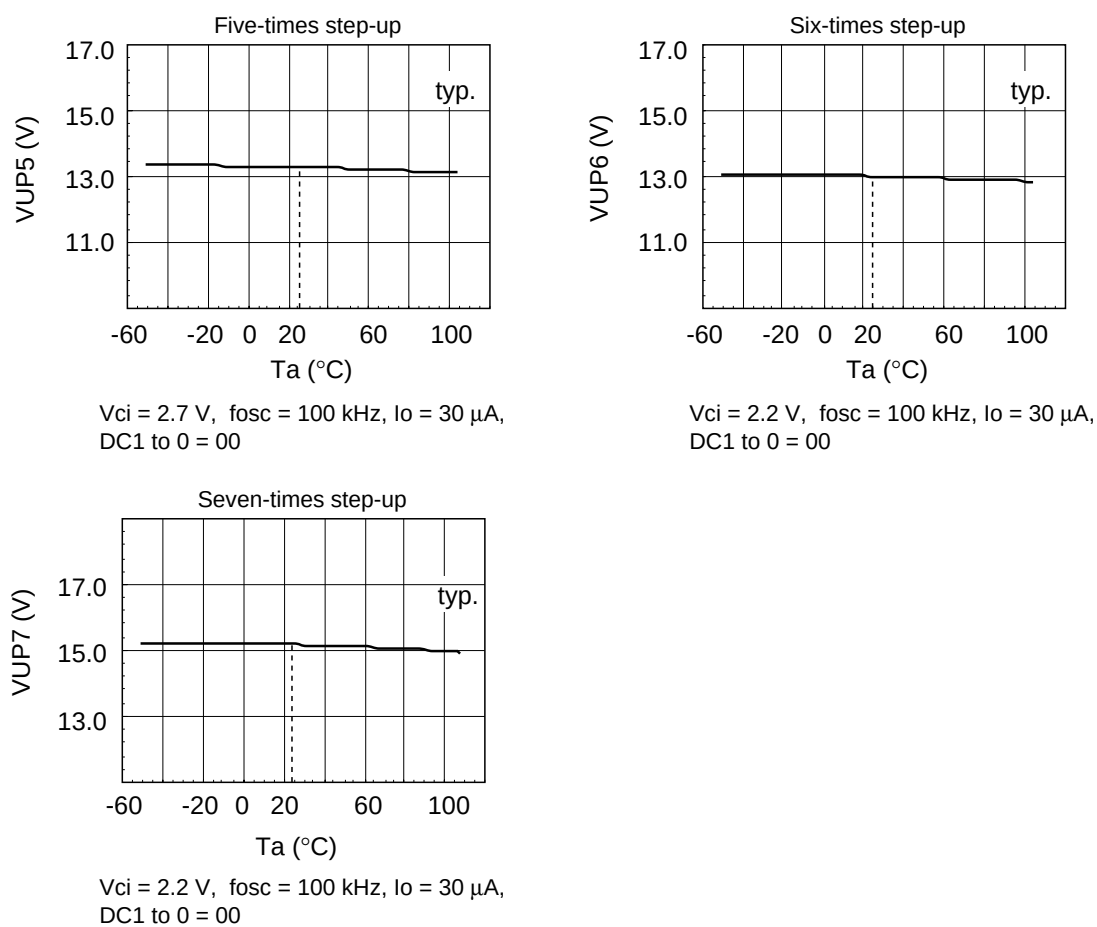


Figure 55 Step-up (cont)

(iii) Relation between the obtained voltage and capacity

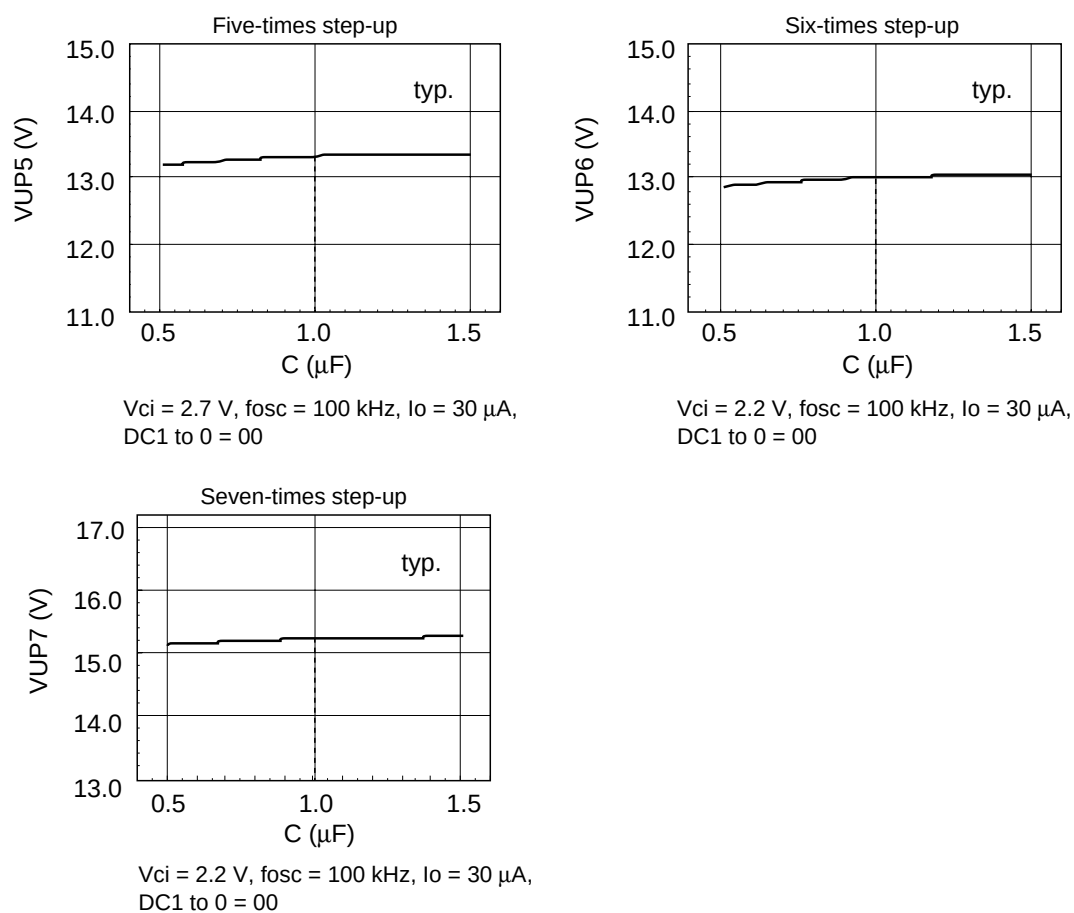


Figure 55 Step-up (cont)

(iv) Relation between the obtained voltage and current

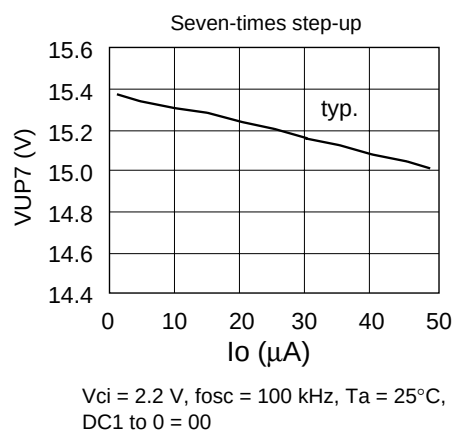
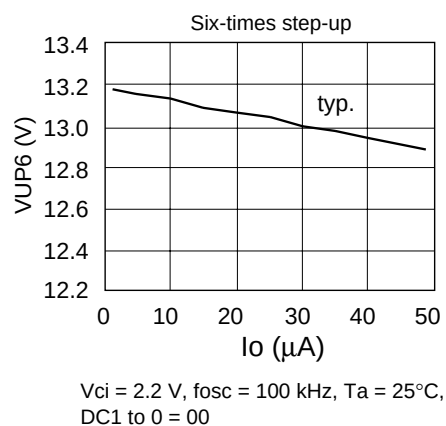
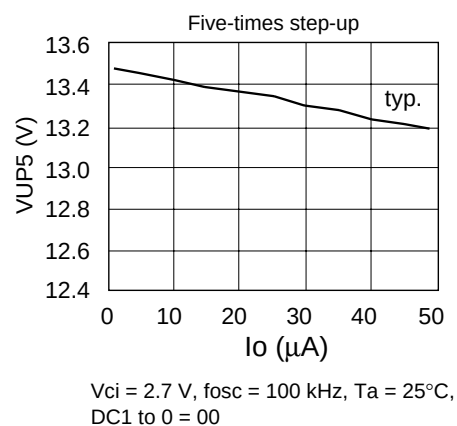


Figure 55 Step-up (cont)

Load Circuits

AC Characteristics Test Load Circuits

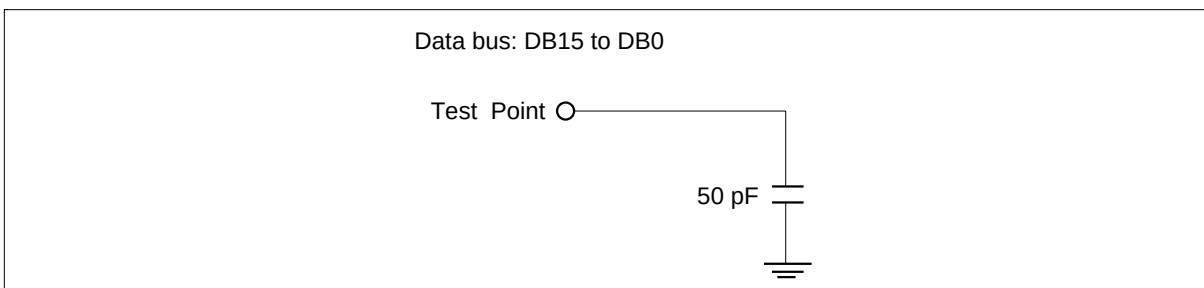


Figure 56 Load Circuit

Timing Characteristics

68-system Bus Operation

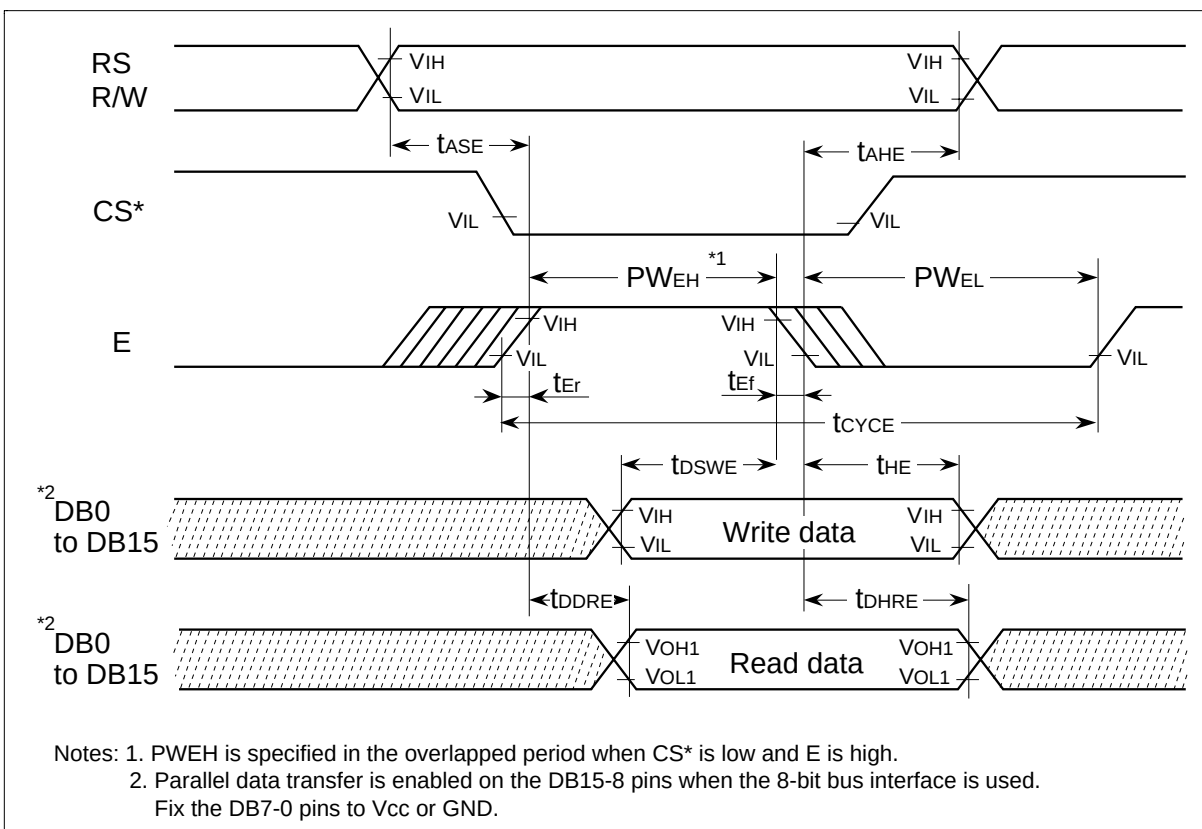


Figure 57 68-system Bus Timing

HD66752

80-system Bus Operation

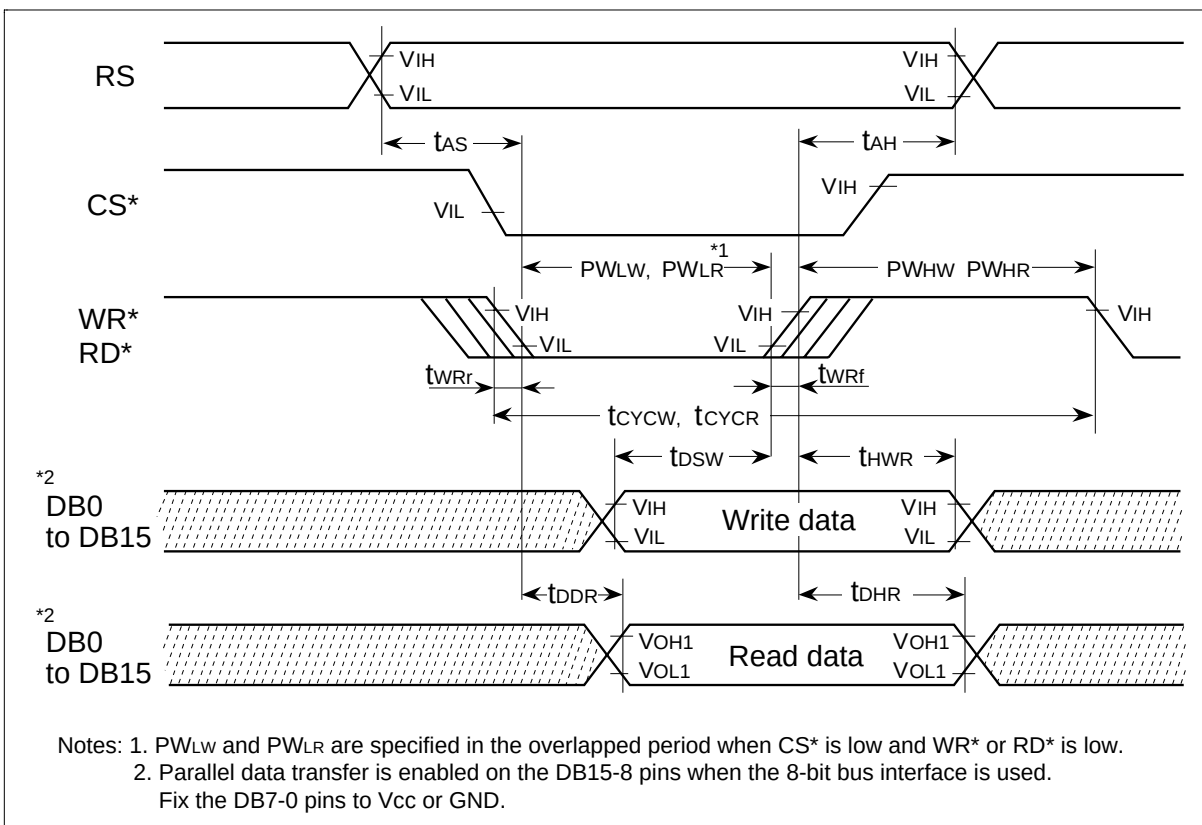


Figure 58 80-system Bus Timing

Reset Operation

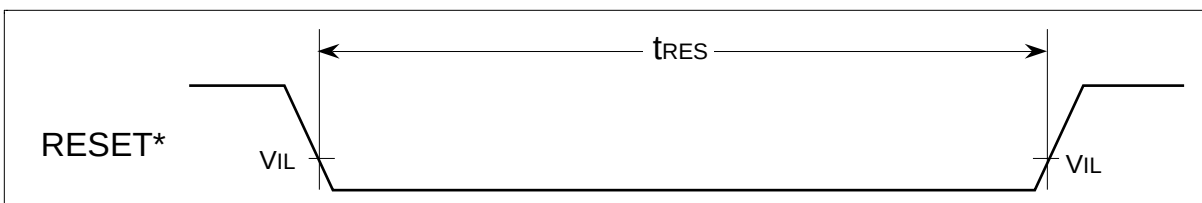


Figure 59 Reset Timing

Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

Power-on Sequence

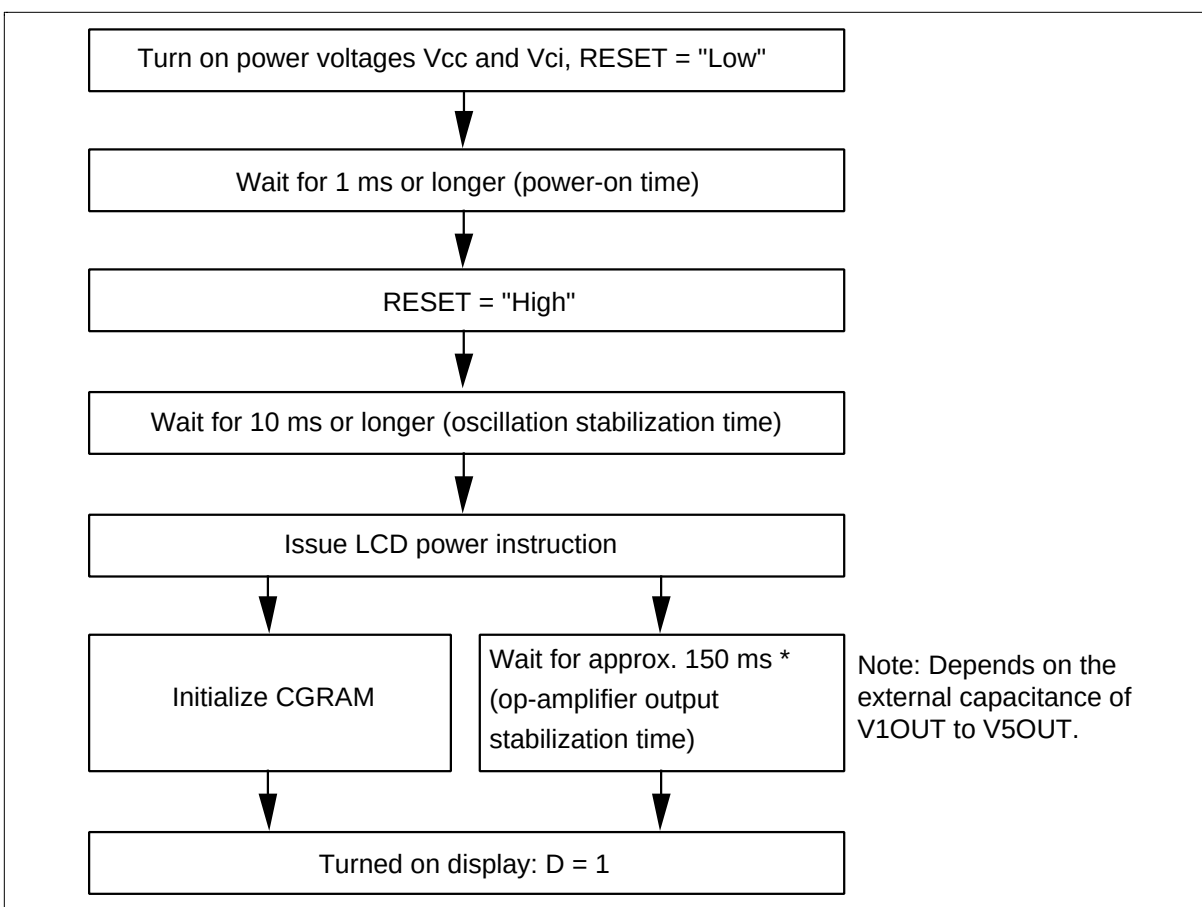


Figure 60 Power-on Sequence

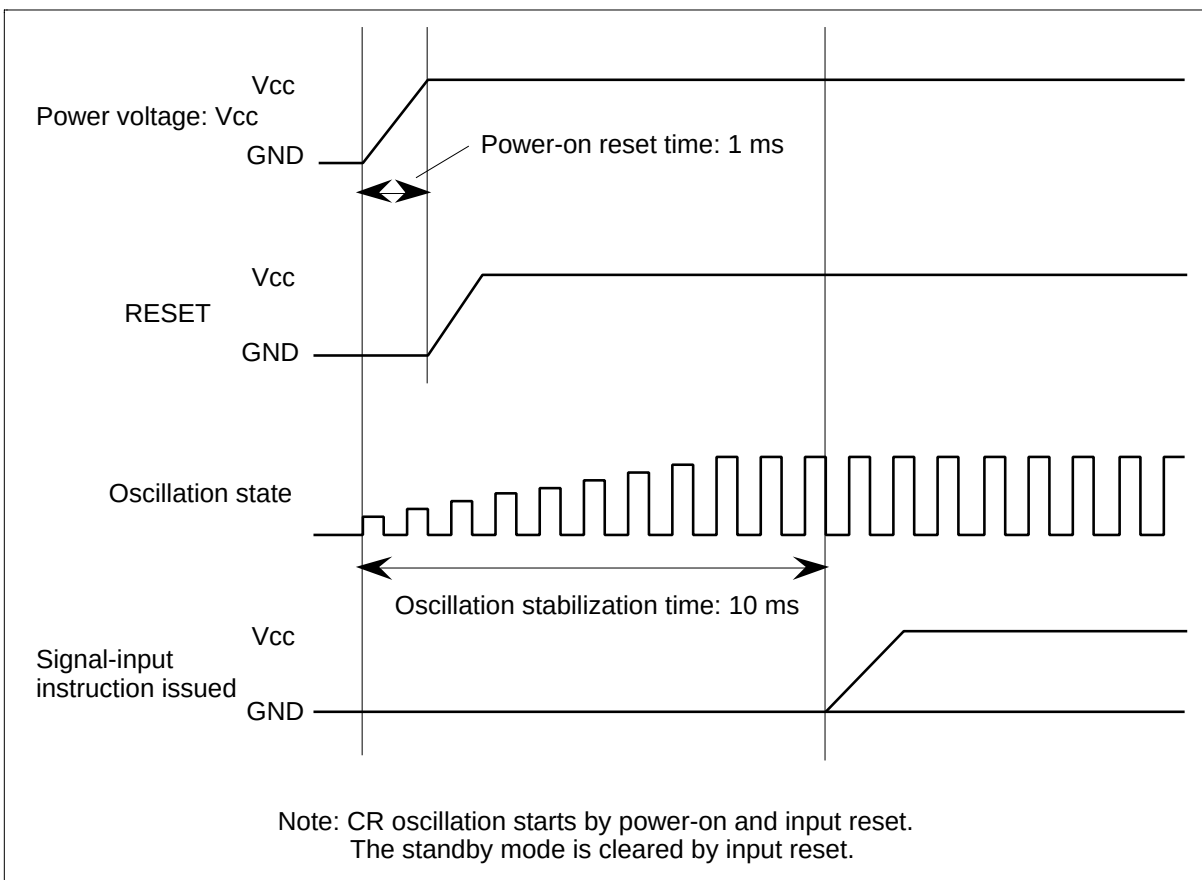
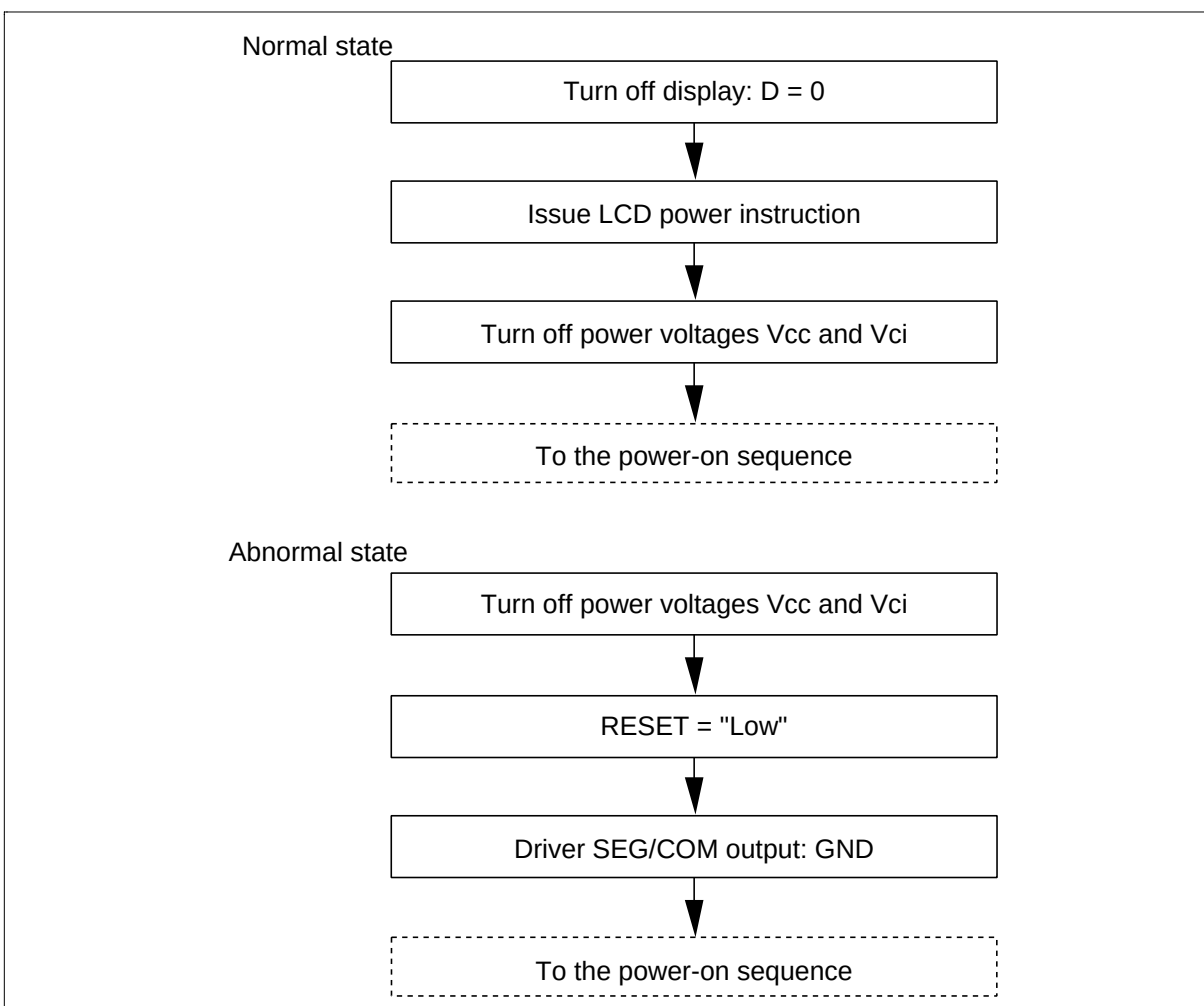


Figure 61 Power-on Timing

Power-off Sequence**Figure 62 Power-off Sequence**

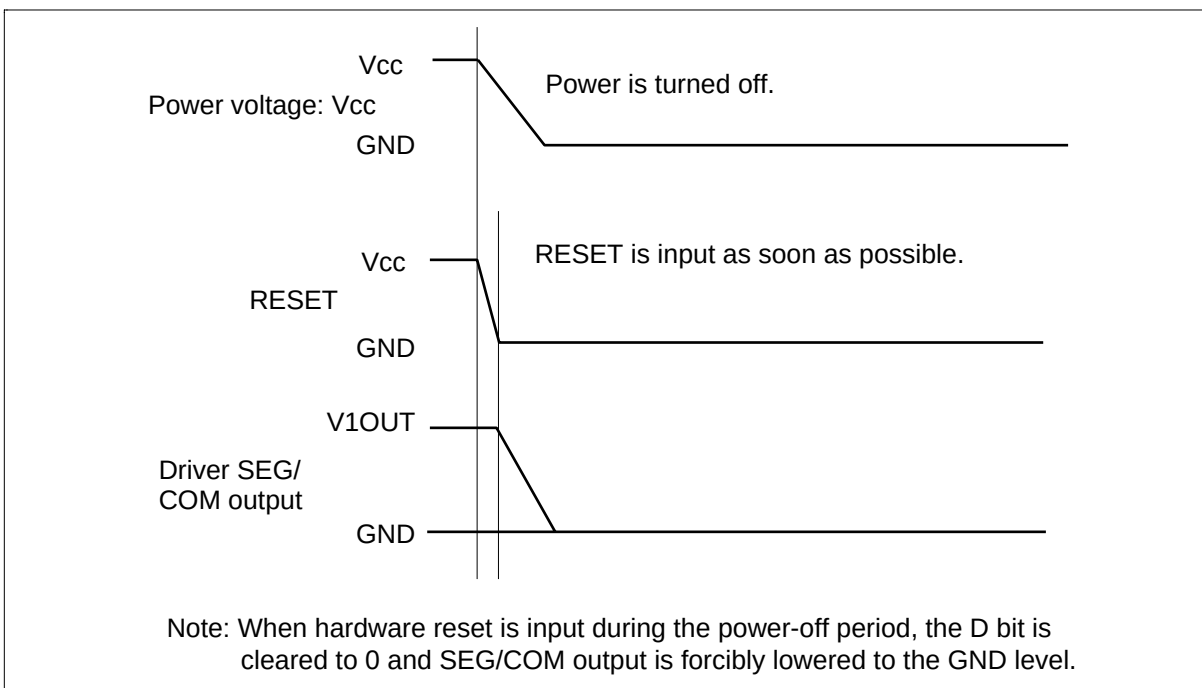


Figure 63 Power-off Timing

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