# Am9301

## Demultiplexer/One-of-Ten Decoder

**Distinctive Characteristics:**

- 22 ns typical propagation delay
- Does not respond to codes above 9
- 100% reliability assurance testing in compliance with MIL-STD-883
- Can be used as one-of-eight decoder with active LOW enable

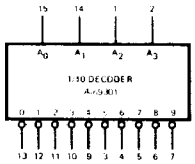
### FUNCTIONAL DESCRIPTION

The Am9301 Demultiplexer/One-of-Ten Decoder accepts four active High BCD inputs and selects one-of-ten mutually exclusive active LOW outputs as shown in Truth Table II. The logic design of the 9301 insures that all outputs are HIGH (unselected) when binary codes greater than nine are applied to the inputs. The inputs $A_0$, $A_1$, $A_2$, and $A_3$ of the 9301 correspond to the respective binary weight of $2^0$, $2^1$, $2^2$, and $2^3$.

Incoming data on input $A_3$ can be demultiplexed to either of the eight outputs, zero through seven, with binary addressing at inputs $A_0$, $A_1$, and $A_2$. This demultiplexing capability is illustrated in figure 5.

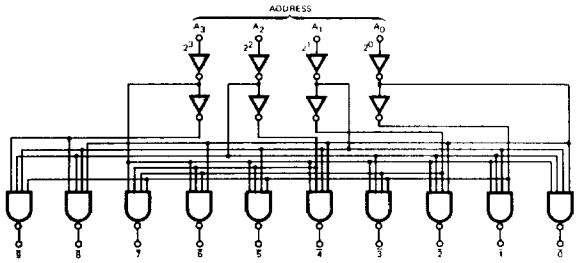
The most significant input, $A_3$, produces an inhibit function when the 9301 is used as a 1-of-8 decoder with binary addressing at inputs $A_0$, $A_1$, and $A_2$. The 1-of-32 decoder, in figure 6 illustrates the inhibit function.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
Gnd = Pin 8

### LOGIC DIAGRAM



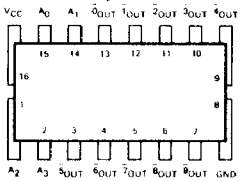

### Am9301 ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-pin Molded DIP | 0°C to +75°C | U9M930159X |
| 16-pin Hermetic DIP | 0°C to +75°C | U7B930159X |
| 16-pin Hermetic DIP | −55°C to +125°C | U7B930151X |
| 16-pin Hermetic Flat Pak | −55°C to +125°C | U4L930151X |
| Dice | Note | UXX9301XXD |

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

### CONNECTION DIAGRAM

**Top View**




NOTE: PIN 1 is marked for orientation.

**MAXIMUM RATI** (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max |
| DC Input Voltage | −0.5 V to +5.5 V |
| Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

930159X $T_A$ = 0°C to +75°C $V_{CC}$ = 5.0 V ±5%
930151X $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0 V ±10%

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −0.8 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | 3.6 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 16.0 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $I_{IL}$ (Note 2) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | −1.0 | −1.6 | mA |
| $I_{IH}$ (Note 2) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.4 V | | | 6.0 | 40 | μA |
| | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −20 | | −70 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | 930151X | | 27 | 44 | mA |
| | | | 930159X | | 27 | 42 | |

Notes: 1) Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

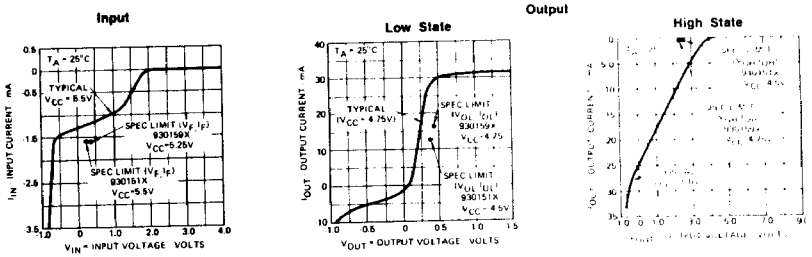
## Switching Characteristics (+25°C)

| Parameters | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd+}$ | Turn Off Delay | $V_{CC}$ = 5.0, $C_L$ = 15 pF | 10 | 23 | 35 | ns |
| $t_{pd-}$ | Turn On Delay | Refer to figure 4. | 10 | 20 | 30 | ns |

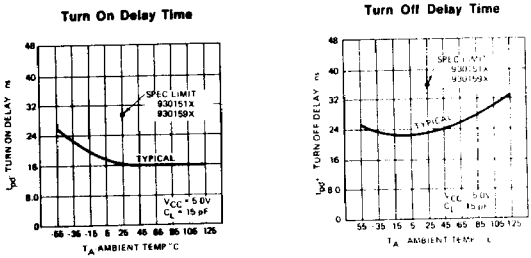
Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.

## PERFORMANCE CURVES

### Input/Output Characteristics




### Switching Characteristics




## DEFINITION OF TERMS

**SUBSCRIPT TERMS:**

**H** HIGH, applying to a HIGH-signal level or when used with $V_{CC}$ to indicate high $V_{CC}$ value.

**I** Input.

**L** LOW, applying to a LOW signal level or when used with $V_{CC}$ to indicate low $V_{CC}$ value.

**O** Output.

**FUNCTIONAL TERMS:**

**BCD** Binary coded decimal notation represents each of the ten decimal digits by a code consisting of a group of four (4) binary digits.

**Decoder/Demultiplexer** On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

**Fan-Out** The logic HIGH or LOW output drive capability in terms of input Unit Loads.

**Unit load** One T²L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to −1.6mA at 0.4V.

**OPERATIONAL TERMS:**

$I_{OH}$ Output HIGH current, forced out of output in $V_{OH}$ test.

$I_{OL}$ Output LOW current, forced into output in $V_{OL}$ test.

$I_{CC}$ The current drawn by the device under a +5.0 V power supply, bias input terminals grounded and output terminals open.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

$V_{IH}$ Minimum logic HIGH input voltage.

$V_{IL}$ Maximum logic LOW input voltage.

$V_{OH}$ Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

$V_{OL}$ Maximum logic LOW output voltage with output LOW current $I_{OL}$ into output.

**SWITCHING TERMS:** (All switching times are measured at the 1.5V logic level).

$t_{pd+}$ The propagation delay measured from the input address transition to a corresponding output signal LOW-HIGH transition.

$t_{pd-}$ The propagation delay measured from the input address transition to a corresponding output signal HIGH-LOW transition.

## MSI INTERFACING RULES

| Interfacing Digital Family | Equivalent Input Unit Load HIGH | LOW |
|---|---|---|
| Advanced Micro Devices 9300/2500 Series | 1 | 1 |
| FSC Series 9300 | 1 | 1 |
| Advanced Micro Devices 54/7400 Series | 1 | 1 |
| TI Series 54/7400 | 1 | 1 |
| Signetics Series 8200 | 2 | 2 |
| National Series DM 75/85 | 1 | 1 |
| DTL Series 930 | 12 | 1 |

## TRUTH TABLE

| INPUTS | | | | OUTPUTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $\overline{0}$ | $\overline{1}$ | $\overline{2}$ | $\overline{3}$ | $\overline{4}$ | $\overline{5}$ | $\overline{6}$ | $\overline{7}$ | $\overline{8}$ | $\overline{9}$ |
| L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | H | H | H | H | H | H |
| L | H | L | L | H | H | L | H | H | H | H | H | H | H |
| H | H | L | L | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | H | H | H | L | H | H | H | H | H |
| H | L | H | L | H | H | H | H | H | L | H | H | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| H | H | H | L | H | H | H | H | H | H | H | L | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| L | H | L | H | H | H | H | H | H | H | H | H | H | H |
| H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H | H | H |

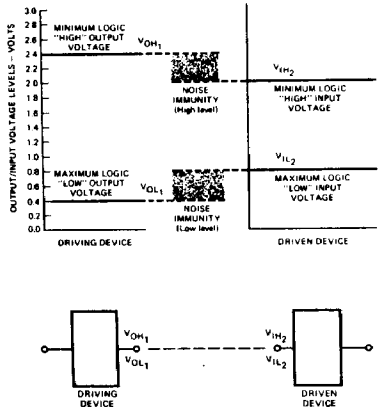
H = HIGH Logic Level
L = LOW Logic Level

## LOADING RULES

| Input/Output | Pin No.'s | Input Unit Load | Fanout Output HIGH | Fanout Output LOW |
|---|---|---|---|---|
| $A_2$ | 1 | 1 | — | — |
| $A_3$ | 2 | 1 | — | — |
| $\overline{5}_{OUT}$ | 3 | — | 20 | 10 |
| $\overline{6}_{OUT}$ | 4 | — | 20 | 10 |
| $\overline{7}_{OUT}$ | 5 | — | 20 | 10 |
| $\overline{8}_{OUT}$ | 6 | — | 20 | 10 |
| $\overline{9}_{OUT}$ | 7 | — | 20 | 10 |
| GND | 8 | — | — | — |
| $\overline{4}_{OUT}$ | 9 | — | 20 | 10 |
| $\overline{3}_{OUT}$ | 10 | — | 20 | 10 |
| $\overline{2}_{OUT}$ | 11 | — | 20 | 10 |
| $\overline{1}_{OUT}$ | 12 | — | 20 | 10 |
| $\overline{0}_{OUT}$ | 13 | — | 20 | 10 |
| $A_1$ | 14 | 1 | — | — |
| $A_0$ | 15 | 1 | — | — |
| $V_{CC}$ | 16 | — | — | — |

## INPUT/OUTPUT INTERFACE CONDITIONS

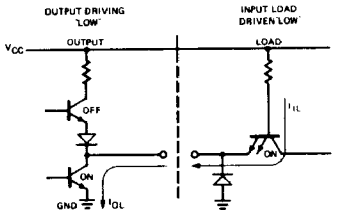
### Voltage Interface Conditions — LOW & HIGH



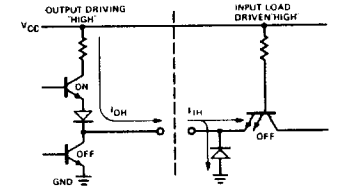




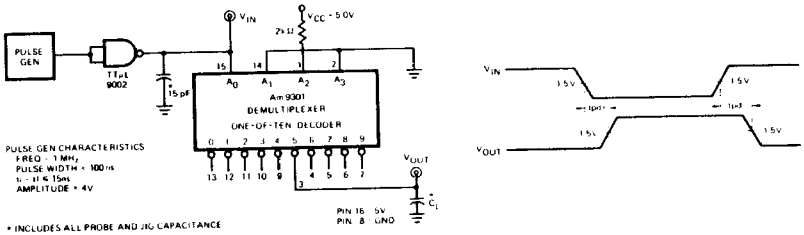
### Current Interface Conditions — LOW




### Current Interface Conditions — HIGH

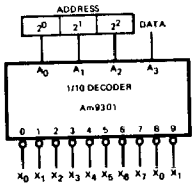


## SWITCHING TIME TEST CIRCUITS & WAVEFORMS




## BASIC DEMULTIPLEXER/DECODER APPLICATIONS

### DIGITAL DEMULTIPLEXER




| ADDRESS $A_0$ $A_1$ $A_2$ | OUTPUT LINE |
|---|---|
| 0 0 0 | 0 |
| 1 0 0 | 1 |
| 0 1 0 | 2 |
| 1 1 0 | 3 |
| 0 0 1 | 4 |
| 1 0 1 | 5 |
| 0 1 1 | 6 |
| 1 1 1 | 7 |

Data may be routed from a source to any of eight (0-7) outputs by addressing that output. The seven non-addressed outputs remain clear.

Figure 5

## ADDITIONAL APPLICATIONS

### ONE-OUT-OF-THIRTY-TWO DECODER

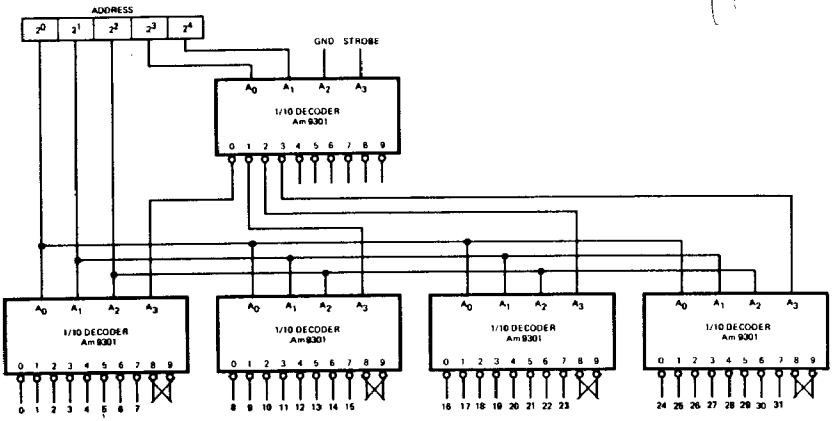
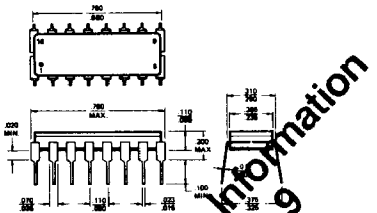



Figure 6

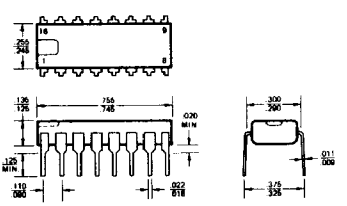
## PHYSICAL DIMENSIONS

### Dual-In-Line

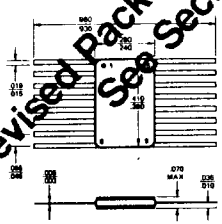
**Hermetic**



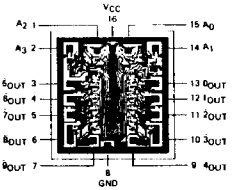
**Molded**



**Flat Package**



**Metallization and Pad Layout**




75 x 78 Mils



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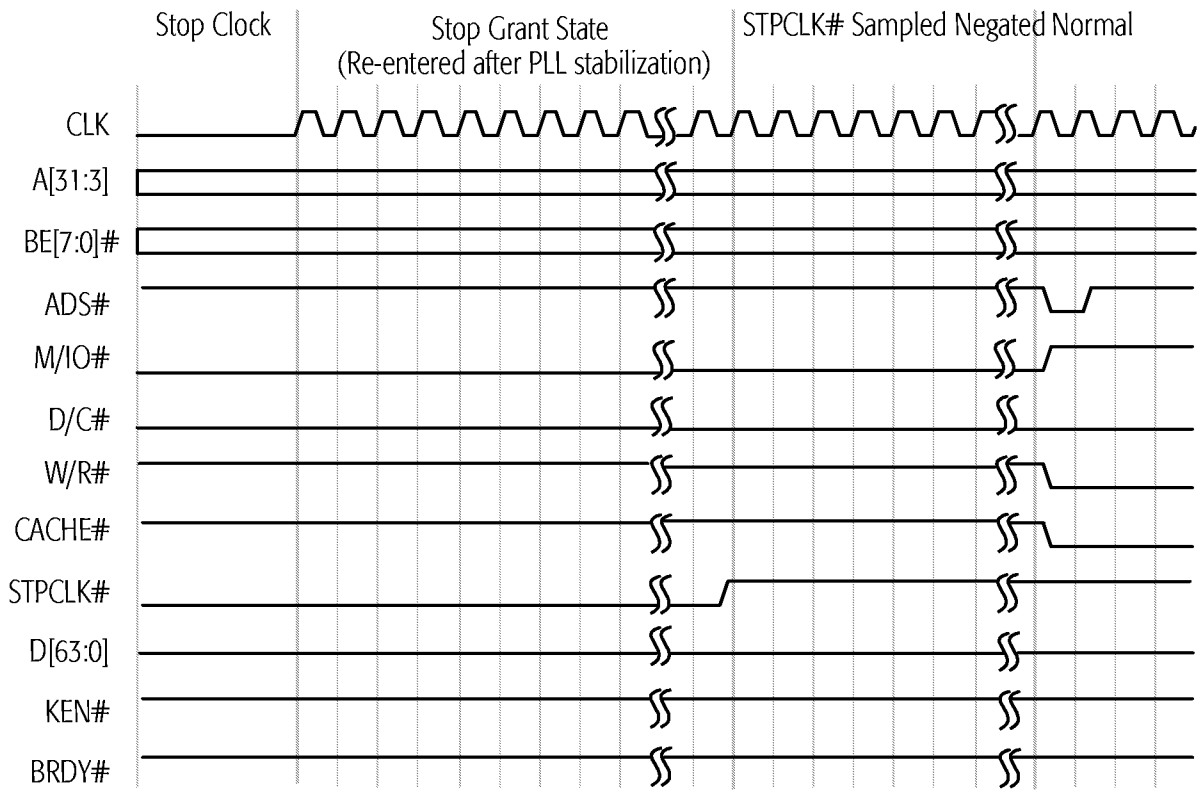


**Figure 75. Stop Grant and Stop Clock Modes, Part 2**

### INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

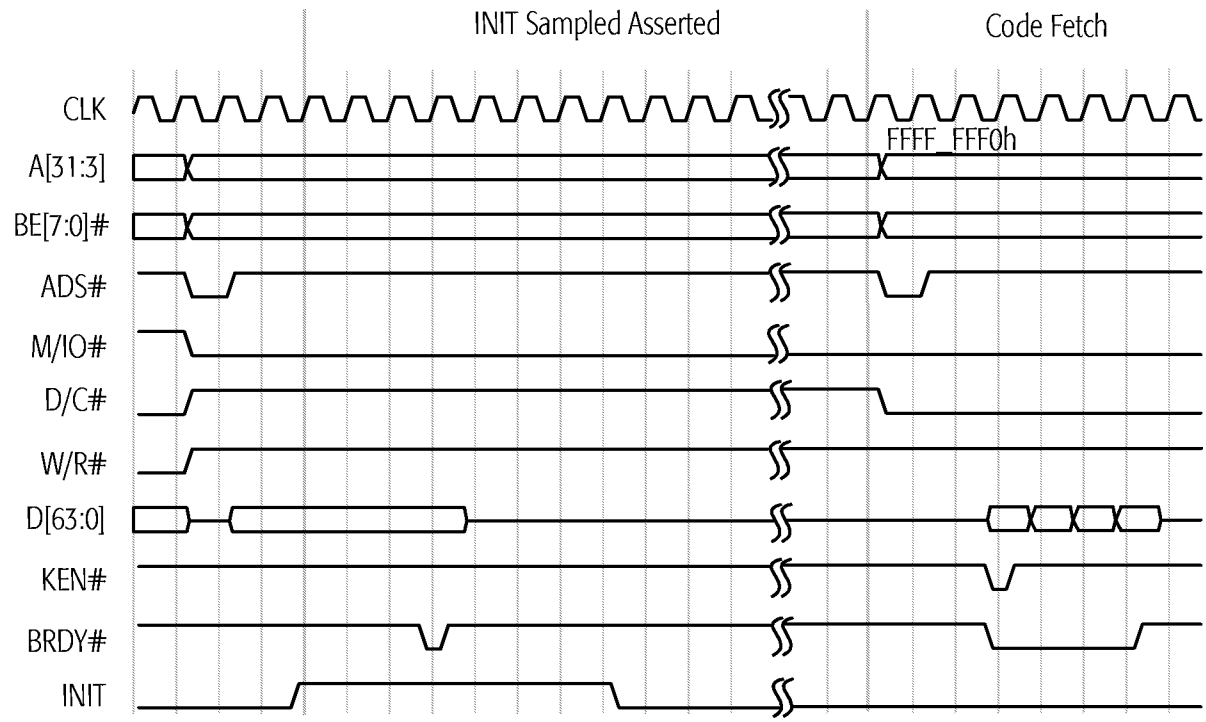


**Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode**

# 6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

## 6.1 Signals Sampled During the Falling Transition of RESET

**FLUSH#** FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

**BF[2:0]** The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

**BRDYC#** BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

## 6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and $V_{CC}$ reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for $V_{CC}$ specifications.)

During a warm reset while CLK and $V_{CC}$ are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

## 6.3 State of Processor After RESET

### Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

**Table 31. Output Signal State After RESET**

| Signal | State | Signal | State |
|---|---|---|---|
| A[31:3], AP | Floating | LOCK# | High |
| ADS#, ADSC# | High | M/IO# | Low |
| APCHK# | High | PCD | Low |
| BE[7:0]# | Floating | PCHK# | High |
| BREQ | Low | PWT | Low |
| CACHE# | High | SCYC | Low |
| D/C# | Low | SMIACT# | High |
| D[63:0], DP[7:0] | Floating | TDO | Floating |
| FERR# | High | VCC2DET | Low |
| HIT# | High | VCC2H/L# | Low |
| HITM# | High | W/R# | Low |
| HLDA | Low | – | – |

### Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.