VSC8486
10 Gbps XAUI or XGMII to XFI LAN/WAN Transceiver

Datasheet

Advance Product Information
Subject to Change

VMDS-10257
Revision 2.1
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Confidential

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 2.1

Revision 2.1 of this datasheet was published in May 2008. The following is a summary of the changes implemented in the datasheet:

- The pin diagram was corrected to show all pins of the VSC8486 device. For more information, see "Pin Diagram," page 228.
- Theta JB thermal specifications were added. For more information, see "Thermal Specifications," page 246.

Revision 2.0

Revision 2.0 of this datasheet was published in March 2008. This was the first publication of the document.

1 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the 10 Gbps XAUI or XGMII to XFI LAN/WAN transceiver.

In addition to datasheets, the Vitesse Web site offers an extensive library of documentation, support files, and application materials specific to each device. The address of the Vitesse Web site is www.vitesse.com.

1.1 Symbols and Operators

Refer to the following table for definitions of the symbols used in this datasheet.

Table 1. Symbol Definitions

Symbol	Definition
+	Addition or, in the context of a logical operation, inclusive OR
–	Subtraction or negative value
=	Equal
/	Division
×	Multiplication
X	Value doesn’t matter
‘H or 0x	Hexadecimal value
‘ ’ or ‘b	Binary value
:	Concatenation, such as 0:3 to indicate 0, 1, 2, and 3
lsb or LSB	Least significant bit or byte
LSW	Least significant word
msb or MSB	Most significant bit or byte
MSW	Most significant word
P/N	Both positive and negative signals (for example, REFCLKP/N)

1.2 Logic Conventions

The following conventions are used to describe boolean states.

Table 2. Boolean States

Term Used in Datasheet	Boolean State
1	True
0	False
High	True
Low	False
Set or assert	True
Clear or de-assert	False

1.3 Register and Bit Conventions

Registers are referenced by their device, address, and bit number. The device and address are in hexadecimal notation and the bit number is in decimal notation. A range of bits is indicated with a colon. For example, a reference to device 1, address 8, bits 15 through 14 is shown as 1x0008.15:14.

Bit numbering follows the IEEE standard with bit 7 being the most significant bit and bit 0 being the least significant bit. However, where this document uses SONET/SDH nomenclature, bit positions are numbered 1 to 8 with bit 1 being the most significant bit and 8 being the least significant bit.

2 Product Overview

The VSC8486 is a LAN/WAN XAUI or XGMII transceiver that converts 3 Gbps XAUI data to a 10 Gbps serial stream. At just 750 mW, the VSC8486 is ideal for applications requiring low power. The device is also equipped with an additional full-rate data port that can be utilized for bypass monitoring or channel monitoring applications. The device meets all specifications for 10 Gigabit Ethernet (GbE) Layer-1 processing, as defined in IEEE 802.3ae.

The VSC8486 offers exceptional 10 Gbps mixed-signal performance with a data output that features programmable pre-emphasis to enable longer traces of copper. The VSC8486 high-speed serial I/O supports 9.9 Gbps, 10.3 Gbps, and 10.5 Gbps, as defined by IEEE 802.3ae and T11 10 GFC, and is fully compliant with the SONET jitter specification defined by Bellcore GR253.

There are four main data processing blocks in the device: XGXS, PCS, WIS, and PMA. The 10 GbE extender sublayer (XGXS) accepts 8b/10b data running at 3.125 Gbps and decodes it for transmission to the physical coding sublayer (PCS). The XGXS is capable of deskewing more than 60 bit times between lanes. The PCS receives data from the XGXS at 10 Gbps and encodes data according to the 64b/66b algorithm described in IEEE 802.3ae clause 49.

The PCS features an optional extended mode (E-PCS) that also runs at the 64b/66b rate. This extended mode uses an alternative framing algorithm that adds forward error correction (FEC) to provide ~2.5 dB of net electrical coding gain. The E-PCS is available for LAN mode but not WAN mode.

The PCS outputs data to the WAN interface sublayer (WIS) when this mode is active (it is bypassed in LAN mode). The WIS optionally takes data from the PCS at 9.953 Gbps and frames data in a SONET STS-192c frame, as described in IEEE 802.3ae clause 50. Additionally, the WIS block contains extended SONET and SDH processing capabilities that allow system operators to leverage valuable performance monitoring data. Finally, data is delivered to the physical media attachment (PMA) block. The PMA multiplexes the internal parallel data bus into a 10 Gbps data stream.

The 10 Gbps to XAUI data channel performs the operations described above in reverse. Notable features in this path are a SONET-compliant LOS detector and a 10 Gbps receiver that is fully compliant with XFI specifications, including stressed eye criteria.

The device operates using a 1.2 V supply dissipating only 700 mW in LAN mode and 750 mW in WAN mode. The VSC8486 is available in standard and lead(Pb)-free (second-level interconnect only) packages, measuring 17 mm × 17 mm with 256 pins and 1.0 mm pin pitch.

2.1 Features

The following list provides the features and benefits of the VSC8486 device.

Low power

- Exceptionally low power (700 mW LAN mode or 750 mW WAN mode) allows for higher port densities

Wide range of support

- Fully compatible with IEEE 802.3ae and T11 10 GFC
- Extended-WIS (E-WIS) provides full Clause 50 support and enables transport over existing SONET networks
- 10 Gbps serial interface exceeds all SONET and 10 GbE requirements
- 4 x 3.125 Gbps and 3.182 Gbps XAUI I/O enable interconnection with a wide range of Layer-2 devices
- Seamless connectivity to XFP and SFP+ modules

Tools for rapid design

- Multiple loopback modes and built-in self test (BIST) capabilities reduce system development costs, enable manufacturing tests, and improve time to market
- JTAG access port facilitates boundary scan for in-circuit test to improve board yield
- Single 1.2 voltage for the whole device with optional power supply range (1.2 V, 1.5 V, 1.8 V, or 3.3 V) for the TTL interface

Flexibility

- XAUI I/O programmability for lane swap, invert, amplitude, pre-emphasis, and equalization
- KX4-compatible 3 Gbps I/O for long-reach copper interconnect provides additional margin to traverse connectors and the backplane up to 40 inches
- Extended-PCS (E-PCS) mode with forward error correction (FEC) auto-negotiation allows extended reach over single-mode and multimode fiber with 10^{-15} error floor
- On the 10-gigabit serial link, enhanced de-emphasis and equalization compensates for connector and channel losses and makes the device SFP+ compatible
- Accessibility of the recovered clock from high speed input and separate clock paths for CMU and CRU enable Layer 1 support for Synchronous Ethernet
- XGMII interface enables the device to be used in a roll-over redundant link application to provide fault tolerance

3 Functional Descriptions

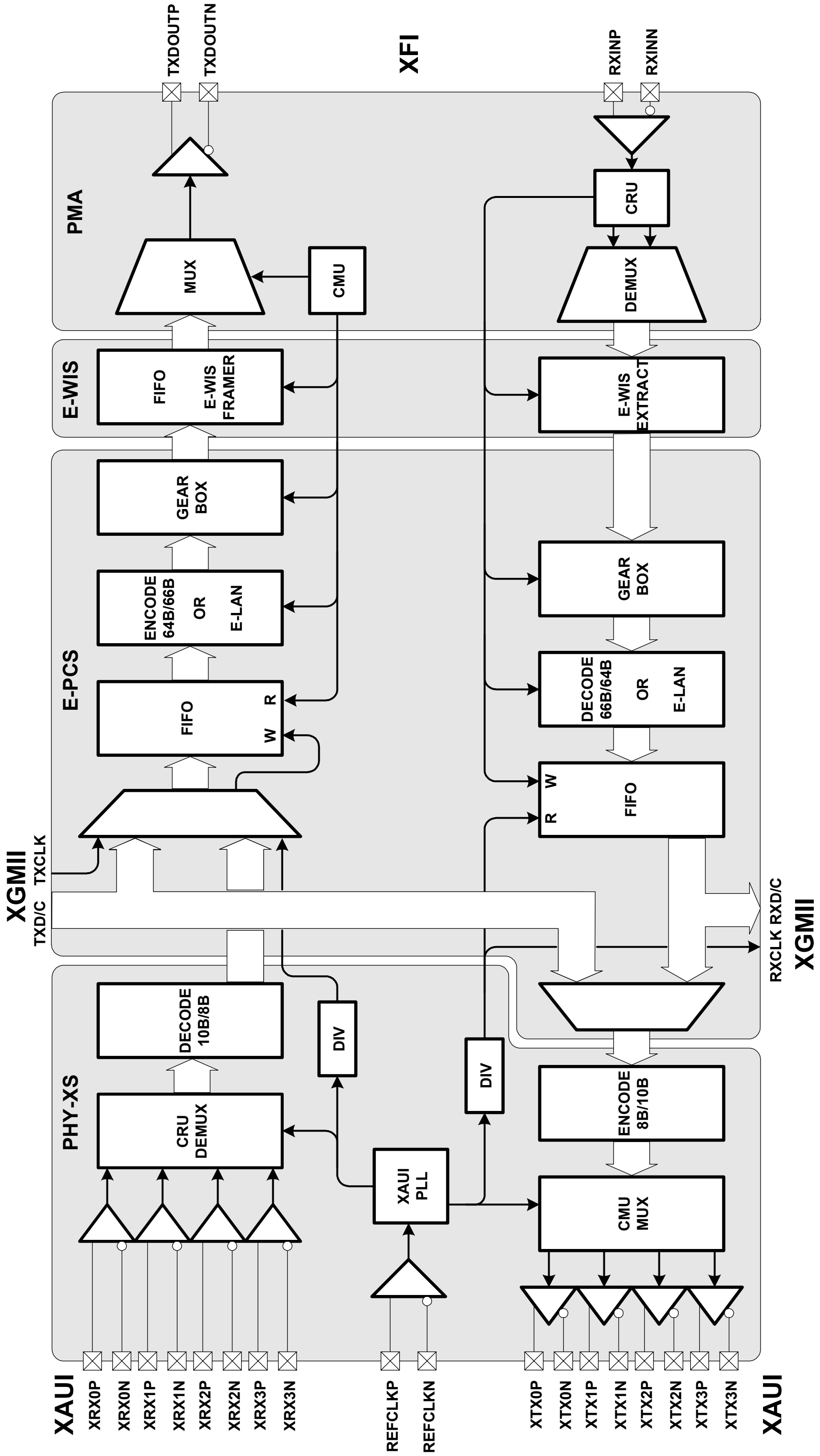
This section presents the functional description for the VSC8486 device. The main areas described are:

- Data paths
- Loopback options
- Implementation of the IEEE MDIO manageable devices (MMDs)
- Extended functionality for WIS and PCS
- Low-speed serial interfaces (MDIO, STW, and JTAG)

3.1 Operating Modes

The following figure summarizes the VSC8486 operations.

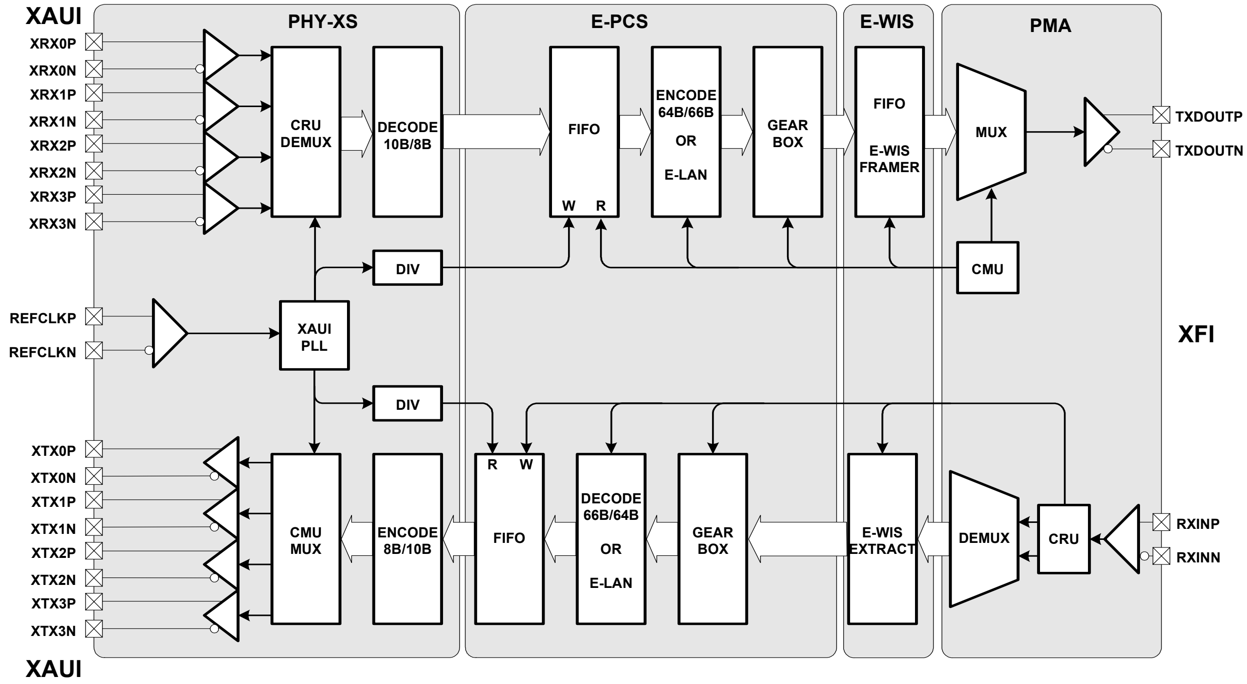
Figure 1. Functional Block Diagram



3.1.1 XAUI to XFI Mode

To put the VSC8486 in the XAUI to XFI mode, set the I/O mode select pin high (IOMODESEL = 1). IOMODESEL sets the default value of XGMII_OE (3x8005.6) and PCS_XGMII_SRC (3x8005.8).

Figure 2. Functions in XAUI to XFI Mode



Transmit Operation for XAUI to XFI Mode As shown in the preceding figure, the PHY XS block receives four 8b/10b encoded 3.125 Gbps (3.1875 Gbps in SAN mode) data lanes on pins XRX[3:0]P/N. The clock is recovered and the data is deserialized on each of the four lanes. Synchronization is performed before the data is passed into the 10b/8b decoders. The decoded data and accompanying control bits are then presented to the FIFO. The FIFO deskews the four lanes and presents the aligned data to the PCS.

The FIFO within the PCS transfers path timing from the PHY XS recovered clock to the PMA transmit clock by adding or deleting idle characters during inter-packet gaps (IPG) as needed. The eight data octets (8-bit characters) and eight control bits pass through the 64b/66b encoder, which maps XGMII data to a single 66-bit transmission block, as defined in Figure 49-7 of IEEE Standard 802.3ae.

In standard PCS mode (EPCS = 0), the first two bits of the 66-bit block contain the sync header, which is used to establish block boundaries for the synchronization process during the receive operation. The remaining 64 bits contain the payload. The payload passes through the scrambler, which implements the polynomial $G(x) = 1 + x^{39} + x^{58}$. The sync header bypasses the scrambler, and joins the scrambled payload at the 64:66 gearbox. The gearbox adapts between the 66-bit width of the blocks and the 64-bit width of the PMA or WIS interface.

In extended PCS mode (EPCS = 1), the 64 payload bits are mapped such that 24 instances of the 64-bit payloads are placed into a larger 1584-bit frame defined by the

Optical Internetworking Forum (OIF) Common Electrical I/O Protocol (CEI-P). Each 64-bit payload is preceded by one transcoding bit, and the remaining 24 bits of the 1584-bit frame are used for synchronization, fire code parity check, supervisory channel, and to indicate the link state. This frame is then scrambled with a free-running linear feedback shift register (LFSR) scrambler with a characteristic polynomial $G(x) = x^{17} + x^{14} + 1$. The scrambled frame then passes through the 64:66 gearbox to the PMA or WIS.

In LAN or SAN mode (WAN_STAT = 0), the PCS data is passed directly to the PMA, while in WAN mode (WAN_STAT = 1), the PCS data is passed to the WIS. The WIS inserts the PCS data into SONET STS-192c/SDH STM-64 frames, and adds the required overhead.

Within the PMA, the data is serialized into the high-speed data stream (10.3125 Gbps in LAN mode, 10.51875 Gbps in SAN mode, and 9.95328 Gbps in WAN mode). The data stream and the divide-by-64 clock (161.13 MHz in LAN mode, 164.35 MHz in SAN mode, and 155.52 MHz in WAN mode) are provided for line transmission on pins TXDOUTP/N and CLK64AP/N, respectively.

Receive Operation for XAUI to XFI Mode High-speed, 10 Gbps NRZ serial data is received on pins RXINP/N where it can be equalized for copper trace dispersion and presented to the clock recovery unit (CRU).

In LAN and SAN mode (WAN_STAT = 0), the output of the CRU is deserialized and presented to the PCS, while in WAN mode (WAN_STAT = 1), the output of the CRU is deserialized and presented to the WIS. The WIS extracts the data from the SONET STS-192c/SDH STM-64 frames and processes the overhead. The resultant data is then presented to the PCS.

In standard PCS mode (EPCS_STAT = 0), the data enters the 66:64 gearbox. The 66-bit block is then aligned using the embedded 2-bit sync header, which generates the 64-bit payload. The payload is descrambled using the polynomial $G(x) = 1 + x^{39} + x^{58}$. The descrambled payload and 2-bit sync header pass through the 64b/66b decoder, where the block is mapped to valid XGMII data, eight data octets, and eight control bits.

In extended PCS mode (EPCS_STAT = 1), the data enters the PCS and is presented to the 66:64 gearbox. The data is then descrambled, framed, and formatted into 1584-bit frames. The Fire Code parity check code in the received data stream is used to delineate frame boundaries. Because the scrambler bits are XOR’ed with the FEC overhead during transmission, the state of the scrambler can be recovered by subtracting the calculated parity from the received scrambled parity. The block is then mapped to valid XGMII data, eight data octets, and eight control bits.

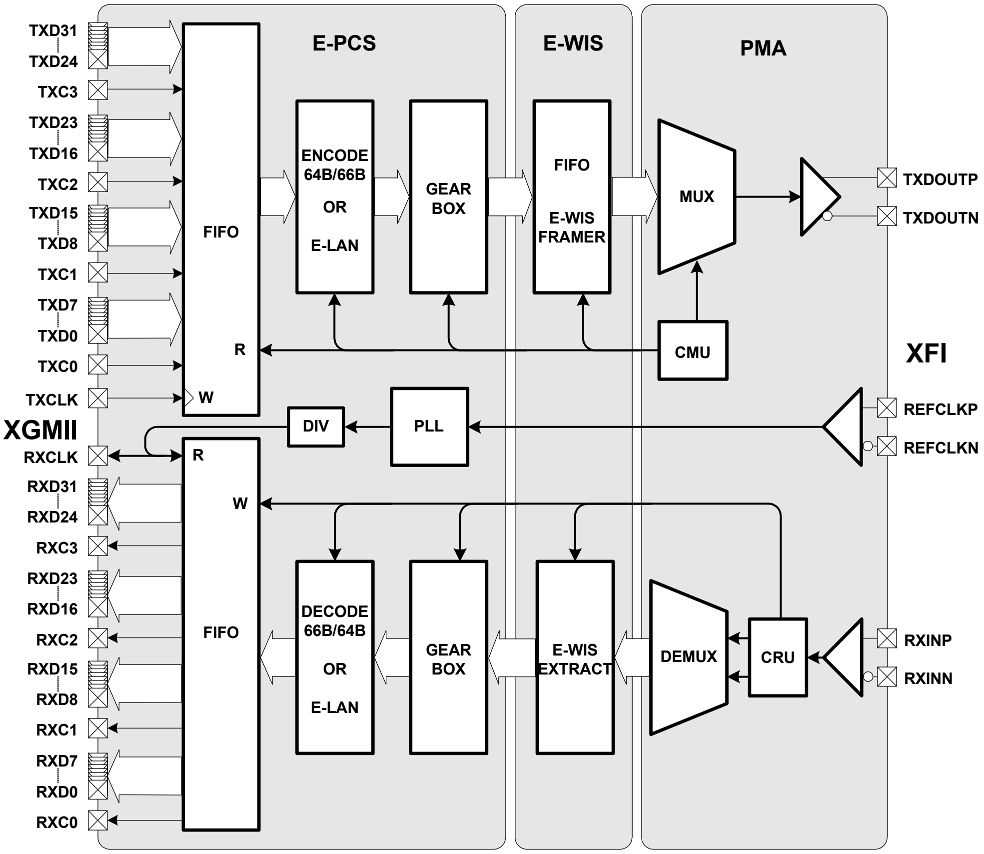
In both standard or extended PCS modes, the eight data octets and eight control bits are passed to the FIFO, where path timing is transferred from the divided (one sixty-forth) recovered clock to the divided (one sixty-sixth) CMU clock. During IPG, idle characters are added or deleted as necessary to adapt between the two clock rates.

The eight data octets and eight control bits are then presented to the PHY XS block where it is 8b/10b encoded and serialized. The serialized code words are then transmitted four at a time on the four XAUI outputs: XTX[3:0]P/N.

3.1.2 XGMII to XFI Mode

To set the VSC8486 into the XGMII to XFI mode, the I/O mode select pin must be set low (IOMODESEL = 0). IOMODESEL sets the default value of XGMII_OE (3x8005.6) and PCS_XGMII_SRC (3x8005.8) appropriately to a value of 0x0140 after a reset is executed. The following figure depicts the data path for this mode.

Figure 3. Functions in XGMII to XFI Mode



Transmit Operation for XGMII to XFI Mode In XGMII to XFI mode, the XGXS (and XAUI input interface) is bypassed and the data is presented directly to the PCS from the XGMII interface. All other transmit functions are the same.

Receive Operation for XGMII to XFI Mode In XGMII to XFI mode, the XGXS (and XAUI output interface) is bypassed and the data from the PCS is directly output from the device on the XGMII interface on RXD[31:0] and RXC[3:0].

3.1.3 XGMII to XAUI Mode

To set the VSC8486 for XGMII to XAUI mode, do the following:

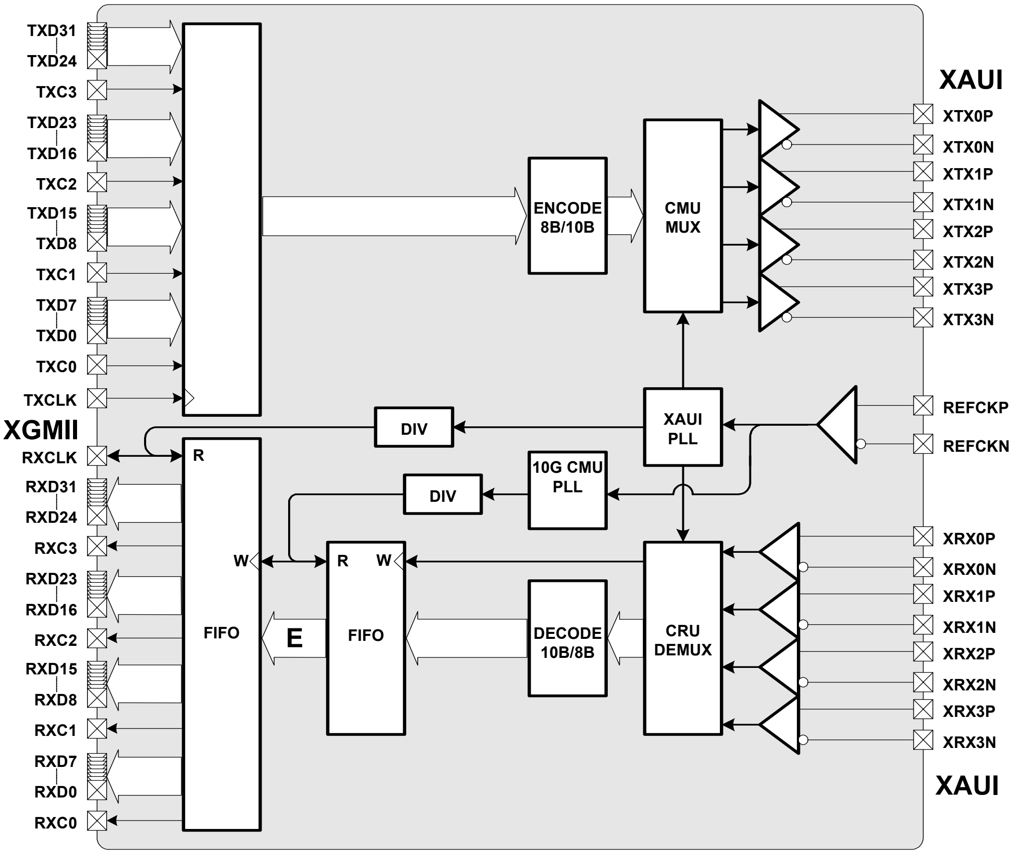
1. Set the I/O mode select pin low (IOMODESEL = 0).
2. Issue a reset to the device.

3. Write the value, 0x01C4, to the PCS Configuration 1 register (3x8005).

In this mode, there are a few restrictions on the clock domains. The restrictions are:

- REFCK and TXCLK (XGMII input clock) must be derived from a common local source.
- RXCLK (XGMII output clock) is derived from REFCK.
- Incoming XAUI data can be ±100 ppm from the REFCK.

Figure 4. Functions in XGMII to XAUI Mode



Transmit Operation for XGMII to XAUI Mode Data and control signals are received on the XGMII Tx input pins TXD[31:0] and TXC[3:0] on each rising and falling edge of TXCLK. The eight data octets and eight control bits are then presented to the PHY XS block, where the data is 8b/10b encoded and serialized. The serialized code words are then transmitted four at a time on the four XAUI outputs: XTX[3:0]P/N.

Note that the XGMII input clock (TXCLK) must be synchronous with the CMU reference clock (REFCLKP/N).

Receive Operation for XAUI to XGMII Mode The PHY XS block receives four 8b/10b encoded 3.1875 Gbps data lanes on pins XRX[3:0]P/N. The clock is recovered and the data is deserialized on each of the four lanes. Synchronization is performed before the data is passed into the 10b/8b decoders. The decoded data and accompanying control bits are then presented to the FIFO. The FIFO deskews the four lanes and transfers path timing from the PHY XS recovered clock to the PMA transmit clock. The path timing is transferred by adding or deleting idle characters during inter-packet gaps (IPGs) as needed.

The eight data octets and eight control bits are then presented at the XMGII output interface on pins RXD[31:0] and RXC[3:0] in two consecutive transfers occurring on both rising and falling edges of output clock RXCLK.

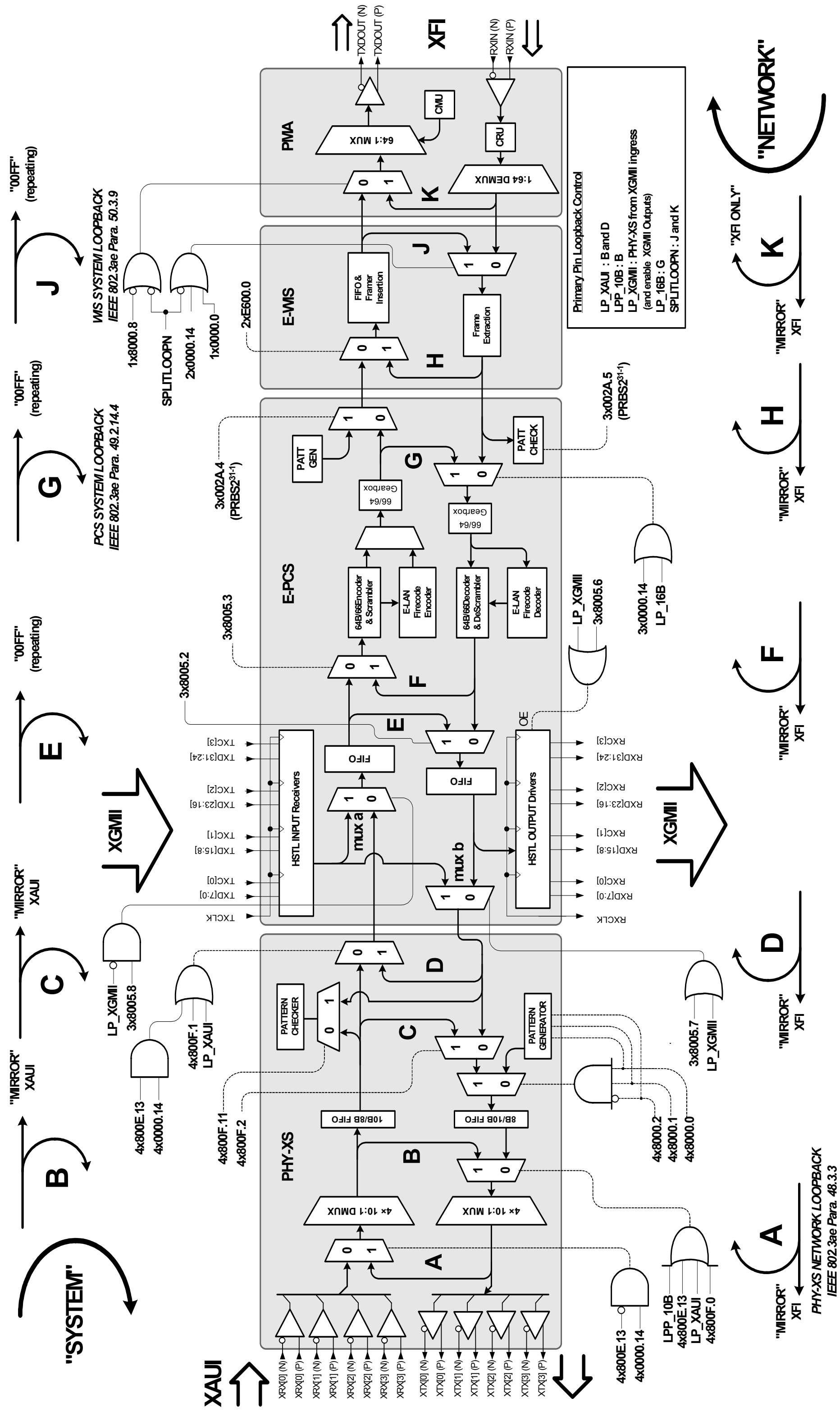
3.2 Loopback Operation

The VSC8486 LAN PHY has three 10-gigabit data ports: XAUI, XFI, and XGMII. There are several options available to the user for routing traffic between the various ports. The purpose of this section is to outline the operation of several modes loosely termed loopbacks. These modes can be extremely useful for both test and debug purposes.

In addition to loopbacks, the device contains several pins that configure the device for XGMII or XAUI operation without requiring MDIO access.

Loopback paths are illustrated in the following figure. Two split loopback paths (that is, two loopback paths simultaneously switched on) are enabled with control pins SPLITLOOPN and LP_XAUI. Most other data path routing and loopback controls are enabled through the MDIO interface.

Figure 5. Loopback Configuration



3.2.1 I/O Mode Select (IOMODESEL) and LP_XGMII

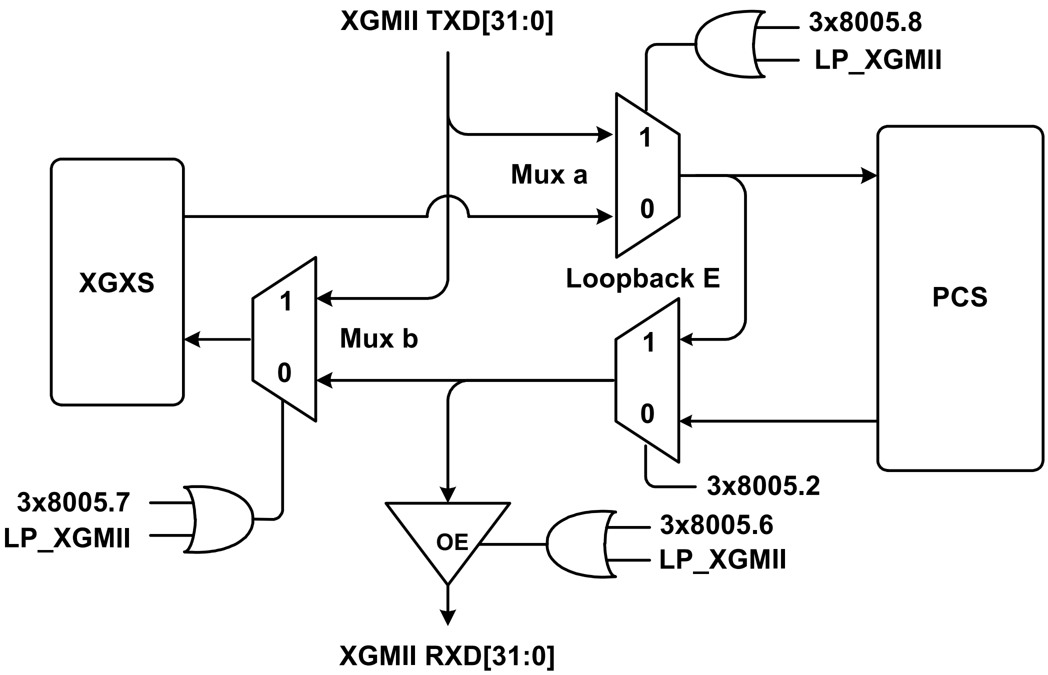
On power up or reset, the state of the IOMODESEL pin sets the VSC8486 data path routing on chip as follows:

1. On reset, if IOMODESEL = 0, then 3x8005.8:6 is set to 101. This setting programs multiplexers a and b for XGMII mode and enables the XGMII output drivers.
2. On reset, if IOMODESEL = 1, 3x8005.8:6 is set to 000. This setting programs multiplexers a and b for XAUI mode and disables the XGMII output.

Mux a, mux b, and OE controls can also be configured after a reset, using the MDIO 3x8005.8:6 bits.

If LP_XGMII is pulled high, the XGMII output is enabled and the XGXS receives its data from the XGMII input, TXD[31:0], regardless of the settings for IOMODESEL or the 3x8005.8:6 bits. The VSC8486 can be programmed to mirror XGMII Tx input data simultaneously to the PCS and the XGXS. Alternatively, the PCS data can be routed simultaneously to the XGMII Rx output and the XGXS.

Figure 6. VSC8486 Data Path XGMII Source



The following table summarizes the control settings using the IOMODESEL pin.

Table 3. Pin Control for XGMII After Reset

IOMODESEL Pin Control	XGMII Data Source XGXS	XGMII Data Source PCS	XGMII Output Driver Enabled?	3x8005 Register Value Set on Reset Bit 8	Bit 7	Bit 6
0		XGMII TXD[31:0]	Yes	1	0	1

Table 3. Pin Control for XGMII After Reset *(continued)*

IOMODESEL Pin Control	XGMII Data Source		XGMII Output Driver Enabled?	3x8005 Register Value Set on Reset		
	XGXS	PCS		Bit 8	Bit 7	Bit 6
1	PCS	XGXS	No	0	0	0

The following table summarizes the control settings using the MDIO registers.

Table 4. MDIO Control for XGMII

3x8005 MDIO Register Settings			Data Source		XGMII Output (Always from PCS)	Description
Bit 8	Bit 7	Bit 6	PCS	XGXS		
0	0	0	XGXS	PCS	Off	XGXS data comes from PCS, PCS data comes from XGXS. XGMII output drivers disabled.
0	0	1	XGXS	PCS	On	XGXS data comes from PCS, PCS data comes from XGXS. XGMII RXD comes from PCS. (Mirror PCS data to XGMII.)
0	1	0	XGXS	XGMII TXD	Off	XGXS data comes from XGMII TXD, PCS data comes from XGXS. XGMII output drivers disabled.
0	1	1	XGXS	XGMII TXD	On	XGXS data comes from XGMII TXD, PCS data comes from XGXS. XGMII RXD comes from PCS.
1	0	0	XGMII TXD	PCS	Off	XGXS data comes from PCS, PCS data comes from XGMII TXD. XGMII output drivers disabled.
1	0	1	XGMII TXD	PCS	On	XGXS data comes from PCS, PCS data comes from XGMII TXD. XGMII RXD comes from PCS. (Mirror PCS data to XGMII.)
1	1	0	XGMII TXD	XGMII TXD	Off	XGXS data comes from XGMII TXD, PCS data comes from XGMII TXD. XGMII output drivers disabled. (Mirror XGMII TXD to XGXS.)
1	1	1	XGMII TXD	XGMII TXD	On	XGXS data comes from XGMII TXD, PCS data comes from XGMII TXD. XGMII RXD comes from PCS. (Mirror XGMII TXD to XGXS.)

3.2.2 Loopback Summary

There are three types of loopback modes: system, network, and split loopbacks. In general, system loopbacks affect XAUI traffic, network loopbacks affect XFI traffic, and split loopbacks affect both. The following table provides a summary of the system loopbacks.

Table 5. System Loopbacks Summary

Loopback	Name	Loopback Enable	Retiming
B	PHY XS shallow system loopback	Any of the following: LPP_10B = 1 LP_XAUI = 1 4x800E.13 = 1 4x800F.0 = 0	Phase delay only, XAUI XTX[3:0] signals retimed from XAUI XRX[3:0] recovered clock
C	PHY XS deep system loopback	4x800F.2 = 1	XAUI XTX[3:0] signals retimed to LAN clock (REFCLKP/N)
E	PCS FIFO system loopback	3x8005.2 = 1	XAUI XTX[3:0] signals retimed to LAN clock (REFCLKP/N)
G	PCS system loopback	LP_16B = 1 or 3x0000.14 = 1	XAUI XTX[3:0] signals retimed to LAN clock (REFCLKP/N)
J	PMA/WIS system loopback	Any of the following: SPLITLOOPN = 0 (active low) 2x0000.14 = 1 1x0000.0 = 1	XAUI XTX[3:0] signals retimed to LAN clock (REFCLKP/N)

For system loopbacks, the XAUI data can be mirrored to the XFI Tx port, depending on the register setting of XFI_LPBK_OVR (1xEF10.2), as shown in the following table.

Table 6. System Loopbacks and XFI Traffic

Loopback	If XFI_LPBK_OVR (1xEF10.2) = 0(1)	If XFI_LPBK_OVR (1xEF10.2) = 1
B	XFI Tx traffic from WIS/PCS	XFI Tx traffic set by 1xEF10.1:0 00: 0x00FF pattern 01: All zeros 10: All ones 11: WIS/PCS
C	XFI Tx traffic from WIS/PCS	XFI Tx traffic set by 1xEF10.1:0 00: 0x00FF pattern 01: All zeros 10: All ones 11: WIS/PCS
E, G, or J	0x00FF pattern	XFI Tx traffic set by 1xEF10.1:0 00: 0x00FF pattern 01: All zeros 10: All ones 11: WIS/PCS

1. The XFI_LPBK_OVR (1xEF10.2) register defaults to 0.

The following table provides a summary of the network loopbacks, which primarily affect XFI traffic.

Table 7. Network Loopbacks Summary

Loopback	Name	Loopback Enable	Retiming
A	PHY XS deep network loopback	4x0000.14 = 1 and 4x800E.13 = 0	See Table 9, page 30
D	PHY XS shallow network loopback	Any of the following: 4x800E.13 = 0 and 4x0000.14 = 0 4x800F.1 = 1 LP_XAUI = 1	See Table 9, page 30
F	PCS gearbox network loopback	3x8005.3 = 1	See Table 9, page 30
H	WIS network loopback	2xE600.0 = 1	See Table 9, page 30
K	PMA network loopback	Any of the following: SPLITLOOPN = 0 (active low) 1x8000.8 = 0	See Table 9, page 30

The split loopbacks affect both XAUI and XFI traffic. They are enabled using the LP_XAUI and SPLITLOOPN pins, as shown in the following table.

Table 8. Split Loopbacks Summary

Loopback	Name	Loopback Enable	Retiming
B and D	XAUI split loopback	LP_XAUI = 1 Internally pulled low	See Table 9, page 30
J and K	PMA split loopback	SPLITLOOPN = 0 Internally pulled high	See Table 9, page 30

Retiming Clock Sources for Network and Split Loopbacks For network and split loopbacks, there are various options for controlling the XFI retiming, as shown in the following table. For retiming XAUI traffic (pins XTX[3:0]), REFCLKP/N is used; however, when the split loopback B and D is active, the recovered clock from XRX[3:0] is used.

Table 9. Retiming Clock Sources for Network and Split Loopbacks

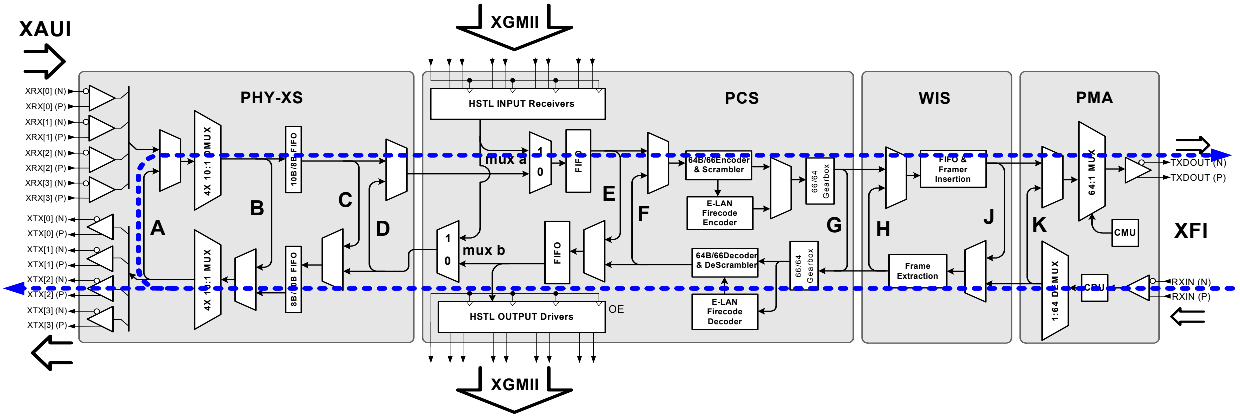
WAN_STAT (1xE606.15)	LINETIME_STAT (1xE606.13)	XFI Retimed With
0	0	REFCLKP/N
0	1	10G LINE_IN
1	0	WREFCLKP/N
1	1	10G LINE_IN

3.2.3 Loopback Descriptions

This section describes each loopback in alphabetical order.

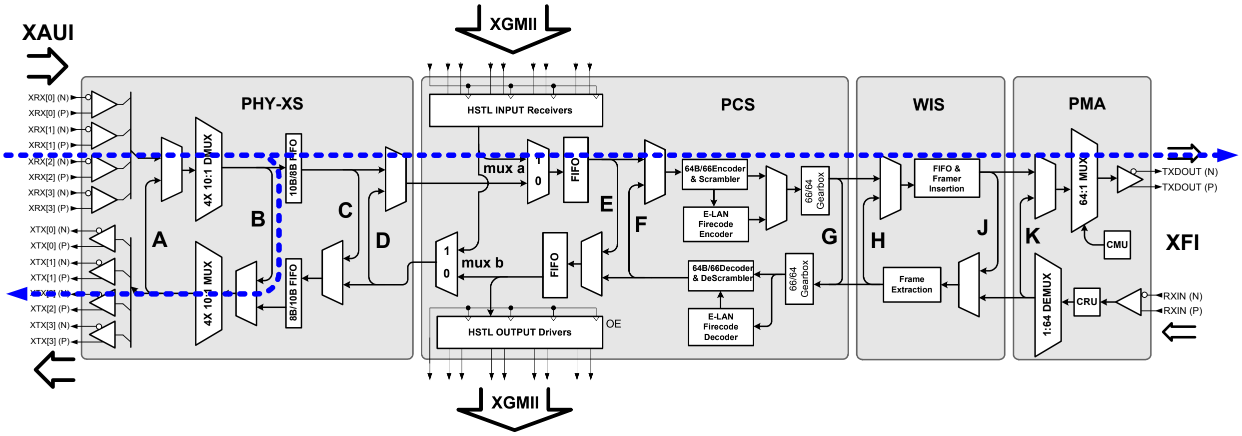
Loopback A - PHY XS Deep Network Loopback Loopback A is located in the XAUI PHY. It reroutes the data from the 10:1 MUX in the XAUI PHY into the 1:10 DEMUX, as shown in the following figure. XFI data is retimed with PMA CRU. To enable loopback A, set both of the following: LPBK_A (4x0000.14) set to 1 and LPBK_B (4x800E.13) set to 0. The default value for bit 14 is 0 (loopback disabled). XFI ingress (RXINP/N) data is mirrored to the XAUI egress port (XTX[3:0]P/N) simultaneously without further MDIO instructions. This loopback cannot be used if LP_XAUI is asserted high.

Figure 7. Loopback A



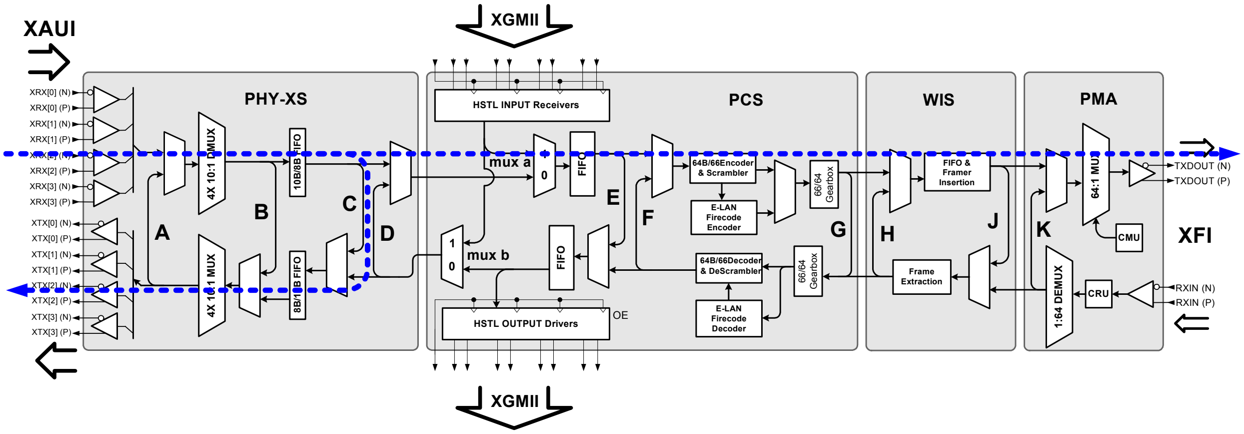
Loopback B - PHY XS Shallow System Loopback Loopback B routes the incoming XAUI data through the 1:10 DEMUX and then loops back before the 10b/8b decoder into the 10:1 MUX. Data is retimed by the recovered XAUI clock. No 10b/8b decoding or lane synchronization is performed. System XAUI data is also mirrored to the XFI Tx port. To enable loopback B, set any of the following: LPBK_B (4x800E.13) set to 1 or the LP_XAUI pin set high or the LPP_10B pin set high. Note that setting LP_XAUI to high simultaneously enables loopback D.

Figure 8. Loopback B



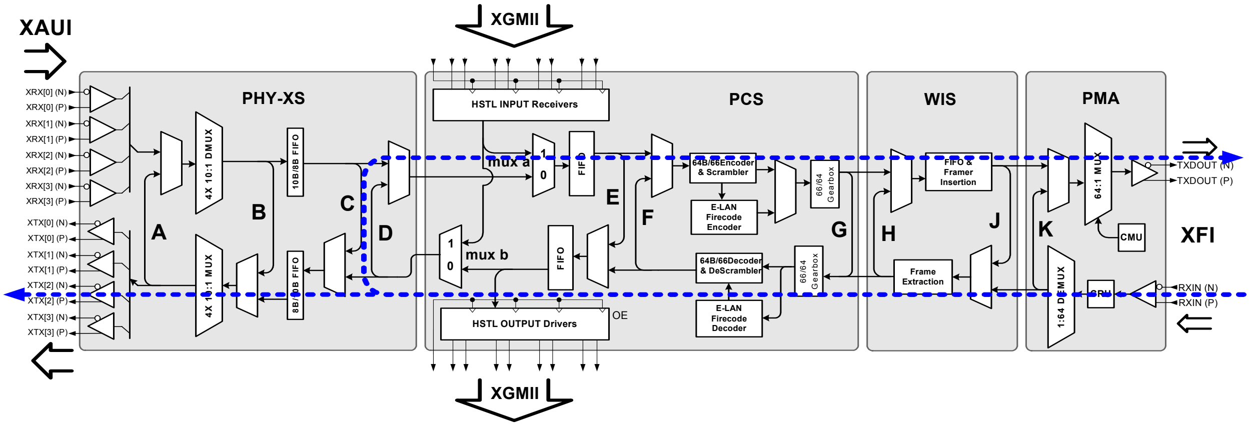
Loopback C - PHY XS Deep System Loopback Loopback C routes the incoming XAUI data after the 10b/8b FIFO back into the 8b/10b FIFO. System XAUI data is also mirrored to the XFI Tx port. To enable loopback C, set LPBK_C (4x800F.2) to 1.

Figure 9. Loopback C



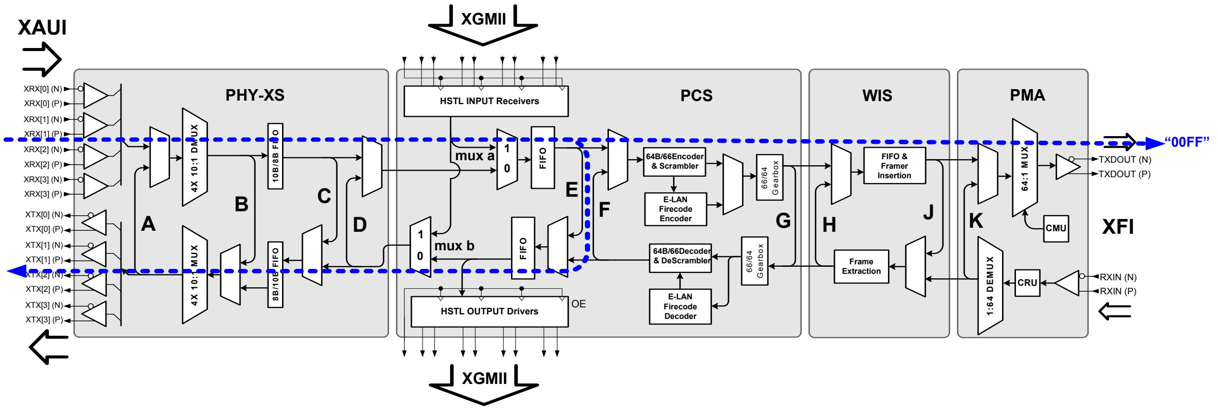
Loopback D – PHY XS Shallow Network Loopback Loopback D routes the incoming XFI data after the PCS FIFO back into the transmit PCS FIFO. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback D, set any of the following: LPBK_D (4x800F.1) set to 1, or both LPBK_B (4x800E.13) and LPBK_A (4x0000.14) set to 1, or the LP_XAUI pin set high. Note that setting LP_XAUI to high simultaneously enables loopback B.

Figure 10. Loopback D



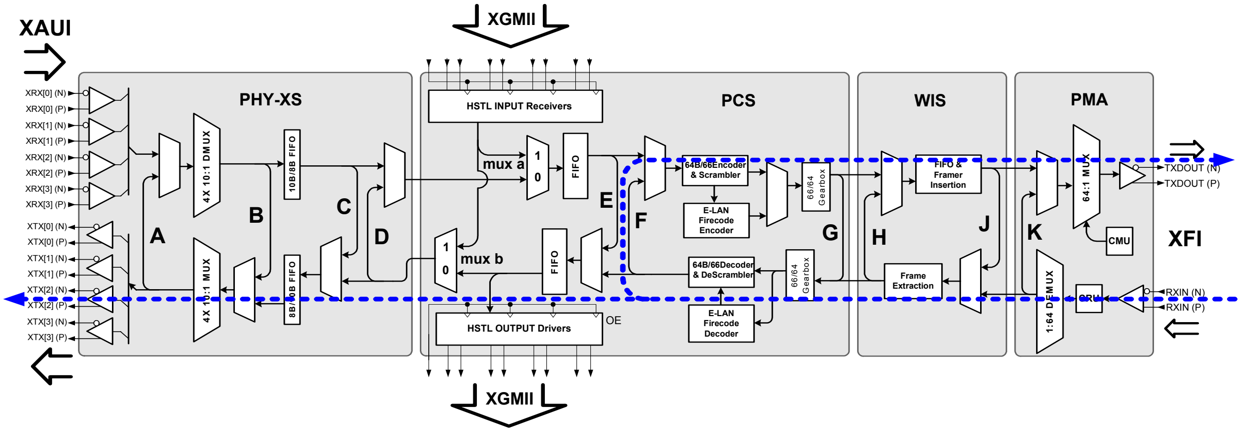
Loopback E – PCS FIFO System Loopback Loopback E routes the incoming XAUI data from the PCS transmit FIFO back into the PCS receive FIFO. The data transmitted to the XFI Tx port is a continuous stream of 0x00FF data words. To enable loopback E, set LPBK_E (3x8005.2) to 1.

Figure 11. Loopback E



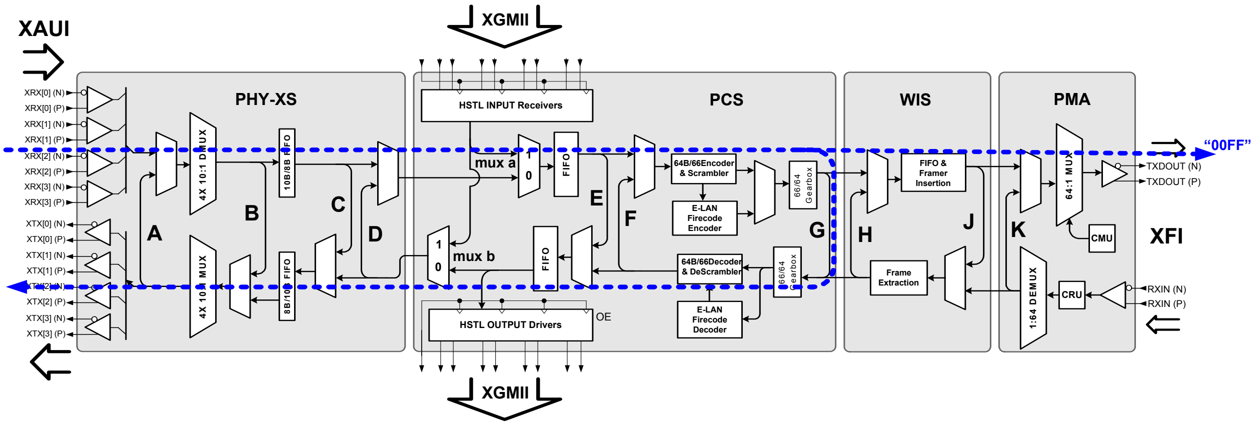
Loopback F - Gearbox Network Loopback Loopback F routes the incoming XFI data after the receive PCS gearbox back into the transmit PCS gearbox. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback F, set LPBK_F (3x8005.3) to 1.

Figure 12. Loopback F



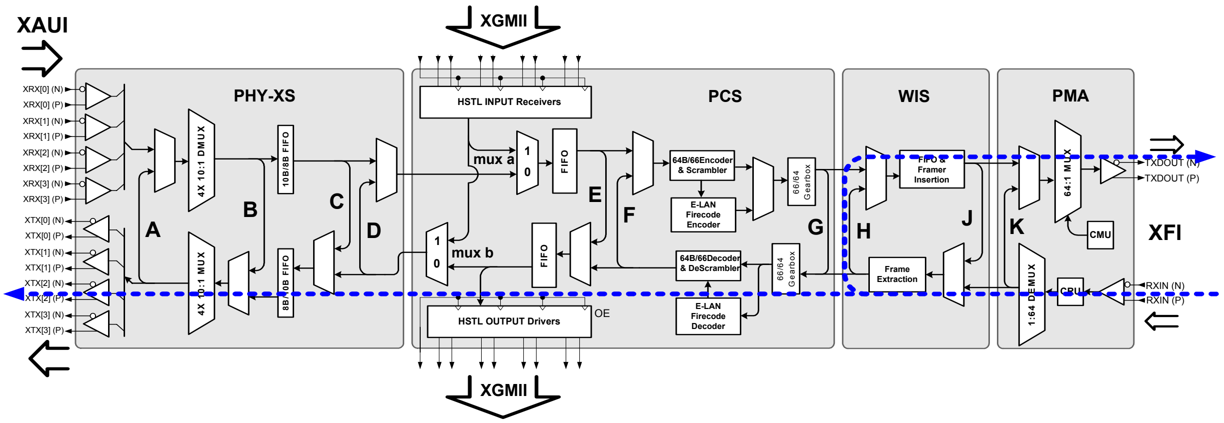
Loopback G - PCS System Loopback Loopback G routes the incoming XAUI data through the PCS transmit gearbox back into the PCS receive gearbox. The data transmitted to the XFI Tx port is a continuous stream of 0x00FF data words. To enable loopback G, either set LPBK_G (3x0000.14) to 1 or set the LP_16B pin high.

Figure 13. Loopback G



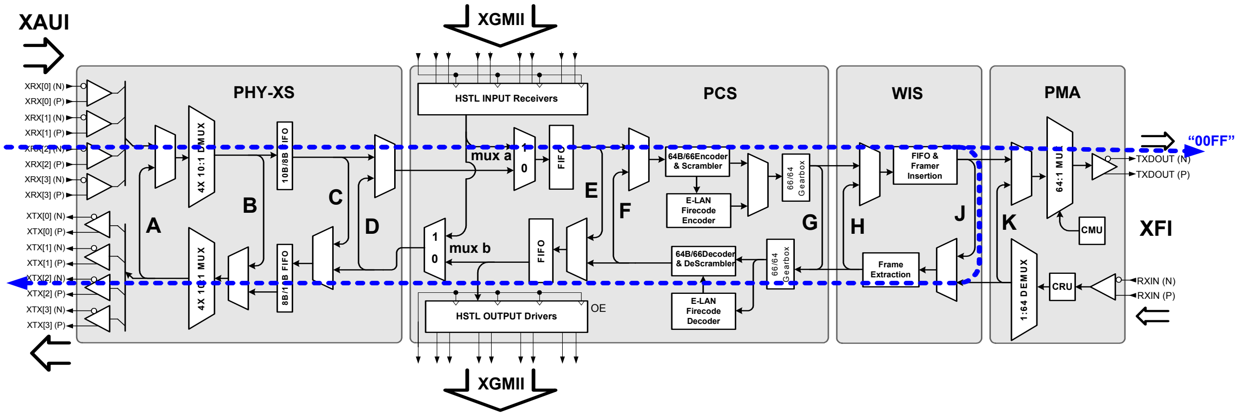
Loopback H - PCS System Loopback Loopback H routes the incoming XFI data from the PMA or WIS received data back into the PMA or WIS transmit path. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback H, set LPBK_H (2xE600.0) to 1.

Figure 14. Loopback H



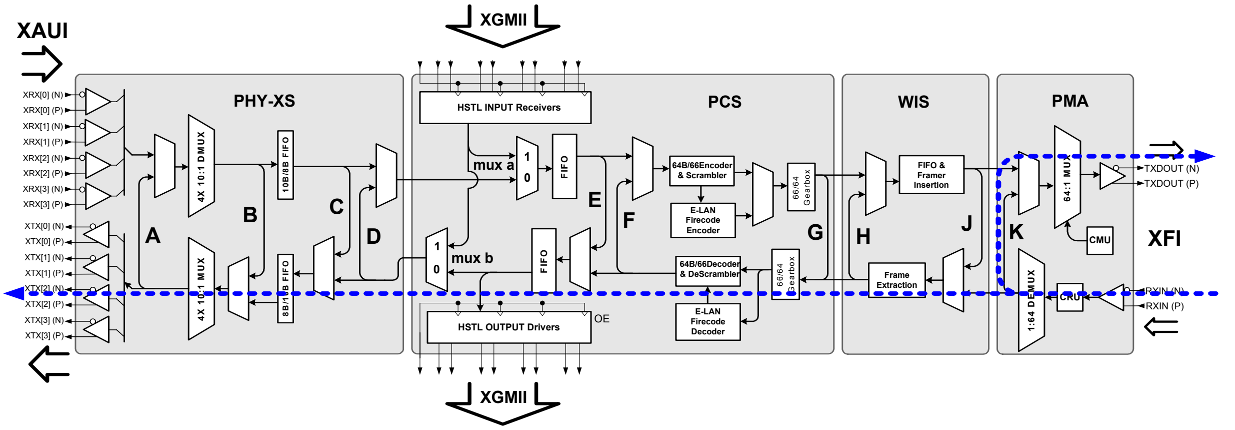
Loopback J - PMA/WIS System Loopback Loopback J routes the incoming XAUI data from the PCS (or WIS if enabled) back into the PCS (or WIS if enabled). This loopback is enabled for both PMA and WIS system loopbacks. The data transmitted to the XFI Tx port is a continuous stream of 0x00FF data words. To enable loopback J, set any of the following: LPBK_J_PMA (1x0000.0) set to 1 or LPBK_J_WIS (2x0000.14) set to 1 or the SPLITLOOPN pin set low. Note that setting the SPLITLOOPN pin low also enables loopback K.

Figure 15. Loopback J



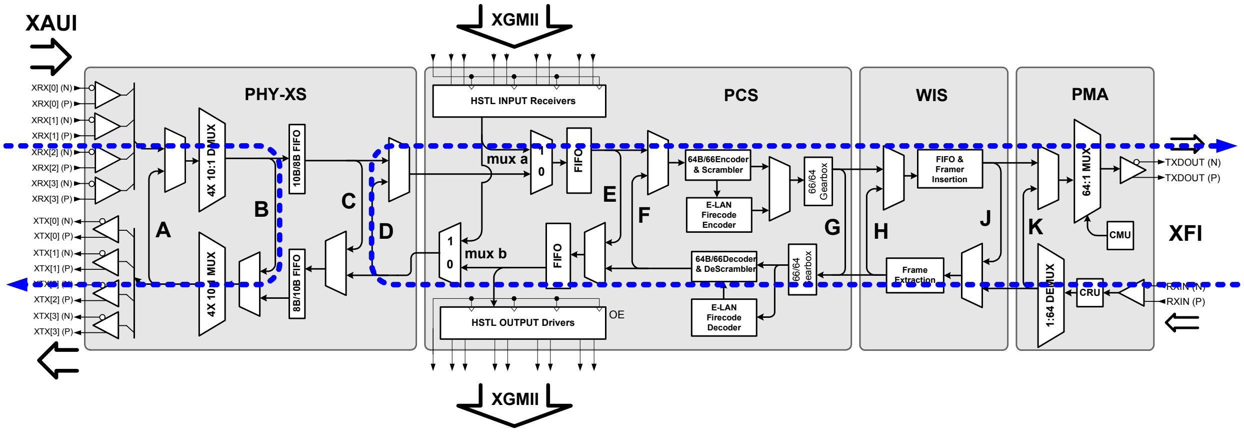
Loopback K - PMA Network Loopback Loopback K routes the incoming 10-gigabit XFI data back to the 10-gigabit XFI output, as shown in the following figure. Loopback K is protocol agnostic. Data is retimed with the 10-gigabit recovered clock. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback K, set any of the following: LPBKN_K (1x8000.8) set to 0 (the default is 1, disabled) or set the SPLITLOOPN pin low. Note that setting the SPLITLOOPN pin low also enables loopback J.

Figure 16. Loopback K



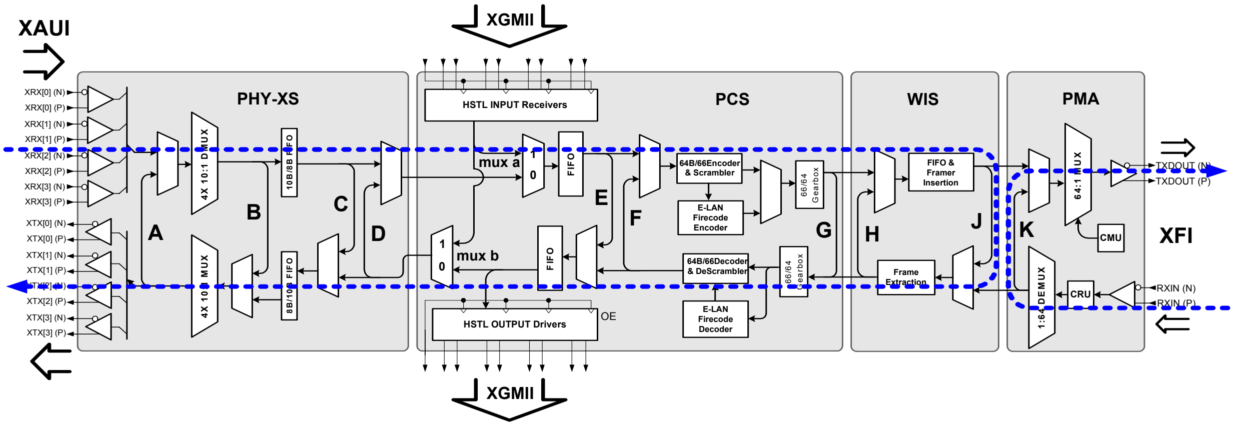
Loopback B and D - XAUI Split Loopback Split loopback paths B and D are simultaneously enabled by setting LP_XAUI high. Loopback D XFI output data is retimed by the local LAN or WAN refclk. If left unconnected, the LP_XAUI input is pulled down on-chip, disabling these loopback paths.

Figure 17. XAUI Split Loopback (LP_XAUI = 1)



Loopback J and K - PMA Split Loopback Split loopback paths J and K are simultaneously enabled by setting SPLITLOOPN low. Loopback J recovers the clock from the XAUI ingress data, passes through a rate compensation FIFO, and is timed out by the LAN REFCK. Loopback K is retimed by the 10-gigabit recovered clock. If left unconnected, the SPLITLOOPN input is pulled up on chip, disabling these loopback paths.

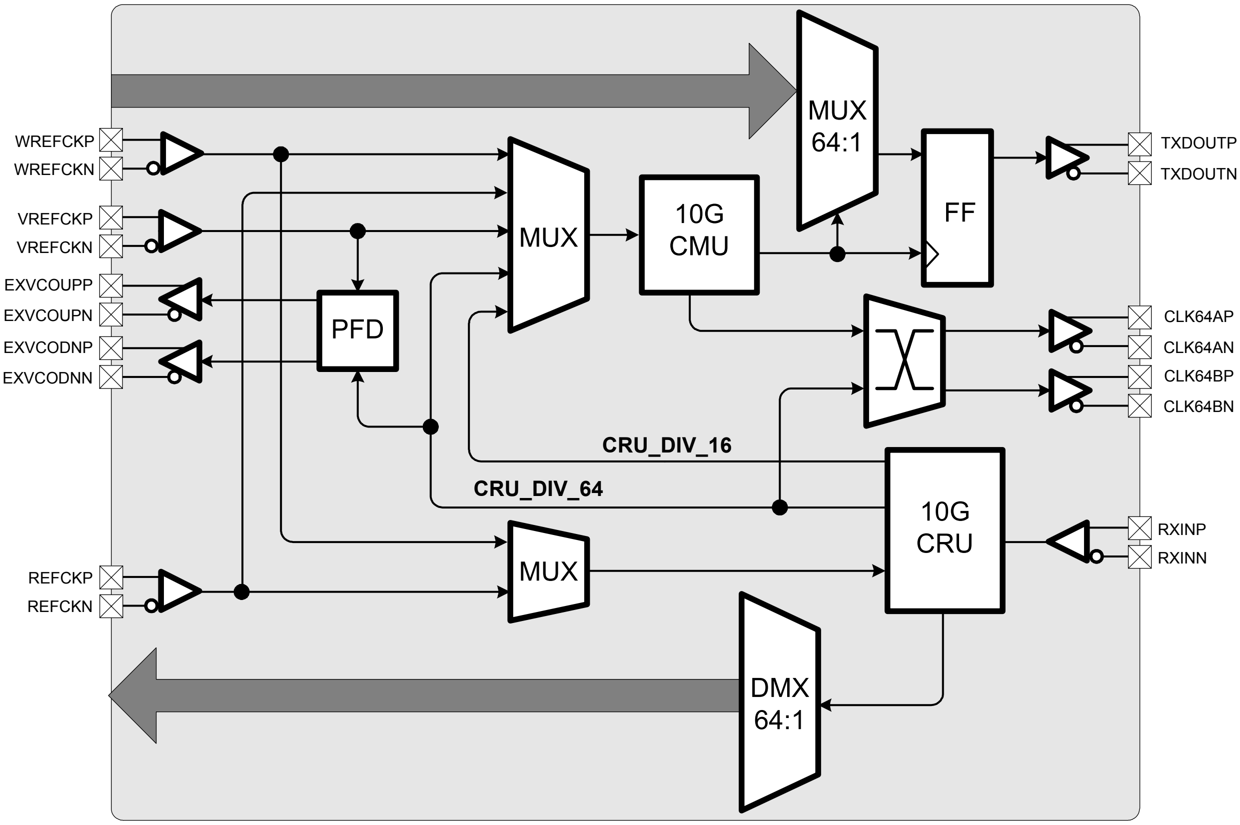
Figure 18. PMA Split Loopback (SPLITLOOPN = 0)



3.3 Physical Media Attachment (PMA)

The following block diagram shows the physical media attachment (PMA).

Figure 19. PMA Block Diagram



3.3.1 Multiplexer Operation

The PMA transmitter includes a CMU and a 64-bit multiplexer that receives 64-bit data from the PCS (or WIS) block, which generates the high-speed serial output on pins TXDOUTP/N. The output speeds are 10.3125 Gbps in LAN mode, 10.51875 Gbps in SAN mode, or 9.95328 Gbps in WAN mode.

The CMU provides a divide-by-64 clock output on pins CLK64AP/N or CLK64BP/N for optional use as a reference clock to an XFP module or external phase lock loop circuit. The clock output speeds are 161.133 MHz in LAN mode, 164.355 MHz in SAN mode, or 155.52 MHz in WAN mode.

By default, TX_MSBSEL (1x8000.6) is set to 1, resulting in the PMA transmitting the least significant bit (LSB) first. Using MDIO, the most significant bit (MSB) can be selected as the first bit transmitted.

The high-speed output data (TXDOUTP/N) can be muted (that is, set to continuous zeros) by setting the TXONOFFI pin low. If left unconnected, the default for TXONOFFI is 1, which is set by an on-chip pull-up.

3.3.2 Timing Operation (LINETIME_STAT)

The VSC8486 supports two types of timing operation, normal and linetime. During normal timing, with LINETIME_STAT (1xE606.13) = 0, the device transmits data synchronous to the REFCLKP/N or WREFCLKP/N input if in WAN mode (1xE606.14). In Linetime mode (LINETIME_STAT = 1), the device transmits data synchronous to the receiver's recovered clock. The VSC8486 provides the necessary divided-down clock outputs and internal phase detector to enable users to synthesize an external phase lock loop jitter attenuation circuit. A voltage controlled SAW oscillator (VCSO) is recommended for optimum phase noise and jitter performance. The VCSO frequency must be 622.08 MHz and connected to the VREFCLKP/N pins.

The default state for the LINETIME_FRC bit (1xE605.4) is 0 (linetime disabled). To enable linetiming, set this bit to 1. The linetime status bit (1xE606.13) shows the linetime status.

3.3.3 REFSEL0 Selection (REFSEL0_STATUS)

The VSC8486 supports two WAN mode reference clock rate options. By default, REFSEL0 controls the REFSEL0_STAT state. The pin control has various overrides, as listed in the following table (X indicates "doesn't matter").

Table 10. REFSEL0_STATUS Logic

Inputs			Result	
REFSEL0	REFSEL0_OVR (1xE605.7)	REFSEL0_FORCE (1xE605.6)	WREFCLK Frequency	REFSEL0_PIN_STATUS (1xE606.12)
Low (default)	0 (default)	X	622.08 MHz	0
High	0	X	155.52 MHz	1
X	1	0	622.08 MHz	X
X	1	1	155.52 MHz	X

3.3.4 WAN Enabled (WAN_STAT)

By default, the WAN_MODE controls the WAN_STAT state. The pin control has various overrides, as listed in the following table (where X indicates "doesn't matter").

Note When written, registers 2x0007 and 3x0007 provide a microcontroller interrupt.

Table 11. WAN Mode Control Logic

Inputs					Result	
WANMODE	**PCS Type Selection (2x0007.0)**	**PCS Mode (3x0007.1:0)**	**WAN_OVR (1xE605.3)**	**WAN_FORCE (1xE605.2)**	**WAN_STAT (1xE606.15)**	**WAN_MODE_ PIN_STATUS (1xE606.14)**
Low	0	00	0	X	0	0
High	X	X	0	X	1	1
X	X	X	1	0	0	X
X	X	X	1	1	1	X
X	1	X	0	X	1	X
X	X	10	0	X	1	X

3.3.5 Clock Multiplier Unit (CMU) Reference Clocking

For LAN and SAN applications (WAN_STAT = 0), an on-chip PLL generates the high-speed transmit clock from the externally provided REFCLKP/N input during normal timing operation or from the recovered high-speed receive clock during linetiming operation. The REFCLKP/N input must be one sixty-sixth of the serial data rate (156.25 MHz for LAN mode or 159.375 MHz for SAN mode). The XAUI transmitter and receiver also use the REFCLKP/N input.

For WAN applications (WAN_STAT = 1), an additional reference clock is required for the high-speed data (9.95328 Gbps). The on-chip PLL generates the high-speed transmit clock from one of three sources: the externally provided WREFCLKP/N input, the recovered high speed receive clock, or from an external VCSO as part of a jitter attenuation PLL circuit that enters the device at VREFCLKP/N. In both normal timing operation and in linetiming operation, the WREFCLKP/N reference clock must be present and can be either 155.52 MHz (REFSEL0 = 1) or 622.08 MHz (REFSEL0 = 0, which is the default). In linetiming operation (LINETIME_STAT = 1), the transmit clock is generated from the 10-gigabit CRU. As with LAN and SAN modes, the XAUI clock is generated from the REFCLKP/N input.

The on-chip PLL uses a low phase noise reactance-based VCO. The reference clock should be of high quality because noise on the reference clock below the PLL loop bandwidth passes through the PLL and appears as jitter on the outputs (TXDOUTP/N and CLK64AP/N). During such conditions, the VSC8486 transfers reference clock noise in addition to its own intrinsic jitter. Preconditioning the reference clock signal might be necessary to avoid passing reference clock noise.

The following table summarizes these reference clock controls and the associated frequencies. The transmit and receive references are also provided.

Table 12. CMU and CRU Reference Clock Control and Frequency Summary

Mode Description	LINETIME_ STAT	WAN_ STAT	REFSEL0_ STATUS	REFCLKP, REFCLKN, (MHz)	WREFCLKP, WREFCLKN (MHz)	Transmit Reference (10G CMU)	Receive Reference (10G CRU)
1: LAN/SAN mode, normal timing	0	0	X	156.25 or 159.375	NC	REFCLKP, REFCLKN	REFCLKP, REFCLKN
2: WAN mode, normal timing	0	1	0	156.25	622.08	WREFCLKP, WREFCLKN	WREFCLKP, WREFCLKN divided by 4
3: WAN mode, 155.52 MHz reference clock normal timing	0	1	1	156.25	155.52	WREFCLKP, WREFCLKN	WREFCLKP, WREFCLKN
4: LAN/SAN mode, linetiming	1	0	0	156.25 or 159.375	NC	CRU recovered clock divided by 64	REFCLKP, REFCLKN
5: LAN/SAN mode, linetiming	1	0	1	156.25 or 159.375	NC	CRU recovered clock divided by 16	REFCLKP, REFCLKN
6: WAN mode, linetiming with external jitter attenuation circuit	1	1	0	156.25	622.08	VREFCLKP, VREFCLKN (only at 622.08 MHz)	WREFCLKP, WREFCLKN divided by 4
7: WAN mode, linetiming with 155.52 reference clock	1	1	1	156.25	155.52	CRU recovered clock divided by 16	WREFCLKP, WREFCLKN

3.3.6 Reference Clock Inputs

The VSC8486 determines the PMA timing mode by decoding the inputs for LINETIME_STAT, WAN_STAT, and REFSEL0_STATUS. The following tables define the logic for these three inputs and the available modes. VSC8486 always requires a 156.25 MHz (159.375 MHz) reference clock applied to REFCLKP/N for all operating modes.

LAN/SAN Only For applications supporting LAN/SAN only, we recommend the configuration depicted in the following table. WAN mode is not supported by this configuration. The input signals for this configuration are:

- REFCLKP/N = 156.25 MHz or 159.375 MHz
- WREFCLKP/N = none
- VREFCLKP/N = none

In the following tables, X indicates "doesn't matter."

Table 13. Configuration for LAN/SAN Only

LINETIME_ STAT	WAN_STAT	REFSEL0_ STATUS	Transmit Reference (10G CMU)	Receive Reference (10G CRU)	Mode Description
0	0	X	REFCLKP/N	REFCLKP/N	Normal timing, LAN/SAN mode
1	0	0	CRU divided by 64	REFCLKP/N	Linetime, LAN, or SAN mode
1	0	1	CRU divided by 16	REFCLKP/N	Linetime, LAN, or SAN mode

LAN/SAN/WAN With SONET/SDH Jitter Generation Compliance For applications that require SONET/SDH jitter performance but do not require clock cleanup, we recommend the configuration depicted in the following table. In this configuration, the 622.08 MHz clock provides the best jitter generation performance. This configuration does not support clock cleanup in linetime mode. The input signals for this configuration are:

- REFCLKP/N = 156.25 MHz or 159.375 MHz
- WREFCLKP/N = 622.08 MHz
- VREFCLKP/N = none

Table 14. Configuration With SONET/SDH Jitter Generation Compliance

LINETIME_ STAT	WAN_STAT	REFSEL0_ STATUS	Transmit Reference (10G CMU)	Receive Reference (10G CRU)	Mode Description
0	0	X	REFCLKP/N	REFCLKP/N	Normal timing, LAN/SAN mode
0	1	0	WREFCLKP/N	WREFCLKP/N	Normal timing, WAN mode
1	0	0	CRU divided by 64	REFCLKP/N	Line timing, LAN/SAN mode
1	0	1	CRU divided by 16	REFCLKP/N	Line timing, LAN/SAN mode

LAN/SAN/WAN Without SONET/SDH Jitter Generation Compliance For applications that do not need to meet SONET/SDH jitter requirements and do not need to use the recovered clock, we recommend the configuration depicted in the following table. In this configuration, the 155.52 MHz clock does not provide the best jitter generation performance. This configuration does not support clock cleanup in linetime mode. The input signals for this configuration are:

- REFCLKP/N = 156.25 MHz or 159.375 MHz
- WREFCLKP/N = 155.52 MHz
- VREFCLKP/N = none

In the following table, X indicates “doesn’t matter.”

Table 15. Configuration Without SONET/SDH Jitter Generation Compliance

LINETIME_ STAT	WAN_STAT	REFSEL0_ STATUS	Transmit Reference (10G CMU)	Receive Reference (10G CRU)	Mode Description
0	0	X	REFCLKP/N	REFCLKP/N	Normal timing, LAN/SAN mode
0	1	1	WREFCLKP/N	WREFCLKP/N	Normal timing, WAN mode
1	0	0	CRU divided by 64	REFCLKP/N	Line timing, LAN/SAN mode
1	0	1	CRU divided by 16	REFCLKP/N	Line timing, LAN/SAN mode
1	1	1	CRU divided by 16	WREFCLKP/N	Line timing, WAN mode

LAN/SAN/WAN With Full SONET/SDH Jitter Compliance For applications that require full SONET/SDH quality jitter in normal and linetime modes, we recommend the configuration depicted in the following table. The input signals for this configuration are:

- REFCLKP/N = 156.25 MHz or 159.375 MHz
- WREFCLKP/N = 622.08 MHz
- VREFCLKP/N = 622.08 MHz

Table 16. Configuration With Full SONET/SDH Jitter Compliance

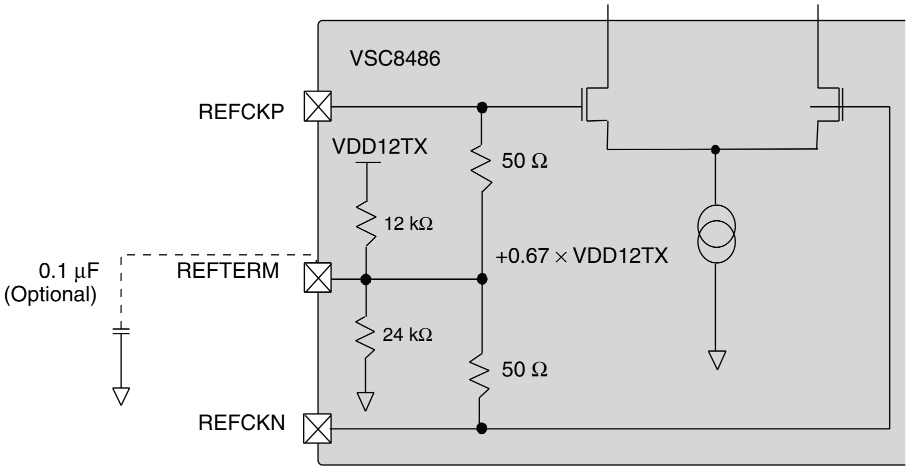
LINETIME_ STAT	WAN_STAT	REFSEL0_ STATUS	Transmit Reference (10G CMU)	Receive Reference (10G CRU)	Mode Description
0	0	X	REFCLKP/N	REFCLKP/N	Normal timing, LAN mode
0	1	0	WREFCLKP/N	WREFCLKP/N	Normal timing, WAN mode
1	0	0	CRU/64	REFCLKP/N	Normal timing, LAN mode
1	0	1	CRU/16	REFCLKP/N	Normal timing, LAN mode
1	1	0	VREFCLKP/N	WREFCLKP/N	Line timing WAN mode

The incoming low-speed reference clock (REFCLKP/N) is received by a differential LVPECL buffer as shown in Figure 20, page 43.

The on-chip termination is 100 Ω equivalent between true and complement. An internal bias generator, nominally set at 0.67 × VDD12TX, is provided for AC-coupling. An internal termination tap, REFTERM, is provided to allow adjustment of the input common-mode voltage. It is recommended to add an external capacitor between REFTERM, and VDD or ground. Single-ended reference clock operation is possible, and when implemented, both inputs must have equivalent termination. However, the best jitter performance is obtained using a low phase noise, differential reference clock.

When interfacing with 3.3 V LVPECL clock sources, always use AC coupling capacitors in series with true and complement reference clock inputs on the VSC8486. The recommended ceramic capacitor value is 0.1 µF, size 0402.

Figure 20. Reference Clock Input Receiver



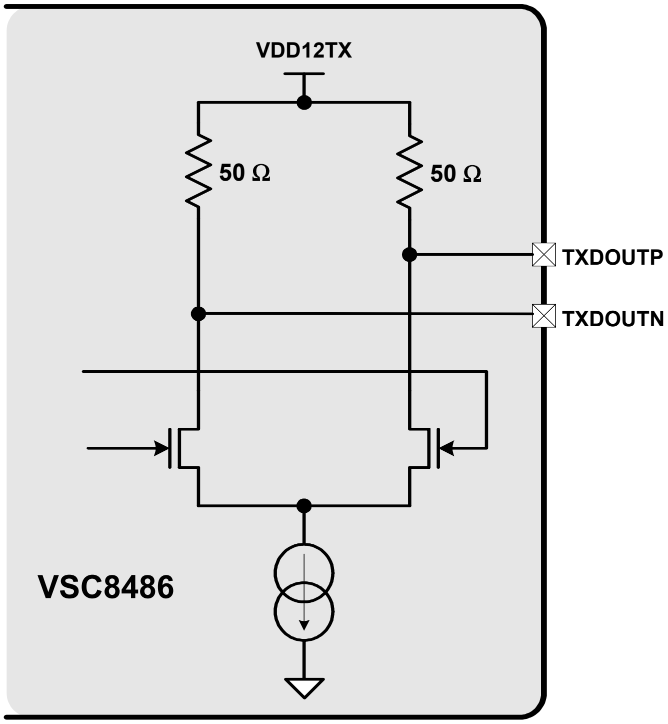
3.3.7 External Capacitors

For loop filter control and for minimizing the impact of power supply noise and other common-mode noise, the on-chip PLLs require 1.0 µF external capacitors. The external capacitors must be connected between pins CMUFILT and ground for the CMU, and between CRUFILT and ground for the CRU. These capacitors should be a multilayer ceramic dielectric with at least a 5 V working voltage rating. X7R dielectric capacitors provide better temperature stability and are recommended for this application.

3.3.8 XFI Transmit Data CML Output (TXDOUTP/N)

The CML high-speed data output driver consists of a differential pair designed to drive a 50 Ω transmission line. As shown in the following figure, the output driver uses an on-chip source termination of 50 Ω to VDD12TX, which minimizes any reflections.

Figure 21. CML XFI Output Driver



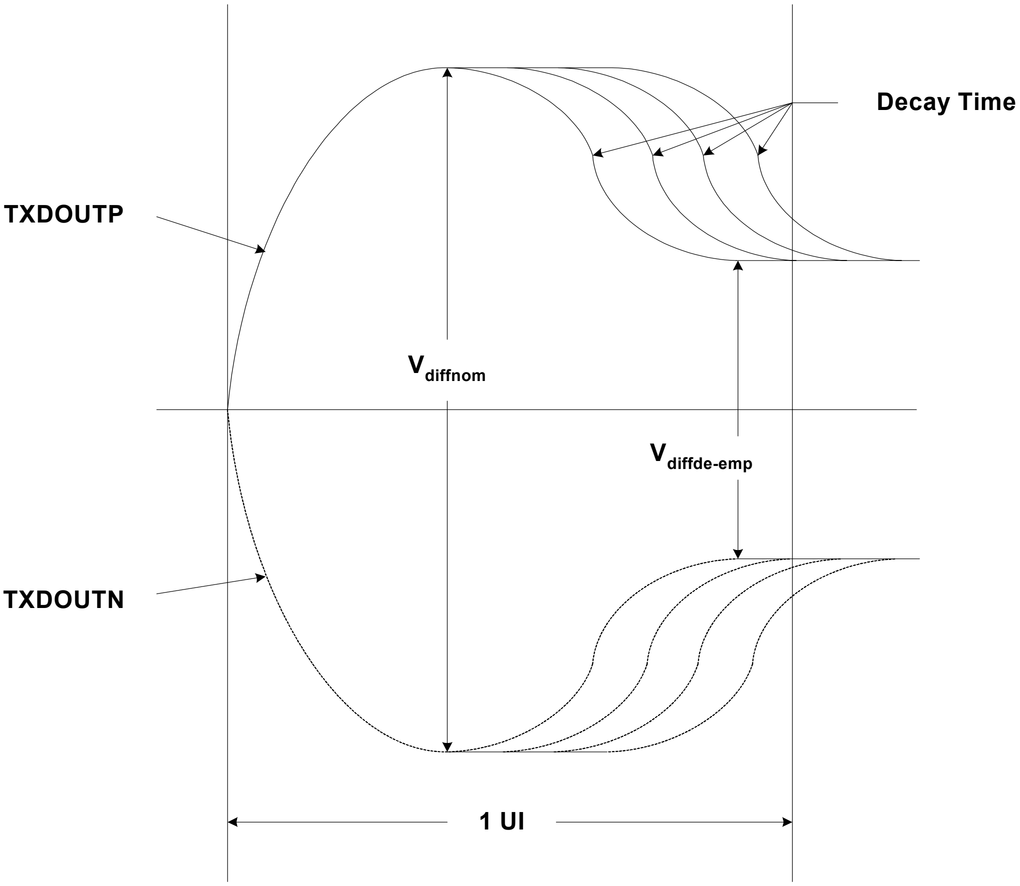
For single-ended operation at the transmitter, the unused TXDOUTP or TXDOUTN signal must be terminated either to VDD in DC couple mode or with a resistor to ground in AC couple mode. The resistor to ground must have a value equal to the characteristic impedance of the copper transmission channel. The TXDOUTP/N outputs can be forced to a static level by asserting TXONOFFI input low.

3.3.9 XFI Transmitter Pre-emphasis and Slew Rate

The XFI output stage includes programmable pre-emphasis, which affects the peaking and decay time (slew rate) of the transmitted bit. The following figure shows the de-emphasized waveform. The figure is for reference only and is not intended to represent an actual waveform.

Figure 22. XFI Data Transmitter Differential Voltage with Pre-emphasis

Pre-emphasis level = $20 \times \mathrm{Log}_{10}(V_{diffnom}/V_{diffde\text{-}emp})$ dB



When used, transmit pre-emphasis shapes the XFI transmitter signal to mitigate dielectric and skin-effect distortion and loss. When signal pre-emphasis is employed, the effects of peaking pre-distortion offsets dielectric and skin-effect distortion, and a higher quality waveform results at the receiving device.

XFI transmitter pre-emphasis settings are programmed by writing to eight bits in register 1xE601[7:0]. The four least significant bits select the inductive peaking level and the four most significant bits adjust the pre-emphasis ratio. Recommended pre-emphasis settings are shown in the following table, along with approximate ratios.

Table 17. XFI Transmitter Pre-emphasis Ratio

Setting for Pre-emphasis Ratio Bits 1xE601.7:4	Setting for Inductor Bits (Slew Rate) 1xE601.3:0	Approximate Ratios
0000 (default)	0000	1.8 dB
0100	0000	2.7 dB
1000	0000	3.3 dB
1111	0000	3.9 dB

Table 17. XFI Transmitter Pre-emphasis Ratio *(continued)*

Setting for Pre-emphasis Ratio Bits 1xE601.7:4	Setting for Inductor Bits (Slew Rate) 1xE601.3:0	Approximate Ratios
0000 (default)	1111	3.8 dB
0100	1111	4.8 dB
1000	1111	6.2 dB
1111	1111	6.4 dB

As a guideline, the default setting is normally sufficient to drive 1 to 2 inches of strip-line or micro-strip transmission line in FR-4. XFI channels with transmission lines that exceed about 2 inches can benefit from increased pre-emphasis adjustment.

3.3.10 Line Rate Divided Clock Outputs

Several divided-down clocks can be selected to exit the VSC8486 at each of two CML clock outputs called CLK64AP/N and CLK64BP/N. Both clock outputs can be disabled using MDIO. CLK64AP/N also has a pin disable: CLK64A_EN. CLK64AP/N, which is normally used to provide an XFP reference clock, defaults to enabled and routes one sixty-forth of the CMU clock rate.

Each clock output driver consists of a differential pair designed to drive a 50 Ω transmission line. Like the high-speed clock output, the output drivers are source-terminated on chip (50 Ω to VDD12TX) to absorb any reflections.

For single-ended operation at the transmitter, the unused output signal must be terminated as close as possible to the characteristic impedance of the transmission line used, which is normally 50 Ω.

The CLK64AP/N and CLK64BP/N outputs provide a similar set of clock signals. CLK64AP/N outputs are normally used for the XFP reference clock. The following table shows the enable and select control logic and available clock outputs for CLK64AP/N.

Table 18. CLK64AP/N Clock Output

TCLKA_EN_SRC (1xE602.6)	TCLKA_EN_REG (1xE602.9)	CLK64A_EN Pin	TCLKA_SEL (1xE602.8:7)	CLK64AP/N Output
0	X	0	XX	Disabled
0 (default)	X	1 (default)	00 (default)	CMU clock divided by 64
0	X	1	01	CMU clock divided by 66
0	X	1	10	CRU clock divided by 64
0	X	1	11	REFCK reference clock
1	0 (default)	X	XX	Disabled
1	1	X	00	CMU clock divided by 64
1	1	X	01	CMU clock divided by 66

Table 18. CLK64AP/N Clock Output *(continued)*

TCLKA_EN_SRC (1xE602.6)	TCLKA_EN_REG (1xE602.9)	CLK64A_EN Pin	TCLKA_SEL (1xE602.8:7)	CLK64AP/N Output
1	1	X	10	CMU clock divided by 64
1	1	X	11	REFCK reference clock

The following table provides the enable and select control logic and available clock outputs for CLK64BP/N.

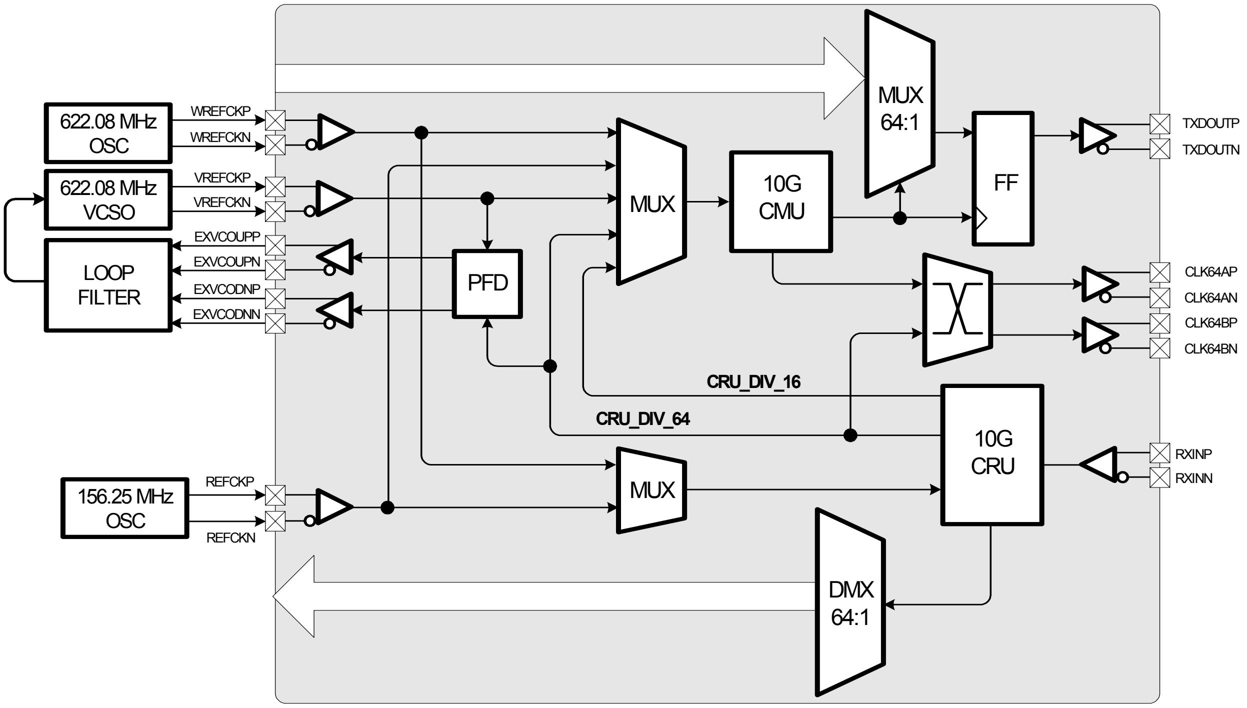
Table 19. CLK64BP/N Clock Output

TCLKB_EN (1xE602.5)	TCLKB_SEL (1xE602.4:3)	CLK64BP/N Output
0 (default)	XX	Disabled
1	00 (default)	CRU clock divided by 64
1	01	CMU clock divided by 66
1	10	CMU clock divided by 64
1	11	Test_Clock (factory use only)

3.3.11 External Phase Lock Loop

An external phase lock loop (PLL) circuit and low phase noise oscillator can be used to transform the VSC8486 IEEE 802.3ae compliant PMA block into a fully GR-253 jitter compliant PMA block in WAN operating mode. The following block diagram shows the required elements.

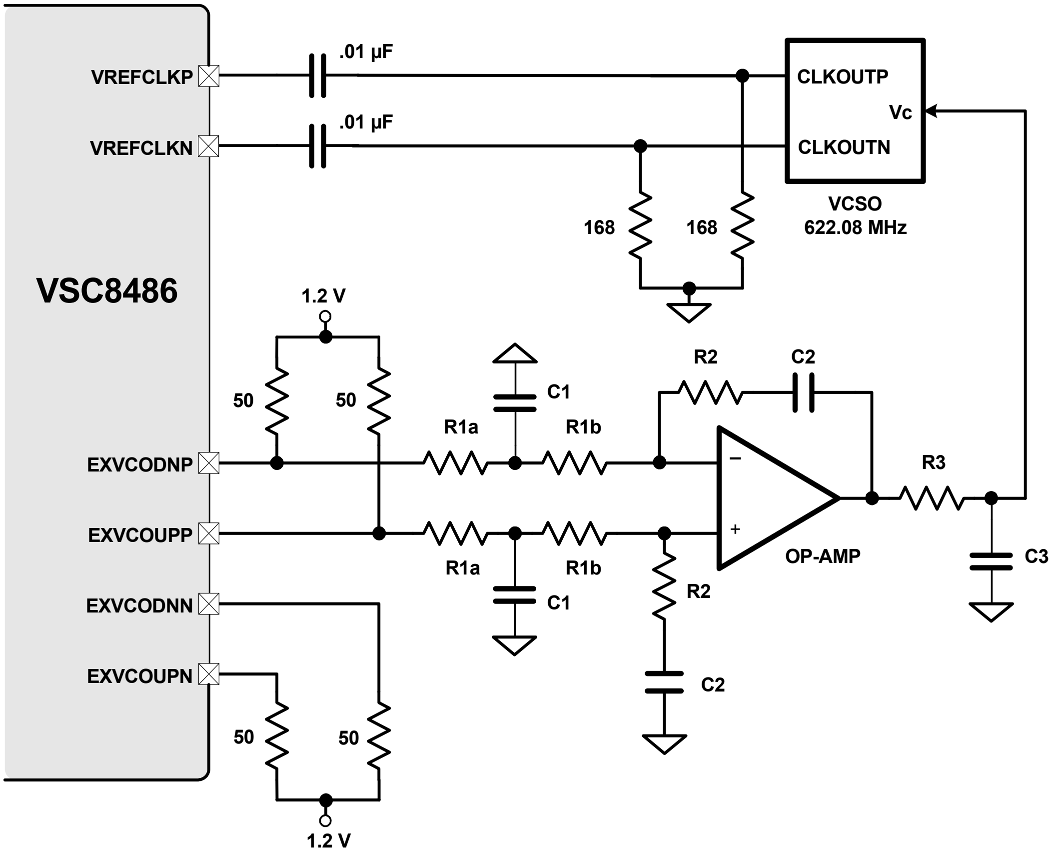
Figure 23. Fully SONET Jitter Compliant Reference Clock Configuration



The preceding figure shows the required elements to achieve SONET Terminal Equipment jitter compliance. Reference clocks must operate at the frequencies shown and each of the 622.08 MHz elements must have SONET quality performance specifications, which is normally based on surface acoustic wave (SAW).

The following figure illustrates a simple schematic diagram showing the significant elements of a typical second-order loop filter PLL topology.

Figure 24. Example External PLL Schematic Diagram



Approximate Filter Values for 100 kHz Loop Bandwidth

R1 = R1a + R1b (kΩ)	C1 (pF)	R2 (kΩ)	C2 (uF)	R3 (kΩ)	C3 (pF)
9.4	22	174	.001	1.0	100

The preceding figure suggests component values to set the loop bandwidth to approximately 100 kHz since the SONET Jitter Transfer 3 dB point is 120 kHz. These values are intended to provide a point of departure for designers and do not guarantee optimal PLL bandwidth or performance. There are other parameters of the PLL design including, but not limited to, peaking, stability, phase noise and damping ratio, which must be considered and are beyond the scope of this document.

3.3.12 High-Speed Serial Data Inputs

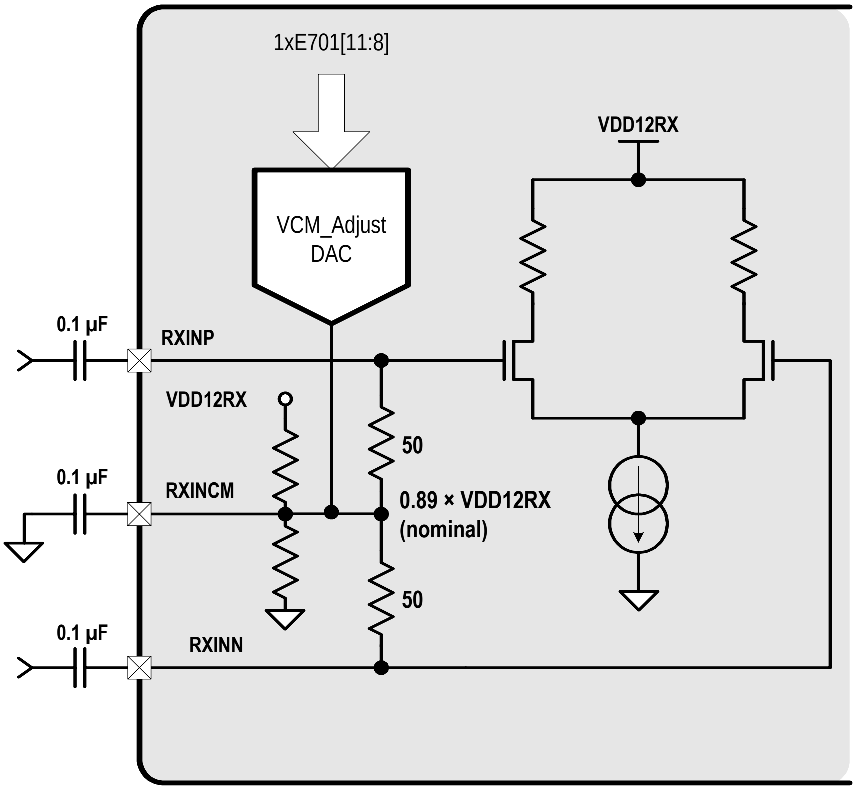
The incoming 10.3125 Gbps (LAN) or 10.51875 Gbps (SAN) or 9.953 Gbps (WAN) data is received by high-speed inputs (RXINP/N). The inputs are terminated internally with 50 Ω to RXINCM, as shown in the following figure. This configuration also forms an impedance equivalent to 100 Ω across the differential pair to terminate the differential mode signal and a center-tapped virtual ground brought out as the RXINCM pin to absorb common mode noise. The receiver's input common mode voltage level is programmable by writing to VCM_ADJ (1xE701.11:6).

The inputs should be AC-coupled to allow for appropriate common mode voltage adjustments. The device can optionally be DC-coupled, which requires proper common mode.

The VSC8486 is designed to operate with XFI signaling based on nominal 100 Ω differential impedance and AC coupling. The AC coupling capacitors on the high-speed serial data inputs (RXINP/N) are expected to be in the XFP module. The RXINCM pin should be AC-coupled to ground through a 0.1 µF capacitor to provide a low impedance AC return path for the 50 Ω termination.

The VSC8486 can also operate in a single-ended mode. The RXINCM pin should be AC-coupled to ground through a 0.1 µF capacitor. The unused input should also be tied to a clean AC ground to prevent the RXINP signal from internally coupling through to RXINN and degrading input sensitivity. Note that the total current through the 50 Ω resistor is limited to 25 mA; therefore, there should never be more than a 1 V difference between RXINP and RXINCM, or between RXINN and RXINCM.

Figure 25. CML XFI Data Receiver



3.3.13 XFI Data Input Receiver Equalization

Incoming data on the RXINP/N inputs might contain a substantial amount of inter-symbol interference (ISI) or deterministic jitter that reduces the ability of the receiver to recover data without errors. A programmable equalizer is provided in the input buffer to compensate for this deterministic jitter. This circuit is designed to effectively reduce the ISI commonly found in the copper PCB traces of an XFI-compliant channel, which can be as long as 12 inches. Typically for FR-4 materials, low frequencies are attenuated less than high frequencies as a result of the skin effect and dielectric losses. See the channel loss model as defined in the XFP multisource agreement.

The RXIP/N input equalizer includes a 2-bit control for peaking and decay to mitigate the effects of FR-4 losses. Overall receiver equalization response is adjusted by setting the four internal register bits, as shown in the following table.

Typical XFP host applications using less than 2 inches of FR-4 do not require modification of the default settings because the VSC8486 default setting includes some intrinsic peaking. For higher loss tangent material and/or XFI channel physical trace lengths exceeding about 2 inches, changing the equalization settings to match those shown in the following table can offer the best performance.

Table 20. Register 1x8002.14:11 RXINP/N Equalization Control

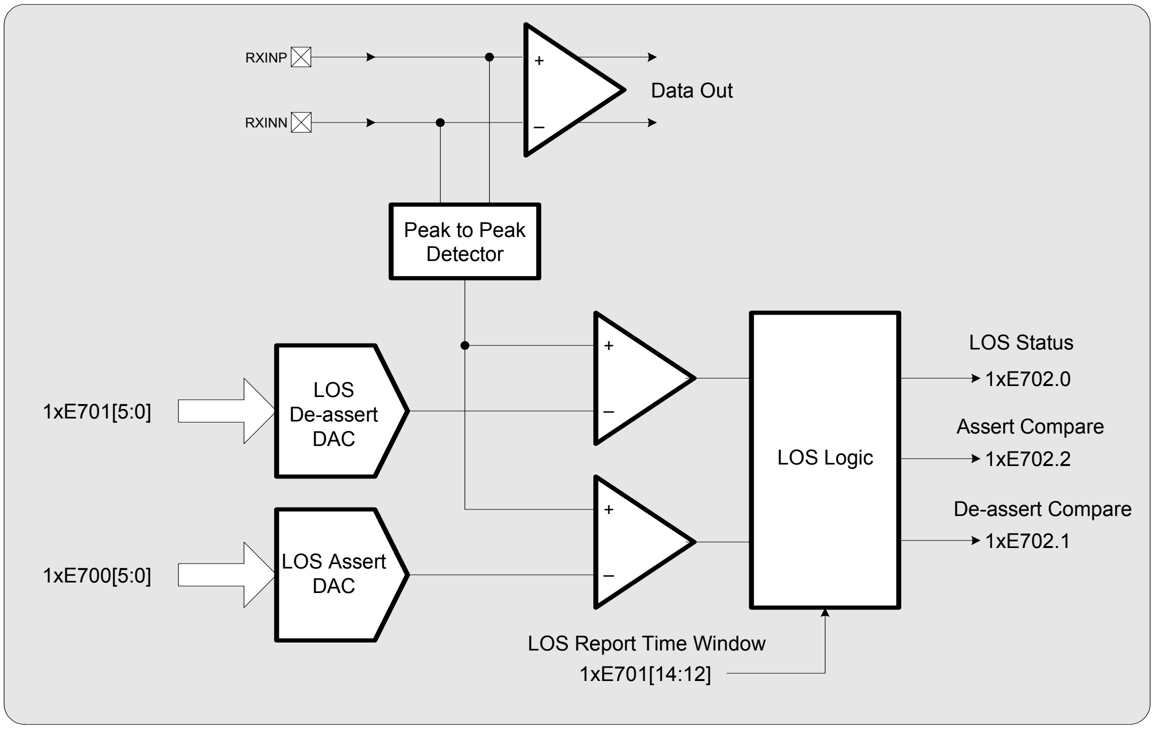
Peaking		Decay		
Bit 14	**Bit 13**	**Bit 12**	**Bit 11**	**Comment**
1	1	1	1	Default (less than 2 inches of FR-4).
1	1	0	0	Recommended for applications greater than 2 inches of FR-4. Recommendations are based on characterization data. Some applications can have optimal settings that diverge from the recommendations.

3.3.14 Loss of Signal (LOS)

The Loss of Signal (LOS) circuitry utilizes peak-to-peak differential signal detection and selectable independent assert and de-assert thresholds to produce an output LOS monitor proportional to the minimum useable signal present at the RXINP/N inputs. The following figure illustrates the PMA LOS block diagram.

The LOS peak-to-peak voltage swing detection is determined by directly sensing the input signal at the input pins. The nominal LOS assert voltage is 50 mV. Calibration and adjustment of the LOS assert and de-assert levels should be expected, because RXINP/N signals vary by application.

Figure 26. PMA LOS Functional Block Diagram



The following table summarizes register access for the VSC8486 PMA LOS functions.

Table 21. PMA LOS Register Status and Control Summary

Register	Name	Function	Remarks
1xE702.0	LOS_STAT	If RXINP/N peak-to-peak signal falls below assert threshold, bit 0 = 1.	
1xE700.5:0	LOS_ASSERT_ DAC (VA_OUT)	LOS assert threshold value. Default is minimum (000000).	Set the LOS assert voltage threshold. 000000: Less than 40 mV. 111111: Greater than 110 mV. All else: Reserved.
1xE701.5:0	LOS_DEASSERT_DAC (VDA_OUT)	LOS de-assert threshold value. Default is minimum (000000).	Set the LOS de-assert voltage threshold. 000000: Less than 40 mV. 111111: Greater than 110 mV. All else: Reserved.
1xE701.14:12	LOS_WIN	LOS reported or cleared when signal falls below assert threshold or remains above the de-assert threshold within these approximate time interval limits.	LOS report range is 50 µs to 100 µs. LOS clear range is 125 µs to 250 µs. The same 3 bits simultaneously change LOS report and clear times from minimum (000) to maximum (111).

Table 21. PMA LOS Register Status and Control Summary *(continued)*

Register	Name	Function	Remarks
1xE702.1	LOS_DEASSERT_STAT	Bit 1 indicates de-assert threshold crossed.	In normal operation, the de-assert threshold is crossed when the peak-to-peak signal is increased following an LOS report.
1xE702.2	LOS_ASSERT_STAT	Bit 2 indicates assert threshold crossed.	In normal operation, the assert threshold is crossed when the peak-to-peak signal falls below a useable range. This range might require adjustment.
1xE701.15	LOS_PWR_DWN	Bit 15 set to 1 disables PMA LOS.	Default is LOS enabled, bit 15 = 0.

3.3.15 Loss of Optical Carrier (LOPC)

LOPC is an input pin for the VSC8486 that is normally connected to the XFP LOS output. Any change in level on the LOPC input asserts LOPC_PEND (2xEF04.11) until read. The current status of the LOPC input pin can be read using LOPC_STAT (2xEF03.11). The LOPC input can be active high or active low by setting the LOPC_POL_SEL (2xEC30.9) bit appropriately. The LOPCS_PEND bit can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask-enabled bits LOPC_MASKA (2xEF05.11) and LOPC_MASKB (2xEF06.11). For WIS applications, the LOPC input can be configured to initiate a line remote defect indication (RDI-L).

3.4 WAN Interface Sublayer (WIS)

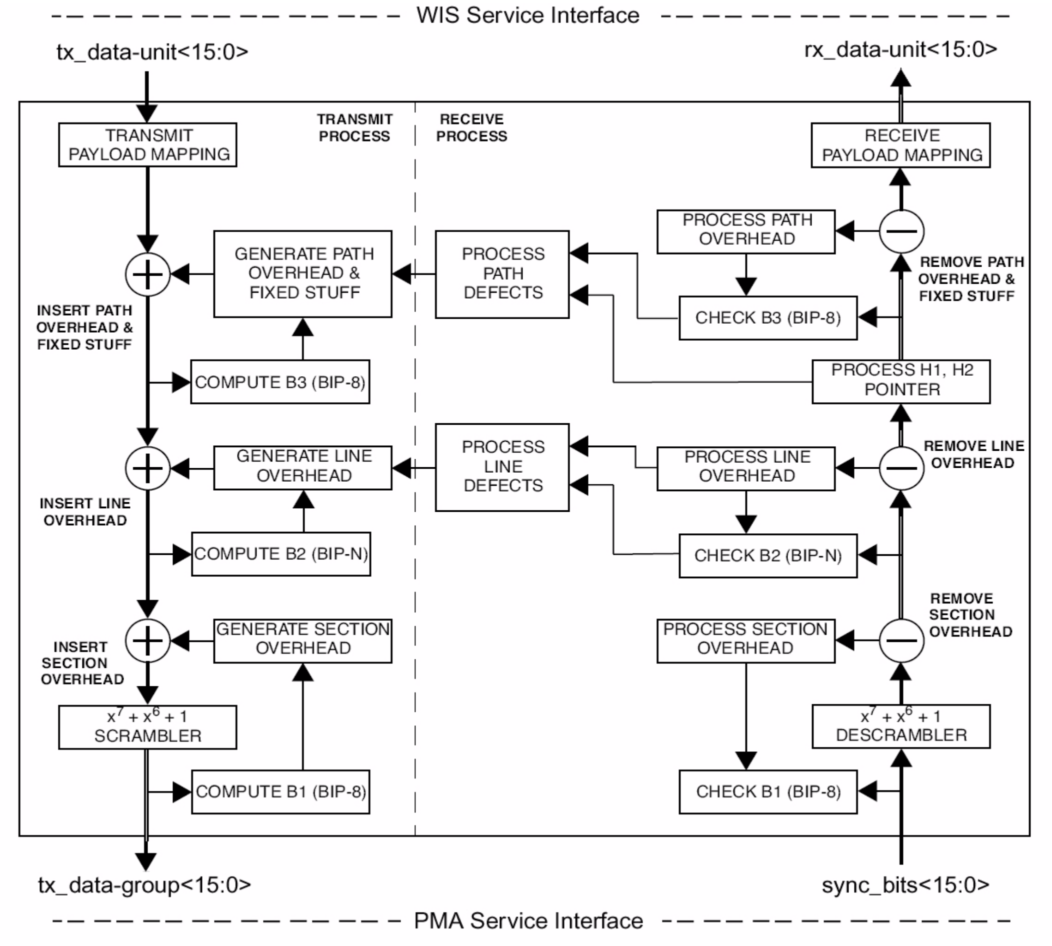
The WAN interface sublayer (WIS) is defined in IEEE Standard 802.3ae Clause 50. The VSC8486 WIS block is fully compliant with this specification. The VSC8486 offers additional controls, ports, and registers to allow integration into a wider array of SONET/SDH equipment. Clocking requirements are a critical component for SONET/SDH equipment as discussed in earlier sections.

In addition to the SONET/SDH features addressed by WIS as defined by IEEE, most SONET/SDH framers/mappers contain additional circuitry for implementing Operation, Administration, Maintenance and Provisioning (OAM&P). These framers/mappers also support special features to enable compatibility with legacy SONET/SDH solutions. Because the VSC8486 WIS leverages Vitesse industry leading framer/mapper technology it contains suitable features for standard SONET/SDH equipment. This includes the Transmit/Receive Overhead Serial Interfaces (TOSI/ROSI) commonly used for network customization and OAM&P, support for SONET/SDH errors not contained in the WIS standard, support for common legacy SONET/SDH implementations, and SONET/SDH jitter and timing quality.

3.4.1 WIS Functional Description

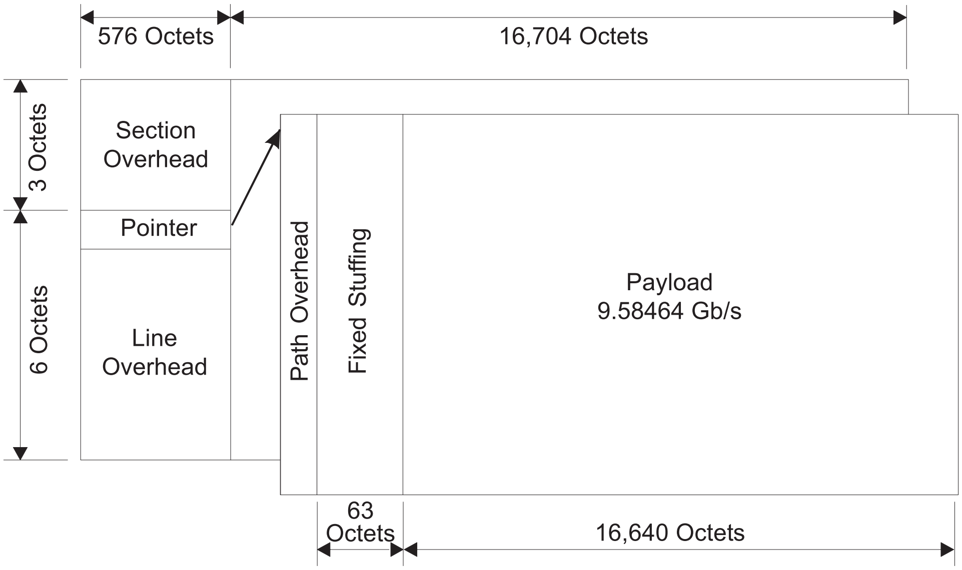
The transmit portion of the WIS maps data from the PCS through the WIS service interface and to the SONET/SDH synchronous payload envelope (SPE). It then generates path, line, and section overhead octets, scrambles the frame, and transmits the frame to the PMA Service Interface. The receive portion of the WIS does the following: receives data from the PMA service interface; delineates octet and frame boundaries; descrambles the frame; processes section, line, and path overhead information that contain alarms and parity errors; interprets the pointer field; and extracts the payload for transmittal to the PCS through the WIS service interface. The WIS block diagram is shown in the following figure.

Figure 27. WIS Transmit and Receive Functions



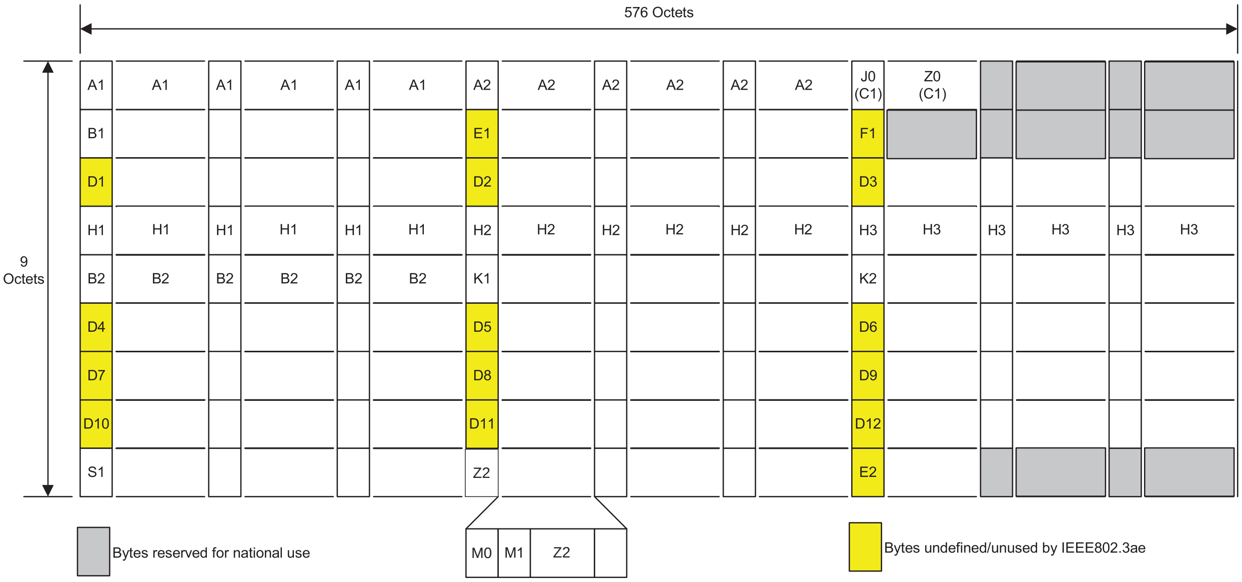
The WIS frame structure is illustrated in the following figure.

Figure 28. WIS Frame Structure



The positions of the section and line overhead octets within the WIS Frame are illustrated in the following figure.

Figure 29. STS-192c/STM-64 Section and Line Overhead Structure



A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	J0 (C1)	Z0 (C1)	▨	▨	▨	▨
B1						E1						F1	▨	▨	▨	▨	▨
D1						D2						D3					
H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3
B2	B2	B2	B2	B2	B2	K1						K2					
D4						D5						D6					
D7						D8						D9					
D10						D11						D12					
S1						Z2						E2		▨	▨	▨	▨

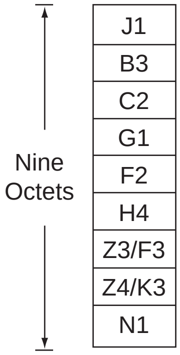
M0	M1	Z2	

▨ Bytes reserved for national use

🟨 Bytes undefined/unused by IEEE802.3ae

The path overhead octet positions are depicted in the following figure.

Figure 30. Path Overhead Octets



3.4.2 WIS Section Overhead Description

The section overhead portion of the SONET/SDH frame supports frame synchronization, a tandem connection monitor (TCM) known as the Section trace, a high-level parity check, and some OAM&P octets. The following table lists each of the octets including their function, specification, and related information.

Note The VSC8486 provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis.

Table 22. Section Overhead

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
A1	Frame alignment	Supported	0xF6	Register (2xE611) TOSI and ROSI access.
A2	Frame alignment	Supported	0x28	Register (2xE611) TOSI and ROSI access.
J0	Section trace	Specified value	See the discussion of J0 (Section Trace)	A 1-byte, 16-byte, or 64-byte trace message can be sent using registers 2x0040 to 2x0047, 2xE700, or 2xE800 to 2xE817 and received using registers 2x0048 to 2x004F, 2xEC20, and 2xE900 to 2xE917. TOSI and ROSI access.
Z0	Reserved for section growth	Unsupported	0xCC	Register 2xE612 TOSI and ROSI access.
B1	Section error monitoring (Section BIP-8)	Supported	Bit interleaved parity - 8 bits, as specified in T1.416	Using the TOSI, the B1 byte can be masked for test purposes. For each B1 mask bit that is cleared to 0 on the TOSI interface, the transmitted bit is left unchanged. For each B1 mask bit that is set to 1 on the TOSI interface, the transmitted bit is inverted. Using the ROSI, the B1 error locations can be extracted. Periodically latched counter (2xECB0-2xECB1) is available.

Table 22. Section Overhead *(continued)*

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
E1	Orderwire	Unsupported	0x00	Register 2xE612 TOSI and ROSI access.
F1	Section user channel	Unsupported	0x00	Register 2xE613 TOSI and ROSI access.
D1-D3	Section data communications channel (DCC)	Unsupported	0x00	Register 2xE613 to 2xE614 TOSI and ROSI access.

A1, A2 (Frame Alignment) The SONET/SDH protocol is based upon a frame structure which is delineated by the framing octets, A1 and A2. The framing octets are defined to be 0xF6 and 0x28 respectively. In the transmit direction all 192 A1 octets are sourced from the TX_A1 (2xE611.15:8) register while the A2 octets are sourced from the TX_A2 (2xE611.7:0) register.

In the receive direction, the frame aligner monitors the input bus from the PMA and performs word alignment. The frame alignment architecture is composed of a primary and secondary state machine. The primary state diagram is shown in the following figure and the variables for the primary state diagram are shown in the following table. The variables are reflected in registers EWIS_RX_FRM_CTRL1 (2xEC00) and EWIS_RX_FRM_CTRL2 (2xEC01) which can be alternately reconfigured. The selected frame alignment and synchronization pattern have implications on the tolerated input BER. The higher the input BER, the less likely the frame boundary can be found. The chances of finding the frame boundary are improved by reducing the number of A1/A2 bytes required to be detected (using a smaller pattern width). According to the WIS specification, the minimum for all parameters allows a signal with an error tolerance of 10^{-12} to be framed.

Figure 31. Primary Synchronization State Diagram

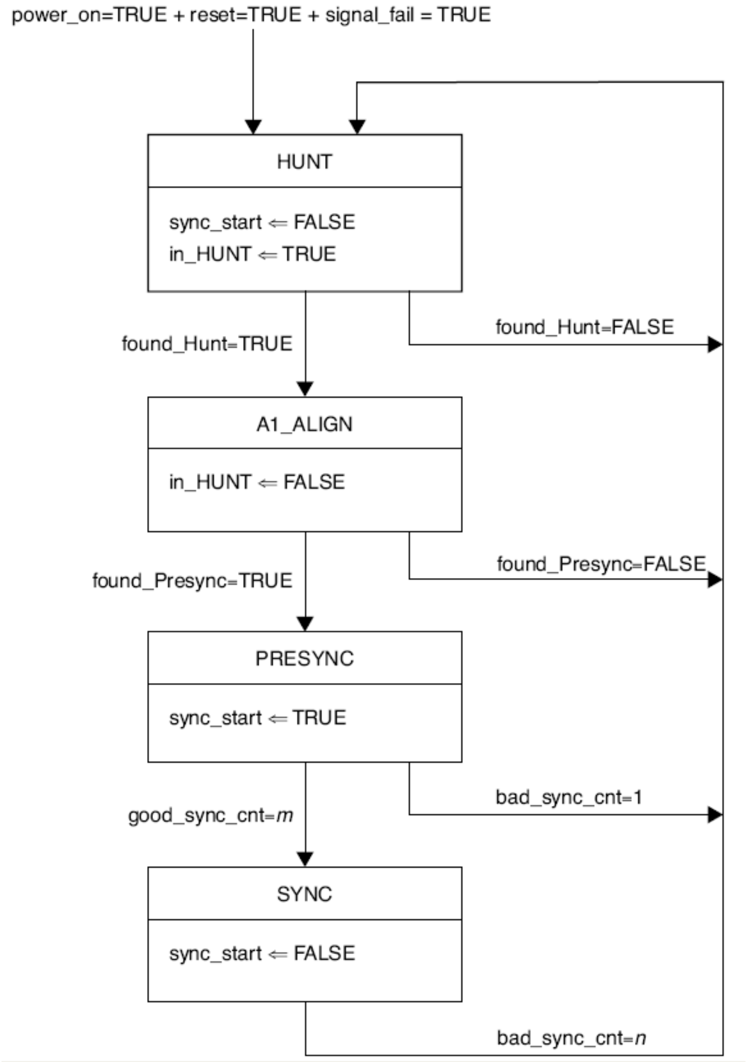
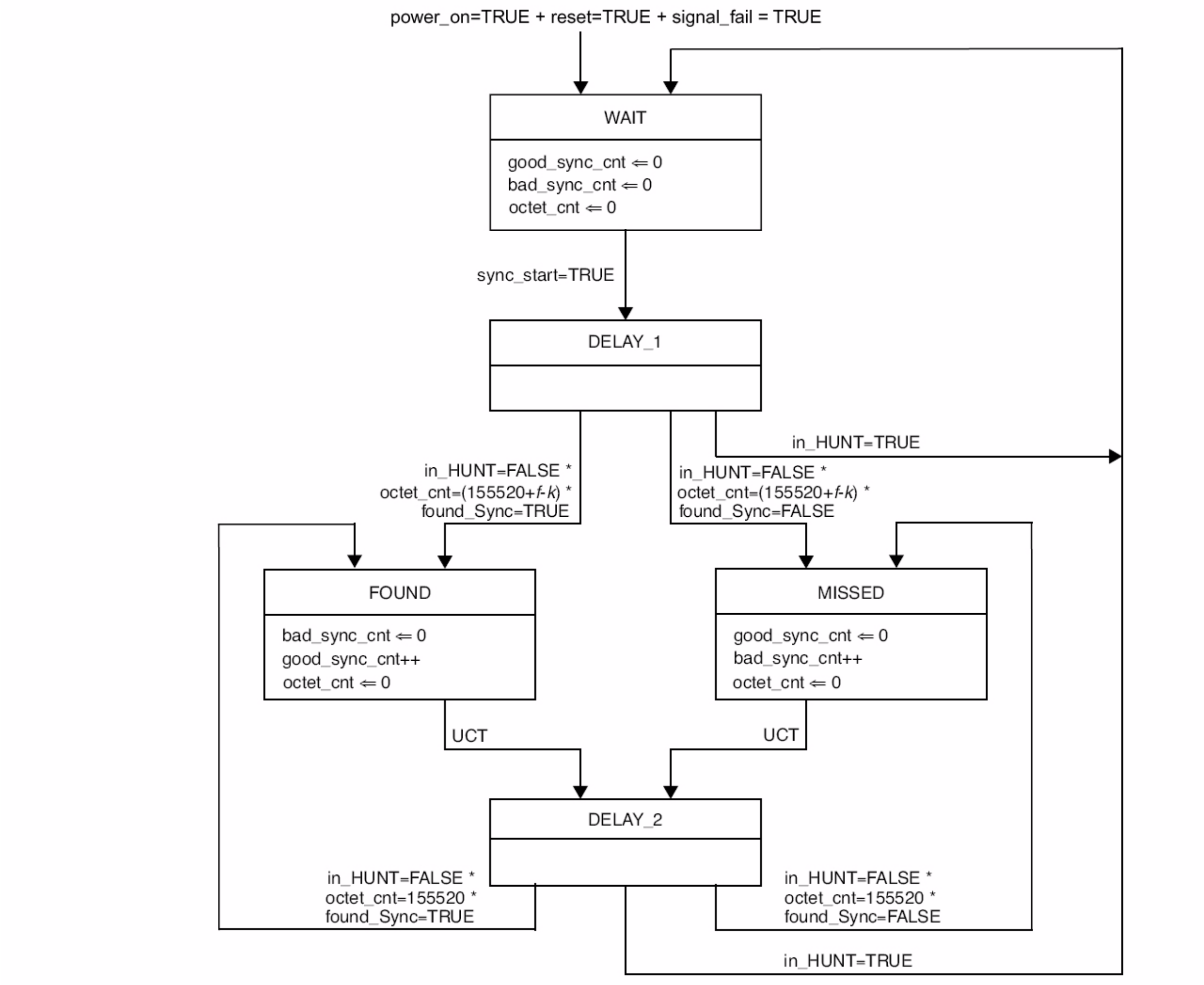


Figure 32. Secondary Synchronization (Interval Pattern Search) State Diagram



The following table describes the variables for the primary state diagram.

Table 23. Framing Parameter Description and Values

Name	Description	IEEE 802.3ae Parameter	IEEE 802.3ae Range	VSC8486 Range	VSC8486 Default
Sync_Pattern width	Sequence of f consecutive A1s followed immediately by a sequence of f consecutive A2s. If f = 2, Sync_Pattern is A1A1A2A2.	f	2 to 192	0 to 16. Exceptions: If f = 0, Sync_Pattern is A1 + 4 MSBs of A2. If f = 1, Sync_Pattern is A1A1A2.	2
Hunt_Pattern width	Sequence of i consecutive A1s.	i	1 to 192	1 to 16.	4

Table 23. Framing Parameter Description and Values *(continued)*

Name	Description	IEEE 802.3ae Parameter	IEEE 802.3ae Range	VSC8486 Range	VSC8486 Default
Presync_Pattern A1 width	Presync_Pattern consists of a sequence of j consecutive A1s followed immediately by a sequence of k consecutive A2s.	j	16 to 190	1 to 16. If set to 0, behaves as if set to 1. If set to 17 to 31, behaves as if set to 16.	16
Presync_Pattern A2 width	Presync_Pattern consists of a sequence of j consecutive A1s followed immediately by a sequence of k consecutive A2s.	k	16 to 192	0 to 16. 0 means only 4 MSB of A2 are used. If set to 17 to 31, behaves as if set to 16.	16
SYNC state entry	Number of consecutive frame boundaries needed to be found after entering the PRESYNC state in order to enter the SYNC state.	m	4 to 8	1 to 15. If set to 0, behaves as if set to 1.	4
SYNC state exit	Number of consecutive frame boundary location errors detected before exiting the SYNC state.	n	1 to 8	1 to 15. If set to 0, behaves as if set to 1.	4

Loss of Signal (LOS) The SONET/SDH Loss of Signal (LOS) alarm is tied to the PMA input receiver logic discussed in "Loss of Signal (LOS)," page 51. The LOS (2x0021.6) alarm is a latch-high register; back-to-back reads provide both the event as well as status information. The LOS event also asserts the LOS_PEND (2xEF00.6) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOS_MASKA (2xEF01.6) and LOS_MASKB (2xEF02.6).

When the near end device experiences a LOS condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end for notification purposes. The TXRDIL_ON_LOS (2xEE00.2), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force a AIS-L state (alarm assertion plus forcing the payload to an all ones state) upon a detection of an LOS condition. This is accomplished by asserting RXAISL_ON_LOS (2xEE00.5).

Loss of Optical Carrier (LOPC) The input pin LOPC can be used by external optic components to directly assert the loss of optical power to the physical media device. Any change in level on the LOPC input asserts LOPC_PEND (2xEF04.11) until read. The current status of the LOPC input pin can be read using LOPC_STAT (2xEF03.11). The LOPC input can be active high or active low by setting the LOPC_POL_SEL (2xEC30.9) bit appropriately. The LOPCS_PEND bit can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOPC_MASKA (2xEF05.11) and LOPC_MASKB (2xEF06.11).

When the near end device experiences a LOPC condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end to notify it of a problem. The TXRDIL_ON_LOPC (2xEE00.3), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force the receive framer into a LOF state, thereby squelching subsequent alarms and invalid payload data processing. This is accomplished by asserting RXLOF_ON_LOPC (2xEC30.8). Similar to the LOF condition forced upon an LOPC, the RXAISL_ON_LOPC (2xEE00.6) can force the AIS-L alarm assertion, plus force the payload to an all ones state to indicate to the PCS the lack of valid data, upon an LOPC condition.

Severely Errored Frame (SEF) Upon reset, the VSC8486 enters the out of frame (OOF) state with both the severely errored frame (SEF) and loss of frame (LOF) alarms active. The SEF defect is terminated when the framer enters the SYNC state. The framer enters the SYNC state after SYNC_ENTRY_CNT (2xEC01.7:4) plus 1 consecutive frame boundaries are identified. A SEF defect state is declared when the framer enters the out-of-frame (OOF) state. The frame changes from the SYNC state to the OOF state when SYNC_EXIT_CNT (2xEC01.3:0) consecutive frames with errored frame alignment words are detected. SEF is indicated by asserting SEF (2x0021.11). This register latches high providing a combination of interrupt pending and status information within consecutive reads.

An additional bi-stable interrupt pending bit SEF_PEND (2xEF00.11) is provided which can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits SEF_MASKA (2xEF01.11) and SEF_MASKB (2xEF02.11).

Loss of Frame (LOF) An LOF occurs when an out of frame state persists for an integrating period of LOF_T1 (2xEC02.11:6) frames. To provide for the case of intermittent OOFs, when not in the LOF state, the integrating timer is not reset to zero until an in-frame condition persists continuously for LOF_T2 (2xEC02.5:0) frames. Once in the LOF state, this state is left when the in-frame state persists continuously for LOF_T3 (2xEC03.6:1) frames. The LOF state is indicated by LOF (2x0021.7) being asserted. This register latches high, providing a combination of pending and status information over consecutive reads.

An additional bi-stable interrupt pending bit LOF_PEND (2xEF00.7) is provided which can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOF_MASKA (2xEF01.7) and LOF_MASKB (2xEF02.7).

When the near end device experiences a LOF condition, it might be required that the far end device be notified of the catastrophic condition. Transmitting an alarm indication signal (AIS-L) can accomplish this. If AISL_on_LOF (2xEE00.4) is asserted, the transmit path is preempted by the AIS-L pattern whenever an LOF alarm condition is asserted.

When the near end device experiences a LOF condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end to notify it of a problem. The TXRDIL_ON_LOF (2xEE00.1), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force a AIS-L state (alarm assertion plus forcing the payload to an all ones state) upon a detection of an LOF condition. This is accomplished by asserting RXAISL_ON_LOF (2xEE00.4).

J0 (Section Trace) The J0 octet often carries a repeating message called the Section Trace Message. The default transmitted message length is 16-octets whose contents are defined in J0_TXMSG (2x0040-2x0047). If no active message is being broadcast, a default Section Trace Message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000 shall be transmitted. The header octet for the 15-octets of zero would be 0x89. The default values of J0_TXMSG (2x0040-2x0047) do not contain the 0x89 value of the header octet, so software must write this value.

The J0 octet in the receive direction by default is assumed to be carrying a 16-octet continuously repeating Section Trace Message. The message is extracted from the incoming WIS frames and stored in J0_RXMSG (2x0048-2x004F). The WIS receive process does not delineate the message boundaries, thus the message might appear rotated between new frame alignment events.

The VSC8486 supports two alternate message types, a single repeating octet and a 64-octet message. The message type can be independently selected for the transmit and receive direction. The transmit direction is configured using J0_TXLEN (2xE700.3:2) while J0_RXLEN (2xEC20.3:2) configures the receive path.

When the transmit direction is configured for a 64-octet message the first 16 octets are programmed in J0_TXMSG (2x0040-2x0047) while the 48 remaining octets are programmed in J0_TXMSG64 (2xE800-2xE817). Likewise, the first 16 octets of the receive message are stored in J0_RXMSG (2x0048-2x004F) while the other 48 octets are stored in J0_RXMSG64 (2xE900-2xE917). The receive message is updated every 125 µs with the recently received octet. Any persistency or message matching is expected to take place within the station manager.

Z0 (Reserved for Section Growth) The WIS standard does not support the Z0 octet and requires transmission of 0xCC in the octet locations. A different Z0 value can be transmitted by configuring TX_Z0 (2xE612.15:8). The TX_Z0 default is 0xCC.

Scrambling/Descrambling The transmit signal (except for row 1 of the section overhead) is scrambled according to the standards when SCR_EN (2xE600.12) is asserted, which is the default state. When deasserted, the scrambler is disabled.

The receive signal descrambler DESCR_EN (2xEC10.1) is enabled by default; however, by deasserting this bit the descrambler can be bypassed.

B1 (Section Error Monitoring) The B1 octet is a bit interleaved parity-8 (BIP-8) code using even parity calculated over the previous STS-192c frame, post scrambling. The computed BIP-8 is placed in the following outgoing SONET frame before scrambling.

In the receive direction, the incoming frame is processed and a BIP-8 is calculated. The calculated value is then compared with the B1 value received in the following frame. The difference between the calculated and received octets are accumulated into B1_CNT (2x003C). This counter rolls over after the maximum count. This counter is cleared upon device reset.

The B1_ERR_CNT[1:0] (2xECB0 to 2xECB1) registers provide a count of the number of received B1 parity errors. This register is updated with the internal count value upon a PMTICK condition, after which the internal counter is reset to zero. When the counter is nonzero, the B1_NZ_PEND (2xEF04.7) event is asserted until read. A non-latch high version of this event, B1_NZ_STAT (2xEF03.7) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits B1_ERR_MASKA (2xEF05.7) and B1_ERR_MASKB (2xEF06.7).

The B1_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. This mode is enabled by asserting B1_BLK (2xEC61.11)

E1 (Section Orderwire) The WIS standard does not support the E1 octet and requires transmission of 0x00 in the octet location. A different E1 value can be transmitted by configuring TX_E1 (2xE612.7:0) whose default is 0x00.

F1 (Section User Channel) The WIS standard does not support the F1 octet and requires transmission of 0x00 in the octet location. A different F1 value can be transmitted by configuring TX_F1 (2xE613.15:8) whose default is 0x00.

DCC-S (Section Data Communication Channel) The WIS standard does not support the DCC-S octets and requires transmission of 0x00 in the octet locations. Different DCC-S values can be transmitted by configuring TX_D1 (2xE613.7:0), TX_D2 (2xE614.15:8), and TX_D3 (2xE614.7:0), all of which default to 0x00.

Reserved, National and Unused Octets The VSC8486 transmits 0x00 for all Reserved, National, and unused overhead octets.

3.4.3 WIS Line Overhead Description

The line overhead portion of the SONET/SDH frame supports pointer interpretation, a per channel parity check, protection switching information, synchronization status messaging, far end error reporting, and some OAM&P octets. The following table lists each of the octets including their function, specification, and related information.

Note The VSC8486 provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis.

Table 24. Line Overhead Octets

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
H1-H2	Pointer	Specified value	SONET mode: STS-1: 0x62, 0x0A STS-n: 0x93, 0xFF SDH mode: STS-1: 0x6A, 0x0A STS-n: 0x9B, 0xFF	Register 2xE615 to 2xE616 TOSI and ROSI access.
H3	Pointer action	Specified value	0x00	Register 2xE616 TOSI and ROSI access.
B2	Line error monitoring (line BIP-1536)	Supported	Bit interleave parity-8, as specified in T1.416	Using the TOSI, the B2 bytes can be masked for test purposes. For each B2 mask bit that is cleared to 0 on the TOSI interface, the transmitted bit is left unchanged. For each B2 mask bit that is set to 1 on the TOSI interface, the transmitted bit is inverted. Using the ROSI, the B2 error locations can be extracted. Periodically latched counter (2xECB0-2xECB1) is available.
K1, K2	Automatic protection switch (APS) channel and line remote defect identifier (RDI-L)	Specified value	For information about K2 coding, see Table 25, page 65	Register 2xE617 to 2xE618 TOSI and ROSI access.

Table 24. Line Overhead Octets *(continued)*

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
D4-D12	Line data communications channel (DCC)	Unsupported	0x00	Register 2xE619 to 2xE61E TOSI and ROSI access.
S1	Synchronization messenging	Unsupported	0x0F	Register 2xE61F TOSI and ROSI access.
Z1	Reserved for Line growth	Unsupported	0x00	Register 2xE61F TOSI and ROSI access.
M0/M1	STS-1/N line remote error indication (REI)	M0 unsupported, M1 supported	0x00/number of detected B2 errors in the receive path, as specified in T1.416	TOSI and ROSI access. The VSC8486 supports a mode that uses only M1 to back report REI-L (REI_MODE = 0) and another mode which uses both M0 and M1 to back report REI-L (REI_MODE = 1). For more information, see the following B2 text.
E2	Orderwire	Unsupported	0x00	Register 2xE620 TOSI and ROSI access.
Z2	Reserved for Line growth	Unsupported	0x00	Register 2xE620 TOSI and ROSI access.

B2 (Line Error Monitoring) The B2 octet is a BIP-8 value calculated over each of the previous STS-1 channels excluding the section overhead and pre-scrambling. As the B2 octet is calculated on an STS-1 basis there are 192 B2 octets within an STS-192/STM-64 frame. Each of the 192 calculated BIP-8 octets are then placed in the outgoing SONET/SDH frame.

In the receive direction, the incoming frame is processed, and a per STS-1 BIP-8 is calculated (excluding section overhead and after descrambling) and then compared to the B2 value in the following frame. Errors are accumulated into a 32-bit counter B2_CNT (2x0039-2x003A). This counter is non-saturating and so rolls over after its maximum count. The counter is cleared only on device reset.

An additional 32-bit B2 error counter is provided at B2_ERR_CNT (2xECB2-2xECB3), which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the B2_NZ_PEND (2xEF04.6) event is asserted until read. A non-latch high version of this event B2_NZ_STAT (2xEF03.6) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on mask enable bits B2_ERR_MASKA (2xEF05.6) and B2_ERR_MASKB (2xEF06.6).

The B2_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. This mode is enabled by asserting B2_BLK (2xEC61.10).

It is possible that two sets of B2 bytes (from two SONET/SDH frames) are received by the Rx WIS logic in a period of time when only one M0/M1 octet is transmitted. In this situation, one of the two B2 error counts delivered to the Tx WIS logic is discarded. This situation occurs when the receive data rate is faster than the transmit data rate. Similarly, when the transmit data rate is faster than the receive data rate, a B2 error count is not available for REI-L insertion into the M0/M1 octets of the transmitted SONET/SDH frame. A value of zero is transmitted in this case. This behavior is achieved by using a FIFO to transfer the detected B2 error count from the receive to transmit domains.

A FIFO overflow or underflow condition is not considered an error. Instead it is recovered from gracefully as described above. A FIFO overflow or underflow eventually occurs unless the transmit and receive interfaces are running at the same average data rate. Because the received and transmitted frames can differ by, at most, 40 ppm (±20 ppm) and still meet the industry standards, this “slip” can happen no more often than once every 3.1 seconds.

K1, K2 (APS Channel and Line Remote Defect Identifier) The K1 and K2 octets carry information regarding Automatic Protection Switching (APS) and Line Remote Defect Identifier (RDI-L). The K1 octet and the most significant five bits of the K2 octet contain the APS channel information. The transmitted values can be configured at TX_K1 (2xE617.7:0) and TX_K2 (2xE618.15:8). The default values of all zeros are compliant with the WIS standard.

The three least significant bits within the K2 octet carry the RDI-L encoding, as defined by section 7.4.1 of ANSI T1.416-1999 and as shown in the following table.

Table 25. K2 Encodings

Indicator	K2 Value for Bits 6, 7, 8	Interpretation
RDI-L	110	Remote error indication. For the receive process, an RDI-L defect occurs after a programmable number of RDI-L signals are received in contiguous frames and is terminated when no RDI-L is received for the same number of contiguous frames. An RDI-L can be forced by asserting FRC_RX_RDIL (2x2xEC30.2). For the transmit process, the WIS standard does not indicate when or how to transmit RDI-L. VSC8486 provides the option of transmitting K2 by programming it through the TOSI, by programming it using the K2_TX MDIO register, or by programming it based on the contents of the K2_TX register with bits 6, 7, and 8 modified depending on the status of the following: LOPC, LOS, LOF, AIS-L and their associated transmit enable bits TXRDIL_ON_LOPC (2xEE00.3), TXRDIL_ON_LOS (2xEE00.2), TXRDIL_ON_LOF (2xEE00.1), and TXRDIL_ON_AISL (2xEE00.0).
AIS-L	111	Alarm indication signal (line). For the receive process, this is detected based on the settings of the K2 byte. When AIS-L is detected, the WIS link status is down and MDIO register 2x0021.4 is set high. This also contributes to errored second (ES) and severally errored second (SES) reports. For standard WIS operation, this is never transmitted.
Idle (normal)	000	Unless RDI-L exists, the standard WIS transmits idle.

Although the transmission of RDI-L is not explicitly defined within the WIS standard, the VSC8486 allows the automatic transmission of RDI-L upon the detection of LOPC, LOS, LOF, or AIS-L conditions. These features are enabled by asserting RDIL_ON_LOPC (2xEE00.3), RDIL_ON_LOS (2xEE00.2), RDIL_ON_LOF (2xEE00.1), and RDIL_ON_AISL (2xEE00.0).

The VSC8486 can force an RDI-L condition independent of the K2 transmit value by asserting FRC_RDIL (2xE600.2). Likewise, an AIS-L condition can be forced by asserting FRC_AISL (2xE600.1). If both conditions are forced, the AIS-L value is transmitted.

In the receive direction the RDI-L alarm (K2[6:8] = 110, using SONET nomenclature) and the AIS-L alarm (K2[6:8] = 111, using SONET nomenclature) are not asserted until the condition persists for a programmable number of contiguous frames. This value is programmable at APS_THRES (2xEC30.7:4) and is typically set to values of 5 or 10.

The WIS standard defines RDIL (2x0021.5) and AISL (2x0021.4) as a read only latch-high register, so a read of a one in this register indicates that an error condition occurred since the last read. A second read of the register provides the current status of the event as to whether the alarm is currently asserted. RDIL_PEND (2xEF00.5) and AISL_PEND (2xEF00.4) assert whenever the RDI-L or AIS-L state changes (assert or deassert). These interrupts have associated mask enable bits, RDIL_MASK/AISL_MASK (2xEF01.5:4/2xEF02.5:4), which, if enabled, propagate an interrupt to the WIS_INTA/B pins.

For test purposes, the VSC8486 can induce an RDI-L condition in the receive direction independent of the received K2 value by asserting FRC_RX_RDIL (2xEC30.2). Likewise, an AIS-L condition can be forced in the receive direction by asserting FRC_RX_AISL (2xEC30.3).

AISFORCE Pin When set high, the AISFORCE pin generates a near end AIS-L defect.

D4 to D12 (Line Data Communications Channel) The WIS standard does not support Line Data Communications Channel (L-DCC) octets (D4-D12) and recommends transmitting 0x00 within these octets. The D4-D12 transmitted values can be programmed at (2xE619-2xE61E). The register defaults are all 0x00. The receive L-DCC octets are only accessible through the ROSI port.

M0 and M1 (STS-1/N Line Remote Error Indication) The M0 and M1 octets are used for back reporting the number of B2 errors received, known as remote error indication (REI-L). The value in this octet comes from the B2 error FIFO, as discussed with the B2 octet. The WIS standard does not support the M0 octet and recommends transmitting 0x00 in place of the M0 octet. However, the WIS standard supports the M1 octet in accordance with T1.416.

Two methods for back-reporting exist and are controlled by G707_2000_REIL (2xEC40.12). Because a single frame can contain up to 1536 B2 errors while the M1 byte alone can only back report a maximum of 255 errors, a discrepancy exists. When G707_2000_REIL is de-asserted, only the M1 byte is used and a maximum of 255 errors are back-reported. When G707_2000_REIL is asserted, two octets per frame are used for back reporting, the M1 octet and the M0 octet (not the first STS-1 octet, but the second STS-1 octet). In this mode, a total of 1536 errors can be back-reported per frame.

In the receive direction the VSC8486 detects and accumulate errors according to the G707_2000_REIL setting. The VSC8486 deviates from the G.707 standard by not interpreting REI-L values greater than 1536 as zero. The WIS standard defines a 32-bit REI-L counter REIL_CNT (2x0037-2x0038). This counter is non-saturating and so rolls over after its maximum count. The counter is cleared only on device reset.

An additional 32-bit REI-L counter is provided at REIL_ERR_CNT (2xEC90-2xEC91) which is a saturating counter and is latched and cleared based upon a PMTICK event.

Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the REIL_NZ_PEND (2xEF04.2) event is asserted until read. A non-latch high version of this event REIL_NZ_STAT (2xEF03.2) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits REIL_NZ_MASKA (2xEF05.2) and REIL_NZ_MASKB (2xEF06.2).

The REIL_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. This mode is enabled by asserting REIL_BLK (2xEC61.4).

S1 (Synchronization Messaging) The S1 octet carries the synchronization status message and provides synchronization quality measures of the transmission link in the least significant 4 bits. The WIS standard does not support the S1 octet and requires the transmission of a 0x0F within the S1 octet. A value other than 0x0F can be programmed in TX_S1 (2xE61F).

Z1 and Z2 (Reserved for Line Growth) The WIS standard does not support the Z1 or Z2 octets and requires the transmission of 0x00 in their locations. Different Z1 and Z2 values can be transmitted by programming the values at TX_Z1 (2xE61F) and TX_Z2 (2xE620) respectively.

E2 (Orderwire) The WIS standard does not support the E2 octet and recommends transmitting 0x00 in place of the E2 octet. A value other than 0x00 can be transmitted by programming the intended value at TX_E1 (2xE620).

3.4.4 WIS Pointer (H1 and H2) Description

The H1 and H2 octets are used as a pointer within the SONET/SDH frame to locate the beginning of the path overhead and the beginning of the synchronous payload envelope (SPE). Within SONET/SDH the SPE can begin anywhere within the payload area, however IEEE Standard 802.3ae specifies that a transmitted SPE must always be positioned solely within a single SONET/SDH frame. The constant pointer value of 522 decimal (0x20A) must be contained in the first channel's H1 and H2 octets. Together these conditions result in the H1 and H2 octets being 0x62 and 0x0A, respectively. These are the default values of TX_H1 (2xE615.7:0) and TX_H2 (2xE616.15:8). Programming these registers with alternate values does not alter the positioning of the SPE, but it might induce a loss of pointer (LOP-P) at the far end, or at least prevent the far end from extracting the proper payload. Furthermore, the WIS standard specifies the frame structure be a concatenated payload. For this reason, the H1 and H2 octets in channels 2 through 192 contain the concatenation indicator.

The VSC8486 supports forcing the loss of pointer (LOP-P) and path alarm indication signal (AIS-P) state.

The WIS standard specifies that a 0x00 be transmitted in the H3 octet. An alternate value can be transmitted by programming TX_H3 (2xE616.7:0).

The WIS specification does not limit the pointer position within the receive SONET/SDH frame to allow interoperability to other SONET/SDH equipment. In addition to supporting the required SONET pointer rules, the VSC8486 pointer interpreter optionally supports SDH pointers. This is selectable using the SDH_RX_MODE (2xEC40.11) bit. The differences between SONET and SDH modes are as follows:

- For SONET, the SS bits are not used and are ignored by the VSC8486 pointer interpreter. For SDH, these bits are set to 10 and are checked by the VSC8486 pointer interpreter to determine the pointer type.

- For SONET, all 192 bytes of H1 and H2 are checked by the pointer interpreter to determine the pointer type. For SDH, only the first 64 bytes (first AU-4 of an AU-4-64c) are checked.
- SONET and SDH have different increment/decrement rules. SONET uses '8 out of 10' GR-253-core objective rule, while SDH uses a majority detect rule.

The H1 and H2 octets combine to form a word with several fields as shown in Figure 33, page 68.

Bit Designations Within Payload Pointer The 'N' bits [15:12] carry a New Data Flag (NDF). This mechanism allows an arbitrary change in the location of the payload. NDF is indicated by at least three out of the four N bits matching the code '1001' (NDF enabled). Normal operation is indicated by three out of the four N bits matching the code '0110' (normal NDF).

The last ten bits of the pointer word ('D' bits and 'I' bits) carry the pointer value. The pointer value has a range from 0 to 782 that indicates the offset between the first byte after the H3 byte and the first byte of the SPE.

The SS bits are located in bits 11 and 10 and are unused in SONET mode. In SDH mode, these bits are compared with pattern '10', and the pointer is considered invalid if it does not match.

Because VSC8486 only supports concatenated frames, only the first pair of bytes (H1, H2) are called the primary pointer and have a normal format. The rest of the H1/H2 bytes contain the concatenation indication (CI). The format for the CI is NDF enabled with a pointer value of all ones.

Figure 33. 16 Bit Designations within Payload Pointer

H1								H2							
15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
N	N	N	N	S	S	I	D	I	D	I	D	I	D	I	D

Pointer Types The VSC8486 supports five different pointer types as described in the following table. A Normal Pointer indicates the current pointer, a New Data Flag indicates a new pointer location, and an AIS pointer indicates AIS. The Pointer Increment and Pointer Decrement mechanism adjusts the frequency offset between the frame overhead and SPE. A Pointer Increment is indicated by a Normal NDF that has the currently accepted pointer with the 'D' bits inverted. A Pointer Decrement is indicated by a Normal NDF that has the currently accepted pointer with 'I' bits inverted.

Table 26. H1/H2 Pointer Types

Pointer Type	NNNN Value	Pointer Value	SS bits
Normal	Three out of the four bits matching '0110'.	0 to 782	Matching in SDH mode, ignored in SONET mode.
New Data Flag (NDF)	Three out of the four bits matching '1001'.	0 to 782	Matching in SDH mode, ignored in SONET mode.
AIS Pointer	1111	1111 1111 11	11
Pointer Increment	Three out of the four bits matching '0110'.	Current pointer with 'D' bits inverted.	Matching in SDH mode, ignored in SONET mode.

Table 26. H1/H2 Pointer Types *(continued)*

Pointer Type	NNNN Value	Pointer Value	SS bits
Pointer Decrement	Three out of the four bits matching '0110'.	Current pointer with 'I' bits inverted.	Matching in SDH mode, ignored in SONET mode.

Table 27. Concatenation Indication Types

Pointer Type	NNNN Value	Pointer Value	SS bits
Normal concatenation indication	Three out of the four bits matching '1001'	1111 1111 11	Matching in SDH mode, ignored in SONET mode
AIS concatenation indication	NNNN value, pointer value, and SS bits are the same as the AIS pointer		
Invalid concatenation indication	Any other concatenation indication other than Normal CI or AIS CI		

Pointer Adjustment Rule The VSC8486 pointer interpreter adjusts the current pointer value according to rules listed in Section 9.1.6 of ANSI T1.105-1995. In addition, the following rule is observed: no increment/decrement is accepted for at least three frames following an increment/decrement or NDF operation.

Pointer Increment/Decrement Majority Rules In SONET mode, the pointer interpreter uses more restrictive GR-253-CORE objective rules, as follows:

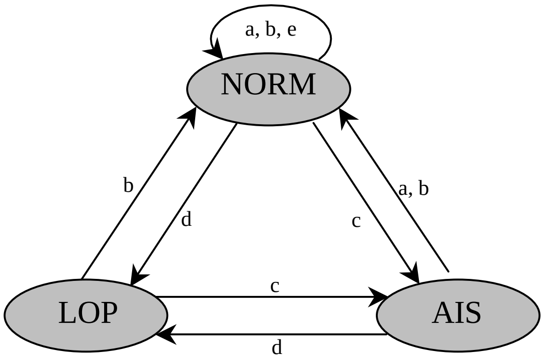
- An increment is indicated by eight or more bits matching non-inverted D bits and inverted I bits.
- A decrement is indicated by eight or more bits matching non-inverted I bits and inverted D bits.

In SDH mode, the majority rules are:

- An increment is indicated by three or more inverted I bits and two or fewer inverted D bits.
- A decrement is indicated by three or more inverted D bits and two or fewer inverted I bits.
- If both, three or more D bits are inverted and three or more I bits are inverted, no action is taken.

Pointer Interpretation States The pointer interpreter algorithm for state transitions can be modeled as a finite state machine with three states, as shown in the following figure. The three states are Normal (NORM), Loss of pointer (LOP), and Alarm Indication State (AIS).

Figure 34. Pointer Interpreter State Diagram



The conditions for transitions between these states are summarized in the following table.

Table 28. Pointer Interpreter State Diagram Transitions

Transitions	States	Description	Required Persistency
a	NORM -> NORM AIS -> NORM	<H1><H2>=<EEEESSPP><PPPPPPPP>. NDF enabled with pointer in range (0 to 782). SS bit match (if enabled).	1 frame
b	NORM -> NORM LOP -> NORM AIS -> NORM	<H1><H2>=<DDDDSSPP><PPPPPPPP>. NDF disabled (NORM pointer) with the same pointer value in range (0 to 782). SS bit match (if enabled).	3 frames
c	NORM -> AIS LOP -> AIS	<H1><H2>=<11111111><11111111>. AIS pointer (0xFFFF).	3 frames
d	NORM -> LOP AIS -> LOP	Anything other than transitions b and c or NDF enabled (transition a) or AIS pointer when not in AIS state or NORM pointer when not in NORM state or NORM pointer with pointer value not equal to current or increment/decrement or CONC pointer or SS bit mismatch (if comparison is enabled).	9 frames
e	Justification	Valid increment or decrement indication.	1 frame

Valid Pointer Definition for Interpreter State Diagram Transitions During an AIS state, only an AIS pointer is a valid pointer. In NORM state, several definitions of “valid pointer” for purpose of LOP detection are possible according to GR-253-CORE. The VSC8486 follows the GR-253-CORE intended definition, but adds a single normal pointer that exactly matches the current 'valid' pointer value.

Any change in the AIS state is reflected in the alarm bit AISP (2x0021.1). This latch-high register reports both the event and status information in consecutive reads. The AISP_PEND (2xEF00.1) bit remains asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on mask enable bits AISP_MASKA (2xEF01.1) and AISP_MASKB (2xEF02.1).

Similarly, any change in the LOP state is reflected in the alarm bit LOPP (2x0021.0). This latch-high register reports both the event and status information in consecutive reads. The LOPP_PEND (2xEF00.0) bit remains asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based upon the mask enable bits LOPP_MASKA (2xEF01.1) and LOPP_MASKB (2xEF02.1).

3.4.5 WIS Path Overhead Description

The path overhead portion of the SONET/SDH frame supports an end-to-end trace identifier, a payload parity check, a payload type indicator, a status indicator, and a user channel. The following table lists each of the octets, including their function.

Note The VSC8486 provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis.

Table 29. STS Path Overhead Octets

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
J1	STS path trace	Specified value	See the following discussion of J1 (overhead octet)	A 1-, 16-, or 64-byte trace message can be sent using registers (2x0027-2x002E, 2xE700, 2xEA00-2xEA17) and received using registers (2x002F-2x0036, 2xEC20, 2xEB00-2xEB17). TOSI and ROSI access.
B3	STS path error monitoring (path BIP-8)	Supported	Bit interleaved parity - 8 bits, as specified in T1.416	Using the TOSI, the B3 byte can be masked for test purposes. For each B3 mask bit that is cleared to 0 on the TOSI interface, the transmitted bit is left unchanged. For each B3 mask bit that is set to 1 on the TOSI interface, the transmitted bit is inverted. Using the ROSI, the B3 error locations can be extracted. Both SONET and SDH mode B3 calculation is supported.
C2	STS path signal label	Specified value	0x1A	Register (2xE615). TOSI and ROSI access. Supports persistency and mismatch detection (2xEC40).
G1	Path status	Supported	As specified in T1.416	Ability to select between RDI-P and ERDI-P formats. TOSI and ROSI access.
F2	Path user channel	Unsupported	0x00	Register (2xE618). TOSI and ROSI access.
H4	Multiframe indicator	Unsupported	0x00	Register (2xE61A). TOSI and ROSI access.
Z3-Z4	Reserved for path growth	Unsupported	0x00	Register (2xE61C, 2xE61E). TOSI and ROSI access.

Table 29. STS Path Overhead Octets *(continued)*

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
N1	Tandem connection maintenance and path data channel	Unsupported	0x00	Register (2xE621). TOSI and ROSI access.

J1 (Overhead Octet) By default, the J1 transmitted octet contains a 16-octet repeating path trace message whose contents are defined in J1_TXMSG (2x0027-2x002E). If no active message is being broadcast, a default path trace message is transmitted, consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000. The header octet for the 15-octets of zero would be 0x89. The default values of J1_TXMSG (2x0027-2x002E) do not contain the 0x89 value of the header octet, thus software must write this value.

The J1 octet in the receive direction by default is assumed to be carrying a 16-octet continuously repeating path trace message. The message is extracted from the incoming WIS frames and presented in J1_RXMSG (2x002F-2x0036). The WIS receive process does not delineate the message boundaries, thus the message might appear rotated between new frame alignment events.

The VSC8486 supports two alternate message types, a single repeating octet and a 64-octet message. The message type can be independently selected for the transmit and receive direction. The transmit direction is configured using J1_TXLEN (2xE700.1:0) while J1_RXLEN (2xEC20.1:0) configures the receive path.

When the transmit direction is configured for a 64-octet message, the first 16 octets are programmed in J1_TXMSG (2x0027-2x002E) while the 48 remaining octets are programmed in J1_TXMSG64 (2xEA00-2xEA17). Likewise, the first 16-octets of the receive message are stored in J1_RXMSG (2x002F-2x0036), while the other 48 octets are stored in J1_RXMSG64 (2xEB00-2xEB17). The receive message is updated every 125 µs with the recently received octet. Any persistence or message matching is expected to take place within the station manager.

B3 (STS Path Error Monitoring) The B3 octet is a bit interleaved parity-8 (BIP-8) code, using even parity, calculated over the previous STS-192c SPE before scrambling. The computed BIP-8 is placed in the B3 byte of the following frame before scrambling.

In the receive direction, the incoming frame is processed and a B3 octet is calculated over the received frame. The calculated value is then compared with the B3 value received in the following frame. The difference between the calculated and received octets are accumulated in block (maximum increment of 1 per errored frame) fashion into a B3 error register, B3_CNT (2x003B). This counter is non-saturating and so rolls over. The counter is cleared upon a device reset.

An additional 32-bit B3 error counter is provided at B3_ERR_CNT (2xECB4-2xECB5) which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated starting from the previous PMTICK event. When the counter is nonzero, the B3_NZ_PEND (2xEF04.5) event is asserted until read. A non-latch high version of this event B3_NZ_STAT (2xEF03.5) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits B3_ERR_MASKA (2xEF05.5) and B3_ERR_MASKB (2xEF06.5).

The B3_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. The B3_BLK (2xEC61.9) control bit, if asserted, places the B3_ERR_CNT counter in block increment mode.

It is possible that two sets of B3 bytes (from two SONET/SDH frames) are received by the Rx WIS logic in a period of time when only one G1 octet is transmitted. In this situation, one of the two B3 error counts delivered to the Tx WIS logic is discarded. This situation occurs when the receive data rate is faster than the transmit data rate. Similarly, when the transmit data rate is faster than the receive data rate, a B3 error count is not available for REI-P insertion into the G1 octets of the transmitted SONET/SDH frame. A value of zero is transmitted in this case. This behavior is achieved by using a FIFO to transfer the detected B3 error count from the receive to transmit domains.

A FIFO overflow or underflow condition is not considered an error. Instead it is recovered from gracefully as described above. A FIFO overflow or underflow eventually occurs, unless the transmit and receive interfaces are running at the same average data rate. Because the received and transmitted frames can differ by, at most, 40 ppm (±20 ppm) and still meet the industry standards, this “slip” can happen no more often than once every 3.1 seconds.

C2 (STS Path Signal Label and Path Label Mismatch) The C2 octet contains a value intended to describe the type of payload carried within the SONET/SDH frame. The WIS standard calls for a 0x1A to be transmitted. This is the default value of TX_C2 (2xEC15).

As specified in T1.416, a path label mismatch (PLM-P) (2x0021.2) event occurs when the C2 octet in five consecutive frames contain a value other than the expected one. The expected value is set in C2_EXP (2xEC40.7:0), whose default value 0x1A is compliant with the WIS standard.

Whenever a value of 0x00 is accepted (received for five or more consecutive frames) the unequipped path pending, UNEQ_PEND (2xEF04.10), event is asserted until read. A non-latch high version of this event UNEQ_STAT (2xEF03.10) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits UNEQ_MASKA (2xEF05.10) and UNEQ_MASKB (2xEF06.10).

If the accepted value is not an unequipped label (0x00) and it differs from the programmed expected value, C2_EXP, then a path label mismatch, PLMP (2x0021.2), is asserted. Similarly the PLM_PEND (2xEF00.2) event is asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits PLM_MASKA (2xEF01.2) and PLM_MASKB (2xEF02.2).

Although PLM-P is not a path level defect, it does cause a change in the setting of one of the ERDI-P codes, as described in Table 30, page 74.

G1 (Remote Path Error Indication) The most significant four bits of the G1 octet is used for back reporting the number of B3 block errors received at the near end. This is typically known as path remote error indication (REI-P). The value in this octet comes from the B3 error FIFO, as discussed with the B3 octet. The WIS standard defines a 16-bit REI-P counter REIP_CNT (2x0025). The WIS standard defines this counter to operate as a block counter as opposed to an individual errored bit counter. This counter is non-saturating and so rolls over after its maximum count. The counter does not clear upon a read, but instead only upon reset as defined in the WIS specification. When the counter is nonzero, the REIP_WISNZ_PEND (2xEF04.3) event is asserted until read. A non-latch high version of this event REIP_WISNZ_STAT (2xEF03.3) is also available.

This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits REIP_WISNZ_MASKA (2xEF05.3) and REIP_WISNZ_MASKB (2xEF06.3), respectively.

An additional 32-bit REI-P counter is provided at REIP_ERR_CNT (2xEC80-2xEC81) which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the REIP_EWISNZ_PEND (2xEF04.1) event is asserted until read. A non-latch high version of this event REIP_EWISNZ_STAT (2xEF03.1) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits REIP_EWISNZ_MASKA (2xEF05.1) and REIP_EWISNZ_MASKB (2xEF06.1), respectively.

The REIP_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. This mode is enabled by asserting REIP_BLK (2xEC61.5).

G1 (Path Status) In addition to back-reporting the far end B3 BIP-8 error count, the G1 octet carries status information from the far end device known as path remote defect indicator (RDI-P). T1.416 allows either support of 1-bit RDI-P or 3-bit ERDI-P, but indicates ERDI-P is preferred. VSC8486 supports both modes and can be independently configured for the Rx and Tx directions by configuring RX_G1_MODE (2xEC40.8) and TX_G1_MODE (2xE600.10). ERDI-P is the default for both directions.

The different structures for this octet are shown in the following figures.

Figure 35. Path Status (G1) Byte for ERDI_RDIN = 0

<table>
<tr><td colspan="4">G1 REI (B3)</td><td>RDI-P</td><td colspan="2">Reserved</td><td>Spare</td></tr>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td colspan="4">Remote Error Indicator count from B3 (0-8 value)</td><td>Remote Defect Indicator</td><td colspan="2">Set to 00 by transmitter</td><td>Ignored by receiver</td></tr>
</table>

Figure 36. Path Status (G1) Byte for ERDI_RDIN = 1

<table>
<tr><td colspan="4">G1 REI (B3)</td><td colspan="3">ERDI-P</td><td>Spare</td></tr>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr>
<tr><td colspan="4">Remote Error Indicator count from B3 (0-8 value)</td><td colspan="3">Enhanced Remote Defect Indicator (see following table)</td><td>Ignored by receiver</td></tr>
</table>

Enhanced RDI is defined for SONET-based systems as listed in GR-253-CORE (Issue 3), reproduced here in the following table, and as a possible enhancement of SDH-based systems (G.707/Y.1322 (10/2000) Appendix VII (not an integral part of that recommendation)).

Table 30. RDI-P and ERDI-P Bit Settings and Interpretation

G1 Bits 5, 6 and 7	Priority of ERDI-P Codes	Trigger	Interpretation
000/011	Not applicable	No defects.	No RDI-P defect

Table 30. RDI-P and ERDI-P Bit Settings and Interpretation *(continued)*

G1 Bits 5, 6 and 7	Priority of ERDI-P Codes	Trigger	Interpretation
100/111	Not applicable	Path alarm indication signal (AIS-P). The remote device sends all ones for H1, H2, H3, and the entire STS SPE. Path loss of pointer (LOP-P).	One-bit RDI-P defect
001	4	No defects.	No ERDI-P defect
010	3	Path label mismatch (PLM-P). Path loss of code group delineation (LCD-P).	ERDI-P payload defect
101	1	Path alarm indication signal (AIS-P). The remote device sends all ones for H1, H2, H3 and entire STS SPE. Path loss of pointer (LOP-P).	ERDI-P server defect
110	2	Path unequipped (UNEQ-P). The received C2 byte is 0x00. Path trace identifier mismatch (TIM-P). This error is not automatically generated, but can be forced using MDIO.	ERDI-P connectivity defect

In the receive direction, with RX_G1_MODE (2xEC40.8) = 0, an RDI-P defect is the occurrence of the RDI-P signal in 10 contiguous frames. An RDI-P defect terminates when no RDI-P signal is detected in 10 contiguous frames. An RDI-P event asserts FERDIP_PEND (2xEF04.8) until read. A non-latch high version of the far-end RDI-P status can be found in FERDIP_STAT (2xEF03.8). This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FERDIP_MASKA (2xEF05.8) and FERDIP_MASKB (2xEF06.8).

When RX_G1_MODE (2xEC40.8) = 1, an ERDI-P defect is the occurrence of any one of three ERDI-P signals in 10 contiguous frames. An ERDI-P defect terminates when no ERDI-P signal is detected in 10 contiguous frames.

The “010” code triggers the latch high register bit FE_PLM-P_LCD-P (2x0021.10). It also asserts FE_PLM-P_LCD-P_PEND (2xEF00.10) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FE_PLM-P_LCD-P_MASKA (2xEF01.10) and FE_PLM-P_LCD-P_MASKB (2xEF02.10), respectively.

The “101” code triggers the latch high register bit FE_AIS-P_LOP-P (2x0021.9). It also asserts FE_AIS-P_LOP-P_PEND (2xEF00.9) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FE_AIS-P_LOP-P_MASKA (2xEF01.9) and FE_AIS-P_LOP-P_MASKB (2xEF02.9), respectively.

The “110” code asserts the FE_UNEQ-P_PEND (2xEF04.9) until read. A non-latch-high version of this register FE_UNEQ_STAT (2xEF03.9) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FE_UNEQ-P_MASKA (2xEF05.9) and FE_UNEQ-P_MASKB (2xEF06.9), respectively.

F2 (Path User Channel) The WIS standard does not support the F2 octet and recommends transmitting 0x00 in place of the F2 octet. A value other than 0x00 can be transmitted by programming the intended value at TX_F2 (2xE618).

H4 (Multi-frame Indicator) The WIS standard does not support the H4 multi-frame octet and recommends transmitting 0x00 in place of the H4 octet. A value other than 0x00 can be transmitted by programming the intended value at TX_H4 (2xE61A).

Z3-Z4 (Reserved for Path Growth) The WIS standard does not support the Z3-Z4 octets and recommends transmitting 0x00 in their place. A value other than 0x00 can be transmitted by programming the intended value at TX_Z3 (2xE61C) and TX_Z4 (2xE61E) respectively.

N1 (Tandem Connection Maintenance / Path Data Channel) The WIS standard does not support the N1 octet and recommends transmitting 0x00 in place of the N1 octet. A value other than 0x00 can be transmitted by programming the intended value at TX_N1 (2xE621).

Loss of Code group Delineation After the overhead is stripped, the payload is passed to the PCS. If the PCS block losses synchronization and cannot delineate valid code groups, the PCS passes a loss of code group delineation (LCD-P) alarm to the WIS. This alarm triggers the latch high register bit LCD-P (2x0021.3). It also asserts LCD-P_PEND (2xEF00.3) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits LCD-P_MASKA (2xEF01.3) and LCD-P_MASKB (2xEF02.3), respectively.

The WIS specification calls for a LCD-P defect persisting continuously for more than 3 ms to be back reported to the far end. Upon device reset a LCD-P shall also be back reported until the PCS signals that valid code groups are being delineated. The LCD-P defect de-asserts (and is not back reported) after the condition is absent continuously for at least 1 ms.

3.4.6 Reading Statistical Counters with PMTICK

The VSC8486 contains several counters that can be read using the MDIO interface. For each error count, there are two sets of counters. The first set is the standard WIS counter implemented according to IEEE Standard 802.3ae, and the second set is for statistical counts using PMTICK.

To read the IEEE Standard 802.3ae counters, the Station Manager must read the most significant register of the 32-bit counter first. This read action latches the internal error counter value into the MDIO readable registers. A subsequent read of the least significant register does not latch new values, but returns the value latched at the time of the most significant register read.

Since the IEEE Standard 802.3ae counters are independently latched it can be difficult to get a clear picture of the timeframes in which errors were received. The PMTICK counters are all latched together, thereby providing a complete snapshot in time. When PMTICK is asserted the internal error counter values are copied into their associated registers and the internal counters are reset.

There are three methods of asserting PMTICK.

- The Station Manager can asynchronously assert PMTICK_FRC (2xEC60.0) to latch the values at a given time, regardless of the PMTICK_ENA (2xEC60.2) setting.

- The VSC8486 can be configured to latch and clear the statistical counters at a periodic interval as determined by the timer (count) value in PMTICK_DUR (2xEC60.15:3). In this mode the PMTICK_SRC (2xEC60.1) must be configured for internal mode and the PMTICK_ENA (2xEC60.2) bit must be asserted. The receive path clock is used to drive the PMTICK counter, thus the periodicity of the timer can vary during times of loss of lock and loss of frame.
- The VSC8486 can be configured to latch and clear the statistical counters at the occurrence of a rising edge detected at the PMTICK input pin. In this mode the PMTICK_SOURCE (2xEC60.1) bit must be deasserted, and the PMTICK_ENA (2xEC60.2) must be asserted.

Regardless of PMTICK_SRC (2xEC60.1), when the PMTICK event occurs the PMTICK_PEND (2xEF04.14) is asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits PMTICK_MASKA (2xEF05.14) and PMTICK_MASKB (2xEF06.14), respectively.

Given the size of the error counters and the maximum allowable error counts per frame, care must be taken in the frequency of polling the registers to ensure accurate values. All PMTICK counters saturate at their maximum values.

Table 31. PMTICK Counters

Counter Name	Description	Registers	Maximum Increase In Count Per Frame	Maximum Increase In Count Per Second	Time Until Overflow(s)
B1_ERROR_CNT	B1 section error count	B1_ERROR_CNT1, B1_ERROR_CNT0	8	64,000	67,109
B2_ERROR_CNT	B2 line error count	B2_ERROR_CNT1, B2_ERROR_CNT0	1536	12,288,000	350
B3_ERROR_CNT	B3 path error count	B3_ERROR_CNT1, B3_ERROR_CNT0	8	64,000	67,109
FAR_B3_ERROR_CNT	Far end B3 path error count	FAR_B3_ERROR_CNT1, FAR_B3_ERROR_CNT0	8	64,000	67,109
FAR_B2_ERROR_CNT	Far end B2 line error count	FAR_B2_ERROR_CNT1, FAR_B2_ERROR_CNT0	1536	12,288,000	350

Both individual and block mode accumulation of B1, B2, and B3 error indications are supported and selectable using the control bits B1_BLK, B2_BLK, and B3_BLK. In individual accumulation mode, ‘0’, the counter is incremented for each bit mismatch between the calculated B1, B2, and/or B3 error and the extracted B1, B2, and/or B3. In block accumulation mode, ‘1’, the counter is incremented only once for any nonzero number of bit mismatches between the calculated B1, B2, and/or B3 and the extracted B1, B2, and/or B3 (maximum of 1 error per frame).

3.4.7 Defects and Anomalies

All defects and anomalies listed in the following table can be forced and masked by the user. Note that the VSC8486 does not automatically generate TIM-P, but does support forcing defects using MDIO.

Table 32. Defects and Anomalies

Defect or Anomaly	Description	Type	Force Bit	Status Bit
Far end PLM-P or LCD-P	These two errors are indistinguishable when reported by the far end through the G1 octet (ERDI-P), because the far end reports both PLM-P and LCD-P with the same error code.	Far end defect.	2xEC31.10	2x0021.10
Far end AIS-P or LOP-P	These two errors are indistinguishable when reported by the far end through the G1 octet (ERDI-P), because the far end reports both AIS-P and LOP-P with the same error code.	Far end defect.	2xEC31.12	2x0021.9
PLM-P	Path label mismatch. The detection and reporting of the PLM-P defect follows section 7.5 of ANSI T1.416-1999.	Near end defect. Propagated to PCS.	2xEC31.14	2x0021.2
AIS-L	Generated on LOPC, LOS, LOF, if enabled by AISL_ON_LOPC (2xEE00.6), AISL_ON_LOS (2xEE00.5), AISL_ON_LOF (2xEE00.4), or when forced by user.	Near end defect.	The AIS-L defect is only processed and reported by the WIS Receive process; it is never transmitted by the WIS Transmit process according to IEEE 802.3ae.	2xEC30.3/2x0021.4
AIS-P	Path alarm indication signal.	Near end defect. Propagated to PCS.	2xEC30.1	2x0021.1
LOP-P	Path loss of pointer. Nine consecutive invalid pointers result in loss of pointer detection. See Figure 34, page 70 for pointer state machine.	Near end defect. Propagated to PCS.	2xEC30.0	2x0021.0
LCD-P	Path loss of code group delineation. See Table 30, page 74. This is also reported to the far end if it persists for at least 3 ms.	Near end defect	2xEC31.2	2x0021.3

Table 32. Defects and Anomalies *(continued)*

Defect or Anomaly	Description	Type	Force Bit	Status Bit
LOPC	Loss of optical carrier alarm. This is an input from the XFP module's loss of signal output. The polarity can be inverted for use with other module types. This defect can be used independently or in place of LOS.	Near end defect	2xEC30.12	2xEF03.11
LOS	The PMA circuitry detects a Loss Of Signal (LOS) defect if the input signal falls below the assert threshold. Refer the PMA LOS section for more details. When a PMA LOS is declared the framer is held in reset to prevent it from looking for a frame boundary.	Near end defect	2xEC30.11	2x0021.6
SEF	Severely errored frame. Generated when device cannot frame to A1 A2 pattern. SEF indicates synchronization process is not in the SYNC state, as defined by the state diagram of IEEE 802.3ae clause 50.4.2.	Near end defect. Propagated to PCS	2xEC31.7	2x0021.11
LOF	Generated when SEF persists for 3 ms. Terminated when no SEF occurs for 1 ms to 3 ms.	Near end defect	2xEC31.6	2x0021.7
B1 PMTICK error count is nonzero	BIP-N(S) - 32-bit near end section BIP error counter is nonzero.	Near end anomaly	2xEC31.5	2xEF03.7
B2 PMTICK error count is nonzero	BIP-N(L) - 32-bit near end line BIP error counter is nonzero.	Near end anomaly	2xEC31.4	2xEF03.6
B3 PMTICK error count is nonzero	BIP-N(P) - 32-bit near end path BIP error counter is nonzero.	Near end anomaly	2xEC31.3	2xEF03.5
REI-L	Line remote error indicator octet is nonzero. Far end BIP-N(L).	Far end anomaly	2xEC31.8	2xEF03.4
REI-L PMTICK error count is nonzero	Line remote error indicator is nonzero. Far end BIP-N(L).	Far end anomaly	2xEC31.1	2xEF03.2
RDI-L	Line remote defect indicator.	Far end defect	2xEC30.2	2x0021.5
REI-P	Path remote error indicator octet is nonzero. Far end BIP-N(P).	Far end anomaly	2xEC31.9	2xEF03.3

Table 32. Defects and Anomalies *(continued)*

Defect or Anomaly	Description	Type	Force Bit	Status Bit
REI-P PMTICK error count is nonzero	Path remote error indicator. Far end BIP-N(P).	Far end anomaly	2xEC31.0	2xEF03.1
UNEQ-P	Unequipped path.	Near end defect	2xEC31.15	2xEF03.10
Far end UNEQ-P	Far end unequipped path.	Far end defect	2xEC31.11	2xEF03.9

3.4.8 Interrupt, Interrupt Masking, and WIS_INTA/B

The VSC8486 generates interrupts for each defect and anomaly. The interrupts for the BIP error counts (B1, B2, and B3 counters) and the interrupts for the far end error counts (REI-L and REI-P) are generated when the PMTICK counters become nonzero. Mask enable bits propagate the interrupt pending event to the pins WIS_INTA and WIS_INTB. Each event can be optionally masked for each WIS_INTA/B pin.

For each defect or anomaly defined in IEEE Standard 802.3ae, the VSC8486 supports the standard WIS register. In addition the VSC8486 supports another set of registers in the WIS Vendor Specific area. These registers provide a STATUS bit to indicate the current real-time status of the event, a PENDING bit to indicate if the STATUS bit has changed state, and two mask enable bits for each interrupt pin (WIS_INTA and WIS_INTB). The STATUS bit is set if and only if the interrupt currently exists. This STATUS bit does not latch.

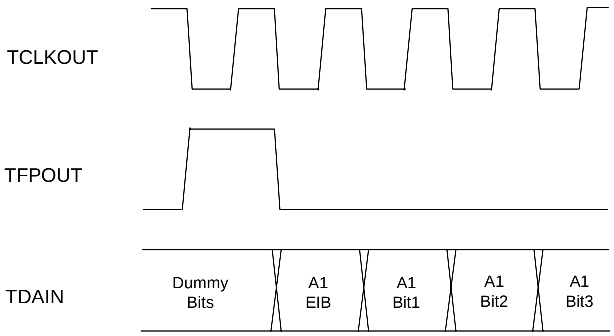
The defects and anomalies are constructed in a hierarchy such that lower order alarms are squelched when higher order events are detected. For more information about the dependencies between squelches and events, see the E-WIS interrupt registers, beginning with Table 170, page 167. Also see Table 101, page 146.

3.4.9 WIS Overhead Serial Interfaces

The VSC8486 includes provisions for off-chip processing of the critical SONET/SDH transport overhead octets through two independent serial interfaces. The transmit overhead serial interface (TOSI) is used to insert octets into the transmit frames, and the receive overhead serial interface (ROSI) is used to recover the octets from the received frames. The interfaces each consists of three pins: a clock output, a frame pulse output, and a data input (Tx) /output (Rx). These I/O are LVTTL compatible for easy connection to an external device such as an FPGA.

Transmit Overhead Serial Interface (TOSI) The TOSI port enables the user to individually program 231 separate octets in the SONET/SDH overhead. The SONET/SDH frame rate is 8 kHz as signaled by the frame pulse (TFPOUT) signal. The TOSI port is clocked from a divided-down version of the WIS transmit clock made available on TCLKOUT. To provide a more standard clock rate, 39 dummy octets are added per frame resulting in a clock running at one five-hundred-twelfth of the line rate or 19.44 MHz. For each octet, the external device indicates the desire to transmit that byte by using an enable indicator bit (EIB) that is appended to the beginning of the octet. If EIB = 0, the data on the serial interface is ignored for that overhead octet. If EIB = 1, the serial interface data takes precedence over the value generated within the VSC8486. The EIB is present before the dummy octets too, however its value has no effect as the dummy octets are ignored within the device. The first EIB bit should be transmitted by the external device on the first rising edge of TCLKOUT after TFPOUT, as illustrated in the following figure. The data should be provided with the most significant bit (MSB) first. After reception of the TOSI data for a complete frame, the values are placed in the overhead for the next transmitted frame.

Figure 37. TOSI Timing Diagram



The following table summarizes the order of octets required by the TOSI port. It is important to note that some octets are error masks, such that the transmitted octet is the XOR of the TOSI octet and the pre-defined value within the chip if the EIB is enabled. This feature is best used for test purposes only.

Table 33. TOSI/ROSI Addresses

Byte Name	Octet Name	TOSI/ROSI Byte Order	Number of Registers (Number of Bytes on the Serial Interface)	Number of Bytes (Number of STS Channels the Byte is Transmitted)	Type
Frame Boundary	A1	0	1	192	Programmable byte that is identical for all locations.
Frame Boundary	A2	1	1	192	Programmable byte that is identical for all locations.
Section Trace	J0	2	1	1	Programmable byte
Section Growth	Z0	3	1	191	Programmable byte that is identical for all locations.
STS Path Trace	J1	4	1	1	Programmable byte
Section BIP-8	B1	5	1	1	TOSI inserts error mask; ROSI extracts XOR of B1 value and received data
Orderwire	E1	6	1	1	Programmable byte
Section User Channel	F1	7	1	1	Programmable byte
Path BIP-8	B3	8	1	1	TOSI inserts error mask; ROSI extracts XOR of B1 value and received data
Section DCC 1	D1	9	1	1	Programmable byte

Table 33. TOSI/ROSI Addresses *(continued)*

Byte Name	Octet Name	TOSI/ROSI Byte Order	Number of Registers (Number of Bytes on the Serial Interface)	Number of Bytes (Number of STS Channels the Byte is Transmitted)	Type
Section DCC 2	D2	10	1	1	Programmable byte
Section DCC 3	D3	11	1	1	Programmable byte
Signal Label	C2	12	1	1	Programmable byte
Pointer 1	H1	13	1	192	Programmable byte that is identical for all locations.
Pointer 2	H2	14	1	192	Programmable byte that is identical for all locations.
Pointer Action	H3	15	1	192	Programmable byte that is identical for all locations.
Path Status	G1	16	1	1	Programmable byte
Line BIP-8	B2	17 to 208	192	192	TOSI inserts error mask for each byte; ROSI extracts XOR of B1 value and received data for each byte
Automatic Protection Switching (APS) channel and Remote Defect Indicator (RDI)	K1	209	1	1	Programmable byte
Automatic Protection Switching (APS) channel and Remote Defect Indicator (RDI)	K2	210	1	1	Programmable byte
Path User Channel	F2	211	1	1	Programmable byte
Line DCC 4	D4	212	1	1	Programmable byte
Line DCC 5	D5	213	1	1	Programmable byte
Line DCC 6	D6	214	1	1	Programmable byte
Multiframe	H4	215	1	1	Programmable byte
Line DCC 7	D7	216	1	1	Programmable byte
Line DCC 8	D8	217	1	1	Programmable byte
Line DCC 9	D9	218	1	1	Programmable byte
Growth / User Channel	Z3 / F3	219	1	1	Programmable byte
Line DCC 10	D10	220	1	1	Programmable byte
Line DCC 11	D11	221	1	1	Programmable byte
Line DCC 12	D12	222	1	1	Programmable byte
Growth / Path APS	Z4 / K3	223	1	1	Programmable byte

Table 33. TOSI/ROSI Addresses *(continued)*

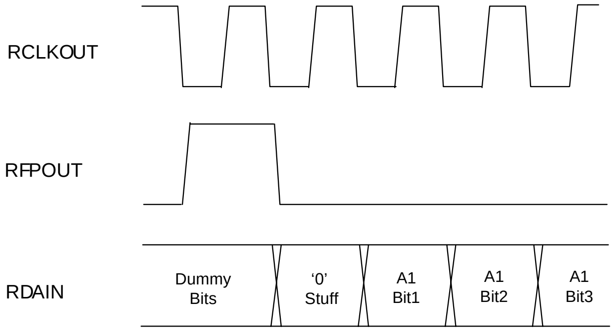
Byte Name	Octet Name	TOSI/ROSI Byte Order	Number of Registers (Number of Bytes on the Serial Interface)	Number of Bytes (Number of STS Channels the Byte is Transmitted)	Type
Synchronization Message	S1	224	1	1	Programmable byte
Growth 1	Z1	225	1	191	Programmable byte that is identical for all locations
Growth 2	Z2	226	1	190/191	Programmable byte that is identical for all locations; dependent upon 2xEC40.12
STS-1 REI-L	M0	227	1	1	Programmable byte
STS-N REI-L	M1	228	1	1	Programmable byte
Orderwire 2	E2	229	1	1	Programmable byte
Tandem Connection	N1	230	1	1	Programmable byte
Dummy Bytes		231 to 270	39		No function

Receive Overhead Serial Interface (ROSI) The ROSI port extracts the same 231 overhead octets from the SONET/SDH frame, and consists of the clock output (RCLKOUT), frame pulse output (RFPOUT), and data output (RDAOUT). The ROSI port is clocked from a divided-down version of the WIS receive clock, and is valid during in-frame conditions only. As with the TOSI port, 39 dummy octets are provided each frame period resulting in a 19.44 MHz RCLKOUT frequency. For each octet, including the dummy octets, an extra ‘0’ bit is stuffed at the beginning of each byte so that the TOSI and ROSI clock rates are identical. The first stuff bit for each frame is transmitted by RDAOUT on the first rising edge of RCLKOUT after the frame pulse (RFPOUT), as illustrated in the following figure.

Since the Receive path overhead can be split across two frames, the VSC8486 buffers the overhead for an additional frame time so that a complete path overhead is presented. Table 33, page 81, outlines the order for each of the octets presented on the ROSI port. With the exception of the M0/M1 octets, the extracted octets are from the first channel position. In place of parity and error octets, the VSC8486 outputs the result of an XOR between the calculated BIP and the received value. Therefore, a count of ones within each of the BIP octets should correspond with the internal error accumulators. The following figure shows the functional timing for the ROSI interface.

The following figure shows the functional timing of the ROSI port.

Figure 38. ROSI Timing Diagram



3.4.10 WIS Pattern Generator and Checker

The VSC8486 implements the square wave, PRBS31, and mixed-frequency test patterns as described in section 50.3.8 of IEEE Standard 802.3ae as well as the Test Signal Structure (TSS) and continuous identical digits (CID) pattern.

The square wave pattern is selected asserting WIS_TEST_PAT_SEL (2x0007.3) while the generator is enabled by asserting WIS_TEST_PAT_GEN (2x0007.1). When WIS_TEST_PAT_SEL (2x0007.3) is deasserted the mixed frequency test pattern is selected. The square wave frequency is configured according to WIS_SQWV_LEN (2x0600.7:4). The WIS_TEST_PAT_ANA (2x0007.2) bit is used to enable the test pattern checker in the receive path. The checker does not operate on square wave receive traffic. Error counts from the mixed frequency pattern are presented in the SONET/SDH BIP-8 counters, B1_CNT (2x003C), B2_CNT (2x0039), and B3_CNT (2x003B).

The VSC8486 supports the PRBS31 test pattern as reflected in PRBS31_SUPPORT (2x0008.1). The transmitter/generator is enabled by asserting WIS_TEST_PRBS_GEN (2x0007.4) while the receiver/checker is enabled by asserting WIS_TEST_PRBS_ANA (2x0007.5). As the mixed frequency/square wave test patterns have priority over the PRBS31 pattern, TEST_PAT_GEN (2x0007.1) must be disabled for the PRBS31 test pattern to be sent. Error counts from the PRBS31 checker are available in WIS_TEST_PAT_CNT (2x0009). This register does not roll over after reaching its maximum count and is cleared after every read operation. Two status bits are available from the PRBS checker. The PRBS_NZ (2xEC51.1) bit indicates whether the error counter is nonzero. The PRBS_SYNC (2xEC51.0) bit if asserted indicates that checker is synchronized and actively checking received bits. For test purposes, the PRBS generator can inject single bit errors. By asserting PRBS_INJ_ERR (2xEC50.1), a single bit error is injected, resulting in three bit errors being detected within the checker. The value of three comes from the specification, which indicates one error should be detected for each tap within the checker.

3.4.11 WIS Protocol Implementation Conformance Statement (PICS)

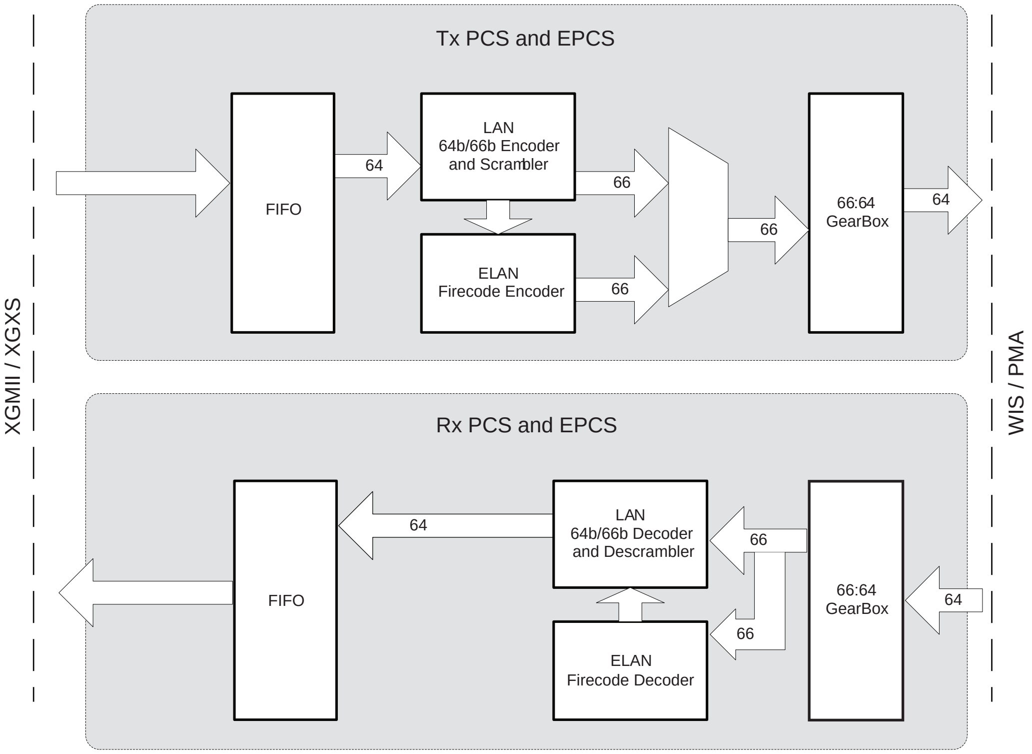
The device supports all mandatory options and functions given in the PICS in section 50.6 of IEEE Standard 802.3ae. Of the “Major capabilities/options,” the device supports the optional MDIO and PRBS31 Test-pattern mode, but does not support the optional XSBI compatible interface.

3.5 Physical Coding Sublayer (PCS)

The physical coding sublayer (PCS) is defined in IEEE Standard 802.3ae Clause 49. The PCS is responsible for transferring data between the XGMII or XGXS clock domain and the WIS/PMA clock domain. In addition, the PCS encodes and scrambles the data for efficient transport across the given medium.

The following figure provides a block diagram of the PCS including how it glues the XGMII/XGXS blocks to the WIS/PMA blocks and shows the alternate paths used by the E-PCS block which is discussed later.

Figure 39. PCS Block Diagram



3.5.1 Control Codes

The VSC8486 supports the use of all control codes and ordered sets necessary for 10 GbE and 10 GFC operation. The following table lists the control characters, notation, and control codes.

Table 34. Control Codes

Control Character	Notation[1]	XGMII Control Code	10-G BASE-R Control Code	10-G BASE-R O Code	8b/10b Code[2]
Idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
Start	/S/	0xfb	Encoded by block type field		K27.7
Terminate	/T/	0xfd	Encoded by block type field		K29.7
Error	/E/	0xfe	0x1e		K30.7
Sequence ordered_set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
Reserved 0	/R/	0x1c	0x2d		K28.0
Reserved 1		0x3c	0x33		K28.1
Reserved 2	/A/	0x7c	0x4b		K28.3
Reserved 3	/K/	0xbc	0x55		K28.5
Reserved 4		0xdc	0x66		K28.6
Reserved 5		0xf7	0x78		K23.7
Signal ordered_set[3]	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

1. The codes for /A/, /K/ and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the PHY XS to send them on the XGMII.
2. For information only. The 8b/10b code is specified in Clause 36. Usage of the 8b/10b code for 10 Gbps operation is specified in Clause 4.
3. Reserved for INCITS T11 - 10 GFC µs.

3.5.2 Transmit Path

In the transmit direction, the PCS accepts data from the XGMII or XGXS interface, depending on PCS_XGMII_SRC (3x8005.8), which has its own clock domain, and transfers the data into the PMA transmit clock domain. Clock rate disparity compensation takes place in a FIFO. The overflow/underflow status bits for the FIFO can be monitored at (3x8009.1:0). Based on the FIFO's fill level, idle characters are added or removed as needed. Two counters accumulate the number of added and removed idle characters, TX_IDLE_ADD (3x800C) and TX_IDLE_DROP (3x800D). These counters can be used to gain some insight into the clock rate disparity.

Once in the PMA clock domain, the characters are checked for validity. The occurrence of invalid characters cause the PCS_TXCHARERR_CNT (3x8014) register to increment. Likewise the occurrence of an invalid sequence causes the PCS_TXSEQERR_CNT (3x8012) register to increment. Transmitted data is handled according to IEEE Standard 802.3ae Clause 49.

The characters are then processed in a two-step manner. First the 64-bits are encoded and a 2-bit header is calculated to form a single 66-bit block. The two header bits are used for block delineation and classification. The only valid header codes are '01' to indicate a payload of all data octets and '10' to indicate the presence of one or more control characters within the payload. The second step is to maintain a DC balanced signal on the serial line, thus the 64-bit encoded payload is scrambled using a self-synchronizing scrambler that implements the polynomial $G(x) = 1 + x^{39} + x^{58}$. The header bits are not scrambled as they are already DC balanced. For debug purposes, the scrambler can be disabled by deasserting SCR_DIS (3x8005.9).

The 66-bit blocks are then passed to the PMA through a 66:64 gearbox. The gearbox merely feeds the 66-bit data into the WIS/PMA's 64-bit data path.

3.5.3 Receive Path

In the receive direction, the PCS accepts data from the WIS/PMA block and reformats it for transmission to the XGMII or XGXS interface. Because of the data path width mismatches between the WIS/PMA and the PCS, a 64:66 gearbox is needed. The gearbox also performs block synchronization/alignment based upon the 2-bit synchronization header. When the receive logic receives 64 continuous valid sync headers the BLOCK_LOCK (3x0021.15) bit is asserted. This bit is a latch-high bit; therefore, a second read of the bit returns the current status. If 16 invalid block sync. headers are detected within a 125 µs period, the PCS_HIGHBER (3x0021.14) bit is asserted. This bit is a latch-high bit, and therefore a second read of the bit returns the current status.

Once block synchronization is achieved, the occurrence of errored blocks are accumulated in the PCS_ERRORED_BLOCKS (3x0021.7:0) counter. An errored block is one that has one or more of the following defects:

- The sync field has a value of 00 or 11.
- The block type field contains a reserved value.
- Any control character contains an incorrect value (for more information about control code values, see Table 34, page 86).
- Any O code contains an incorrect value (for more information about control code values, see Table 34, page 86).
- The set of eight XGMII characters does not have a corresponding block format shown in the following figure.

Figure 40. 64b/66b Block Formats

Input Data	**Sync**	**Block Payload**								
Bit Position: Data Block Format:	0 1	2								65
D0 D1 D2 D3/D4 D5 D6 D7	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
Control Block Formats:		**Block Type Field**								
C0 C1 C2 C3/C4 C5 C6 C7	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C0 C1 C2 C3/O4 D5 D6 D7	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
C0 C1 C2 C3/S4 D5 D6 D7	10	0x33	C_0	C_1	C_2	C_3	▨	D_5	D_6	D_7
O0 D1 D2 D3/S4 D5 D6 D7	10	0x66	D_1	D_2	D_3	O_0	▨	D_5	D_6	D_7
O0 D1 D2 D3/O4 D5 D6 D7	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
S0 D1 D2 D3/D4 D5 D6 D7	10	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
O0 D1 D2 D3/C4 C5 C6 C7	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
T0 C1 C2 C3/C4 C5 C6 C7	10	0x87	▨	C_1	C_2	C_3	C_4	C_5	C_6	C_7
D0 T1 C2 C3/C4 C5 C6 C7	10	0x99	D_0	▨	C_2	C_3	C_4	C_5	C_6	C_7
D0 D1 T2 C3/C4 C5 C6 C7	10	0xaa	D_0	D_1	▨	C_3	C_4	C_5	C_6	C_7
D0 D1 D2 T3/C4 C5 C6 C7	10	0xb4	D_0	D_1	D_2	▨	C_4	C_5	C_6	C_7
D0 D1 D2 D3/T4 C5 C6 C7	10	0xcc	D_0	D_1	D_2	D_3	▨	C_5	C_6	C_7
D0 D1 D2 D3/D4 T5 C6 C7	10	0xd2	D_0	D_1	D_2	D_3	D_4	▨	C_6	C_7
D0 D1 D2 D3/D4 D5 T6 C7	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D0 D1 D2 D3/D4 D5 D6 T7	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Valid blocks then recover their original payload data by being descrambled. The descrambler is the same polynomial as used by the transmitter. For test purposes, the descrambler can be disabled by asserting DSCR_DIS (3x8005.10). The data is checked for valid characters and sequencing. The occurrence of invalid characters causes the RXCHARERR_CNT (3x8015) to increment, while the occurrence of a sequence error causes the RXSEQERR_CNT (3x8011) to increment.

The data is passed from the PMA/WIS clock domain to the XGMII or XGXS clock domain through a FIFO. The overflow/underflow status bits for the FIFO are reflected in RX_OFLOW (3x8009.3) and RX_UFLOW (3x8009.2). Based upon the FIFO's fill level, idle characters are added or removed as needed. RX_IDLE_ADD (3x800E) and RX_IDLE_DROP (3x800F) accumulate the number of added and dropped idle characters at this interface.

3.5.4 PCS Test Modes

The PCS block offers all of the standard defined test pattern generators and analyzers. In addition the VSC8486 supports a 64-bit static user pattern and the optional PRBS31 pattern. Two error counters are available. Each are saturating counters and cleared upon a read operation. The first, PCS_ERR_CNT (3x002B), is located in the IEEE

Standard area while the 32-bit, PCS_VSERR_CNT (3x8007-3x8008), is located in the vendor specific area.

The IEEE specification defines two test pattern modes, a square wave generator and a pseudo-random test pattern. The square wave generator is enabled by first selecting the square wave pattern by asserting PCS_TSTPAT_SEL (3x002A.1) then enabling the test pattern generator PCS_TSTPAT_GEN (3x002A.3). The period of the square wave can be controlled in terms of bit times by writing to PCS_SQPW (3x8004) There is no associated square wave checker within the VSC8486. The pseudo-random test pattern is selected by deasserting PCS_TSTPAT_SEL (3x002A.1). The pseudo-random test pattern contains two data modes. When PCS_TSTDAT_SEL (3x002A.0) is deasserted, the pseudo-random pattern is a revolving series of four blocks with each block 128-bits in length. The four blocks are the resultant bit sequence produced by the PCS scrambler when pre-loaded with the following seeds:

- PCS_SEEDA (3x0022-3x0025)
- PCS_SEEDA invert
- PCS_SEEDB (3x0026-3x0029)
- PCS_SEEDB invert

The pattern generator is enabled by asserting PCS_TSTPAT_GEN (3x002A.3), while the analyzer is enabled by asserting PCS_TSTPAT_ANA (3x002A.2). Errors are accumulated in the clear-on-read saturating counter, PCS_ERR_CNT (3x002B). In pseudo-random pattern mode, the error counter counts the number of errored blocks.

Support for the optional PRBS31 pattern is indicated by PCS_PRBS31_ABILITY (3x0020.2) whose default is high. The PRBS31 test generator is selected by asserting PCS_PRBS31_GEN (3x202A.4) while the checker is enabled by asserting PCS_PRBS31_ANA (3x202A.5). Note that the IEEE standard specifies the error counter should increment for each linear feedback shift register (LFSR) tap that a bit is in error. Therefore, a single bit error increments the counter by 3 as there are three taps in the PRBS31 polynomial.

The user defined 64-bit static pattern can be written to PCS_USRPAT (3x8000-3x8003) and enabled by asserting PCS_USRPAT_ENA (3x8005.0) and PCS_TSTPAT_GEN (3x002A.3). Enabling the user defined pattern enables both the generator and analyzer.

3.6 Extended PCS (E-PCS)

The VSC8486 provides an optional Extended PCS (E-PCS) mode to improve link quality (BER), provide a supervisory channel, and monitor the error rate at the PHY level. The E-PCS feature utilizes the frame format specified in the Common Electrical I/O Protocol (CEI-P) document created as an Implementation Agreement (IA) within the Optical Network Forum’s (OIF). The CEI-P maintains a similar EMI spectrum as that generated by a standard PCS. The E-PCS mode operates at the same line rate as PCS and therefore does not require any special clocks or changes to the PMD layer.

When enabled, E-PCS mode provides a net electrical coding gain (NECG) of approximately 2.5 dB. For example, a link operating without E-PCS at a BER of 10^{-10} would operate at a BER of better than 10^{-16} with E-PCS.

Electronic dispersion compensated (EDC) applications produce burst errors due to the commonly used decision feedback equalizer (DFE) architecture. DFEs typically used in

10GBASE-LRM produce burst errors that are typically the same bit length as the number of taps. E-PCS mode is capable of correcting burst-errors up to 7 bits in length, which is a common DFE tap size.

E-PCS mode is supported when the VSC8486 device is configured in LAN mode only, not in WAN mode.

3.6.1 Autonegotiation

The VSC8486 can be configured to autonegotiate between standard and extended PCS modes or can be controlled manually. The AUTONEG input pin, if set low, places the device into manual mode, meaning that E-PCS is enabled only when the EPCS input pin is set high. Both the AUTONEG and EPCS pins can be overridden by software by setting the AUTONEG_OVR (1xE605.13) and EPCS_OVR (1xE605.11) bits. Once overridden, the autonegotiation and E-PCS states are dependent upon the settings of AUTONEG_FORCE (1xE605.12) and EPCS_FORCE (1xE605.10).

In autonegotiation mode the device transmits in the format defined by the EPCS mode after reset or power-up. The high-speed received data is processed by both the PCS and the E-PCS. If the received format is different than the transmitted format, the device switches the format to match the received data. During a loss of lock (LOL), the device continues to transmit in the currently negotiated format, but changes to a new format if the receiver detects one. The following table describes the logic of the EPCS and AUTONEG bits.

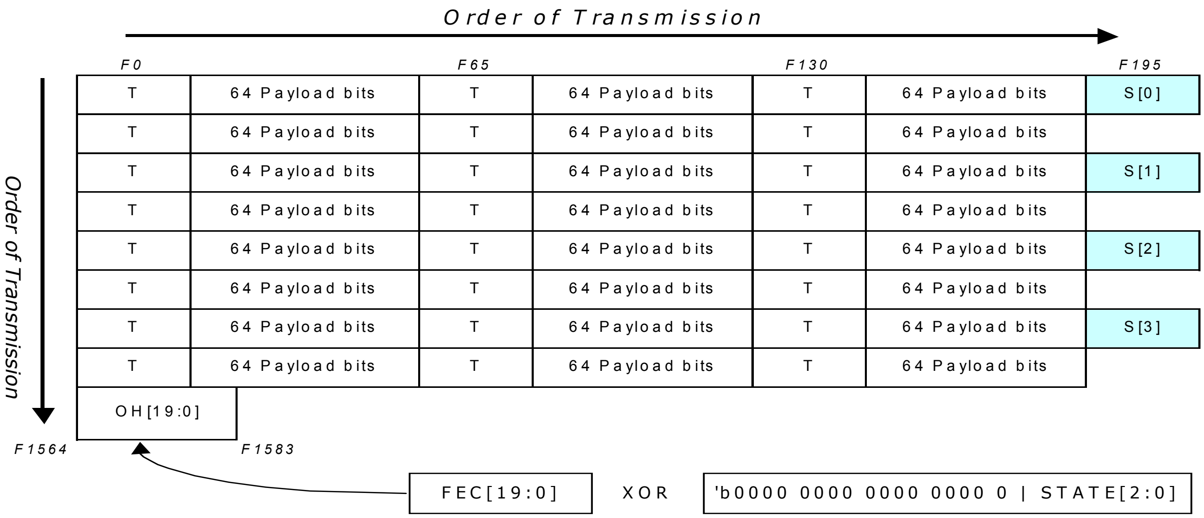
Table 35. E-PCS Logic

EPCS	AUTONEG	Transmission Format
0	0	Standard PCS.
0	1	Device begins transmitting in standard PCS format, but switches to E-PCS format if and only if the receiver detects E-PCS format.
1	0	Extended PCS.
1	1	Device begins transmitting in E-PCS format, but switches to standard PCS if and only if the receiver detects PCS data.

3.6.2 E-PCS Frame Format

The frame format for E-PCS mode is given in Section 4.2 of the OIF CEI-P. The two-bit overhead of the 64B/66B PCS frame is replaced with a single overhead bit, thereby freeing up one bit per PCS frame. By accumulating these saved bits over 24 PCS frames, there are 24 new bits available to implement the supervisory channel and FEC firecode. Seventeen of these bits (OH[19:3]) are used for framing, scrambler synchronization, error detection, and forward error correction. Three of these bits (OH[0:2]) are used to optionally determine link state and assist in error detection and forward error correction. Four of these bits (S[0:3]) are used as a supervisory channel.

Figure 41. E-PCS Frame Format

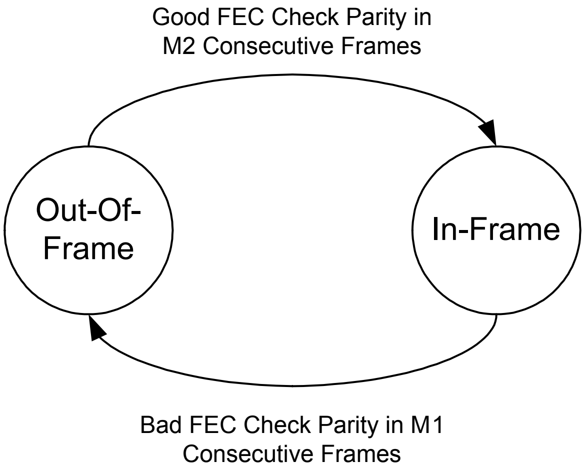


3.6.3 Link State Machines

The Rx and Tx Link training State Machines (LSMs) are compliant with the CEI-P specification. TX_LSM (3xE604.7:5) reports the current state of the Tx Link State Machine. This state information can be used for diagnostics or monitoring of link training success. By default the Tx_LSM_ENA (3xE602.6) bit is deasserted, meaning that the Tx LSM skips the training sequence and handshake and moves directly to the idle state. If the VSC8486 is used in a system where training is desired, the Tx_LSM_ENA (3xE602.6) bit must be asserted during initial configuration. If Tx_LSM_ENA (3xE602.6) is asserted, the Tx LSM can be forced to restart and retrain the link by asserting TX_LSM_RESTART (3xE602.5). This bit has no value when operating with TX_LSM_ENA (3xE602.6) deasserted. Although intended for applications with multiple clients, the TX_LSM_HOLD (3xE602.4) is available for payload synchronization purposes. The TX_LSM_TIMEOUT (2xE603) value, also referred to as D1 in the CEI-P specification, is used to progress the LSM from the training state to the operational state in the case of a simplex (uni-directional) link application.

Within the receive link state machine the current state is reflected in RX_LSM (3xE605.2:0). The criteria for moving among Rx LSM states is based upon consecutive state indications being stable for a number of frames. This number, also known as the accepted value, is set in RX_LSM_R1 (3xE602.3:0) in units of CEI-P frames. The link's status of in-frame or out-of-frame is indicated in RX_IN_FRM (3xE605.4). The following figure shows the E-PCS Framing State Diagram. The in-frame condition occurs when the number of consecutive E-PCS frames without parity errors (M2) exceeds 4. The out-of-frame condition occurs when the number of consecutive frames with parity errors (M1) exceeds 15.

Figure 42. **E-PCS Framing State Diagram**



3.6.4 FEC Controls and Feedback

The forward error correction (FEC) code also known as the Firecode, occupies the last 20 bits within the E-PCS frame. Two counters are used to provide a rough indication of the link quality. The RX_FIXED_CNT (3xE605) frame counter displays the number of E-PCS frames in which errors were corrected over the previous one second. The RX_UNFIXED_CNT (3xE606) frame counter increments upon each E-PCS frame where the number of errors exceed the Firecode algorithm, namely an error burst greater than 7 bits per frame. The user must assert LATCH_N_CLR_CNT (3xE601.1) to latch the internal counter values into the MDIO accessible registers and clear the internal counters.

For purposes of BER characterization, the error correction mechanism can be disabled by de-asserting EPCS_CORR (3xE601.2). By default, error correction is enabled.

3.6.5 Supervisory Channel

The four supervisory channel bits per E-PCS frame can be set for two different configurations. The first configuration involves sending static values as defined in TX_SCHAN (3xE601.7:10). These static bits are enabled by TX_SCHAN_EN (3xE601.6). The second configuration, which is the default, involves sending a 136-bit repeating message in a bit-wise fashion utilizing S[0]. In this mode, S[3:1] are automatically set to zero. The 136-bit message contains 8-bits of framing (0x7E) and a 128-bits of user programmable area. The intended 128-bit message is programmed in TX_MSG (3xE60A–3xE611). Once the message is programmed, the user must assert the TX_NEW_MSG (3xE601.0) bit. This action latches the 128-bit message into internal registers, which are serialized and repetitively streamed out in the S[0] bit.

In the received direction, the S[0] bit is monitored for the framing byte (0x7E) to appear 136-bits apart, which is defined as frame alignment. After alignment, the incoming message bits are written to RX_MSG (3xE612-3xE619). Whenever the previous message and the current message differ. the RX_NEW_MSG (3xE604.3) bit asserts.

It is important to note that with a simplistic framing algorithm based upon a single byte (0x7E) occurring repeatedly 136-bits apart, any message containing the 0x7E byte can cause a false frame alignment. In such a case software must reconstruct the intended message.

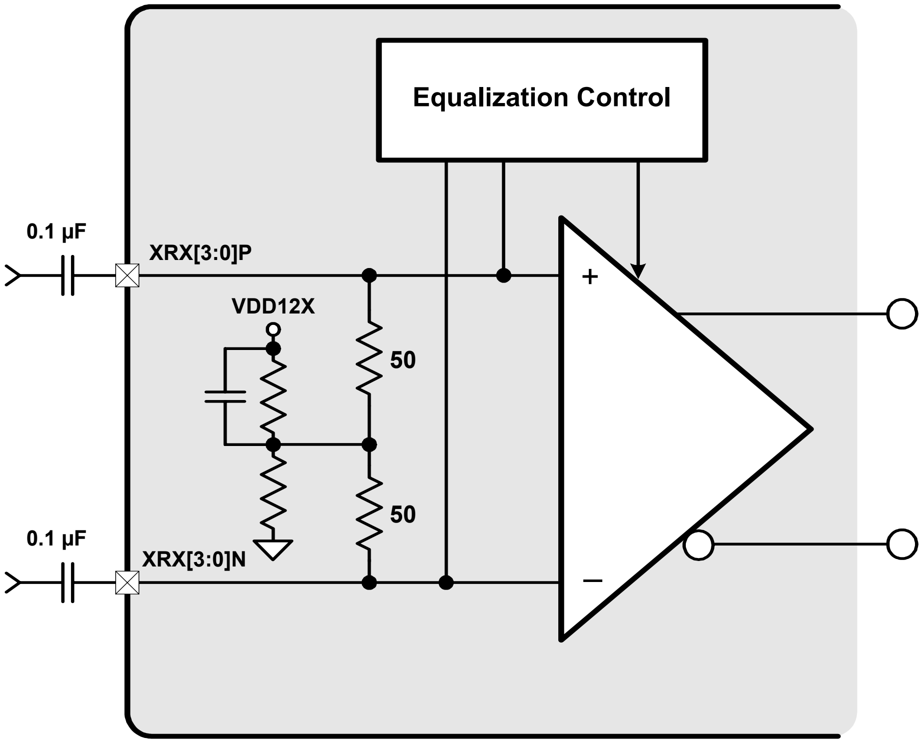
3.7 XGMII Extender Sublayer (PHY-XS)

The PHY XS block interfaces from the four-lane 10 Gbps attachment unit interface (XAUI) to the PCS. Each AC-coupled lane has 8b/10b encoded data running at 3.125 Gbps (3.1875 Gbps for 10 GFC).

3.7.1 XAUI Receiver

The XAUI interface features on-chip terminations of 100 Ω for all XAUI inputs, as shown in the following figure.

Figure 43. XAUI Input Simplified Schematic (XAUI_RCVR)



3.7.2 XAUI Loss of Signal (LOS)

Each XRX[3:0]P/N channel's input buffer has a loss of signal (LOS) detection that can be accessed through the MDIO registers (4x8012.3:0). For each XAUI lane, a loss of signal level status is set low when the differential signal peak-to-peak swing exceeds the global de-assert threshold level for that lane. The XAUI LOS assert and de-assert thresholds cannot be set independently. Two bits in register (4x8011.3:2) are used to program four separate de-assert and assert level ranges, as shown in the following table.

For each lane, a high indicates that the signal amplitude is below the assert threshold level. The LOS status bits are considered undefined when the signal swing is between the de-assert threshold and assert threshold.

The approximate upper (de-assert) and lower (assert) threshold levels are shown in the following table.

Table 36. XAUI Lane LOS Threshold Summary

LOS Assert/Deassert Threshold Range (4x8011.3:2)	Assert Threshold (mV)	De-assert Threshold (mV)	LOS Status (4x8012.3:0)	Remarks
00 (default)	50	175	Lane 3; bit 3 Lane 2; bit 2 Lane 1; bit 1 Lane 0; bit 0	For each lane: 1: LOS declared 0: LOS not declared
01	60	185	Lane 3; bit 3 Lane 2; bit 2 Lane 1; bit 1 Lane 0; bit 0	For each lane: 1: LOS declared 0: LOS not declared
10	70	195	Lane 3; bit 3 Lane 2; bit 2 Lane 1; bit 1 Lane 0; bit 0	For each lane: 1: LOS declared 0: LOS not declared
11	80	205	Lane 3; bit 3 Lane 2; bit 2 Lane 1; bit 1 Lane 0; bit 0	For each lane: 1: LOS declared 0: LOS not declared

3.7.3 XAUI Receiver Equalization

Incoming data on the XRX[3:0]P/N inputs typically contains a substantial amount of intersymbol interference (ISI) or deterministic jitter, which reduces the ability of the receiver to recover data without errors. Each XAUI lane includes a programmable equalizer circuit designed to effectively reduce the ISI resulting from copper cables or long printed circuit board (PCB) traces. XAUI lane equalization settings are programmed by writing to the appropriate bits in register LANE_EQ (4x8010.15:0) as shown in the following table.

Table 37. XAUI Receiver Lane Equalization Setting

EQ Control Bits Per Lane	EQ Setting Per Lane	Remarks
Lane 3 (4x8010.3:0) Lane 2 (4x8010.7:4) Lane 1 (4x8010.11:8) Lane 0 (4x8010.15:12)	0000: 0.0 dB (default) 0001: 1.4 dB 0010: 2.2 dB 0011: 2.8 dB 0100: Not defined 0101: 4.5 dB 0110: 5.4 dB 0111: 6.1 dB 1000: Not defined 1001: 6.2 dB 1010: 7.1 dB 1011: 7.8 dB 1100: Not defined 1101: 10.0 dB 1110: 10.8 dB 1111: 11.6 dB	Optimum XAUI lane equalization settings are application specific. Typically, micro-strip traces require less equalization to compensate because of lower losses than stripline construction. Normally, no equalization adjustment is required for XAUI tracks less than approximately 3 inches in FR-4 (microstrip or stripline). Beyond 3 inches, some amount of equalization is recommended for best performance.

3.7.4 XAUI Clock and Data Recovery

At the XAUI receiver, each channel contains an independent clock recovery unit (CRU) that accepts the selected serial input source, extracts the high-speed clock, and retimes the data. Each CRU automatically locks on to data and, if the data is not present, it automatically locks to the reference clock. The clock recovery unit must perform bit synchronization, which occurs when the CRU locks onto and properly samples the incoming serial data.

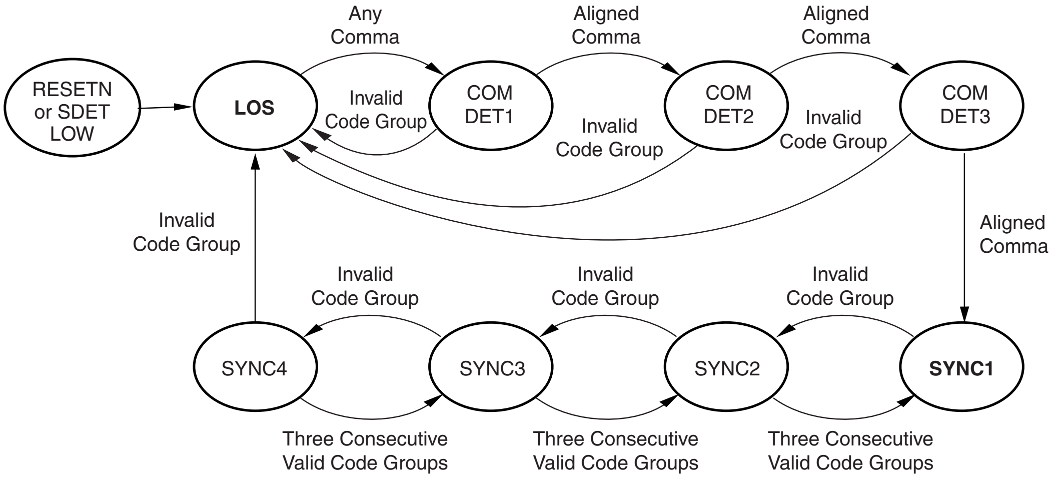
3.7.5 XAUI Code Group Synchronization

The retimed serial data stream is delineated into 10-bit code groups by the deserializer. A special 7-bit comma pattern, 0011111xxx or 1100000xxx (where x is don’t care), is recognized by the receiver as a 10-bit code group boundary.

Character, or code group, alignment occurs when the deserializer synchronizes the 10-bit code group boundary to a comma pattern in the incoming serial data stream. If the receiver identifies a comma pattern in the incoming data stream that is misaligned to the current framing boundary and the receiver is in LOS state, the receiver re-synchronizes the recovered data to align the data to the new comma pattern. Re-synchronization ensures that the comma character is output on the internal 10-bit bus so that bits 0 through 9 equal 0011111xxx or 1100000xxx. If the comma pattern is aligned with the current framing boundary, then the re-synchronization does not change the current alignment.

The detection of a series of consecutive 10-bit code group violations is the mechanism by which loss of synchronization, LANE_SYNC (4x0018.3:0), is declared by the XAUI receiver. The loss of synchronization condition is cleared by the detection of a series of comma characters that are properly aligned on code group boundaries. For additional information, see IEEE Standard 802.3ae Clause 48, Figure 48-7 and the following figure.

Figure 44. Loss of Synchronization (Lane Sync) State Diagram



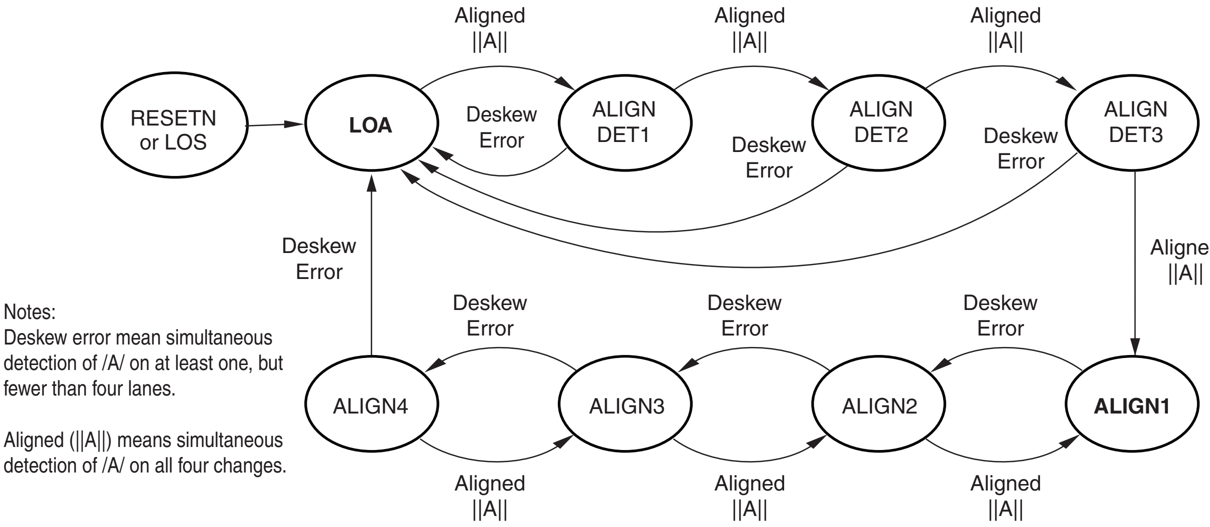
Note that comma detection is enabled only when in the loss of synchronization (LOS) state rather than at all times. This is desirable to prevent incorrect character realignment due to the appearance of false commas, resulting from single-bit errors.

3.7.6 XAUI Lane Deskew

XAUI lane skew occurs due to the skew between channels of a XAUI transmitter and the skew accumulated across the transmission medium. The VSC8486 can deskew up to 63-bit periods of lane-to-lane skew by using elastic buffers. XAUI channel lane deskew is performed by detecting the alignment character /A/ on all four lanes. The PHY XS LANES_ALIGNED bit (4x0018.12), when read as one, indicates all lanes are aligned.

For inter-channel alignment to occur, the ||A|| ordered set consisting of four /A/ code groups must appear, one /A/ on each of the four XAUI lanes. This provides a unique synchronization point across the four serial data streams, which are used to align the received channels. Alignment status is governed by the reception of ||A|| ordered sets across the inputs, as shown in the following loss of alignment (LOA) state diagram.

Figure 45. Loss of Alignment (LOA) State Diagram



Successive synchronization points must be separated by at least 170 bit periods in order for up to 63 bit periods of lane to lane skew to be corrected unambiguously. An IEEE compliant source of XAUI data provides a minimum spacing between sync points of 17 code groups, or 170 bit periods (at least 16 other IDLE code groups must occur between consecutive occurrences of ||A||). The alignment mechanism is always enabled when code group synchronization is attained on all four channels.

3.7.7 10b/8b Decoder

The 10-bit code group from the deserializer is decoded in the 10b/8b decoder, which outputs the data and control bits to the physical coding sublayer (PCS).

If the 10-bit code group does not match a valid code, a code group error is generated that increments the code group error counter GRPERR_CNT_LSW/MSW (4x8003/4x8004). Similarly, if the running disparity of the code group does not match the expected value, a disparity error is generated that increments a running disparity error counter DISPERR_CNT_LSW/MSW (4x8006/4x8007).

3.7.8 8b/10b Encoder and Serializer

Each channel contains an 8b/10b encoder that translates 8-bit data fed internally from the PCS block into a 10-bit code word. This data is then routed into a multiplexer that serializes the word, using the synthesized transmit clock. The most significant bit of the 10-bit data is transmitted first. Each channel has a serial output port, XTX[3:0]P/N, which consists of a differential XAUI output buffer operating at 3.125 Gbps (3.1875 Gbps for 10 GFC).

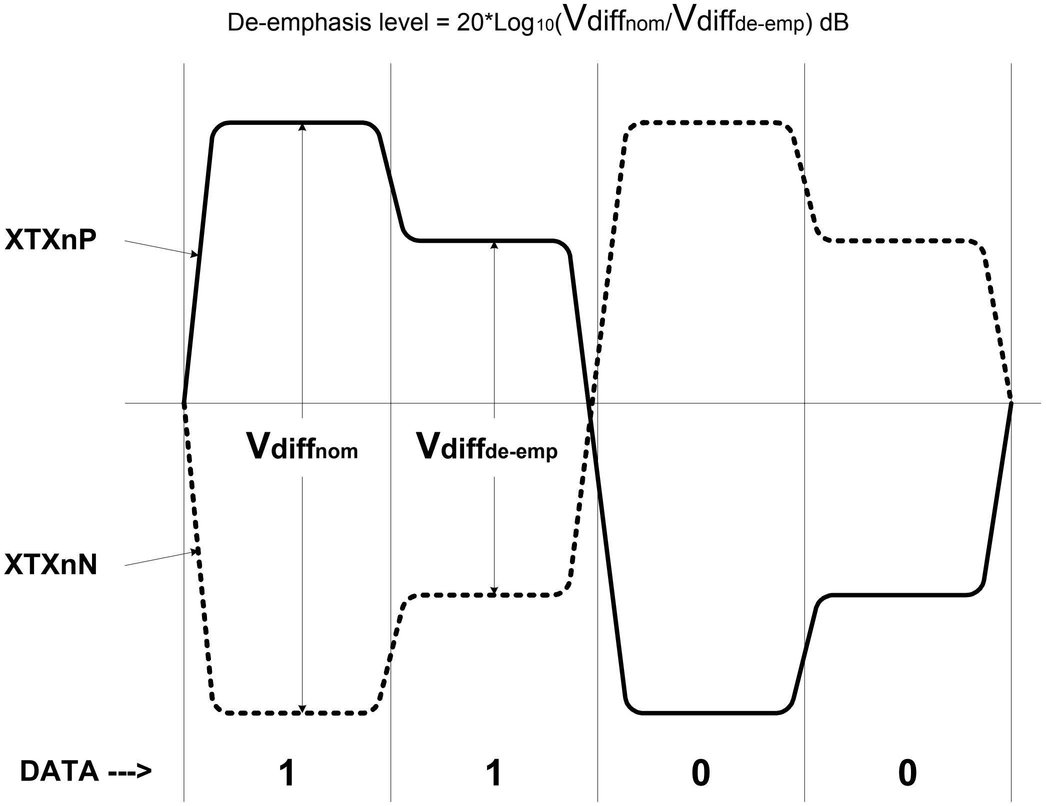
3.7.9 XAUI Transmitter

On the XAUI PHY transmit side (XTX[3:0]P/N), each polarity of the CML-type output driver is back-terminated with 50 Ω to VDDA12, providing a 100 Ω differential output impedance.

3.7.10 XAUI Transmitter Pre-Emphasis

The XAUI output stages include programmable peaking of the transmitted signal for each lane called pre-emphasis. The following figure shows the pre-emphasis waveform definition.

Figure 46. XAUI Output Differential Voltage with Pre-emphasis



When used, transmit pre-emphasis causes the XAUI transmitter signals to be shaped to mitigate skin effect distortion, as shown in the preceding figure. When signal pre-emphasis is employed, the effects of pre-distortion and skin effect distortion offset each other, and a higher quality waveform results at the receiving device.

XAUI lane pre-emphasis settings are programmed by writing to the appropriate bits in XAUI_PE_CFG (4x8011), as shown in the following table. Optimum XAUI lane pre-emphasis settings are application-specific. Normally no pre-emphasis adjustment is required for XAUI tracks less than approximately 5 inches in FR-4 (microstrip or stripline). Beyond about 5 inches, some amount of pre-emphasis is recommended for best performance.

Table 38. XAUI Transmitter Lane Pre-emphasis Setting

Pre-emphasis Control Bits	Pre-emphasis Setting Per Lane
Lane 3 (4x8011.5:4)	00: 0.0 dB (default)
Lane 2 (4x8011.8:7)	01: 2.5 dB
Lane 1 (4x8011.11:10)	10: 6.0 dB
Lane 0 (4x8011.14:13)	11: 12.0 dB

3.7.11 XAUI Transmitter Programmable-Output Swing

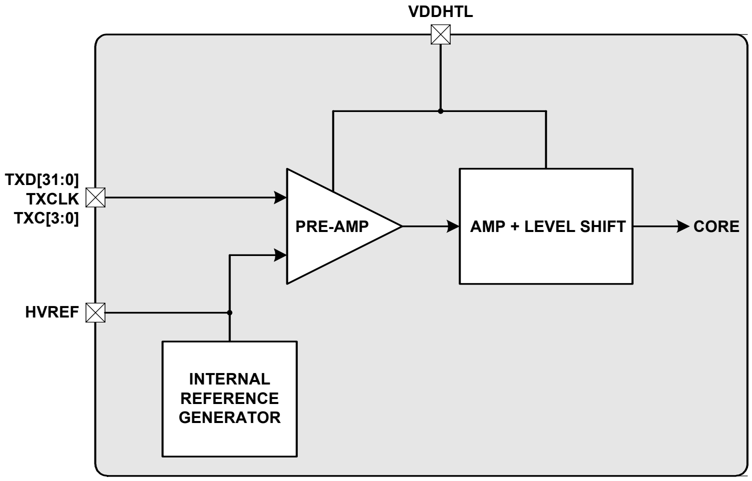
All XAUI output lanes include two peak-to-peak voltage swing settings. Asserting HS_ENA (4x8011.1) increases the output swing on all lanes by approximately 20% over the default output swing.

3.7.12 XGMII Tx Input Interface

The VSC8486 expects to receive a continuous stream of data and control characters from the MAC or 10 GFC equivalent at the XGMII input. The XGMII interface is organized into four groups of eight data bits (octet) and one control bit. Octets originating from a MAC device are received on TXD[31:0] in octet-striped fashion with the first octet appearing on TXD[7:0] (lane 0), the second on TXD[15:8] (lane 1), and so forth. Within the octets, bit ordering is set so that bit 0 of a serial bit stream appears on TXD0, bit 1 appears on TXD1, and so forth. Within each octet, the lowest-numbered bit (bit 0 in the first octet, bit 8 in the second octet, etc.) is considered the LSB.

XGMII data is latched into the VSC8486 on both the rising and falling edges of TXCLK, which serves as a timing reference for the transfer of TXD[31:0] and TXC[3:0] across the XGMII interface. TXCLK is 156.25 (159.375) MHz clock, ±100 ppm. The XGMII interface follows the high-speed transceiver logic (HSTL) electrical specifications for a 1.5 V supply voltage, as specified in EIA/JESD8-6 for Class I output buffers. The HSTL inputs are designed to function with or without termination. For the specifications and timing diagrams, see “XGMII Specifications,” page 223. Simplified diagrams of the XGMII input and output structures are illustrated in the following figure.

Figure 47. XGMII Input Simplified Schematic

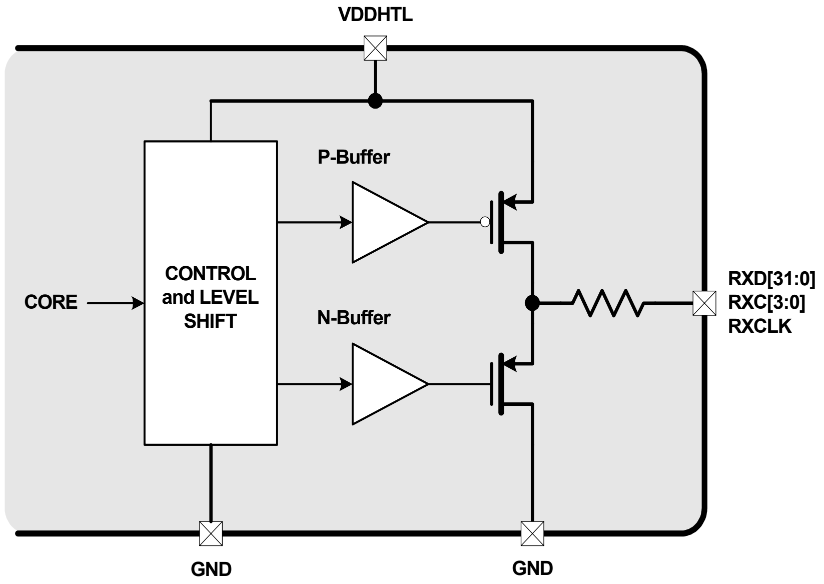


3.7.13 XGMII Rx Output Interface

The VSC8486 provides a continuous stream of data and control characters to the MAC or 10GFC equivalent on its XGMII outputs. The XGMII interface is organized into four groups of eight data bits (octet) and one control bit. Octets originating from the PCS block are transmitted on RXD[31:0] in octet striped fashion, with the first octet appearing on RXD[7:0] (lane 0), the second on RXD[15:8] (lane 1), and so forth. Within the octets, bit ordering is such that bit 0 of a serial bit stream appears on RXD0, bit 1 appears on RXD1, and so forth. Within each octet, the lowest-numbered bit (bit 0 in the first octet, bit 8 in the second octet, and so forth.) is considered the LSB.

XGMII data is latched to the output of the VSC8486 on both rising and falling edges of RXCLK, which serves as a timing reference for the transfer of RXD[31:0] and RXC[3:0] across the XGMII interface. The RXCLK output is 156.25 MHz (159.375 MHz) ±100 ppm. The XGMII interface follows the high-speed transceiver logic (HSTL) electrical specifications for a 1.5 V supply voltage, as specified in the EIA/JESD8-6 for Class I output buffers. The HSTL outputs are designed to function with or without termination and swing from the ground rail to the power supply rail without termination. For more information about specifications and timing diagrams, see "XGMII Specifications," page 223. For more information about the simplified diagrams of the XGMII output structures, see the following diagram.

Figure 48. XGMII Output Structure and Termination



3.8 MDIO Serial Interface

The VSC8486 contains a management data input/output (MDIO) interface, as specified in IEEE Standard 802.3ae Clause 45. This section provides an overview of the operation of the MDIO interface. For more information, see IEEE Standard 802.3ae Clause 45.

3.8.1 MDIO Interface Operation

The operational sublayers within the device are individually known as MDIO-manageable devices (MMDs). Using the PRTAD[4:0] pins, the station management entity (STA) can access up to 32 PHYs. Using the 5-bit DEVAD field within the management frame format, up to 32 MMDs can be addressed in each PHY. The MDIO-manageable device addresses are shown in the following table.

Table 39. MDIO-Manageable Device Addresses

Device Address	MMD Name
0	Reserved
1	PMA
2	WIS
3	PCS
4	PHY XS
5	DTE XS (not implemented)
6:29	Reserved
30	Vendor-specific name for two-wire serial CPU interface
31	Vendor specific name

The management frame format supports indirect addressing to provide more accessible register space within each MMD (for more information, see Figure 49, page 103). The management frame field structure is shown in the following table.

Table 40. Management Frame Format for Indirect Register Access

	Management Frame Fields							
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**Address/Data**	**Idle**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read increment	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

A 16-bit address register stores the address of the register to be accessed by data transaction frames. The address register is overwritten by address frames. Upon device-reset, the contents of the address register is set to zero. At power up, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames access the register whose address is stored in the address register. Write and read frames do not modify the contents of the address register.

After receiving a post-read-increment-address frame and completing the read operation, the address register is incremented by one. When the register contains 65,535, the address register is not incremented.

The idle condition is a high-impedance state. All tri-state drivers are disabled, and the pull-up resistor pulls the MDIO line to a one.

At the beginning of each transaction, the station management entity (STA) sends a preamble (PRE) sequence of 32 continuous one-bits on MDIO during 32 corresponding cycles on the management data clock (MDC), providing a pattern that the MMD uses to establish synchronization. All MMDs observe the 32 continuous one-bits before responding to any transaction.

Figure 49. MDIO Frame Format

The MDIO frame format consists of the eight segments, shown above. Definitions for the segments are shown in the following table.

PRE 32	32 bits of 1 supplied by the STA.
ST	2 bits of 0, which indicates the start of frame.
OP	2 bits of Op-Code as described in IEEE 802.3ae Clause 45.
PA 5	5 bits of port address, which provides up to 32 ports to a physical bus.
DA 5	5 bits of destination MMD address, which provides up to 32 MMDs to a port.
TA	2 bits of turnaround time to change the bus ownership from the STA to MMD if required.
D 16	16 bits for address/data driven on the bus by the current master of the bus, the STA for write operation, and the MMD for a read or read-address-increment operation.
Z	Idle time, bus tri-stated.

The start of frame (ST) is indicated by the ‘00’ pattern. Frames containing the ST = ‘01’ pattern that is defined in IEEE Standard 802.3ae Clause 22, are ignored.

The operation code (OP) indicates the type of transaction being performed by the frame. A ‘00’ pattern indicates that the frame payload contains the address of the register to access. A ‘01’ pattern indicates that the frame payload contains data to be written to the register whose address is provided in the previous address frame. A ‘11’ pattern indicates that the frame is a read operation. A ‘10’ pattern indicates that the frame is a post-read-increment-address operation.

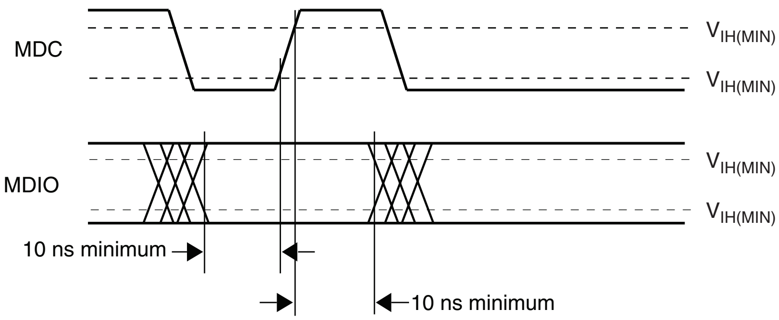
The port address (PRTAD) consists of five bits. The first bit to be transmitted and received is the MSB. The device address (DEVAD) also consists of five bits. The first bit transmitted and received is the MSB.

Turnaround (TA) is a two-bit time spacing between the DEVAD field and data field of a frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, the STA and MMD remain in a high-impedance state for the first-bit time of the turnaround. The MMD drives a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA drives a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround.

The address or data field consists of 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, and increment read cycles, the field contains the data for the register. The first bit transmitted and received is bit 15.

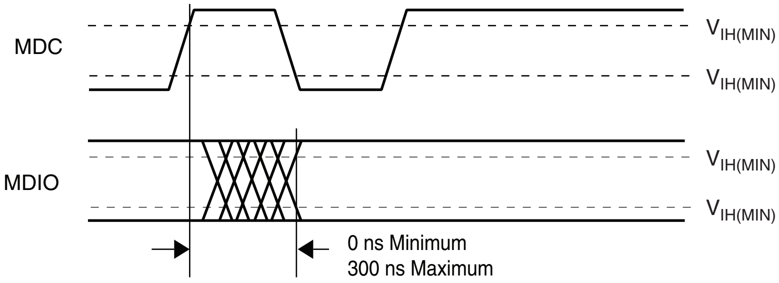
MDIO is a bidirectional signal that can be sourced by STA or the MMD. When STA sources the MDIO signal, a minimum of 10 ns of setup time and 10 ns of hold time with reference to the rising edge of MDC is provided, as shown in the following figure.

Figure 50. Timing When MDIO Is Sourced by STA



When MDIO is sourced by the MMD, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock-to-output delay from the MMD, as measured at STA, is a minimum of 0 ns and a maximum of 300 ns, as shown in the following figure.

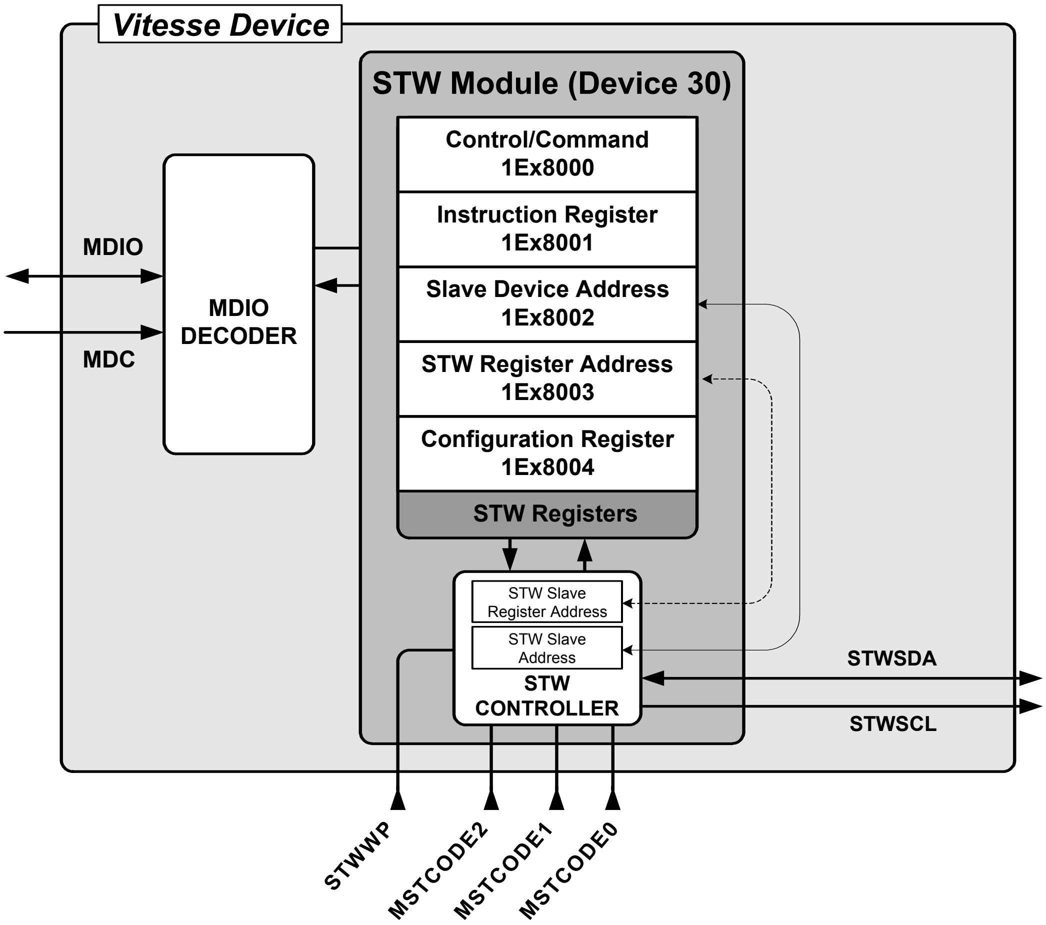
Figure 51. Timing When MDIO Is Sourced by MMD



3.9 Serial Two-Wire (STW) Interface

The VSC8486 contains a serial two-wire management interface that provides a communication bus to slave peripherals such as non-volatile registers (NVR) or digital optical monitor (DOM) devices. The bus is intended to facilitate serial communication within a XENPAK/X2 module or with an XFP-compliant device; however, other devices can also be used. The two-wire serial bus is controlled using the MDIO interface. The STW interface is an industry-standard, master-only controller and supports two rates: standard (100 kbps) and fast (400 kbps). The MDIO control registers are shown in the following figure.

Figure 52. Serial Management Interface



The STW interface uses a bidirectional data and clock signal named STWSDA and STWSCL, respectively. The STW write protect pin STWWP, when pulled high, inhibits STW write activity.

The STW interface controller supports 7-bit addressing, as configured in STW_ADDR_MODE (1Ex8004.11).

Writing to the MDIO register STW_CTRL1 (1Ex8000) initiates activity on the STW interface. There are two modes of operation: Automatic and Manual. In Automatic mode, up to 256 bytes are automatically copied from an external NVR device to the internal STW interface registers or vice versa. In Manual mode, you can access bus peripherals on a per-byte basis. In this mode, any instruction written to STW_CTRL2 (1Ex8001) initiates execution of the instruction.

The STW controller logic operates independently from the MDIO interface. Thus, when the MDIO initiates an STW read/write command, the MDIO logic is not halted or locked while waiting for the STW command to complete. Because there is no queuing of STW commands, station management software must poll the STW controller to ensure that each STW command is complete before initiating the next command.

3.9.1 STW Controller Description

The STW bus is controlled using five registers located in device 30 (0x1E).

STW_CTRL1 (1Ex8000) This register is the same as the NVR Control/Status register x8000 defined in XENPAK MSA Revision 3.0, with one exception. In addition to the XENPAK defined structure, the VSC8486 uses bit 8 of this register to set the STW interface operational mode. The MDIO decoder activates the STW interface module by writing to this register. Writes to this register through MDIO during a STW interface action are ignored.

STW_CTRL2 (1Ex8001) This register is only active when Manual mode is selected. One instruction written to this register using MDIO causes the STW interface controller to read or write one data byte from or to the STW bus. Writes to this register through MDIO during execution of an instruction are ignored.

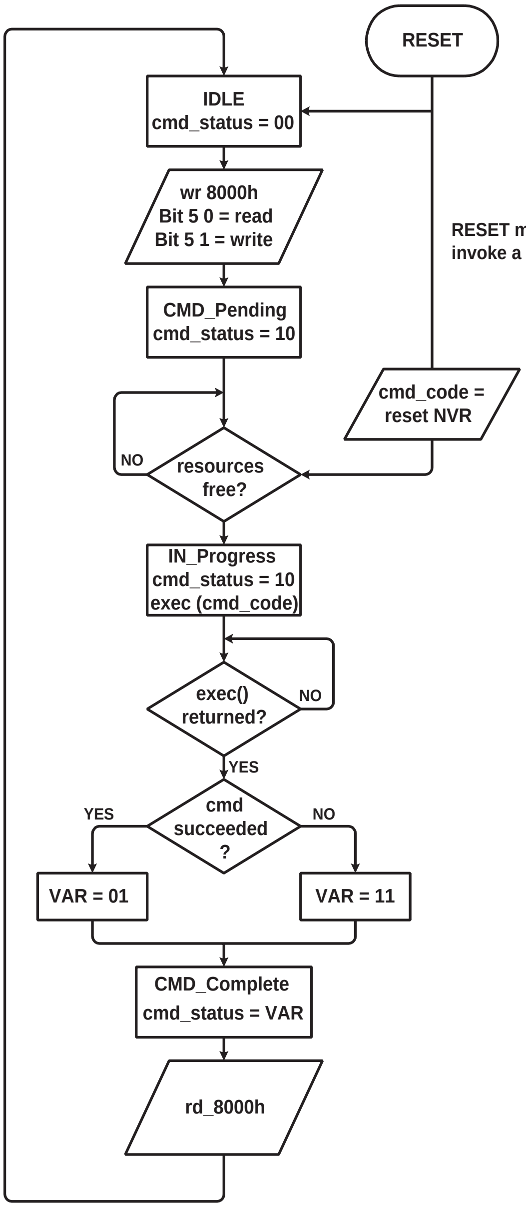
STW_DEVADDR (1Ex8002) This register stores the STW slave device address that is read or written. Note that the 7-bit address is entered into bits 6:0 in the register. The STW controller does not directly use the register contents, but instead latches the contents into internal logic when SYNC_ADDR (1Ex8001.9) is asserted. This allows the address register to be updated while the STW controller is active. All XFP modules use the same seven-bit address 0xA0, which, when entered into the registers, become 0x50.

STW_REGADDR (1Ex8003) This register is used to store the address of the STW target register which is used to store the data read from or written to the slave device. Similar to register 1Ex8002, this register is not directly used by the STW controller, but is latched into internal logic when SYNC_REGADDR (1Ex8001.8) is asserted.

STW_CFG1 (1Ex8004) This register is used to configure the desired operating mode for the STW controller. Bits 11:9 configure the STW interface master bus controller operating characteristics, bus signaling speed, and addressing mode. Bit 12 sets the STW controller to make block reads or writes in accordance with the XENPAK or XFP register maps. The XFP and XENPAK modes are different only when the STW_MODE (1Ex8000.8) is configured for Automatic mode. In Manual mode, the XENPAK and XFP modes are same. In Automatic mode, the XFP or XENPAK register contents are mapped into 256 eight-bit registers beginning at internal address 1Ex8007 and ending with 1Ex8106.

The STW controller is initiated by writing to the STW_CTRL1 (1Ex8000). After each transaction begins the controller updates the STW_CMDSTAT (1Ex8000.3:2) field with a ‘10’ command in progress status. In this state, the MDIO interface cannot read or write to the STW control registers. After the controller completes the data read or write transaction, the STW_CMDSTAT (1Ex8000.3:2) field is updated to either ‘01’ to reflect a successful operation or ‘11’ to reflect a failed operation. The MDIO interface then regains access to the STW controller registers. The following figure shows the state diagram of the STW controller.

Figure 53. STW Access State Diagram



3.9.2 Automatic Mode

Automatic mode provides easy access to non-volatile registers (NVR), such as EEPROM, used in XENPAK and XFP modules. In Automatic mode, the STW interface controller performs reads or writes to different sections of non-volatile memory according to the value of the extended command bits, STW_EXT_CMD (1Ex8000.1:0). A value of ‘11’ reads or writes all NVR contents, which is compliant with XENPAK MSA revision 3.0, section 10.10. STW_CMD (1Ex8000.5) determines whether the operation is read or write.

In Automatic mode, the STW interface maps internal registers 1Ex8007 through 1Ex8106 to external NVR address 0 to 255. To perform an automatic read, first write STW_DEVADDR (1Ex8002), and then write STW_CTRL1 (1Ex8000) using the proper settings. The STW interface controller reads the data stored in a certain section of NVR, which is defined by STW_EXT_CMD (1Ex8000.1:0), and saves data to the corresponding section of internal VSC8486 registers. For example, if the data written to STW_CTRL1 (1Ex8000) is 0x0000, the STW interface controller reads XFP EEPROM bytes 2-57, and stores the data in registers 1Ex8009 to 1Ex8040. The automatic write operation is similar.

The auto read or write operations are compatible with the ATMEL AT24Cxx series serial two-wire EEPROM. For a detailed description of the read or write operations, see the ATMEL AT24Cxx Series Two-Wire Serial EEPROM specification. After the read or write operation is complete, the STW interface controller writes to STW_CMD_STATUS (1Ex8000.3:2) to set the appropriate code. A ‘01’ indicates a successful operation, and a ‘11’ indicates a failed operation.

Example 1 Use the following procedure to perform an automatic block read operation:

1. Write the address of the slave device to the Slave Device Address register (1Ex8002) (50’h for XFP modules).
2. Write to the configuration register (1Ex8004) bit 12 = 1 (XFP module).
3. Write 0x0000 to STW_CTRL1 (1Ex8000). XFP bytes 2 through 57 are auto read.

3.9.3 Manual Mode

A value of 1 in STW_MODE (1Ex8000.8) sets the STW interface module to Manual mode. This mode can be used to achieve communication with any other STW-compliant devices connected to the STW bus through the MDIO interface, or to access single bytes within the non-volatile registers. In this mode, any instruction written to STW_CTRL2 (1Ex8001) initiates a connection with other devices, or to read or write byte data from or to other devices. The instruction set is shown in the following table.

Table 41. STW Instruction Summary

Instruction (1Ex8001)	Description
0x0301	Read registers 1Ex8002 and 1Ex8003 to controller and start or restart with slave transmitter
0x0201	Read register 1Ex8003 to controller and start or restart with slave transmitter
0x0101	Read register 1Ex8002 to controller and start or restart with slave transmitter
0x0001	Start or restart with slave transmitter
0x0309	Read registers 1Ex8002 and 1Ex8003 to controller and start or restart with slave receiver
0x0209	Read register 1Ex8003 to controller and start or restart with slave receiver
0x0109	Read register 1Ex8002 to controller and start or restart with slave receiver
0x0009	Set connection with the slave receiver

Table 41. STW Instruction Summary *(continued)*

Instruction (1Ex8001)	Description
0x0204	Read 1Ex8003 to controller, read data from slave transmitter, and save data to register addressed 1Ex8003
0x0004	Read data from slave transmitter and save data to the register whose address is stored in controller
0x0202	Read 1Ex8003 to controller, read data from slave transmitter, save data to register addressed by 1Ex8003, and then terminate the transfer and disconnects with slave transmitter
0x0002	Read data from slave transmitter, save data to the register whose address is stored in controller, and then terminate the transfer and disconnects with slave transmitter
0x0208	Read 1Ex8003 to controller and write the data stored in the register addressed by 1Ex8003 to slave receiver
0x0008	Write content of the register whose address is stored in controller to slave receiver
0x020A	Read 1Ex8003 to controller, write the data stored in the register addressed 1Ex8003 to slave receiver, and then terminate the transfer and disconnects with slave receiver
0x000A	Write the content of the register whose address is stored in the controller to slave receiver and then terminate the transfer and disconnect from the slave receiver
0x0020	Soft reset transceiver

Following a write transaction to STW_CTRL2 (1Ex8001), the STW interface module reads the contents of that register and sets STW_MAN_STATUS (1Ex8001.7:6) to ‘10’ (instruction in progress).

- If the instruction executes successfully, the STW interface module writes to STW_CTRL2 (1Ex8001), setting the STW_CMD_STATUS bits to ‘01’ (instruction completed successfully), and is then ready to take the next instruction. Successful execution of instructions 0x0002 and 0x000A makes the command completion successful.
- If the instruction execution fails, STW_MAN_STATUS is set to 11. Execution failure of an instruction also leads to command failure, and 11 is written to the STW_CMD_STATUS (1Ex8000.3:2).

3.9.4 Serial Two-Wire Interface Command Sequence Examples

The next two examples describe the command sequence for a single-byte read or write from a slave device connected to the STW interface bus in Manual mode.

Example 2 Use the following procedure to perform a manual random-read operation to a STW device. This example reads an XFP module's address of 0x13 and places the contents in 1Ex8023.

1. Read STW_CMD_STATUS (1Ex8000.3:2) to ensure the STW controller is in the idle state.

2. Write the necessary address value(s) into temporary holding registers between 1Ex8007 and 1Ex8106. Note the registers between 1Ex8007 and 1Ex8106 must be set prior to a write to STW_CTRL1 (1Ex8000), because these registers are locked from MDIO access until the STW controller returns to the idle state.
3. Write the target address into a temporary register. For example, set 1Ex801E to 0x13.
4. Configure the STW_CFG1 (1Ex8004) as needed.
5. Enter manual STW mode by writing 0x0100 into STW_CTRL1 (1Ex8000).
6. Write the device address of the STW target device into STW_DEVADDR (1Ex8002). Note the placement of the value within the register fills bits 6:0, so a target device within an XFP module would have a value of 0x50).
7. Write the address of the temporary holding register used in step 2 into STW_REGADDR (1Ex8003); for example, set 1Ex8003 to 0x801E.
8. Initiate the STW instructions by setting STW_CTRL2 (1Ex8001) to 0x0309. This initialization updates the STW controller with the values held in registers STW_DEVADDR (1Ex8002) and STW_REGADDR (1Ex8003). It then send a start command followed by the device address and write bits.
9. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
10. Continue the STW instructions by setting STW_CTRL2 (1Ex8001) to 0x0008. This setting sends the target address. This byte is the value held in the register pointed to by STW_REG_ADDR (1Ex8003); for example, 1Ex8003 points to 1Ex801E, which contains the value 0x13.
11. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
12. Tell the STW instruction where to place the contents of the value read by writing a temporary holding register address between 0x8007-0x8106 into STW_REGADDR (1Ex8003); for example, set 1Ex8003 to 0x8023.
13. Send the STW instruction to perform the read preparation command by setting STW_CTRL2 (1Ex8001) to 0x0001. This setting sends a start command followed by the device address and read bits.
14. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
15. Send the STW instruction to perform the capture the data setting STW_CTRL2 (1Ex8001) to 0x0202. This setting updates the STW controller with the contents of STW_DEVADDR (1Ex8002). It then reads the contents from the slave device, after which a stop command is sent. The read data is placed in the specified register.
16. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
17. Ensure the STW controller completed successfully by reading STW_CMD_STATUS (1Ex8000.3:2) and expect the ‘01’ (command complete) value.
18. Read the contents of the temporary holding register. In this case, it was 1Ex8023.

Example 3 Use the following procedure to perform manual random write operations to a STW device. This example writes the power-down bit (0x6E.3) within an XFP module.

1. Read STW_CMD_STATUS (1Ex8000.3:2) to ensure the STW controller is in the idle state.
2. Write the necessary address and data values into temporary holding register between 1Ex8007-1Ex8106. Note, the registers between 1Ex8007-1Ex8106 must be set prior to a write to STW_CTRL1 (1Ex8000), because these registers are locked from MDIO access until the STW controller returns to the idle state.
3. Write the target address into a temporary register. For example, set 1Ex8022 to 0x6E).
4. Write the target data value into a temporary register. For example, set 1Ex8029 to 0x08.
5. Configure STW_CFG1 (1Ex8004) as needed.
6. Enter manual mode by writing 0x0100 into STW_CTRL1 (1Ex8000).
7. Write the device address of the STW target device into STW_DEVADDR (1Ex8002). Note the placement of the value within the register fills bits 6:0, so a target device within an XFP module has a value of 0x50.
8. Write the address of the temporary holding register used in step 2 into STW_REGADDR (1Ex8003); for example, set 1Ex8003 to 0x801E.
9. Initiate the STW instructions by setting STW_CTRL2 (1Ex8001) to 0x0309. This setting updates the STW controller with the values held in registers STW_DEVADDR (1Ex8002) and STW_REGADDR (1Ex8003). It then sends a start command followed by the device address and write bits.
10. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
11. Continue the STW instructions by setting STW_CTRL2 (1Ex8001) to 0x0008. This setting sends the target address. This byte is the value held in the register pointed to by STW_REGADDR (1Ex8003); for example, 1Ex8003 points to 1Ex801E, which contains the value 0x13.
12. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.
13. Tell the STW controller where to obtain the intended write data by writing the address of the temporary holding register used in step 2 into STW_REGADDR (1Ex8003); for example, set 1Ex8003 to 0x8029.
14. Send the STW instruction to perform the write by setting STW_CTRL2 (1Ex8001) to 0x020A. This setting updates the controller with the pointer found in STW_REGADDR (1Ex8003). It then sends the data followed by a stop command.
15. Ensure the STW instruction completed successfully by reading STW_MAN_STATUS (1Ex8001.7:6) and expect the ‘01’ (instruction complete) value.

16. Ensure the STW controller completed successfully by reading STW_CMD_STATUS (1Ex8000.3:2) and expect the ‘01’ (command complete) value.

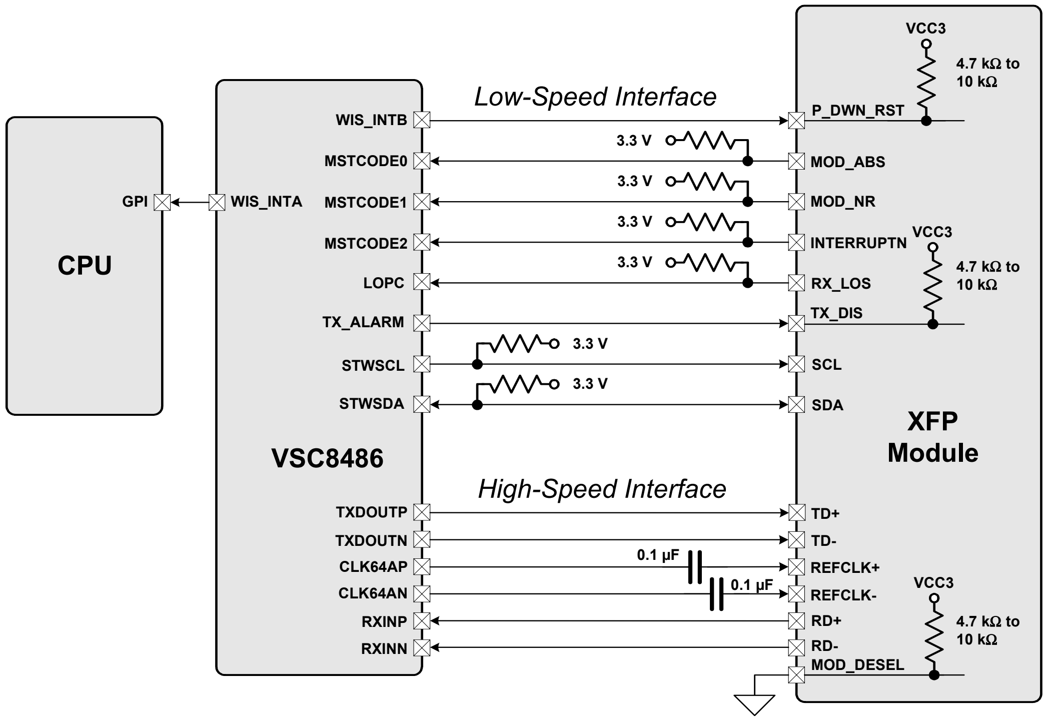
17. Read the contents of the temporary holding register, in this case 1Ex8023.

3.10 XFP or SFP+ Module Interface

Several VSC8486 I/O pins can be reconfigured (using MDIO) from their default function to interface with all of the XFP or SFP+ status and control I/O pins, including the serial two-wire (STW) bus.

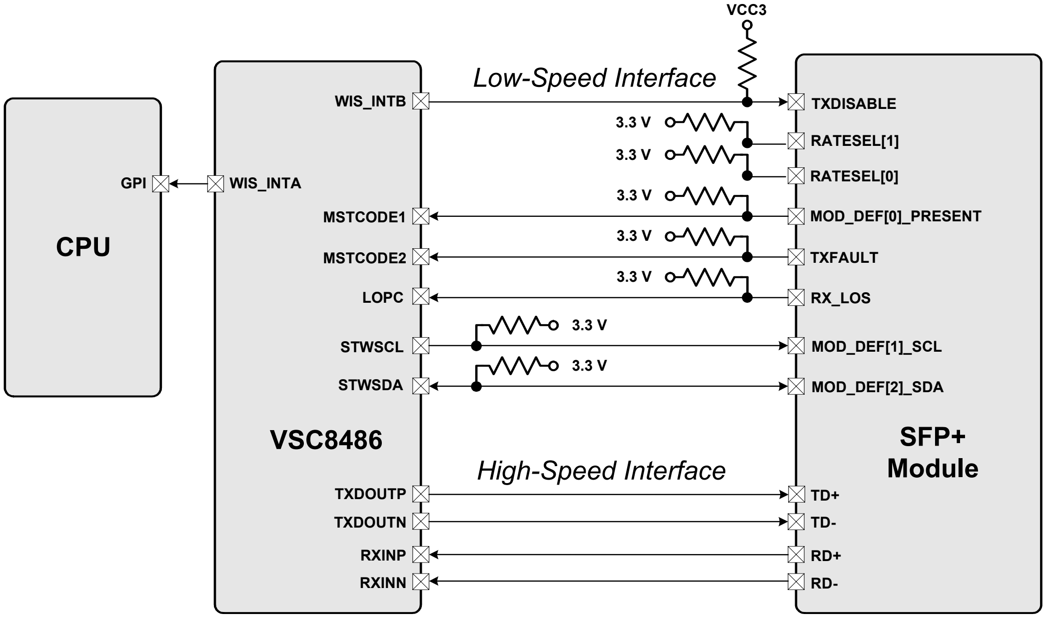
In an XFP host application, the recommended pin connections are as shown in the following figure.

Figure 54. VSC8486 to XFP Host Recommended Interface Connections



In an SFP+ host application, the recommended pin connections are as shown in the following figure.

Figure 55. VSC8486 to SFP+ Host Recommended Interface Connections



Note To avoid a criss-cross in the connection to SFP+, it is recommended the TXDOUTP/N polarity be swapped. To program the TXDOUTP/N polarity, use register 1x8000.7.

Each of the recommended low-speed interface signals used on the VSC8486 in an XFP or SFP+ host application are summarized in the following table.

Note Because the VSC8486 device operates at 10 gigabits, the SFP+ module pins KSO (pin 7) and RS1 (pin 9) should be tied high externally.

Table 42. XFP or SFP+ Host Application Pin Connections Summary

VSC8486 Pin	I/O	Default Operation	XFP Host Operation	SFP+ Host Operation	Comments
WIS_INTB	Open-drain output	XFP module P_DWN_RST	XFP module P_DWN_RST	SFP+ module TXDISABLE	Pull-up resistor provided inside the XFP or SFP+ module. See register 1xE902.2:0 and 1xE901.9 for additional options. Polarity invert (1xE902.1 and 1xE605.15).
MSTCODE0(1)	LVTTL input	STW high-speed master code0	MOD_ABS	Not used with SFP+	See interrupt pending register (2xEF00.14:12) and mask (2xEF01.14:12) and pin status (1xE607.15:13).
MSTCODE1(1)	LVTTL input	STW high-speed master code1	MOD_NR	GPIO_PRESENT	See interrupt pending register (2xEF00.14:12) and mask (2xEF01.14:12) and pin status (1xE607.15:13).

Table 42. XFP or SFP+ Host Application Pin Connections Summary *(continued)*

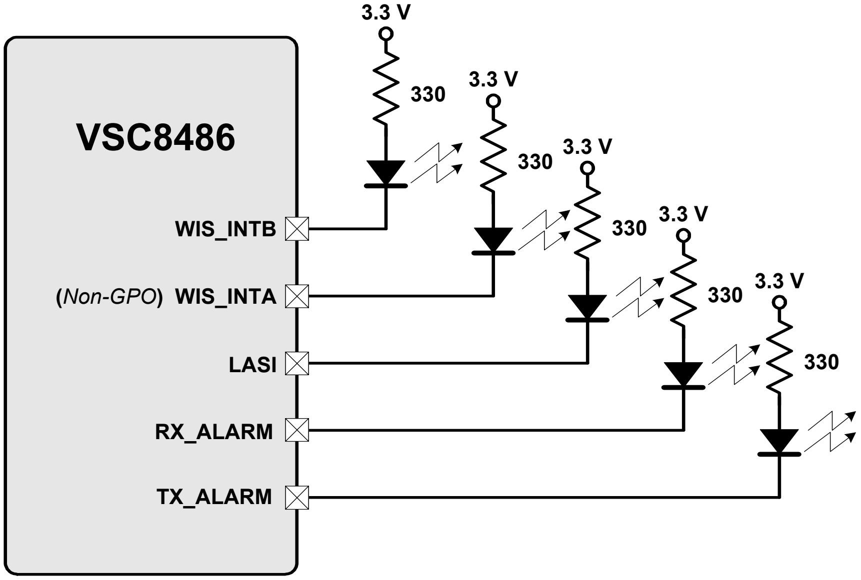
VSC8486 Pin	I/O	Default Operation	XFP Host Operation	SFP+ Host Operation	Comments
MSTCODE2[1]	LVTTL input	STW high-speed master code2	INTERRUPTN	GPIO_TXFAULT	See interrupt pending register (2xEF00.14:12) and mask (2xEF01.14:12) and pin status (1xE607.15:13).
LOPC	LVTTL input	Loss of optical signal	Loss of optical signal	Loss of optical signal	Provide pull-up externally, nominally 4.7 kΩ. Provide pin status on 1xE607.0.
TX_ALARM	Open-drain output	Global SERDES transmit channel fault	TX_DIS	Not used with SFP+	For XFP, configure as GPO using 1xE901.14:13 set to 10 (default is 00) and then use 1xE901.8 set to force.
STWSCL	Open-drain output	STW clock source	SCL	SCL	STW interface clock. See 1xE900.3:0.
STWSDA	Bidirectional open-drain output	STW bidirectional data line	SDA	SDA	STW interface data line. See 1xE900.3:0.
TXDOUTP/N	CML diff pair output	XFI Tx	TD+/–	TD+/–	10-gigabit serial data from the VSC8486 to the XFP or SFP+ module.
REFCLKAP/N	CML diff pair output	Div/64 reference clock to XFP	REFCLKP/N	REFCLKP/N	For XFP, CLK64AP/N (CMU/64) enabled by default. Disable using CLK64A_EN or register 1xE602.9.
RXINP/N	CML diff pair output	XFI Rx	RD+/-	RD+/-	10-gigabit serial data to the VSC8486 from the XFP or SFP+ module.
WIS_INTA	Open-drain output	Selectable WIS interrupt output	Output to CPU	Output to CPU	Global XFP or SFP+ alarm interrupt signal to CPU.

1. With the MSTCODE[2:0] pins utilized for XFP or SFP+ operation, the STW interface can still be used in high-speed mode. To accomplish this, assert register bit 1xE900.3 to set the master code from registers 1xE900.2:0 instead of from the MSTCODE[2:0] pins.

3.10.1 General Purpose and LED Driver Outputs

The VSC8486 includes several output pins that are capable of directly driving light emitting diodes (LEDs) and are programmable through MDIO. These outputs use open drain configuration and require pull-up resistors as shown in the following diagram.

Figure 56. Interrupt/Status/Activity LED Connections



The following table includes configuration options for the general purpose output (GPO) pins. Registers 1xE900, 1xE901, and 1xE902 are used to program the GPO function.

Table 43. GPO Configuration Control Summary

Pin Name	Source Select	GPO Mode Output Control	Other Controls
WIS_INTB (L6)	1xE901.9 0: XFP module reset or SFP+ TXDISABLE (default) 1: WIS interrupt B function	If WIS interrupt B enabled (1xE901.9 = 1), then 1xE607.2 displays WIS_INTB pin status.	WIS_INTB_POL (1xE605.15). EWIS_MASKB_1 (2xEF02). EWIS_INTR_MASKB2 (2xEF06).
LASI (E5)	1xE901.10 0: Normal LASI output (default) 1: GPO mode	If GPO mode is active (1xE901.10 = 1), then bit 1xE901.6 is transmitted to LASI.	LASI output is disabled by default and enabled using 1Ex9002.0 (reference is Xenpak 3.0).
RX_ALARM (C4)	1xE901.12:11 00: Normal RX_ALARM (default) 01: Rx link/activity LED 10: GPO mode 11: Reserved	If GPO mode is active (1xE901.12:11 = 10), then bit GPO_RXALARM (1xE901.7) is transmitted to RX_ALARM.	RX_ALARM is clear on read by default and controlled using 1Ex9003 (reference is Xenpak 3.0). Other controls: Rx LED mode control (1xE901.1:0) and Rx data activity LED blink time (1xE901.4).
TX_ALARM (E4)	1xE901.14:13 00: Normal TX_ALARM (default) 01: Tx Link/Activity Mode 10: GPO Mode 11: Reserved	If GPO mode is active (1xE901.14:13 = 10), then bit GPO_TXALARM (1xE901.8) is transmitted to TX_ALARM.	TX_ALARM is clear on read by default and controlled using 1Ex9004 (reference is Xenpak 3.0). Other controls: Tx LED mode control (1xE901.3:2) and Tx data activity LED blink time (1xE901.5).

When the RX_ALARM output is programmed to Rx Link/Activity Mode, an external LED responds as follows: Rx Activity Status indicates receipt of ||S|| characters, and Rx Link Status indicates PCS block lock = 1. (LED is on during block lock.)

The Combination Rx Link/Activity Status mode (1xE901.12:11 = 01) indicates the following:

- LED is off – Rx Link is down
- LED is on steady – Rx Link is up, but no ||S|| characters received
- LED blinking – Link is up and receiving ||S|| characters (steady state blink with off time set to approximately 100 milliseconds)

When the TX_ALARM output is programmed to Tx Link/Activity Mode, an external LED responds as follows: Tx Activity Status indicates transmission of ||S|| characters, and Tx Link Status indicates XAUI Lanes is aligned or is transmitting ||S|| characters when the transmitted traffic source is XGMII.

The Combination Tx Link/Activity Status mode (1xE901.14:13 = 01) indicates the following:

- LED is off – Tx Link is down
- LED is on steady – Tx Link is up, but no ||S|| characters transmitted
- LED blinking – Tx Link is up and transmitting ||S|| characters (steady state blink with off time set to approximately 100 milliseconds)

Both Rx and Tx combination link/activity status outputs initially hold the LED on for up to 5 seconds, even if data activity begins in less time. If the link is down, the LED is off, regardless of elapsed time.

Note The link/activity status outputs only work for PCS mode, not E-PCS mode.

3.11 JTAG Access Port

A JTAG access port is provided on the VSC8486 transceiver to facilitate device level and board-level testing. All pins with the exception of the 10 Gbps serial pins and some analog pins can be accessed or controlled through this port. This port is compliant with IEEE Standard 1149.1-2001 (subsequently referred to as the JTAG specification) with the five control TTL signals listed in the following table.

Table 44. JTAG TTL Signals

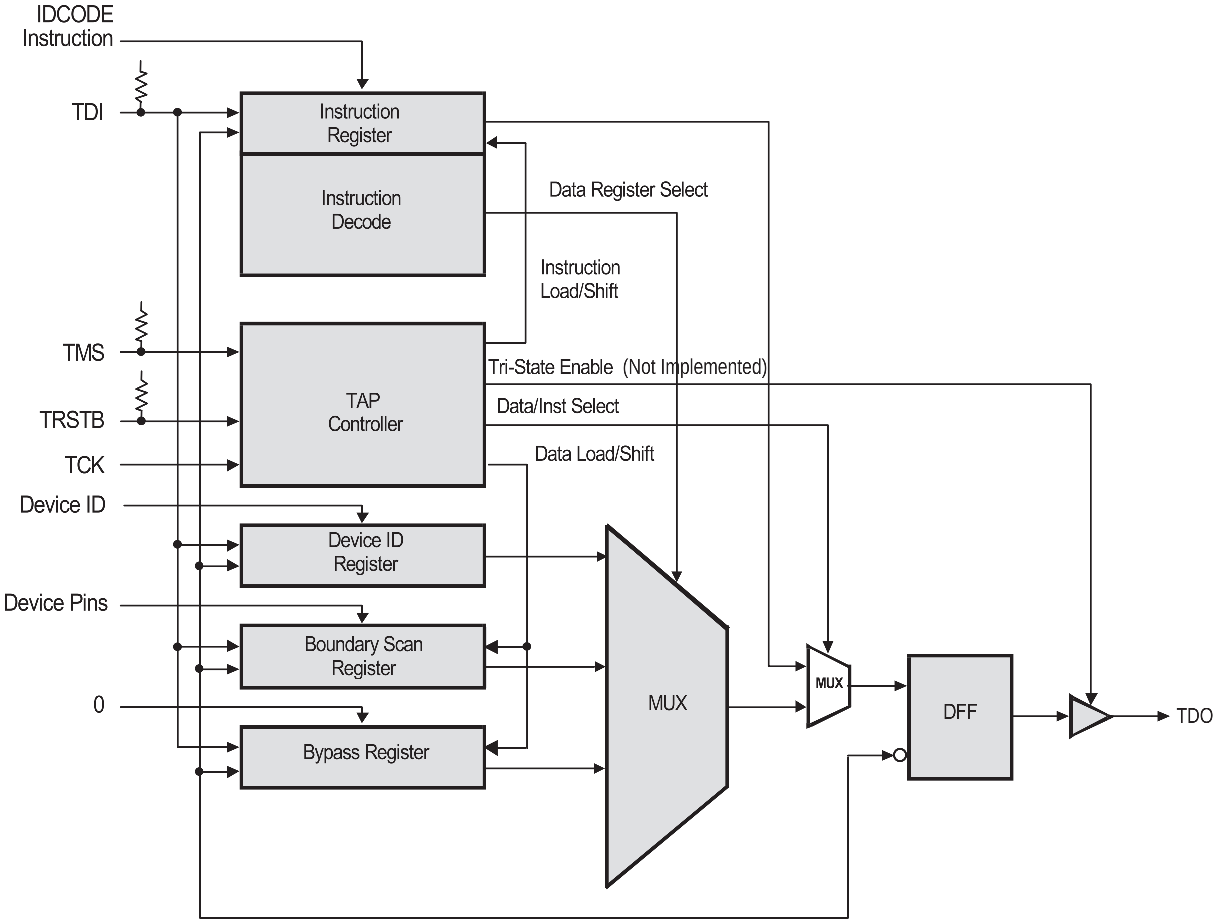
Signal	Description
TCK	Test clock input
TMS	Test mode select input
TDI	Test data input
TDO	Test data output
TRSTB	Test reset input

These signals control the Test Access Port (TAP) and associated circuitry to enable boundary and internal scan testing operations.

To ensure reliability, a TRSTB input (instead of a power-on reset circuit) is provided to initialize the JTAG logic. This input, TRST* in the JTAG specification, is asserted when in the low (logic 0) state. The TRSTB, TDI, and TMS input pins have an on-chip, high-impedance, pull-up resistor connected to the VDDTTL supply so that an un-driven input behaves as though a logic 1 were applied. Because the TAP controller is reset from the TRSTB signal and not a power-on reset circuit, the TAP controller, without a reset, can come up in an indeterminate state, thereby affecting the mode of inputs and outputs. It is imperative that users ensure that the TAP controller is reset prior to normal operation. This can be achieved by tying TRSTB low (logic 0) if JTAG is undesired or ensuring the pull-down is strong enough to overcome the internal pull-up resistor, yet weak enough that the JTAG exerciser can overcome the pull-down.

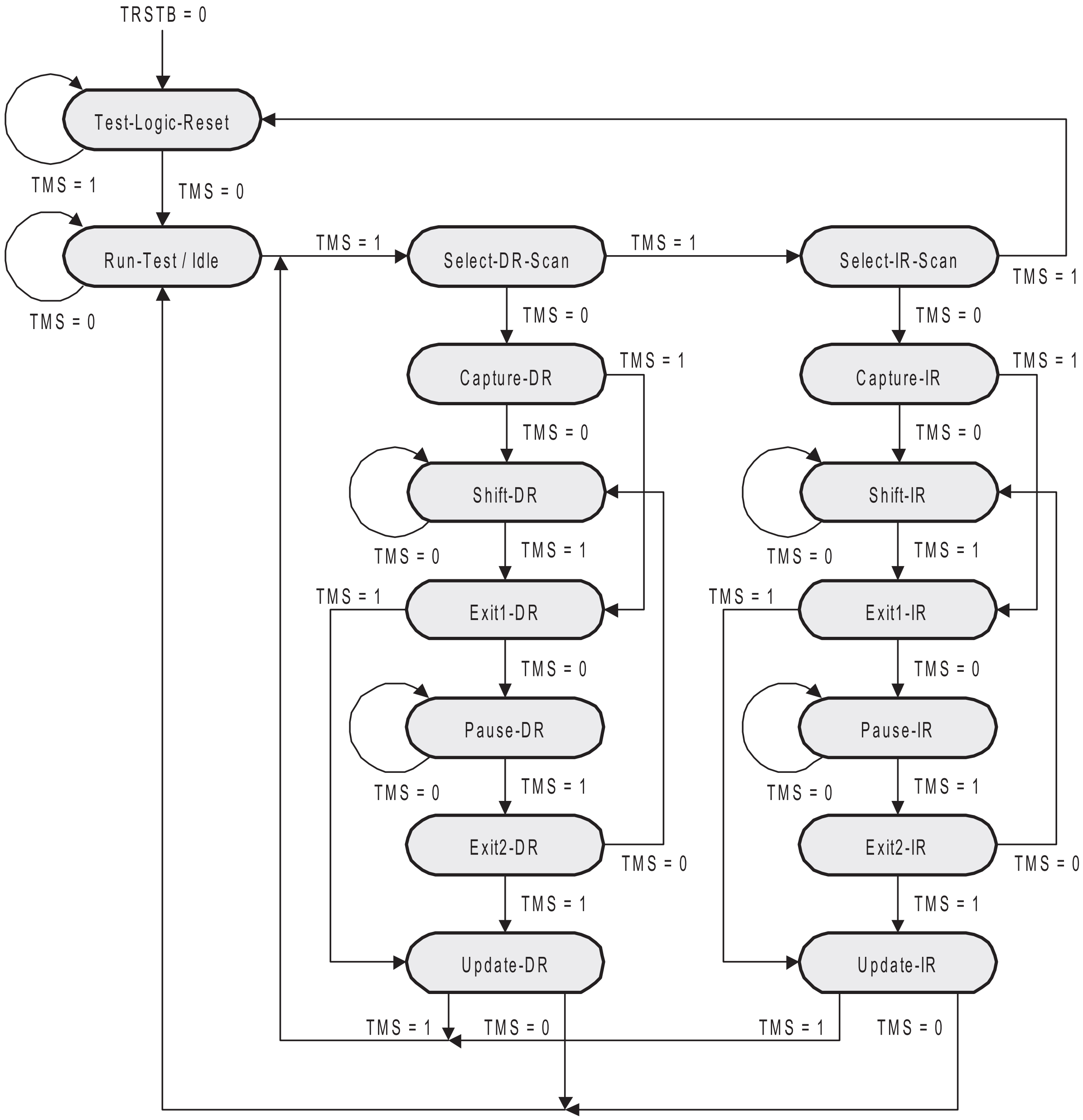
Boundary scan and internal scan testing is supported through the JTAG standard TAP and associated circuitry. This circuitry consists of a TAP controller, an instruction register with decoder, and four data registers, including a device ID register, a boundary scan register, a bypass register and the internal scan chain register. In general, these data registers consist of two parts: a serial shift register and a parallel output (or shadow) register. The parallel output registers maintain their values during shift operations and are loaded with new values from the shift register during an update state. The following figure shows the architecture of the boundary scan test circuitry.

Figure 57. JTAG TAP Boundary Scan Test Architecture



The TAP controller is a synchronous state machine that captures and shifts test data through the test registers. State transitions occur on the rising edge of TCK and are controlled by the TMS signal as illustrated in the following figure.

Figure 58. TAP Controller State Diagram



The following table describes the TAP Controller states.

Table 45. TAP Controller States

TAP Controller State	Description
Test-Logic-Reset	Activating TRSTB forces the TAP Controller to asynchronously enter the Test-Logic-Reset state. This state is also entered synchronously within five TCK cycles if TMS is held high. In Test-Logic-Reset state all of the associated test logic is reset and disabled, allowing the device to operate normally. The Instruction register is loaded with the IDCODE instruction while the data registers are reset to logic 0.
Run-Test/Idle	Run-Test/Idle state is an idle state in which the test logic is disabled and the device operates normally. It is different than the Test-Logic-Reset state in that the current state of the test logic is maintained.
Select-DR-Scan, Select-IR-Scan	These states are single TCK states that allow the selection of data register scan operations or Instruction register scan operations.
Capture-DR	Capture-DR state causes the selected serial data register to be loaded in parallel with a data value determined by the current instruction. The data is loaded on the rising edge of TCK as the TAP Controller transitions to the next state.
Shift-DR	Shift-DR state causes the selected data register to shift one bit in the direction going from TDI (MSB) towards TDO (LSB). Repeated single-bit shifts are performed on each rising TCK edge that TMS is held low.
Exit1-DR, Exit2-DR	These states are single TCK states at the end of a data register shift that allow a return to the Shift-DR state without going through the Capture-DR state, or allow the state machine to exit the data register shifting process back to the idle condition. TDO transitions to the high-impedance state on the first falling edge of TCK after the Exit1-DR state is entered.
Pause-DR	Pause-DR state allows the data register shifting process to be suspended without change or loss of the data register contents.
Update-DR	Update-DR state causes the parallel output (shadow) register part of the selected data register to be updated to match the value currently stored in the serial data register part. This update occurs on the first falling edge of TCK after the Update-DR state is entered. (Currently only the boundary scan register has parallel output registers.)
Capture-IR	Capture-IR state causes the Instruction register serial part to be loaded in parallel with status information. The status is loaded on the rising edge of TCK as the TAP Controller transitions to the next state. (Currently the status information is simply the IDCODE instruction.)
Shift-IR	Shift-IR state causes the Instruction register to shift one bit in the direction going from TDI (MSB) towards TDO (LSB). Repeated single-bit shifts are performed on each rising TCK edge that TMS is held low.
Exit1-IR, Exit2-IR	These states are single TCK states at the end of an Instruction register shift that allow a return to the Shift-IR state without going through the Capture-IR state, or allow the state machine to exit the Instruction register shifting process back to the idle condition. TDO transitions to the high-impedance state on the first falling edge of TCK after the Exit1-IR state is entered.
Pause-IR	Pause-IR state allows the Instruction register shifting process to be suspended without change or loss of the Instruction register contents.

Table 45. TAP Controller States *(continued)*

TAP Controller State	Description
Update-IR	Update-IR state causes the instruction currently loaded into the serial shift register part of the Instruction register to be loaded into the parallel output (shadow) register part of the Instruction register. This causes the instruction to become active. This activation of the instruction occurs on the first falling edge of TCK after the Update-IR state is entered.

3.11.1 Instruction Register

The four-bit Instruction register and associated decode circuitry determine the operation performed by the scan test logic, and which data register is selected in the scan path for the operation. In the Test-Logic-Reset state, the Instruction register is initialized to the IDCODE instruction. The Instruction register is then loaded with status information during the Capture-IR state, in which the two least-significant bits must be 01 for scan-path testing purposes (currently the status information is the IDCODE instruction). Serially-loaded instructions become active at the Update-IR state.

The following table lists supported test instructions, including the data register selected for each test, plus the device-operating mode during the selected test. When the device is in Test mode, the output pins are affected by the test operation. In Normal mode, device inputs, outputs and internal logic are unaffected by the test operation.

Table 46. Supported Boundary Scan Test Instructions

Instruction Code	Instruction	Selected Data Register	Device Operating Mode
0000	EXTEST	Boundary Scan	Test
0001	IDCODE	Device ID	Normal
0010	SAMPLE/PRELOAD	Boundary Scan	Normal
1111	BYPASS	Bypass	Normal
All Others	Invalid	Unknown	Unknown

The following table provides a description of each supported test instruction.

Table 47. Boundary Scan Test Instruction Descriptions

Instruction	Description
EXTEST	The EXTEST instruction enables board-level interconnect testing and device I/O level testing by allowing device inputs to be observed and controlled. The device inputs are captured during the Capture-DR state and subsequently shifted out on TDO with the Shift-DR state. Device outputs can be set by providing the desired values on TDI during the Shift-DR state, and then driving the outputs with the loaded values at the Update-DR state.
IDCODE	The IDCODE instruction enables the Device ID register to be read by serially-shifting bit values out on TDO with the Shift-DR state. This instruction is automatically loaded by entering the Test-Logic-Reset state in addition to the normal serial instruction loading mechanism.

Table 47. Boundary Scan Test Instruction Descriptions *(continued)*

Instruction	Description
SAMPLE/ PRELOAD	The SAMPLE/PRELOAD instruction enables observation of device inputs and internal output signals while the normal operation. The signal values are loaded into the boundary scan register during the Capture-DR state and observed by shifting the values out with the Shift-DR state. The pre-load aspect of this instruction occurs at the Update-DR state, when values in the serial part of the boundary scan register are loaded into the parallel output (shadow) part. This allows the boundary scan register to be pre-loaded for subsequent test operations such as EXTTEST or CLAMP.
BYPASS	The BYPASS instruction allows serial data on TDI to be transferred to TDO with only one TCK delay. This facilitates board-level testing by allowing the serial test data to quickly pass on to the next device. The bypass register is loaded with a logic 0 during the Capture-DR state.

3.11.2 Device ID Register

The 32-bit device ID register is used to identify the manufacturer, part number, and version of the device through the JTAG test access port. When the IDCODE instruction is loaded, this identification data is loaded into the Device ID shift register during the Capture-DR state, and can be shifted out on TDO through the use of the Shift-DR state. The following table includes a description of the device identification information.

Note The version number depicted does not necessarily reflect the latest revision of the VSC8486 device.

Table 48. Device Identification Information

Type	Version Number	Part Number	Manufacturer ID	Fixed
Register bits	[31...28]	[27...12]	[11...1]	0
Hex value	0x2	0x8486	0x074	2

3.11.3 Bypass Register

The single-bit Bypass register enables system serial test data to bypass the device with only one TCK cycle delay. This register is used in the scan path during the BYPASS instruction. This register is set to logic 0 during the Capture-DR state.

3.11.4 Boundary Scan Register

The 127-bit Boundary Scan register (BSR) provides the means to force values on the device outputs and to capture values on the device inputs (and internal output signals). The direction of shift is from TDI (MSB), through bits 1-127, to TDO (LSB). The BSR bits and their associated device signals are summarized in the following table. A full Boundary Scan Description Language (BSDL) file is available upon request.

Table 49. Boundary Scan Register Bits

				(continued)	
BSR Bit	**Device Signal**	**BSR Cell Type**	**BSR Bit**	**Device Signal**	**BSR Cell Type**
0	RXALARM	OUT	63	XRX3	IN
1	TXALARM	OUT	64	XRX2	IN
2	LASI	OUT	65	XRX1	IN
3	REFSEL1	IN	66	XRX0	IN
4	REFSEL0	IN	67	IOMODESEL	IN
5	SPLITLOOPN	IN	68	TFPOUT	OUT
6	TXD[0]	IN	69	MSTCODE[0]	IN
7	TXD[1]	IN	70	EPCS	IN
8	TXD[2]	IN	71	MSTCODE[1]	IN
9	TXD[3]	IN	72	AUTONEG	IN
10	TXD[4]	IN	73	STWWP	IN
11	TXD[5]	IN	74	MSTCODE[2]	IN
12	TXD[6]	IN	75	PRTAD[0]	IN
13	TXD[7]	IN	76	PRTAD[1]	IN
14	TXC[0]	IN	77	PRTAD[2]	IN
15	TXD[8]	IN	78	PRTAD[3]	IN
16	TXD[9]	IN	79	PRTAD[4]	IN
17	TXD[10]	IN	80	MDIO	IN
18	TXD[11]	IN	81	MDIO	OUT
19	TXC[1]	IN	82	RXC[3]	OUT
20	TXD[13]	IN	83	RXD[31]	OUT
21	TXD[14]	IN	84	RXD[30]	OUT
22	TXD[15]	IN	85	RXD[29]	OUT
23	TXD[12]	IN	86	RXD[28]	OUT
24	TXCLK	IN	87	RXD[27]	OUT
25	TXD[16]	IN	88	RXD[26]	OUT
26	TXD[17]	IN	89	RXD[25]	OUT
27	TXD[18]	IN	90	RXD[24]	OUT
28	TXD[19]	IN	91	RXC[2]	OUT
29	TXD[20]	IN	92	RXD[23]	OUT
30	TXD[21]	IN	93	RXD[22]	OUT
31	TXD[22]	IN	94	RXD[21]	OUT
32	TXC[2]	IN	95	RXD[20]	OUT
33	TXD[23]	IN	96	RXD[19]	OUT
34	TXD[24]	IN	97	RXD[18]	OUT
35	TXD[25]	IN	98	RXD[17]	OUT
36	TXD[26]	IN	99	RXD[16]	OUT
37	TXD[27]	IN	100	RXCLK	OUT

Table 49. Boundary Scan Register Bits *(continued)*

				(continued)	
BSR Bit	**Device Signal**	**BSR Cell Type**	**BSR Bit**	**Device Signal**	**BSR Cell Type**
38	TXD[28]	IN	101	RXD[13]	OUT
39	TXD[29]	IN	102	RXD[15]	OUT
40	TXD[30]	IN	103	RXD[14]	OUT
41	TXD[31]	IN	104	RXC[1]	OUT
42	TXC[3]	IN	105	RXD[12]	OUT
43	PMTICK	IN	106	RXD[11]	OUT
44	TXONOFFI	IN	107	RXD[10]	OUT
45	WIS_INTA	OUT	108	RXD[9]	OUT
46	LP_16B	IN	109	RXD[6]	OUT
47	LP_XGMII	IN	110	RXC[0]	OUT
48	FORCE_AIS	IN	111	RXD[7]	OUT
49	WANMODE	IN	112	RXD[8]	OUT
50	LPP_10B	IN	113	RXD[5]	OUT
51	RFPOUT	OUT	114	RXD[4]	OUT
52	LP_XAUI	IN	115	RXD[3]	OUT
53	CLK64A_EN	IN	116	RXD[2]	OUT
54	LOPC	IN	117	RXD[1]	OUT
55	RCLKOUT	OUT	118	RXD[0]	OUT
56	RDAOUT	OUT	119	MDC	IN
57	TCLKOUT	OUT	120	STWSCL	IN
58	TDAIN	IN	121	STWSCL	OUT
59	XTX0	OUT	122	STWSDA	IN
60	XTX1	OUT	123	STWSDA	OUT
61	XTX2	OUT	124	WIS_INTB	OUT
62	XTX3	OUT	125	RESETN	IN
			126	RXINOFFN	IN

4 Registers

This section describes the registers for the VSC8486 device. The registers marked reserved and factory test should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- RW: Read and Write
- RWSC: Read Write Self Clearing

The registers are organized into the following sections:

- "Device 1: PMA Registers," page 124
- "Device 2: WIS Registers," page 142
- "Device 3: PCS Registers," page 177
- "Device 4: PHY-XS Registers," page 192
- "Device 30 (0x1E): NVR and DOM Registers," page 205

4.1 Device 1: PMA Registers

The following tables provide settings for the registers related to the PMA.

Table 50. PMA_CTRL1: PMA Control 1 (1x0000)

Bit	Name	Access	Description	Default
15	SOFT_RST	RWSC	Reset all MMDs. 0: Normal operation. 1: Reset.	0
14	RESERVED	RO	Reserved (value always 0, writes ignored).	0
13	SPEED_SEL_A	RO	Indicates whether the device operates at 10 Gbps and above. 0: Unspecified. 1: Operates at 10 Gbps and above.	1
12	RESERVED	RO	Reserved (value always 0, writes ignored).	0

Table 50. PMA_CTRL1: PMA Control 1 (1x0000) *(continued)*

Bit	Name	Access	Description	Default
11	LOW_PWR	RW	PMA low power mode control. 0: Normal. 1: Low Power Mode. TXEN is cleared low and everything except MDIO, SPI, and reference clock receiver is disabled.	0
10:7	RESERVED	RO	Reserved (value always 0, writes ignored).	All zeros
6	SPEED_SEL_B	RO	Indicates whether the device operates at 10 Gbps and above. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
5:2	SPEED_SEL_C	RO	Speed selection. 1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps.	All zeros
1	RESERVED	RO	Reserved (value always 0, writes ignored).	0
0	LPBK_J_PMA	RW	PMA/WIS system loopback (J). 0: Disable. 1: Enable. All zeros output on XFI.	0

Table 51. PMA_STAT1: PMA Status 1 (1x0001)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved (ignore when read).	All zeros
7	FAULT	RO	Indicates a fault condition on either the transmit or receive paths. 0: Fault condition not detected. PMA receive local fault (1x0008.10) = 0 AND PMA transmit local fault (1x0008.11) = 0. 1: Fault condition detected. PMA receive local fault (1x0008.10) = 1 OR PMA transmit local fault (1x0008.11) = 1.	0
6:3	RESERVED	RO	Reserved (ignore when read).	All zeros
2	LNK_STAT	RO/LL	Receive link status. 0: PMA receive link down. (RXLOS = 1 AND SUPPRESS_RXLOS = 0) OR (RXLOCK = 0 AND SUPPRESS_RXLOL = 0). 1: PMA receive link up. (RXLOS = 0 OR SUPPRESS_RXLOS = 1) AND (RXLOCK = 1 OR SUPPRESS_RXLOL = 1).	1
1	LOW_PWR_ABILITY	RO	Indicates that MMD supports low power mode. 0: PMA does not support low power mode. 1: PMA supports low power mode.	1
0	RESERVED	RO	Reserved (ignore when read).	0

Table 52. PMA_DEVID1: PMA Device Identifier 1 (1x0002)

Bit	Name	Access	Description	Default
15:0	DEV_ID_MSW	RO	Upper 16 bits of a 32-bit unique PMA device identifier. Bits 3-18 of the device manufacturer's OUI.	0x0007

Table 53. PMA_DEVID2: PMA Device Identifier 2 (1x0003)

Bit	Name	Access	Description	Default
15:0	DEV_ID_LSW	RO	Lower 16 bits of a 32-bit unique PMA device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0x0400

Table 54. PMA_SPEED: PMA Speed Capability (1x0004)

Bit	Name	Access	Description	Default
15:1	RESERVED	RO	Reserved for future speeds (value always 0, writes ignored)	All zeros
0	RATE_ABILITY	RO	PMA rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	1

Table 55. PMA_DEVPKG1: PMA Devices in Package 1 (1x0005)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved (ignore when read)	All zeros
5	DTE_XS_PRES	RO	Indicates whether DTE XS is present in the package 0: Not present 1: Present	0
4	PHY_XS_PRES	RO	Indicates whether PHY XS is present in the package 0: Not present 1: Present	1
3	PCS_PRES	RO	Indicates whether PCS is present in the package 0: Not present 1: Present	1
2	WIS_PRES	RO	Indicates whether WIS is present in the package 0: Not present 1: Present	1
1	PMD_PMA_PRES	RO	Indicates whether PMA is present in the package 0: Not present 1: Present	1

Table 55. PMA_DEVPKG1: PMA Devices in Package 1 (1x0005) *(continued)*

Bit	Name	Access	Description	Default
0	CLS22_PRES	RO	Indicates whether Clause 22 registers are present in the package 0: Not present 1: Present	0

Table 56. PMA_DEVPKG2: PMA Devices in Package 2 (1x0006)

Bit	Name	Access	Description	Default
15	VS2_PRES	RO	Vendor specific device 2 present 0: Not present 1: Present	0
14	VS1_PRES	RO	Vendor specific device 1 present 0: Not present 1: Present	0
13:0	RESERVED	RO	Reserved (ignore when read)	All zeros

Table 57. PMA_CTRL2: PMA Control 2 (1x0007)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
2:0	PMA_MODE	RO	Indicates the PMA type selected 111: 10GBASE-SR 110: 10GBASE-LR 101: 10GBASE-ER 100: 10GBASE-LX-4 011: 10GBASE-SW 010: 10GBASE-LW 001: 10GBASE-EW 000: Reserved	111

Table 58. PMA_STAT2: PMA Status 2 (1x0008)

Bit	Name	Access	Description	Default
15:14	DEV_PRES	RO	Reflects the presence of a MMD responding at this address. 00: No device responding at this address. 01: No device responding at this address. 10: Device responding at this address. 11: No device responding at this address.	10
13	FAULT_TX_ABILITY	RO	Indicates a fault condition on the transmit path. 0: PMA does not have the ability to detect a fault condition on the transmit path. 1: PMA has the ability to detect a fault condition on the transmit path.	1

Table 58. PMA_STAT2: PMA Status 2 (1x0008) *(continued)*

Bit	Name	Access	Description	Default
12	FAULT_RX_ABILITY	RO	Indicates a fault condition on the receive path. 0: PMA does not have the ability to detect a fault condition on the receive path. 1: PMA has the ability to detect a fault condition on the receive path.	1
11	FAULT_TX	RO/LH	Indicates a fault condition on the transmit path. 0: No faults asserted. TXFAULT = 0 AND TXLOCK = 1. 1: Fault(s) asserted. TXFAULT = 1 OR TXLOCK = 0. Linked to 1Ex9004.4. A read to either 1x0008.11 or 1Ex9004.4 clears both bits if the fault condition no longer exists.	0
10	FAULT_RX	RO/LH	Indicates a fault condition on the receive path. 0: No faults asserted. (RXLOS = 0 OR SUPPRESS_RXLOS = 1) AND (RXLOCK = 1 OR SUPPRESS_RXLOL = 1). 1: Fault(s) asserted. (RXLOS = 1 AND SUPPRESS_RXLOS = 0) OR (RXLOCK = 0 AND SUPPRESS_RXLOL = 0). Linked to 1Ex9003.4. A read to either 1x0008.10 or 1Ex9003.4 clears both bits if the fault condition no longer exists.	0
9	RESERVED	RO	Reserved (ignore when read).	0
8	TXDIS_ABILITY	RO	Device capability to disable the transmit path. 0: Not capable. 1: Capable.	1
7	BASE_SR_ABILITY	RO	Device capability to support 10GBASE-SR. 0: Not capable. 1: Capable.	1
6	BASE_LR_ABILITY	RO	Device capability to support 10GBASE-LR. 0: Not capable. 1: Capable.	1
5	BASE_ER_ABILITY	RO	Device capability to support 10GBASE-ER. 0: Not capable. 1: Capable.	1
4	BASE_LX4_ABILITY	RO	Device capability to support 10GBASE-LX4. 0: Not capable. 1: Capable.	0
3	BASE_SW_ABILITY	RO	Device capability to support 10GBASE-SW. 0: Not capable. 1: Capable. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0
2	BASE_LW_ABILITY	RO	Device capability to support 10GBASE-LW. 0: Not capable. 1: Capable **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0

Table 58. PMA_STAT2: PMA Status 2 (1x0008) *(continued)*

Bit	Name	Access	Description	Default
1	BASE_EW_ABILITY	RO	Device capability to support 10GBASE-EW. 0: Not capable. 1: Capable. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0
0	PMA_LPBK_ABILITY	RO	Device capability to support a PMA loopback. 0: Not capable. 1: Capable.	1

Table 59. PMA_CTRL3: PMA Control 3 (1x0009)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved (value always 0, writes ignored).	All zeros
4:1	RESERVED	RO	Reserved (value always 0, writes ignored).	All zeros
0	TX_DIS	RW	Disable PMA transmit driver. This mode is also entered upon a low power mode, driving of the external pin, or a software override and force of the external pin signal. 0: Enable. 1: Disable.	0

Table 60. PMA_STAT3: PMA Status 3 (1x000A)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved (value always 0, writes ignored).	All zeros
4:1	RESERVED	RO	Reserved (value always 0, writes ignored).	All zeros
0	RX_SD	RO	Receive signal detected. 0: Signal not detected. (RXLOS = 1 AND SUPPRESS_RXLOS = 0). 1: Signal detected. (RXLOS = 0 OR SUPPRESS_RXLOS = 1).	0

Table 61. Factory Test Register (1x000B-000D)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 62. PMA_PKGID1: PMA Package Identifier 1 (1x000E)

Bit	Name	Access	Description	Default
15:0	PKG_ID_MSW	RO	Upper 16 bits of a 32-bit unique PMA package identifier. Bits 3-18 of the device manufacturer's OUI.	All zeros

Table 63. PMA_PKGID2: PMA Package Identifier 2 (1x000F)

Bit	Name	Access	Description	Default
15:0	PKG_ID_LSW	RO	Lower 16 bits of a 32-bit unique PMA package identifier. Bits 19-24 of the device manufacturer’s OUI. Six-bit model number, and a four-bit revision number.	All zeros

Table 64. PMA_CFG1: PMA Configuration 1 (1x8000)

Bit	Name	Access	Description	Default
15:14	CRU_LOOP_BANDWIDTH [1:0]	RW	CRU loop bandwidth adjustment 00: 3x 01: 4x 10: 5x (default) 11: 6x	10
13	RESERVED	RW	Factory test only (do not modify this bit group)	1
12	RESERVED	RO	Factory test only (do not modify this bit group)	1
11	RESERVED	RO	Factory test only (do not modify this bit group)	0
10	TX_FIFORSTN	RWSC	Reset transmit PMA FIFO 0: Reset FIFO 1: Normal Operation	1
9	TX_FIFORSTN_MODE	RW	Disable automatic transmit PMA FIFO reset upon an overflow/underflow condition. If in manual mode, use bit 10 to perform the manual reset. 0: Automatic 1: Manual	0
8	LPBKN_K	RW	Disable PMA serial loopback (loopback K) 0: Enable 1: Disable	1
7	TX_DATAINVN	RW	Select polarity of the transmit XFI/SFI data 0: Invert Tx data polarity 1: Normal operation	1
6	TX_MSBSEL	RW	Select the transmission bit order 0: MSB transmitted first with bit 63 being the MSB 1: LSB transmitted first with bit 0 being the MSB (IEEE style)	1
5	RESERVED	RW	Factory test only (do not modify this bit group)	0
4	RESERVED	RW	Factory test only (do not modify this bit group)	1
3	RX_LOSDATASQN	RW	Select data squelch mode (See Lock to Reference Table within the text) 0: Automatic data squelch mode 1: Manual data squelch mode	1
2	RX_LCKREFN	RW	Select Lock to Reference (See Lock to Reference Table within the text) 0: Lock to Refclk (squelch data) 1: Normal operation	1
1	RX_DATAINVN	RW	Select polarity of the receive XFI/SFI data 0: Invert Rx data polarity 1: Normal operation	1

Table 64. PMA_CFG1: PMA Configuration 1 (1x8000) *(continued)*

Bit	Name	Access	Description	Default
0	RX_MSBSELN	RW	Select the receive bit order 0: MSB received first with bit 63 being the MSB 1: LSB received first with bit 0 being the MSB (IEEE style)	1

Table 65. Factory Test Register (1x8001)

Bit	Name	Access	Description	Default
15:1	RESERVED	RO	Reserved (ignore when read)	All zeros
0	RESERVED	RO	Factory test only (do not modify this bit group)	1

Table 66. PMA_RXEQ_CTRL: PMA Rx Equalization Control (1x8002)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Factory test only (do not modify this bit group)	1
14:11	RX_EQ_CTRL	RW	Amount of receive signal equalization	1111
10:0	RESERVED	RO	Factory test only (do not modify this bit group)	10101010 101

Table 67. PMA_STAT4: PMA Status 4 (1xE600)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved (ignore when read)	All zeros
3	RESERVED	RO	Factory test only (do not modify this bit group)	1
2	TXLOCKERRN	RO	Transmit clock multiplier lock error status 0: Lock error 1: Normal operation	1
1	RXLOCKERRN	RO	Receive clock recovery lock error status 0: Lock error 1: Normal operation	1
0	RXLOSN	RO	Receiver loss of signal status 0: Loss of signal 1: Normal operation	1

Table 68. PMA_CTRL4: PMA Control 4 (1xE601)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Factory test only (do not modify this bit group)	10101010

Table 68. PMA_CTRL4: PMA Control 4 (1xE601) *(continued)*

Bit	Name	Access	Description	Default
7:4	TX_EMPH_SEL	RW	Amount of PMA transmit pre-emphasis Type 1 0000: 1.8 dB (default) 0100: 2.7 dB 1000: 3.3 dB 1111: 3.9 dB Type 2 0000: 3.8 dB 0100: 4.8 dB 1000: 6.2 dB 1111: 6.4 dB	All zeros
3:0	TX_SLEW_SEL	RW	Amount of PMA transmit slew rate 0000: Type 1 1111: Type 2 all others: Reserved	All zeros

Table 69. PMA_CTRL5: PMA Control 5 (1xE602)

Bit	Name	Access	Description	Default
15	TX_SQUELCH	RW	Enable transmit data squelch. Force all zeros out the serial interface 0: Disable 1: Enable	0
14	RX_SQUELCH	RW	Enable received data squelch. Forces all zeros into the core. 0: Disable 1: Enable	0
13	RESERVED	RW	Factory test only (do not modify this bit group)	0
12	TXEN_INV	RW	Inverts the logic state of the TXEN pin and the txen status bit (1xE607.12) 0: The TXEN pin and status bit are 0 when the PMA transmit driver is disabled 1: The TXEN pin and status bit are 1 when the PMA transmit driver is disabled	0
11	RESERVED	RW	Factory test only (do not modify this bit group)	0
10	FULLSWG_EXVCO	RW	Enable high swing on EXVCOPU/PD output signals 0: Low swing 1: High swing	0
9	CLK64A_ENA	RW	Enable the CLK64A output signal. This signal is used when CLK64A_SRC is asserted. 0: Disable 1: Enable	0
8:7	CLK64A_SEL	RW	Select which internal clock signal to output on CLK64A 00: CMU divided by 64 01: CMU divided by 66 10: CRU divided by 64 11: REFCK	All zeros
6	CLK64A_SRC	RW	Select the source of the CLK64_EN signal 0: Enable CLK64A via CLK64_EN pin 1: Enable CLK64A via CLK64A_ENA (1xE602.9)	0

Table 69. PMA_CTRL5: PMA Control 5 (1xE602) *(continued)*

Bit	Name	Access	Description	Default
5	CLK64B_ENA	RW	Enable the CLK64B output 0: Disable 1: Enable	0
4:3	CLK64B_SEL	RW	Select which internal clock signal to output on CLK64B 00: CRU divided by 64 01: CMU divided by 66 10: CMU divided by 64 11: Factory test	All zeros
2	RESERVED	RW	Factory test only (do not modify this bit group)	0
1	RESERVED	RO	Reserved (value always 0, writes ignored)	0
0	RESERVED	RO	Reserved (value always 0, writes ignored)	0

Table 70. Factory Test Register (1xE603)

Bit	Name	Access	Description	Default
15:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 71. Factory Test Register (1xE604)

Bit	Name	Access	Description	Default
15:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 72. DEV_CTRL3: DEVICE Control 3 (1xE605)

Bit	Name	Access	Description	Default
15	WIS_INTB_POL	RW	Active level (polarity) used for the output pin, WIS_INTB 0: Active low 1: Active high	0
14	WIS_INTA_POL	RW	Active level (polarity) used for the output pin, WIS_INTA 0: Active low 1: Active high	0
13	AUTONEG_OVR	RW	Enable overriding the input pin value and instead use the force bit setting 0: Use the AUTONEG input pin state 1: Override enable	0
12	AUTONEG_FRC	RW	Value to be used if the override bit is enabled 0: If AUTONEG_OVR = 1, AUTONEG = 0 1: If AUTONEG_OVR = 1, AUTONEG = 1	0
11	EPCS_OVR	RW	Enable overriding the input pin value and instead use the force bit setting 0: Use the EPCS input pin state 1: Override enable	0

Table 72. DEV_CTRL3: DEVICE Control 3 (1xE605) *(continued)*

Bit	Name	Access	Description	Default
10	EPCS_FRC	RW	Value to be used if the override bit is enabled 0: If EPCS_OVR = 1, EPCS = 0 1: If EPCS_OVR = 1, EPCS = 1	0
9	TXONOFF_OVR	RW	Enable overriding the input pin value and instead use the force bit setting 0: Use the TXONOFF input pin state 1: Override enable	0
8	TXONOFF_FRC	RW	Value to be used if the override bit is enabled 0: If TXONOFF_OVR = 1, TXONOFF = 0 1: If TXONOFF_OVR = 1, TXONOFF = 1	0
7	REFSEL0_OVR	RW	Enable overriding the input pin value and instead use the force bit setting 0: Use the REFSEL0 input pin state 1: Override enable	0
6	REFSEL0_FRC	RW	Value to be used if the override bit is enabled 0: If REFSEL0_OVR = 1, REFSEL0 = 0 1: If REFSEL0_OVR = 1, REFSEL0 = 1	0
5	RESERVED	RO	Reserved (ignored when read)	0
4	LINETIME_FRC	RW	Force the device into linetime mode 0: Normal operation 1: Linetime enable	0
3	WAN_OVR	RW	Enable overriding the input pin value and instead use the force bit setting 0: Use the WAN input pin state 1: Override enable	0
2	WAN_FRC	RW	Value to be used if the override bit is enabled 0: If WAN_OVR = 1, WAN is disabled regardless of any other control setting 1: If WAN_OVR = 1, WAN is enabled regardless of any other control setting	0
1	SUPPRESS_RXLOL	RW	Disable receive LOL status from propagating into the fault logic 0: Receive LOL signal is used for fault logic 1: Receive LOL signal is ignored by fault logic	0
0	SUPPRESS_RXLOS	RW	Disable receive LOS status from propagating into the fault logic 0: Receive LOS signal is used for fault logic 1: Receive LOS signal is ignored by fault logic	0

Table 73. DEV_STAT1: DEVICE Status 1 (1xE606)

Bit	Name	Access	Description	Default
15	WAN_STAT	RO	Status of WAN mode 0: Disabled 1: Enabled	0
14	WAN_MODE_PSTAT	RO	Input level received on the WAN_MODE pin 0: Low 1: High	0

Table 73. DEV_STAT1: DEVICE Status 1 (1xE606) *(continued)*

Bit	Name	Access	Description	Default
13	LINETIME_STAT	RO	Current state of the linetime signal 0: Low 1: High	0
12	REFSEL0_PSTAT	RO	Input level received on the REFSEL0 pin 0: Low 1: High	0
11	LPP_10B_PSTAT	RO	Input level received on the LPP_10B pin 0: Low 1: High	0
10	LP_XAUI_PSTAT	RO	Input level received on the LP_XAUI pin 0: Low 1: High	0
9	SPLITLOOPN_PSTAT	RO	Input level received on the SPLITLOOPN pin 0: Low 1: High	0
8	LP_XGMII_PSTAT	RO	Input level received on the LP_XGMII pin 0: Low 1: High	0
7	LP_16B_PSTAT	RO	Input level received on the LP_16B pin 0: Low 1: High	0
6	IOMODESEL_PSTAT	RO	Input level received on the IOMODESEL pin 0: Low 1: High	0
5	AUTONEG_PSTAT	RO	Input level received on the AUTONEG pin 0: Low 1: High	0
4	EPCS_PSTAT	RO	Input level received on the EPCS pin 0: Low 1: High	0
3	TXONOFF_PSTAT	RO	Input level received on the TXONOFF pin 0: Low 1: High	0
2	LASI_FORCEN_PIN_STAT	RO	Input level received on the LASI_FORCEN pin 0: Low 1: High	0
1	LASI_PSTAT	RO	Output level sent on the LASI pin 0: Low 1: High	0
0	RESERVED	RO	Factory test only (do not modify this bit group)	0

Table 74. DEV_STAT2: DEVICE Status 2 (1xE607)

Bit	Name	Access	Description	Default
15:13	MST_CODE_PSTAT	RO	Received signal levels of the MST_CODE[2:0] input pins.	All zeros

Table 74. DEV_STAT2: DEVICE Status 2 (1xE607) *(continued)*

Bit	Name	Access	Description	Default
12	TXEN_STAT	RO	Indicates PMA transmit output driver enabled. The output driver is disabled when the Global PMD transmit disable bit is set (1x0009.0) and when the part is in low power mode. The logic state of this bit and the TXEN pin depends upon TXEN_INV (1xE602.12). 0: When TXEN_INV = 0, the PMA transmit output driver is disabled. When TXEN_INV = 1, the PMA transmit output driver is enabled. 1: When TXEN_INV = 0, the PMA transmit output driver is enabled. When TXEN_INV = 1, the PMA transmit output driver is disabled.	0
11	TESTEN_PSTAT	RO	Input level received on the TESTEN pin. 0: Low. 1: High.	0
10	RESERVED	RO	Factory test only (do not modify this bit group).	0
9	TX_FAULT_PSTAT	RO	Input level received on the TXFAULT pin. 0: Low. 1: High.	0
8	RESERVED	RO	Factory test only (do not modify this bit group).	0
7	SCAN_EN_PSTAT	RO	Factory test only (do not modify this bit group).	0
6	EPCS_PSTAT	RO	Input level received on the EPCS pin. 0: Low. 1: High.	0
5	AUTONEG_PSTAT	RO	Input level received on the AUTONEG pin. 0: Low. 1: High.	0
4	FORCEAIS_PSTAT	RO	Input level received on the FORCEAIS pin. 0: Low. 1: High.	0
3	WIS_INTA_PSTAT	RO	Output level sent on the WIS_INTA pin. 0: Low. 1: High.	0
2	WIS_INTB_PSTAT	RO	Output level sent on the WIS_INTB pin. 0: Low. 1: High.	0
1	PMTICK_PSTAT	RO	Input level received on the TESTEN pin. 0: Low. 1: High.	0
0	LOPC_PSTAT	RO	Input level received on the LOPC pin. 0: Low. 1: High.	0

Table 75. PMA_LOS_ASSERT: PMA Loss of Signal Assert Control (1xE700)

Bit	Name	Access	Description	Default
15:10	RESERVED	RO	Reserved.	All zeros
9	RESERVED	RW	Factory test only (do not modify this bit group).	0
8	RESERVED	RW	Factory test only (do not modify this bit group).	0

Table 75. PMA_LOS_ASSERT: PMA Loss of Signal Assert Control (1xE700)

Bit	Name	Access	Description	Default
7	RESERVED	RW	Factory test only (do not modify this bit group).	0
6	LOS_MODE_SEL	RW	Select which style of LOS monitoring to use. 0: Monitor LOS at the input. 1: Monitor LSO after signal cleanup. Must be 0 for correct sensitivity performance in the VSC8486.	0
5:0	LOS_ASSERT_DAC	RW	Set the LOS assert voltage threshold. Asserted values should be higher than de-asserted values set by register 1xE701. 000000: Less than 40 mV. 111111: Greater than 110 mV. All else: Reserved.	All zeros

Table 76. PMA_LOS_DEASSERT: PMA Loss of Signal De-assert Control (1xE701)

Bit	Name	Access	Description	Default
15	LOS_PWR_DWN	RW	Enable power down of the LOS circuitry. 0: LOS normal operation. 1: LOS power down.	0
14:12	LOS_WIN	RW	LOS report/clear time setting.	All zeros
11:8	VCM_ADJ	RW	Input receiver common mode voltage adjust. Observable on RXINCM (pin N3).	1000
7	RESERVED	RW	Factory test only (do not modify this bit group)	0
6	RESERVED	RW	Factory test only (do not modify this bit group)	0
5:0	LOS_DEASSERT_DAC	RW	Set the LOS de-assert voltage threshold. De-asserted values should be lower than asserted values set by register 1xE700. 000000: Less than 40 mV. 111111: Greater than 110 mV. All else: Reserved.	All zeros

Table 77. PMA_LOS_STAT: PMA Loss of Signal Status (1xE702)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved	All zeros
2	LOS_ASSERT_STAT	RO	Assert comparison (see also 1xE700.5:0) 0: Assert threshold is less than peak detector monitor 1: Assert threshold is greater than peak detector monitor	0
1	LOS_DEASSERT_STAT	RO	Deassert comparison (see also 1xE701.5:0) 0: Deassert threshold is less than peak detector monitor 1: Deassert threshold is greater than peak detector monitor	0

Table 77. PMA_LOS_STAT: PMA Loss of Signal Status (1xE702) *(continued)*

Bit	Name	Access	Description	Default
0	LOS_STAT	RO	Loss of signal status (identical to 1xE600.0) 0: Loss of signal 1: Normal operation	0

Table 78. DEV_ID: DEVICE Identifier (1xE800)

Bit	Name	Access	Description	Default
15:0	CHIP_ID	RO	Contains the identification number of the chip	0x8486

Table 79. DEV_REV: DEVICE Revision (1xE801)

Bit	Name	Access	Description	Default
15:0	CHIP_REV	RO	Contains the revision number of the chip	0x0001

Table 80. DEV_STW_CTRL: DEVICE Serial Two-Wire Interface Control (1xE900)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
3	STW_MST_ADDR_SRC	RW	Select the source of the Master Address serial two-wire interface 0: MSTCODE[2:0] pins 1: Register controlled (1xE900.2:0)	0
2:0	STW_MST_ADDR	RW	Master Address value	111

Table 81. DEV_GPIO_CTRL: DEVICE General Purpose I/O Control (1xE901)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved (value always 0, writes ignored)	0
14:13	TXALARM_SEL	RW	Select source of TXALARM output 00: Normal TXALARM 01: Tx link/activity LED 10: GPO mode 11: Reserved	All zeros
12:11	RXALARM_SEL	RW	Select source of RXALARM output 00: Normal RXALARM 01: Rx link/activity LED 10: GPO mode 11: Reserved	All zeros
10	LASI_SEL	RW	Select source of LASI output 0: Normal LASI output 1: GPO mode	0

Table 81. DEV_GPIO_CTRL: DEVICE General Purpose I/O Control (1xE901)

Bit	Name	Access	Description	Default
9	WIS_INTB_SEL	RW	Select source of WIS_INTB output 0: XFP module reset or SFP+ TXDISABLE 1: WIS interrupt B function	0
8	GPO_TXALARM	RW	Transmitted on TXALARM when in GPO mode	0
7	GPO_RXALARM	RW	Transmitted on RXALARM when in GPO mode	0
6	GPO_LASI	RW	Transmitted on LASI when in GPO mode	0
5	TX_LED_BLINK_TIME	RW	Tx data activity LED blink time 0: 50 ms interval 1: 100 ms interval	1
4	RX_LED_BLINK_TIME	RW	Rx data activity LED blink time 0: 50 ms interval 1: 100 ms interval	1
3:2	TX_LED_MODE	RW	Tx LED mode control 00: Display Tx link status in XAUI mode or Tx data activity status in XGMII mode 01: Display Tx data activity status 10: Display combo of link and data activity status in XAUI mode or data activity status in XGMII mode 11: Reserved	10
1:0	RX_LED_MODE	RW	Rx LED mode control 00: Display Rx link status 01: Display Rx data activity status 10: Display combo of link and data activity status 11: Reserved	10

Table 82. DEV_XFP_CTRL: DEVICE XFP Control (1xE902)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
2	XFP_RST_ON_LOWPWR or SFP+_Tx_DIS	RW	**XFP** Select for XFP reset on low power mode 0: No low power mode contribution to XFP reset 1: XFP reset in low power mode **SFP+** Select for Tx_DIS 0: SFP+ module functioning regardless of no low power mode 1: Disables SFP+ module in low power mode	1
1	XFP_RST_INV or SFP+_Tx_DIS_INV	RW	**XFP** Invert XFP reset state on WIS_INTB 0: Active high 1: Active low **SFP+** Invert SFP+ Tx_DIS state on WIS_INTB 0: Active high 1: Active low	0

Table 82. DEV_XFP_CTRL: DEVICE XFP Control (1xE902) *(continued)*

Bit	Name	Access	Description	Default
0	XFP_RST or SFP+_DIS	RW	**XFP** Force XFP power-down reset 0: Normal operation 1: Hold in power down reset state **SFP+** Force SFP+ transmit to be disabled 0: Normal operation 1: Hold the SFP+ transmit in disable state	0

Table 83. DEV_STAT: DEVICE Status (1xEC00)

Bit	Name	Access	Description	Default
15	HWRESET_PEND	RO-RO/LH	If set, indicates a hardware RESET is currently high or was set high between previous and current read to this register	0
14	TXONOFF_PEND	RO-RO/LH	If set, TXONOFF is currently low or was set low between previous and current read to this register	0
13	LASI_PEND	RO-RO/LH	If set, LASI is currently low or was set low between previous and current read to this register	0
12	SWRESET_PEND	RO-RO/LH	If set, software RESET is currently high or was set high between previous and current read to this register	0
11	RESET_PEND	RO-RO	If set, hardware or software RESET is currently high	0
10	MDIO_WR_PEND	RO-RO/LH	If set, a MDIO write to an interrupt-enabled register has taken place	0
9	MDIO_RI_PEND	RO-RO/LH	If set, an MDIO read increment to an interrupt-enabled register has taken place	0
8	MDIO_RD_PEND	RO-RO/LH	If set, a MDIO read to an interrupt-enabled register has taken place	0
7	MDIO_AD_PEND	RO-RO/LH	If set, an interrupt-enabled register has been addressed by MDIO	0
6	MDIO_NE_PEND	RO-RO/LH	If set, a nonexistent register address was received	0
5	MDIO_XP_PEND	RO-RO/LH	If set, a XENPAK register (8000-AFFF) address was received	0
4	MDIO_PMAVS_PEND	RO-RO/LH	If set, an upper PMA (B000-FFFF) address was received	0
3	MDIO_DEV4_PEND	RO-RO/LH	If set, a device 4 (PHY XS) address was received	0
2	MDIO_DEV3_PEND	RO-RO/LH	If set, a device 3 (PCS) address was received	0
1	MDIO_DEV2_PEND	RO-RO/LH	If set, a device 2 (WIS) address was received	0
0	MDIO_DEV1_PEND	RO-RO/LH	If set, a device 1 (PMA) address was received	0

Table 84. Factory Test (1xEC01–EC34)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros

Table 85. Factory Test (1xED00–ED0F)

Bit	Name	Access	Description	Default
15:0	TEST	RW	Factory test only (do not modify this bit group)	All zeros

Table 86. DEV_REG_MODE: DEVICE Read Only Mode (1xEF00)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
1	RESERVED	RW	Factory test only (do not modify this bit group)	0
0	RO_MODE	RW	Enable the latch state on all bits labeled RO/LH 0: RO/LH bits are read-only 1: RO/LH bits are read-only latch high	1

Table 87. DEV_RST_CTRL: DEVICE Block Reset Control (1xEF01)

Bit	Name	Access	Description	Default
15:9	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
8	RST_WIS_TX	RWSC	Reset the WIS Tx path 0: Normal operation 1: WIS Tx path reset	0
7	RST_WIS_TXFIFO	RWSC	Reset the Tx WIS FIFO 0: Normal operation 1: Tx WIS FIFO reset	0
6	RST_WIS_TXFIFOPTR	RWSC	Reset the Tx WIS FIFO pointers 0: Normal operation 1: Tx WIS FIFO pointer reset	0
5	RST_WIS_INTR	RWSC	Reset the WIS interrupt tree 0: Normal operation 1: Reset WIS interrupt tree	0
4	RST_WIS_RXFIFO	RWSC	Reset the Rx WIS FIFO 0: Normal operation 1: Rx WIS FIFO reset	0
3	RST_WIS_RX	RWSC	Reset the WIS Rx path 0: Normal operation 1: WIS Rx path reset	0
2	RST_PCS_TX	RWSC	Reset the PCS Tx path 0: Normal operation 1: PCS Tx path reset	0
1	RST_PCS_RX	RWSC	Reset the PCS Rx path 0: Normal operation 1: PCS Rx path reset	0
0	RST_XGXS_FIFO	RWSC	Reset the XGXS FIFO 0: Normal operation 1: XGXS FIFO reset	0

Table 88. DEV_XFI_CTRL2: DEVICE XFI Loopback Control 2 (1xEF10)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
2	XFI_LPBK_OVR	RW	Override the default data pattern to transmit out the XFI port while in loopback 0: Normal operation 1: Override XFI transmit data according to bits 1:0.	0
1:0	XFI_TXDATA_SEL	RW	Select the data pattern to transmit out the XFI port while in loopback 00: 0x00FF repeating pattern 01: All zeros 10: All ones 11: Tx data from WIS/PCS	All zeros

4.2 Device 2: WIS Registers

The following tables provide settings for the registers related to WIS.

Table 89. WIS_CTRL1: WIS Control 1 (2x0000)

Bit	Name	Access	Description	Default
15	SOFT_RST	RWSC	Reset all MMDs. 0: Normal operation. 1: Reset.	0
14	LPBK_J	RW	Enable WIS system loopback (loopback J). 0: Disable. 1: Enable.	0
13	SPEED_SEL_A	RO	WIS speed capability. 0: Unspecified. 1: Operates at 10 Gbps or above.	1
12	RESERVED	RO	Reserved.	0
11	LOW_PWR	RW	Enter low power mode. 0: Normal operation. 1: Low power mode. The XAUI and PMA high-speed output driver are disabled. TXEN is active to indicate low power state. Register bit TXEN_INV (1xE602.12) selects whether TXEN is active high or low.	0
10:7	RESERVED	RO	Reserved.	All zeros
6	SPEED_SEL_B	RO	WIS speed capability. 0: Unspecified. 1: Operates at 10 Gbps or above.	1
5:2	SPEED_SEL_C	RO	WIS speed selection. 1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps.	All zeros
1:0	RESERVED	RO	Reserved.	All zeros

Table 90. WIS_STAT1: WIS Status 1 (2x0001)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved.	All zeros
7	FAULT	RO/LH	WIS fault status. WIS fault is defined by LOF. 0: No faults asserted. 1: Fault(s) asserted.	0
6:3	RESERVED	RO	Reserved.	All zeros
2	LNK_STAT	RO/LL	WIS receive link status. Link up means no AIS-P, AIS-L, PLM-P, or SEF alarms. 0: Link down. 1: Link up. Link up: AIS-P = 0 AND AIS-L = 0 AND PLM-P = 0 AND WIS SEF = 0. WIS link down: AIS-P = 1 OR AIS-L = 1 OR PLM-P = 1 OR WIS SEF = 1.	1
1	LOW_PWR_ABILITY	RO	Low power mode support ability. 0: Not supported. 1: Supported.	1
0	RESERVED	RO	Reserved.	0

Table 91. WIS_DEVID1: WIS Device Identifier 1 (2x0002)

Bit	Name	Access	Description	Default
15:0	DEV_ID_MSW	RO	Upper 16 bits of a 32-bit unique WIS device identifier. Bits 3-18 of the device manufacturer’s OUI.	0x0007

Table 92. WIS_DEVID2: WIS Device Identifier 2 (2x0003)

Bit	Name	Access	Description	Default
15:0	DEV_ID_LSW	RO	Lower 16 bits of a 32-bit unique WIS device identifier. Bits 19-24 of the device manufacturer’s OUI. Six-bit model number, and a four-bit revision number.	0x0400

Table 93. WIS_SPEED: WIS Speed Capability (2x0004)

Bit	Name	Access	Description	Default
15:1	RESERVED	RO	Reserved	All zeros
0	RATE_ABILITY	RO	WIS rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	1

Table 94. WIS_DEVPKG1: WIS Devices in Package 1 (2x0005)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved	All zeros
5	DTE_XS_PRES	RO	Indicates whether DTE XS is present in the package 0: Not present 1: Present	0
4	PHY_XS_PRES	RO	Indicates whether PHY XS is present in the package (this bit depends upon the IOMODESEL pin setting) 0: Not present 1: Present	1
3	PCS_PRES	RO	Indicates whether PCS is present in the package 0: Not present 1: Present	1
2	WIS_PRES	RO	Indicates whether WIS is present in the package 0: Not present 1: Present	1
1	PMD_PMA_PRES	RO	Indicates whether PMA/PMD is present in the package 0: Not present 1: Present	1
0	CLS22_PRES	RO	Indicates whether Clause 22 registers are present in the package 0: Not present 1: Present	0

Table 95. WIS_DEVPKG2: WIS Devices in Package 2 (2x0006)

Bit	Name	Access	Description	Default
15	VS2_PRES	RO	Vendor specific device 2 present 0: Not present 1: Present	0
14	VS1_PRES	RO	Vendor specific device 1 present 0: Not present 1: Present	0
13:0	RESERVED	RO	Reserved	All zeros

Table 96. WIS_CTRL2: WIS Control 2 (2x0007)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved.	All zeros
5	TEST_PRBS31_ANA	RW	Enable WIS PRBS31 test pattern checking function 0: Disable. 1: Enable.	0
4	TEST_PRBS31_GEN	RW	Enable WIS PRBS31 test pattern generation function. 0: Disable. 1: Enable.	0

Table 96. WIS_CTRL2: WIS Control 2 (2x0007) *(continued)*

Bit	Name	Access	Description	Default
3	TEST_PAT_SEL	RW	Selects the pattern type sent by the transmitter when TEST_PAT_GEN (2x0007.1) is low. 0: Mixed frequency test pattern 1: Square wave	0
2	TEST_PAT_ANA	RW	Enable the WIS test pattern checker. Doing so prevents the loss of code-group delineation (LCD-P) alarm from being set while the WIS is receiving the mixed frequency test pattern. 0: Disable. 1: Enable.	0
1	TEST_PAT_GEN	RW	Enable WIS test pattern generation. 0: Disable. 1: Enable.	0
0	WAN_MODE	RW	Enable 10GBASE-W logic and sets the speed of the WIS-PMA interface to 9.95328 Gbps. The proper reference clock frequency must be provided to set the data rate. Note that there are multiple ways to enable WAN mode. 0: Disable. 1: Enable.	0

Table 97. WIS_STAT2: WIS Status 2 (2x0008)

Bit	Name	Access	Description	Default
15:14	DEV_PRES	RO	Reflects the presence of a MMD responding at this address 00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	10
13:2	RESERVED	RO	Reserved	All zeros
1	PRBS31_ABILITY	RO	Indicates if WIS supports PRBS31 pattern testing 0: Not supported 1: Supported	1
0	BASE_R_ABILITY	RO	Indicates if WIS supports a bypass to allow support of 10GBASE-R 0: Not supported 1: Supported	1

Table 98. WIS_TSTPAT_CNT: WIS Test Pattern Error Counter (2x0009)

Bit	Name	Access	Description	Default
15:0	TSTPAT_CNT	ROCR	PRBS31 test pattern error counter. The saturating counter clears on read. The counter does not increment until the analyzer has reached pattern synchronization. After the counter begins to increment, the counting is not affected by changes to the pattern synchronization.	All zeros

Table 99. WIS_PKGID1: WIS Package Identifier 1 (2x000E)

Bit	Name	Access	Description	Default
15:0	PKG_ID_MSW	RO	Upper 16 bits of a 32-bit unique WIS package identifier. Bits 3-18 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	All zeros

Table 100. WIS_PKGID2: WIS Package Identifier 2 (2x000F)

Bit	Name	Access	Description	Default
15:0	PKG_ID_LSW	RO	Lower 16 bits of a 32-bit unique WIS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	All zeros

Table 101. WIS_STAT3: WIS Status 3 (2x0021)

Bit	Name	Access	Description	Default
15:12	RESERVED	RO	Reserved	All zeros
11	SEF	RO/LH	Severely errored frame 0: No SEF detected 1: SEF detected	0
10	FEPLMP_LCDP	RO/LH	Indicates far-end PLM-P/LCD-P defect in WIS Rx 0: No far-end path label mismatch / Loss of code-group delineation 1: Far-end path label mismatch / Loss of code-group delineation	0
9	FEAISP_LOPP	RO/LH	Indicates far-end AIS-P/LOP-P defect in WIS Rx 0: Far-end path alarm indication signal / path loss of pointer 1: No far-end path alarm indication signal / Path loss of pointer	0
8	RESERVED	RO	Reserved	0
7	LOF	RO/LH	Loss of frame 0: Loss of frame flag lowered 1: Loss of frame flag raised	0
6	LOS	RO/LH	Loss of signal 0: Loss of signal flag lowered 1: Loss of signal flag raised	0
5	RDIL	RO/LH	Line remote defect indication 0: Line remote defect flag lowered 1: Line remote defect flag raised	0
4	AISL	RO/LH	Line alarm indication signal 0: Line alarm indication flag lowered 1: Line alarm indication flag raised	0
3	LCDP	RO/LH	Path loss of code-group delineation 0: Path loss of code-group delineation flag lowered 1: Path loss of code-group delineation flag raised	0

Table 101. WIS_STAT3: WIS Status 3 (2x0021) *(continued)*

Bit	Name	Access	Description	Default
2	PLMP	RO/LH	Path label mismatch 0: Path label mismatch flag lowered 1: Path label mismatch flag raised	0
1	AISP	RO/LH	Path alarm indication signal 0: Path alarm indication signal lowered 1: Path alarm indication signal raised	0
0	LOPP	RO/LH	Loss of pointer 0: Loss of pointer flag lowered 1: Loss of pointer flag raised	0

Table 102. WIS_REI_CNT: WIS Far-End Path Block Error Count (2x0025)

Bit	Name	Access	Description	Default
15:0	REIP_CNT	RO	Far-end path block error count. Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 103. WIS_TXJ1: WIS Tx J1s (2x0027-002E)

Bit	Name	Access	Description	Default
15:8	TX_J1_ODD	RW	Contains one octet of the transmitted path trace message. The transmitted path trace octet 1 is in address 2x0027. Octet 3 is in address 2x0028. Octet 15 is in address 2x002E.	All zeros
7:0	TX_J1_EVEN	RW	Contains one octet of the transmitted path trace message. The transmitted path trace octet 0 is in address 2x0027. Octet 2 is in address 2x0028. Octet 14 is in address 2x002E.	All zeros

Table 104. WIS_RXJ1: WIS Rx J1s (2x002F-0036)

Bit	Name	Access	Description	Default
15:8	RX_J1_ODD	RO	Contains one octet of the received path trace message. The received path trace octet 1 is in address 2x002F. Octet 3 is in address 2x0030. Octet 15 is in address 2x0036.	All zeros
7:0	RX_J1_EVEN	RO	Contains one octet of the received path trace message. The received path trace octet 0 is in address 2x002F. Octet 2 is in address 2x0030. Octet 14 is in address 2x0036.	All zeros

Table 105. WIS_REIL_CNT1: WIS Far-End Line BIP Errors 1 (2x0037)

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_MSW	RO	Most significant word of the WIS far-end line BIP error counter. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 106. WIS_REIL_CNT0: WIS Far-End Line BIP Errors 0 (2x0038)

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_LSW	RO	Least significant word of the WIS far-end line BIP error counter. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 107. WIS_B2_CNT1: WIS L-BIP Error Count 1 (2x0039)

Bit	Name	Access	Description	Default
15:0	B2_CNT_MSW	RO	Most significant word of the WIS line BIP error counter. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 108. WIS_B2_CNT0: WIS L-BIP Error Count 0 (2x003A)

Bit	Name	Access	Description	Default
15:0	B2_CNT_LSW	RO	Least significant word of the WIS line BIP error counter. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 109. WIS_B3_CNT: WIS P-BIP Block Error Count (2x003B)

Bit	Name	Access	Description	Default
15:0	B3_CNT	RO	Path block error counter. Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on WIS reset.	All zeros

Table 110. WIS_B1_CNT: WIS S-BIP Error Count (2x003C)

Bit	Name	Access	Description	Default
15:0	B1_CNT	RO	Section BIP error counter. Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on WIS reset.	All zeros

Table 111. WIS_TXJ0: WIS Transmit J0s (2x0040-0047)

Bit	Name	Access	Description	Default
15:8	TX_J0_ODD	RW	Contains one octet of the transmitted section trace message. The transmitted section trace octet 1 is in address 2x0040. Octet 3 is in address 2x0041. Octet 15 is in address 2x0047.	All zeros
7:0	TX_J0_EVEN	RW	Contains one octet of the transmitted section trace message. The transmitted section trace octet 0 is in address 2x0040. Octet 2 is in address 2x0041. Octet 14 is in address 2x0047.	All zeros

Table 112. WIS_RXJ0: WIS Rx J0s (2x0048-004F)

Bit	Name	Access	Description	Default
15:8	RX_J0_ODD	RO	Contains one octet of the received section trace message. The received section trace octet 1 is in address 2x0048. Octet 3 is in address 2x0049. Octet 15 is in address 2x004F.	All zeros
7:0	RX_J0_EVEN	RO	Contains one octet of the received section trace message. The received section trace octet 0 is in address 2x0048. Octet 2 is in address 2x0049. Octet 14 is in address 2x004F.	All zeros

Table 113. EWIS_TXCTRL1: WIS Vendor-Specific Tx Control 1 (2xE600)

Bit	Name	Access	Description	Default
15	REIL_TXBLK_MODE	RW	Selects either using B2 block error count or bit error count mode to generate the M0/M1 bytes for REI-L back reporting. 0: Bit error mode 1: Block error mode	0

Table 113. EWIS_TXCTRL1: WIS Vendor-Specific Tx Control 1 (2xE600)

Bit	Name	Access	Description	Default
14	REIP_TXBLK_MODE	RW	Selects either using B2 block error count or bit error count mode to generate the G1 byte for REI-L back reporting. 0: Bit error mode 1: Block error mode	0
13	AUTO_SYNC_DIS	RW	Inhibits automatic pointer synchronization upon overflow/underflow is allowed in the Tx WIS FIFO. This FIFO is between the Tx WIS and PMA. 0: Automatic pointer sync is allowed 1: Automatic pointer sync is not allowed	0
12	SCR	RW	Enable transmit WIS scrambler 0: Disable 1: Enable	1
11	FRC_TX_TIMP	RW	Force transmission of a TIM-P condition within the G1 byte 0: Normal operation. 1: Force TIM-P	0
10	ERDI_TX_MODE	RW	Selects ERDI as the transmit WIS G1 byte mode 0: RDI mode 1: ERDI mode	1
9	SDH_TX_MODE	RW	Selects the format of the WIS frame structure 0: SONET mode 1: SDH mode	1
8	RESERVED	RW	Factory test only (do not modify this bit group)	0
7:4	SQ_WV_PW	RW	Select the transmit WIS square wave test pattern length 0000 - 0011: Invalid 0100: 4 zeros and 4 ones 0101: 5 zeros and 5 ones 0110: 6 zeros and 6 ones 0111: 7 zeros and 7 ones 1000: 8 zeros and 8 ones 1001: 9 zeros and 9 ones 1010: 10 zeros and 10 ones 1011: 11 zeros and 11 ones 1100 - 1111: Invalid	0100
3	RESERVED	RW	Factory test only (do not modify this bit group)	0
2	FRC_TX_RDI	RW	Force transmission of RDI-L in the K2 byte 0: Normal operation 1: Force RDI-L	0
1	FRC_TX_AISL	RW	Force transmission of AIS-L in the K2 byte. AIS-L takes precedence over RDI-L if both are asserted. 0: Normal operation. 1: Force AIS-L	0
0	LPBK_H	RW	Enable WIS network loopback (loopback H) 0: Disable 1: Enable	0

Table 114. Factory Test Register (2xE601)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
1	RESERVED	RW	Factory test only (do not modify this bit group)	0
0	RESERVED	RWSC	Factory test only (do not modify this bit group)	0

Table 115. Factory Test Register (2xE602)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
7:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 116. Factory Test Register (2xE603)

Bit	Name	Access	Description	Default
15:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 117. Factory Test Register (2xE604)

Bit	Name	Access	Description	Default
15:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 118. Factory Test Register (2xE605)

Bit	Name	Access	Description	Default
15:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

Table 119. EWIS_TX_A1_A2: E-WIS Tx A1/A2 Octets (2xE611)

Bit	Name	Access	Description	Default
15:8	TX_A1	RW	A1 byte to be transmitted when the TOSI data is inactive.	0xF6
7:0	TX_A2	RW	A2 byte to be transmitted when the TOSI data is inactive.	0x28

Table 120. EWIS_TX_Z0_E1: E-WIS Tx Z0/E1 Octets (2xE612)

Bit	Name	Access	Description	Default
15:8	TX_Z0	RW	Z0 byte to be transmitted when the TOSI data is inactive	0xCC
7:0	TX_E1	RW	E1 byte to be transmitted when the TOSI data is inactive	All zeros

Table 121. EWIS_TX_F1_D1: E-WIS Tx F1/D1 Octets (2xE613)

Bit	Name	Access	Description	Default
15:8	TX_F1	RW	F1 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_D1	RW	D1 byte to be transmitted when the TOSI data is inactive	All zeros

Table 122. EWIS_TX_D2_D3: E-WIS Tx D2/D3 Octets (2xE614)

Bit	Name	Access	Description	Default
15:8	TX_D2	RW	D2 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_D3	RW	D3 byte to be transmitted when the TOSI data is inactive	All zeros

Table 123. EWIS_TX_C2_H1: E-WIS Tx C2/H1 Octets (2xE615)

Bit	Name	Access	Description	Default
15:8	TX_C2	RW	C2 byte to be transmitted when the TOSI data is inactive	0x1A
7:0	TX_H1	RW	H1 byte to be transmitted when the TOSI data is inactive	0x62

Table 124. EWIS_TX_H2_H3: E-WIS Tx H2/H3 Octets (2xE616)

Bit	Name	Access	Description	Default
15:8	TX_H2	RW	H2 byte to be transmitted when the TOSI data is inactive	0x0A
7:0	TX_H3	RW	H3 byte to be transmitted when the TOSI data is inactive	All zeros

Table 125. EWIS_TX_G1_K1: E-WIS Tx G1/K1 Octets (2xE617)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros
7:0	TX_K1	RW	K1 byte to be transmitted when the TOSI data is inactive	All zeros

Table 126. EWIS_TX_K2_F2: E-WIS Tx K2/F2 Octets (2xE618)

Bit	Name	Access	Description	Default
15:8	TX_K2	RW	K2 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_F2	RW	F2 byte to be transmitted when the TOSI data is inactive	All zeros

Table 127. EWIS_TX_D4_D5: E-WIS Tx D4/D5 Octets (2xE619)

Bit	Name	Access	Description	Default
15:8	TX_D4	RW	D4 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_D5	RW	D5 byte to be transmitted when the TOSI data is inactive	All zeros

Table 128. EWIS_TX_D6_H4: E-WIS Tx D6/H4 Octets (2xE61A)

Bit	Name	Access	Description	Default
15:8	TX_D6	RW	D6 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_H4	RW	H4 byte to be transmitted when the TOSI data is inactive	All zeros

Table 129. EWIS_TX_D7_D8: E-WIS Tx D7/D8 Octets (2xE61B)

Bit	Name	Access	Description	Default
15:8	TX_D7	RW	D7 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_D8	RW	D8 byte to be transmitted when the TOSI data is inactive	All zeros

Table 130. EWIS_TX_D9_Z3: E-WIS Tx D9/Z3 Octets (2xE61C)

Bit	Name	Access	Description	Default
15:8	TX_D9	RW	D9 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_Z3	RW	Z3 byte to be transmitted when the TOSI data is inactive	All zeros

Table 131. EWIS_TX_D10_D11: E-WIS Tx D10/D11 Octets (2xE61D)

Bit	Name	Access	Description	Default
15:8	TX_D10	RW	D10 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_D11	RW	D11 byte to be transmitted when the TOSI data is inactive	All zeros

Table 132. EWIS_TX_D12_Z4: E-WIS Tx D12/Z4 Octets (2xE61E)

Bit	Name	Access	Description	Default
15:8	TX_D12	RW	D12 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_Z4	RW	Z4 byte to be transmitted when the TOSI data is inactive	All zeros

Table 133. EWIS_TX_S1_Z1: E-WIS Tx S1/Z1 Octets (2xE61F)

Bit	Name	Access	Description	Default
15:8	TX_S1	RW	S1 byte to be transmitted when the TOSI data is inactive	0x0F
7:0	TX_Z1	RW	Z1 byte to be transmitted when the TOSI data is inactive	All zeros

Table 134. EWIS_TX_Z2_E2: E-WIS Tx Z2/E2 Octets (2xE620)

Bit	Name	Access	Description	Default
15:8	TX_Z2	RW	Z2 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	TX_E2	RW	E2 byte to be transmitted when the TOSI data is inactive	All zeros

Table 135. EWIS_TX_N1: E-WIS Tx N1 Octet (2xE621)

Bit	Name	Access	Description	Default
15:8	TX_N1	RW	N1 byte to be transmitted when the TOSI data is inactive	All zeros
7:0	RESERVED	RO	Reserved	All zeros

Table 136. Factory Test Register (2xE622)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
7:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 137. EWIS_TX_MSGLEN: E-WIS Tx Trace Message Length Control (2xE700)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	All zeros
3:2	J0_TXLEN	RW	Selects length of transmitted section trace message 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	All zeros
1:0	J1_TXLEN	RW	Selects length of transmitted path trace message 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	All zeros

Table 138. EWIS_TXJ0: E-WIS Tx J0s 16-63 (2xE800-E817)

Bit	Name	Access	Description	Default
15:8	J0_TX64_ODD	RW	Contains one octet of the transmitted section trace message. Octet 17 is in 2xE800, octet 19 is in 2xE801, and so on.	All zeros
7:0	J0_TX64_EVEN	RW	Contains one octet of the transmitted section trace message. Octet 16 is in 2xE800, octet 18 is in 2xE801, and so on.	All zeros

Table 139. EWIS_RXJ0: E-WIS Rx J0s 16-63 (2xE900-E917)

Bit	Name	Access	Description	Default
15:8	J0_RX64_ODD	RO	Contains one octet of the received section trace message. Octet 17 is in 2xE900, octet 19 is in 2xE901, and so on.	All zeros

Table 139. EWIS_RXJ0: E-WIS Rx J0s 16-63 (2xE900-E917) *(continued)*

Bit	Name	Access	Description	Default
7:0	J0_RX64_EVEN	RO	Contains one octet of the received section trace message. Octet 16 is in 2xE900, octet 18 is in 2xE901, and so on.	All zeros

Table 140. EWIS_TXJ1: E-WIS Tx WIS J1s 16-63 (2xEA00-EA17)

Bit	Name	Access	Description	Default
15:8	J1_TX64_ODD	RW	Contains one octet of the transmitted path trace message. Octet 17 is in 2xEA00, octet 19 is in 2xEA01, and so on.	All zeros
7:0	J1_TX64_EVEN	RW	Contains one octet of the transmitted path trace message. Octet 16 is in 2xEA00, octet 18 is in 2xEA01, and so on.	All zeros

Table 141. EWIS_RXJ1: E-WIS Rx J1s 16-63 (2xEB00-EB17)

Bit	Name	Access	Description	Default
15:8	J1_RX64_ODD	RO	Contains one octet of the received path trace message. Octet 17 is in 2xEB00, octet 19 is in 2xEB01, and so on.	All zeros
7:0	J1_RX64_EVEN	RO	Contains one octet of the received path trace message. Octet 16 is in 2xEB00, octet 18 is in 2xEB01, and so on.	All zeros

Table 142. EWIS_RX_FRM_CTRL1: E-WIS Rx Framer Control 1 (2xEC00)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14:10	HUNT_A1	RW	The number of consecutive A1 octets that the receive framer must find before it can exit the HUNT state 0: Undefined 1-16: 1-16 17-31: Undefined	00100
9:5	PRESYNC_A1	RW	The number of consecutive A1 octets in the presync pattern preceding the first A2 octet 0: 1 1-16: 1-16 17-31: 16	10000
4:0	PRESYNC_A2	RW	The number of consecutive A2 octets in the presync pattern following the last A1 octet 0: Only the four MSB of the first A2 byte are compared 1-16: 1-16 17-31: 16	10000

Table 143. EWIS_RX_FRM_CTRL2: E-WIS Rx Framer Control 2 (2xEC01)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved.	All zeros
12:8	SYNC_PAT	RW	Synchronization pattern to be used after the presync pattern has been detected. 0: Sync pattern is A1 plus the four most significant bits of A2. 1: Sync pattern is two A1s plus one A2 (A1A1A2). 2-16: Sync pattern is the number of consecutive A1s followed by the same number of A2s. For example, the sync pattern is A1A1A2A2 when 2 is the setting. 17-31: Undefined.	00010
7:4	SYNC_ENTRY_CNT	RW	Number of consecutive frame boundaries to be detected after finding the presync pattern before the framer can enter the SYNC state. 0: 1. 1-15: 1-15.	0100
3:0	SYNC_EXIT_CNT	RW	Number of consecutive frame boundary location errors tolerated/detected before exiting the SYNC state. 0: 1. 1-15: 1-15.	0100

Table 144. EWIS_LOF_CTRL1: E-WIS Loss of Frame Control 1 (2xEC02)

Bit	Name	Access	Description	Default
15:12	RESERVED	RO	Reserved	All zeros
11:6	LOF_T1	RW	Defines the number of frames periods (nominally 125 microseconds) during which OOF must persist to trigger LOF. This is not a count of continuous frames. An integrating counter is used. 0x0: Undefined. 0x1: 1 frame time (125 µs). 0x2: 2 frame times (250 µs). - - - 0x18: 24 frame times (3 ms). 0x3F: 63 frame times (7.875 ms).	0x18
5:0	LOF_T2	RW	Defines the number of consecutive frame periods (nominally 125 µs) during which OOF status must not be true in order to clear loss of frame set count (the counter associated with 2xEC02.11:6). 0x0: Undefined. 0x1: 1 frame time (125 µs). 0x2: 2 frame times (250 µs). - - - 0x18: 24 frame times (3 ms). 0x3F: 63 frame times (7.875 ms).	0x18

Table 145. EWIS_LOF_CTRL2: E-WIS Loss of Frame Control 2 (2xEC03)

Bit	Name	Access	Description	Default
15:7	RESERVED	RO	Reserved	All zeros
6:1	LOF_T2	RW	Defines number of consecutive frames (normally 125 µs) for which the receive framer must be in its sync state in order to clear the LOF status 0x0: Undefined 0x1: 1 frame time (125 µs) 0x2: 2 frame times (250 µs) - - - 0x18: 24 frame times (3 ms) 0x3F: 63 frame times (7.875 ms)	0x18
0	RESERVED	RW	Factory test only (do not modify this bit group)	0

Table 146. EWIS_RX_CTRL1: E-WIS Rx Control 1 (2xEC10)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Reserved	All zeros
1	DSCR_ENA	RW	Enable the WIS descrambler 0: Disable 1: Enable	1
0	B3_CALC_MODE	RW	Selects whether or not the fixed stuff bytes are included in the receive Path BIP error calculation 0: The fixed stuff bytes are excluded from the B3 calculation 1: The fixed stuff bytes are included in the B3 calculation	1

Table 147. EWIS_RX_MSGLEN: E-WIS Rx Trace Message Length Control (2xEC20)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	All zeros
3:2	J0_RX_LEN	RW	Selects the expected length of the received Section trace message 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	All zeros
1:0	J1_RX_LEN	RW	Selects the length of the expected Path trace message 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	All zeros

Table 148. EWIS_RX_ERR_FRC1: E-WIS Rx Error Force Control 1 (2xEC30)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	All zeros
12	FRC_LOPC	RW	Force a loss of optical carrier (LOPC) condition 0: Normal operation 1: Force LOPC	0
11	FRC_LOS	RW	Force a loss of signal (LOS) condition in the WIS receive data path 0: Normal operation 1: Forced receive LOS	0
10	FRC_OOF	RW	Force the receive framer into the out-of-frame (OOF) state 0: Normal operation 1: Force receive OOF	0
9	LOPC_POL_SEL	RW	Select the polarity of the LOPC input pin 0: LOPC asserted when input is low 1: LOPC asserted when input is high	0
8	RXLOF_ON_LOPC	RW	Selects whether or not the LOPC input has any effect on alarm conditions detected by the device 0: A LOPC condition does not effect the state of the LOF or SEF status, nor the state of the receive path framer 1: LOF and SEF are asserted and the receive path framer is put into its out-of-frame state during a LOPC condition	0
7:4	APS_THRES	RW	Defines the number of consecutive frames received before asserting the AIS-L and RDI-L alarms 1-15: Threshold value All others: Reserved	0101
3	FRC_RX_AISL	RW	Force a line alarm indication signal (AIS-L) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx AIS-L condition	0
2	FRC_RX_RDIL	RW	Force a line remote defect identifier (RDI-L) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx RDI-L condition	0
1	FRC_RX_AISP	RW	Force a path alarm indication signal (AIS-P) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx AIS-P condition	0
0	FRC_RX_LOP	RW	Force a loss of pointer (LOP) condition to the starting location of the frame's SPE (synchronous payload envelope) in the WIS receive data path 0: Normal operation 1: Device forced into Rx LOP condition	0

Table 149. EWIS_RX_ERR_FRC2: E-WIS Rx Error Force Control 2 (2xEC31)

Bit	Name	Access	Description	Default
15	FRC_RX_UNEQP	RW	Force a unequipped path (UNEQ-P) defect in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx UNEQ-P condition.	0
14	FRC_RX_PLMP	RW	Force a payload label mismatch (PLM-P) defect in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx PLM-P condition.	0
13	FRC_RX_RDIP	RW	Force a far-end path remote defect identifier condition in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx far-end RDI-P condition.	0
12	FRC_RX_FE_AISP	RW	Force a far-end path alarm indication signal condition in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx far-end AIS-P condition.	0
11	FRC_RX_FE_UNEQP	RW	Force a far-end unequipped path defect in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx far-end UNEQ-P condition.	0
10	FRC_RX_FE_PLMP	RW	Force a far-end payload label mismatch defect in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx far-end PLM-P condition.	0
9	FRC_RX_REIP	RW	Force a path remote error indication (REI-P) condition in the WIS receive data path. The error is reflected in register 2xEF04.3. 0: Normal operation. 1: Device forced into Rx REI-P condition.	0
8	FRC_RX_REIL	RW	Force a line remote error indication (REI-L) condition in the WIS receive data path. The error is reflected in register 2xEF04.4. 0: Normal operation. 1: Device forced into Rx REI-L condition.	0
7	FRC_RX_SEF	RW	Force a severely errored frame (SEF) condition in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx SEF condition.	0
6	FRC_RX_LOF	RW	Force a loss of frame (LOF) condition in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx LOF condition.	0
5	FRC_RX_B1	RW	Force a PMTICK B1 BIP error condition (B1NZ) in the WIS receive data path. 0: Normal operation. 1: Device forced into PMTICK B1 BIP error condition.	0

Table 149. EWIS_RX_ERR_FRC2: E-WIS Rx Error Force Control 2 (2xEC31)

Bit	Name	Access	Description	Default
4	FRC_RX_B2	RW	Force a PMTICK B2 BIP error condition (B2NZ) in the WIS receive data path. 0: Normal operation. 1: Device forced into PMTICK B2 BIP error condition.	0
3	FRC_RX_B3	RW	Force a PMTICK B3 BIP error condition (B3NZ) in the WIS receive data path. 0: Normal operation. 1: Device forced into PMTICK B3 BIP error condition.	0
2	FRC_RX_LCDP	RW	Force a loss of code-group delineation (LCD-P) defect in the WIS receive data path. 0: Normal operation. 1: Device forced into Rx LCD-P condition.	0
1	FRC_RX_REIL_NZ	RW	Force a far-end line BIP error condition (far-end B2NZ) in the WIS receive data path. The error is reflected in register 2xEF04.2. 0: Normal operation. 1: Device forced into Rx far-end line BIP error condition.	0
0	FRC_RX_REIP_NZ	RW	Force a far-end path BIP error condition (far-end B3NZ) in the WIS receive data path. The error is reflected in register 2xEF04.1. 0: Normal operation. 1: Device forced into Rx far-end path BIP error condition.	0

Table 150. EWIS_MODE_CTRL: E-WIS Mode Control (2xEC40)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved.	All zeros
12	REI_MODE	RW	Selects how REI is extracted from the M0/M1 bytes in the WIS receive data path. 0: SONET mode enabled. Uses M0 only. 1: SDH mode enabled. Uses M0 and M1.	0
11	SDH_RX_MODE	RW	Selects how the H1/H2 pointer processing is performed. 0: SONET mode. 1: SDH mode.	0
10:9	RESERVED	RW	Factory test only (do not modify this bit group).	All zeros
8	RX_ERDI_MODE	RW	Selects how ERDI-P/RDI-P is extracted from the G1 byte in the WIS received data. 0: RDI-P is reported in bit 5, bits 6 and 7 are unused. 1: ERDI is reported in bits 5-7. 101 indicates far-end AIS-P. 110 indicates far-end UNEQ-P. 010 indicates far-end PLM-P.	1
7:0	C2_EXP	RW	Expected C2 receive octet. A PLM-P alarm is generated if this octet value is not received.	0x1A

Table 151. EWIS_STAT: E-WIS Status (2xEC41)

Bit	Name	Access	Description	Default
15:11	RESERVED	RO	Reserved.	All zeros
10	TX_FIFO_OUFLOW	RO	Indicates overflow/underflow status in the Tx WIS FIFO. This FIFO is between the Tx WIS and PMA. 0: No error condition. 1: A FIFO overflow/underflow condition has occurred.	0
9:0	RESERVED	RO	Factory test only (do not modify this bit group).	All zeros

Table 152. EWIS_PRBS31_ANA_CTRL: E-WIS PRBS31 Analyzer Control (2xEC50)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Reserved.	All zeros
1	PRBS31_FRC_ERR	RW	Inject a single bit error into the WIS PRBS31 pattern checker. A single bit error results in the error counter incrementing by 3 (one error for each tap of the checker). 0: Normal operation. 1: Inject error.	0
0	PRBS31_FRC_SAT	RWSC	Force the PRBS31 pattern error counter to a value of 65528. This can be useful for testing the saturating feature of the counter. 0: Normal operation. 1: Force the PRBS31 error counter to a value of 65528. **Note** Forcing the counter to 65528 through this bit has no effect on register 2xEC51.1.	0

Table 153. EWIS_PRBS31_ANA_STAT: E-WIS PRBS31 Analyzer Status (2xEC51)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Reserved.	All zeros
1	PRBS31_ERR	RO	Status bit indicating if the WIS PRBS31 error counter is non-zero. 0: Counter is zero. 1: Counter is non-zero. **Note** When the WIS PRBS31 analyzer is disabled, this bit might still be on. When the analyzer is re-enabled, this bit is cleared. If needed, the device reset can be used to clear the status.	0
0	PRBS31_ANA_STATE	RO	Indicates when the Rx WIS PRBS31 pattern checker is synchronized to the incoming data. 0: PRBS31 pattern checker is not synchronized to the data. PRBS31 error counter value is not valid. 1: PRBS31 pattern checker is synchronized to the data.	0

Table 154. EWIS_PMTICK_CTRL: E-WIS Performance Monitor Control (2xEC60)

Bit	Name	Access	Description	Default
15:3	PMTICK_DUR	RW	Sets the interval for updating the PMTICK error counters when the PMTICK_SRC bit is 1. The value represents the number of 125 μs increments between PMTICK events. 0: Undefined. 1: Undefined. 2: 250 μs. - - - 8: 1 ms. 8000: 1 second 8191: 1.024 seconds	0x1F40
2	PMTICK_ENA	RW	Enable the PMTICK counters to be updated on a PMTICK event. The source of the PMTICK event is determined by the PMTICK_SRC bit. 0: Disable. 1: Enable.	0
1	PMTICK_SRC	RW	Selects how the PMTICK counters are updated. The PMTICK counters are updated with the selected source only if the PMTICK enable bit is set. 0: PMTICK counters updated on a rising edge of the PMTICK pin. 1: PMTICK counters updated when the PMTICK. counter reaches its terminal count.	1
0	PMTICK_FRC	RWSC	Force the PMTICK counters to update, regardless of the PMTICK_ENA or PMTICK_SRC settings. 0: Normal operation. 1: Forces PMTICK event.	0

Table 155. EWIS_CNT_CFG: E-WIS Counter Configuration (2xEC61)

Bit	Name	Access	Description	Default
15:12	RESERVED	RO	Reserved	All zeros
11	B1_BLK_MODE	RW	Enable block mode (increment once for each errored frame) counting for the B1 BIP PMTICK counter. 0: Bit mode 1: Block mode	0
10	B2_BLK_MODE	RW	Enable block mode (increment once for each errored frame) counting for the B2 BIP PMTICK counter 0: Bit mode 1: Block mode	0
9	B3_BLK_MODE	RW	Enable block mode (increment once for each errored frame) counting for the B3 BIP PMTICK counter 0: Bit mode 1: Block mode	0
8:6	RESERVED	RO	Reserved	All zeros

Table 155. EWIS_CNT_CFG: E-WIS Counter Configuration (2xEC61) *(continued)*

Bit	Name	Access	Description	Default
5	REIP_BLK_MODE	RW	Enable block mode (increment once for each errored frame) counting for the REI-P (far-end B3 error count in the G1 byte) PMTICK counter 0: Bit mode 1: Block mode	0
4	REIL_BLK_MODE	RW	Enable block mode (increment once for each errored frame) counting for the REI-L (far-end B2 error count in the M0/M1 byte) PMTICK counter 0: Bit mode 1: Block mode	0
3:0	RESERVED	RO	Reserved	All zeros

Table 156. EWIS_CNT_STAT: E-WIS Counter Status (2xEC62)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved	All zeros
2	REIP_CNT_STAT	RO	Status bit indicating if the REI-P (far-end B3) PMTICK counter is non-zero 0: Counter is zero 1: Counter is non-zero **Note** Counter is not impacted by FRC_RX_REIP or FRC_RX_REIP_NZ.	0
1	REIL_CNT_STAT	RO	Status bit indicating if the REI-L (far-end B2) PMTICK counter is non-zero 0: Counter is zero 1: Counter is non-zero **Note** Counter is not impacted by FRC_RX_REIL or FRC_RX_REIL_NZ.	0
0	RESERVED	RO	Factory test only (do not modify this bit)	0

Table 157. EWIS_REIP_CNT1: E-WIS P-REI Counter 1 (MSW) (2xEC80)

Bit	Name	Access	Description	Default
15:0	REIP_ERR_CNT_MSW	RO	PMTICK statistical error count of the far-end B3 errors (reported in the G1 byte). 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	0

Table 158. EWIS_REIP_CNT0: E-WIS P-REI Counter 0 (LSW) (2xEC81)

Bit	Name	Access	Description	Default
15:0	REIP_ERR_CNT_LSW	RO	PMTICK statistical error count of the far-end B3 errors (reported in the G1 byte). 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 159. EWIS_REIL_CNT1: E-WIS L-REI Counter 1 (MSW) (2xEC90)

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_MSW	RO	PMTICK statistical error count of the far-end B2 errors (reported in the M0/M1 bytes). 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 160. EWIS_REIL_CNT0: E-WIS L-REI Counter 0 (LSW) (2xEC91)

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_LSW	RO	PMTICK statistical error count of the far-end B2 errors (reported in the M0/M1 bytes). 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 161. Factory Test Register (2xECA0)

Bit	Name	Access	Description	Default
15:7	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
6:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 162. EWIS_B1_ERR_CNT1: E-WIS S-BIP Error Counter 1 (MSW) (2xECB0)

Bit	Name	Access	Description	Default
15:0	B1_ERR_CNT_MSW	RO	PMTICK statistical error count of the B1 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 163. EWIS_B1_ERR_CNT0: E-WIS S-BIP Error Counter 0 (LSW) (2xECB1)

Bit	Name	Access	Description	Default
15:0	B1_ERR_CNT_LSW	RO	PMTICK statistical error count of the B1 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 164. EWIS_B2_ERR_CNT1: E-WIS L-BIP Error Counter 1 (MSW) (2xECB2)

Bit	Name	Access	Description	Default
15:0	B2_ERR_CNT_MSW	RO	PMTICK statistical error count of the B2 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 165. EWIS_B2_ERR_CNT0: E-WIS L-BIP Error Counter 0 (LSW) (2xECB3)

Bit	Name	Access	Description	Default
15:0	B2_ERR_CNT_LSW	RO	PMTICK statistical error count of the B2 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 166. EWIS_B3_ERR_CNT1: E-WIS P-BIP Error Counter 1 (MSW) (2xECB4)

Bit	Name	Access	Description	Default
15:0	B3_ERR_CNT_MSW	RO	PMTICK statistical error count of the B3 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 167. EWIS_B3_ERR_CNT0: E-WIS P-BIP Error Counter 0 (LSW) (2xECB5)

Bit	Name	Access	Description	Default
15:0	B3_ERR_CNT_LSW	RO	PMTICK statistical error count of the B3 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	All zeros

Table 168. Factory Test Register (2xED00–ED08)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 169. EWIS_RXTX_CTRL: E-WIS Rx to Tx Control (2xEE00)

Bit	Name	Access	Description	Default
15:7	RESERVED	RO	Reserved.	All zeros

Table 169. EWIS_RXTX_CTRL: E-WIS Rx to Tx Control (2xEE00) *(continued)*

Bit	Name	Access	Description	Default
6	RXAISL_ON_LOPC	RW	Select if a LOPC condition contributes to the Rx AIS-L alarm. 0: A LOPC condition does not cause the AIS-L alarm to be set. 1: A LOPC condition causes the AIS-L alarm to be set.	0
5	RXAISL_ON_LOS	RW	Selects if a LOS condition contributes to the Rx AIS-L alarm. 0: A LOS condition does not cause the AIS-L alarm to be set. 1: A LOS condition causes the AIS-L alarm to be set.	0
4	RXAISL_ON_LOF	RW	Select if a LOF condition contributes to the Rx AIS-L alarm. 0: A LOF condition does not cause the AIS-L alarm to be set. 1: A LOF condition causes the AIS-L alarm to be set.	0
3	TXRDIL_ON_LOPC	RW	Select if a RDI-L is reported in the Tx frame’s K2 byte when a LOPC condition is detected. 0: RDI-L is not reported when LOPC is detected. 1: RDI-L is reported when LOPC is detected.	0
2	TXRDIL_ON_LOS	RW	Selects whether or not RDI-L is reported in the Tx frame’s K2 byte when a LOS condition is detected. 0: RDI-L is not reported when LOS is detected. 1: RDI-L is reported when LOS is detected.	0
1	TXRDIL_ON_LOF	RW	Selects whether or not RDI-L is reported in the Tx frame’s K2 byte when a LOF condition is detected. 0: RDI-L is not reported when LOF is detected. 1: RDI-L is reported when LOF is detected.	0
0	TXRDIL_ON_AISL	RW	Selects whether or not RDI-L is reported in the Tx frame’s K2 byte when a Rx AIS-L condition is detected. 0: RDI-L is not reported when a Rx AIS-L condition is detected. 1: RDI-L is reported when a Rx AIS-L condition is detected.	0

Table 170. EWIS_PEND1: E-WIS Interrupt Pending 1 (2xEF00)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved.	0
14	MSTCODE2_PEND	ROCR	Interrupt pending. MSTCODE[2] input pin has changed state since this register was last read. The MSTCODE[2] pin status is reported in 1xE607.15. 0: MSTCODE[2] pin has not changed state since last read of this register. 1: MSTCODE[2] pin has changed state.	0

Table 170. EWIS_PEND1: E-WIS Interrupt Pending 1 (2xEF00) *(continued)*

Bit	Name	Access	Description	Default
13	MSTCODE1_PEND	ROCR	Interrupt pending. MSTCODE[1] input pin has changed state since this register was last read. The MSTCODE[1] pin status is reported in 1xE607.14. 0: MSTCODE[1] pin has not changed state since last read of this register. 1: MSTCODE[1] pin has changed state.	0
12	MSTCODE0_PEND	ROCR	Interrupt pending. MSTCODE[0] input pin has changed state since this register was last read. The MSTCODE[1] pin status is reported in 1xE607.13. 0: MSTCODE[0] pin has not changed state since last read of this register. 1: MSTCODE[0] pin has changed state.	0
11	SEF_PEND	ROCR	Interrupt pending. SEF has changed state since this register was last read. 0: SEF condition has not changed state. 1: SEF condition has changed state.	0
10	FEPLMP_LCDP_PEND	ROCR	Interrupt pending. Far-end path label mismatch (PLM-P) / Loss of code-group delineation (LCD-P) condition has changed state since this register was last read. 0: PLM-P/LCD-P has not changed state. 1: PLM-P/LCD-P condition has changed state.	0
9	FEAISP_LOPP_PEND	ROCR	Interrupt pending. Far-end path alarm indication signal (AIS-P) / Path loss of pointer (LOP) condition has changed state since this register was last read. 0: Far-end AIS-P/LOP-P condition has not changed state. 1: Far-end AIS-P/LOP-P condition has changed state.	0
8	RESERVED	RO	Reserved	0
7	LOF_PEND	ROCR	Interrupt pending. Loss of frame (LOF) condition has changed state since this register was last read. 0: LOF condition has not changed state. 1: LOF condition has changed state.	0
6	LOS_PEND	ROCR	Interrupt pending. Loss of signal (LOS) condition has changed state since this register was last read. This bit does not assert if LOPC is active at the time LOS changes state. 0: LOS condition has not changed state. 1: LOS condition has changed state.	0
5	RDIL_PEND	ROCR	Interrupt pending. Line remote defect indication (RDI-L) has changed state since this register was last read. 0: RDI-L condition has not changed state. 1: RDI-L condition has changed state.	0
4	AISL_PEND	ROCR	Interrupt pending. Line alarm indication signal (AIS-L) has changed state since this register was last read. This bit does not assert if LOPC, LOS, LOF, or SEF are asserted at the time AIS-L changes state. 0: AIS-L condition has not changed state. 1: AIS-L condition has changed state.	0

Table 170. EWIS_PEND1: E-WIS Interrupt Pending 1 (2xEF00) *(continued)*

Bit	Name	Access	Description	Default
3	LCDP_PEND	ROCR	Interrupt pending. Loss of code-group delineation (LCD-P) has changed state since this register was last read. This bit does not assert if AIS-L, AIS-P, UNEQ-P, or PLM-P are asserted at the time LCD-P changes state. 0: LCD-P condition has not changed state. 1: LCD-P condition has changed state.	0
2	PLMP_PEND	ROCR	Interrupt pending. Path label mismatch (PLM-P) has changed state since this register was last read. This bit does not assert if LOP-P or AIS-P are asserted at the time PLM-P changes state. 0: PLM-P condition has not changed state. 1: PLM-P condition has changed state.	0
1	AISP_PEND	ROCR	Interrupt pending. Path alarm indication signal (AIS-P) has changed state since this register was last read. This bit does not assert if LOPC, LOS, SEF, LOF, or AIS-L are asserted at the time AIS-P changes state. 0: AIS-P condition has not changed state. 1: AIS-P condition has changed state.	0
0	LOPP_PEND	ROCR	Interrupt pending. Path loss of pointer (LOP-P) has changed state since this register was last read. 0: LOP-P condition has not changed state. 1: LOP-P condition has changed state.	0

Table 171. EWIS_MASKA_1: E-WIS Interrupt Mask A 1 (2xEF01)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14	MSTCODE2_MASKA	RW	Enable propagation of MSTCODE2_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
13	MSTCODE1_MASKA	RW	Enable propagation of MSTCODE1_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
12	MSTCODE0_MASKA	RW	Enable propagation of MSTCODE0_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
11	SEF_MASKA	RW	Enable propagation of SEF_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
10	FEPLMP_LCDP_MASKA	RW	Enable propagation of FEPLMP_LCDP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0

Table 171. EWIS_MASKA_1: E-WIS Interrupt Mask A 1 (2xEF01) *(continued)*

Bit	Name	Access	Description	Default
9	FEAISP_LOPP_MASKA	RW	Enable propagation of FEAISP_LOPP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
8	RESERVED	RO	Reserved	0
7	LOF_MASKA	RW	Enable propagation of LOF_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
6	LOS_MASKA	RW	Enable propagation of LOS_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
5	RDIL_MASKA	RW	Enable propagation of RDIL_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
4	AISL_MASKA	RW	Enable propagation of AISL_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
3	LCDP_MASKA	RW	Enable propagation of LCDP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
2	PLMP_MASKA	RW	Enable propagation of PLMP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
1	AISP_MASKA	RW	Enable propagation of AISP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
0	LOPP_MASKA	RW	Enable propagation of LOPP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0

Table 172. EWIS_MASKB_1: E-WIS Interrupt Mask B 1 (2xEF02)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14	MSTCODE2_MASKB	RW	Enable propagation of MSTCODE2_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
13	MSTCODE1_MASKB		Enable propagation of MSTCODE1_PEND to the WIS_INTB pin 0: Disable 1: Enable	

Table 172. EWIS_MASKB_1: E-WIS Interrupt Mask B 1 (2xEF02) *(continued)*

Bit	Name	Access	Description	Default
12	MSTCODE0_MASKB		Enable propagation of MSTCODE0_PEND to the WIS_INTB pin 0: Disable 1: Enable	
11	SEF_MASKB	RW	Enable propagation of SEF_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
10	FEPLMP_LCDP_MASKB	RW	Enable propagation of FEPLMP_LCDP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
9	FEAISP_LOPP_MASKB	RW	Enable propagation of FEAISP_LOPP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
8	RESERVED	RO	Reserved	0
7	LOF_MASKB	RW	Enable propagation of LOF_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
6	LOS_MASKB	RW	Enable propagation of LOS_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
5	RDIL_MASKB	RW	Enable propagation of RDIL_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
4	AISL_MASKB	RW	Enable propagation of AISL_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
3	LCDP_MASKB	RW	Enable propagation of LCDP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
2	PLMP_MASKB	RW	Enable propagation of PLMP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
1	AISP_MASKB	RW	Enable propagation of AISP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
0	LOPP_MASKB	RW	Enable propagation of LOPP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0

Table 173. EWIS_INTR_STAT2: E-WIS Interrupt Status 2 (2xEF03)

Bit	Name	Access	Description	Default
15:14	RESERVED	RO	Reserved	0
13	TXLOL_STAT	RO	PMA CMU loss of lock status 0: No PMA CMU lock error 1: PMA CMU lock error	0
12	RXLOL_STAT	RO	PMA CRU loss of lock status 0: No PMA CRU lock error 1: PMA CRU lock error	0
11	LOPC_STAT	RO	Loss of optical carrier (LOPC) status 0: The LOPC input pin is de-asserted 1: The LOPC input pin is asserted	0
10	UNEQP_STAT	RO	Unequipped path (UNEQ-P) status 0: UNEQ-P is de-asserted 1: UNEQ-P is asserted	0
9	FEUNEQP_STAT	RO	Far-end unequipped path (UNEQ-P) status 0: Far-end UNEQ-P is de-asserted 1: Far-end UNEQ-P is asserted	0
8	FERDIP_STAT	RO	Far-end path remote defect identifier (RDI-P) status 0: Far-end RDI-P is de-asserted 1: Far-end RDI-P is asserted	0
7	B1_NZ_STAT	RO	PMTICK B1 BIP (B1_ERR_CNT) counter status 0: B1_ERR_CNT is zero 1: B1_ERR_CNT is non-zero	0
6	B2_NZ_STAT	RO	PMTICK B2 BIP (B2_ERR_CNT) counter status 0: B2_ERR_CNT is zero 1: B2_ERR_CNT is non-zero	0
5	B3_NZ_STAT	RO	PMTICK B3 BIP (B3_ERR_CNT) counter status 0: B3_ERR_CNT is zero 1: B3_ERR_CNT is non-zero	0
4	REIL_STAT	RO	Line remote error indication (REI-L) value status 0: The REI-L value in the last received frame reported no errors 1: The REI-L value in the last received frame reported errors	0
3	REIP_STAT	RO	Path remote error indication (REI-P) value status 0: The REI-P value in the last received frame reported no errors 1: The REI-P value in the last received frame reported errors	0
2	REIL_NZ_STAT	RO	PMTICK REI-L (REIL_ERR_CNT) counter status 0: REIL_ERR_CNT is zero 1: REIL_ERR_CNT is non-zero	0
1	REIP_NZ_STAT	RO	PMTICK REI-P (REIP_ERR_CNT) counter status 0: REIP_ERR_CNT is zero 1: REIP_ERR_CNT is non-zero	0
0	HIGH_BER_STAT	RO	PCS high bit error rate (BER) status 0: No high BER 1: The PCS block indicates a high bit error rate	0

Table 174. EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEF04)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved.	0
14	PMTICK_PEND	ROCR	Interrupt pending. A PMTICK event (regardless of the source) has occurred since this register was last read. 0: A PMTICK event has not occurred. 1: A PMTICK event occurred.	0
13	TXLOL_PEND	ROCR	Interrupt pending. PMA CMU lock signal (TXLOL_STAT) has changed state since this register was last read. 0: TXLOL_STAT has not changed state. 1: TXLOL_STAT has changed state.	0
12	RXLOL_PEND	ROCR	Interrupt pending. PMA CRU lock signal (RXLOL_STAT) has changed state since this register was last read. 0: RXLOL_STAT has not changed state. 1: RXLOL_STAT has changed state.	0
11	LOPC_PEND	ROCR	Interrupt pending. Loss of optical carrier (LOPC) input pin (LOPC_STAT) has changed state since this register was last read. 0: LOPC_STAT has not changed state. 1: LOPC_STAT has changed state.	0
10	UNEQP_PEND	ROCR	Interrupt pending. Unequipped path (UNEQP_STAT) has changed state since this register was last read. This bit does not assert if LOP-P or AIS-P are asserted at the time UNEQP changes state. 0: UNEQP_STAT has not changed state. 1: UNEQP_STAT has changed state.	0
9	FEUNEQP_PEND	ROCR	Interrupt pending. Far-end unequipped path (FEUNEQP_STAT) has changed state since this register was last read. 0: FEUNEQP_STAT has not changed state. 1: FEUNEQP_STAT has changed state.	0
8	FERDIP_PEND	ROCR	Interrupt pending. Far-end path remote defect identifier (FERDIP_STAT) has changed state since this register was last read. 0: FERDIP_STAT has not changed state. 1: FERDIP_STAT has changed state.	0
7	B1_NZ_PEND	ROCR	Interrupt pending. PMTICK B1 error counter (B1_ERR_CNT) has changed from zero to a non-zero value since this register was last read. This bit does not assert if LOS or LOF are asserted at the time B1_NZ changes from 0 to 1. 0: B1_NZ_STAT has not changed from a 0 to 1 state. 1: B1_NZ_STAT has changed from a 0 to 1 state.	0

Table 174. EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEF04) *(continued)*

Bit	Name	Access	Description	Default
6	B2_NZ_PEND	ROCR	Interrupt pending. PMTICK B2 error counter (B2_ERR_CNT) has changed from zero to a non-zero value since this register was last read. This bit does not assert if AIS-L is asserted at the time B2_NZ changes from 0 to 1. 0: B2_NZ_STAT has not changed from a 0 to 1 state. 1: B2_NZ_STAT has changed from a 0 to 1 state.	0
5	B3_NZ_PEND	ROCR	Interrupt pending. PMTICK B3 error counter (B3_ERR_CNT) has changed from zero to a non-zero value since this register was last read. This bit does not assert if LOP-P or AIS-P are asserted at the time B3_NZ changes from 0 to 1. 0: B3_NZ_STAT has not changed from a 0 to 1 state. 1: B3_NZ_STAT has changed from a 0 to 1 state.	0
4	REIL_PEND	ROCR	Interrupt pending. REI-L changed from zero to non-zero. 0: REI-L has not received a non-zero value. 1: REI-L has received a non-zero value.	0
3	REIP_PEND	ROCR	Interrupt pending. REI-P changed from zero to non-zero. 0: REI-P has not received a non-zero value. 1: REI-P has received a non-zero value.	0
2	REIL_NZ_PEND	ROCR	Interrupt pending. PMTICK far-end B2 error counter (REIL_ERR_CNT) has changed from a zero to a non-zero value since this register was read. 0: REIL_NZ_STAT has not changed from a 0 to 1 state. 1: REIL_NZ_STAT has changed from a 0 to 1 state.	0
1	REIP_NZ_PEND	ROCR	Interrupt pending. PMTICK far-end B3 error counter (REIP_ERR_CNT) has changed from a zero to a non-zero value since this register was read. 0: REIP_NZ_STAT has changed from a 0 to 1 state. 1: REIP_NZ_STAT has changed from a 0 to 1 state.	0
0	HIGH_BER_PEND	ROCR	Interrupt pending. PCS high bit error rate (BER) condition has changed state since this register was read. 0: No change in PCS high BER condition. 1: PCS high BER condition has changed state.	0

Table 175. EWIS_INTR_MASKA2: E-WIS Interrupt Mask A 2 (2xEF05)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14	PMTICK_MASKA	RW	Enable propagation of PMTICK_PEND to the WIS_INTA pin 0: Disable 1: Enable	0

Table 175. EWIS_INTR_MASKA2: E-WIS Interrupt Mask A 2 (2xEF05)

Bit	Name	Access	Description	Default
13	TXLOL_MASKA	RW	Enable propagation of TXLOL_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
12	RXLOL_MASKA	RW	Enable propagation of RXLOL_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
11	LOPC_MASKA	RW	Enable propagation of LOPC_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
10	UNEQP_MASKA	RW	Enable propagation of UNEQP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
9	FEUNEQP_MASKA	RW	Enable propagation of FEUNEQP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
8	FERDIP_MASKA	RW	Enable propagation of FERDIP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
7	B1_NZ_MASKA	RW	Enable propagation of B1_NZ_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
6	B2_NZ_MASKA	RW	Enable propagation of B2_NZ_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
5	B3_NZ_MASKA	RW	Enable propagation of B3_NZ_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
4	REIL_MASKA	RW	Enable propagation of REIL_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
3	REIP_MASKA	RW	Enable propagation of REIP_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
2	REIL_NZ_MASKA	RW	Enable propagation of REIL_NZ_PEND to the WIS_INTA pin 0: Disable 1: Enable	0
1	REIP_NZ_MASKA	RW	Enable propagation of REIP_NZ_PEND to the WIS_INTA pin 0: Disable 1: Enable	0

Table 175. EWIS_INTR_MASKA2: E-WIS Interrupt Mask A 2 (2xEF05)

Bit	Name	Access	Description	Default
0	HIGH_BER_MASKA	RW	Enable propagation of HIGH_BER_PEND to the WIS_INTA pin 0: Disable 1: Enable	0

Table 176. EWIS_INTR_MASKB2: E-WIS Interrupt Mask B 2 (2xEF06)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14	PMTICK_MASKB	RW	Enable propagation of PMTICK_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
13	TXLOL_MASKB	RW	Enable propagation of TXLOL_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
12	RXLOL_MASKB	RW	Enable propagation of RXLOL_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
11	LOPC_MASKB	RW	Enable propagation of LOPC_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
10	UNEQP_MASKB	RW	Enable propagation of UNEQP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
9	FEUNEQP_MASKB	RW	Enable propagation of FEUNEQP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
8	FERDIP_MASKB	RW	Enable propagation of FERDIP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
7	B1_NZ_MASKB	RW	Enable propagation of B1_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
6	B2_NZ_MASKB	RW	Enable propagation of B2_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
5	B3_NZ_MASKB	RW	Enable propagation of B3_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	0

Table 176. EWIS_INTR_MASKB2: E-WIS Interrupt Mask B 2 (2xEF06) *(continued)*

Bit	Name	Access	Description	Default
4	REIL_MASKB	RW	Enable propagation of REIL_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
3	REIP_MASKB	RW	Enable propagation of REIP_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
2	REIL_NZ_MASKB	RW	Enable propagation of REIL_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
1	REIP_NZ_MASKB	RW	Enable propagation of REIP_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	0
0	HIGH_BER_MASKB	RW	Enable propagation of HIGH_BER_PEND to the WIS_INTB pin 0: Disable 1: Enable	0

4.3 Device 3: PCS Registers

The following tables provide settings for the registers related to the PCS.

Table 177. PCS_CTRL1: PCS Control 1 (3x0000)

Bit	Name	Access	Description	Default
15	SOFT_RST	RWSC	Reset all MMDs 0: Normal operation 1: Reset	0
14	LPBK_G	RW	Enable PCS system loopback (loopback G) 0: Disable 1: Enable NOTE: XFI outputs 0x00FF	0
13	SPEED_SEL_A	RO	PCS speed capability 0: Unspecified 1: Operates at 10 Gbps or above	1
12	RESERVED	RO	Reserved (value always 0, writes ignored)	0
11	LOW_PWR	RW	Enter low power mode on all MMDs 0: Normal operation 1: Low power	0
10:7	RESERVED	RO	Reserved (value always 0, writes ignored)	0
6	SPEED_SEL_B	RO	PCS speed capability 0: Unspecified 1: Operates at 10 Gbps or above	1

Table 177. PCS_CTRL1: PCS Control 1 (3x0000) *(continued)*

Bit	Name	Access	Description	Default
5:2	SPEED_SEL_C	RO	PCS speed selection 1xxx: Reserved x1xx: Reserved xx1x: Reserved 0001: Reserved 0000: 10 Gbps	0000
1:0	RESERVED	RO	Reserved (value always 0, writes ignored)	0

Table 178. PCS_STAT1: PCS Status 1 (3x0001)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved (ignore when read).	All zeros
7	FAULT	RO	PCS fault status. Asserted when either the PCS FAULT_RX (3x0008.10) or PCS FAULT_TX (3x0008.11) is asserted. 0: No faults asserted. 1: Fault(s) asserted.	0
6:3	RESERVED	RO	Reserved (ignore when read).	All zeros
2	RX_LNK_STAT	RO/LL	PCS receive link status. 0: Link down. 1: Link up.	1
1	LOW_PWR_ABILITY	RO	Low power mode support ability. 0: Not supported. 1: Supported.	1
0	RESERVED	RO	Reserved (ignore when read).	0

Table 179. PCS_DEVID1: PCS Device Identifier 1 (3x0002)

Bit	Name	Access	Description	Default
15:0	DEV_ID_LSW	RO	Upper 16 bits of a 32-bit unique PCS device identifier. Bits 3-18 of the device manufacturer’s OUI.	0x0007

Table 180. PCS_DEVID2: PCS Device Identifier 2 (3x0003)

Bit	Name	Access	Description	Default
15:0	DEV_ID_MSW	RO	Lower 16 bits of a 32-bit unique PCS device identifier. Bits 19-24 of the device manufacturer’s OUI. Six-bit model number, and a four-bit revision number.	0x0400

Table 181. PCS_SPEED: PCS Speed Capability (3x0004)

Bit	Name	Access	Description	Default
15:1	RESERVED	RO	Reserved for future speeds (value always 0, writes ignored)	All zeros
0	RATE_ABILITY	RO	PCS rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	1

Table 182. PCS_DEVPKG1: PCS Devices in Package 1 (3x0005)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved.	All zeros
5	DTE_XS_PRES	RO	Indicates whether DTE XS is present in the package. 0: Not present. 1: Present.	0
4	PHY_XS_PRES	RO	Indicates whether PHY XS is present in the package (this bit depends upon the IOMODESEL pin setting). 0: Not present. 1: Present.	1
3	PCS_PRES	RO	Indicates whether PCS is present in the package. 0: Not present. 1: Present.	1
2	WIS_PRES	RO	Do not use this bit as the WIS presence indicator. Use 1x0005.2 or 2x0005.2 for that purpose.	0
1	PMD_PMA_PRES	RO	Indicates whether PMA/PMD is present in the package. 0: Not present. 1: Present.	1
0	CLS22_PRES	RO	Indicates whether Clause 22 registers are present in the package. 0: Not present. 1: Present.	0

Table 183. PCS_DEVPKG2: PCS Devices in Package 2 (3x0006)

Bit	Name	Access	Description	Default
15	VS2_PRES	RO	Vendor specific device 2 present 0: Not present 1: Present	0
14	VS1_PRES	RO	Vendor specific device 1 present 0: Not present 1: Present	0
13:0	RESERVED	RO	Reserved	All zeros

Table 184. PCS_CTRL2: PCS Control 2 (3x0007)

Bit	Name	Access	Description	Default
15:2	RESERVED	RO	Reserved	All zeros
1:0	PCS_MODE	RW	Indicates the PCS type selected 11: Reserved 10: 10GBASE-W PCS 01: Reserved 00: 10GBASE-R PCS	All zeros

Table 185. PCS_STAT2: PCS Status 2 (3x0008)

Bit	Name	Access	Description	Default
15:14	DEV_PRES	RO	Reflects the presence of a MMD responding at this address. 00: No device responding at this address. 01: No device responding at this address. 10: Device responding at this address. 11: No device responding at this address.	10
13:12	RESERVED	RO	Reserved.	All zeros
11	FAULT_TX	RO/LH	Indicates a fault condition on the transmit path. 0: No faults asserted. 1: Fault(s) asserted. Set error triggers with 3xE600.1. Linked to 1Ex9004.3. A read to either 1Ex9004.3 or 3x0008.11 clears both bits if a fault condition no longer exists.	0
10	FAULT_RX	RO/LH	Indicates a fault condition on the receive path. 0: No faults asserted. 1: Fault(s) asserted. Set error triggers with 3xE600.0. Linked to 1Ex9003.3. A read to either 1Ex9003.3 or 3x0008.10 clears both bits if a fault condition no longer exists.	0
9:3	RESERVED	RO	Reserved.	0
2	BASE_W_ABILITY	RO	Device capability to support 10GBASE-W. 0: Not capable. 1: Capable.	1
1	BASE_X_ABILITY	RO	Device capability to support 10GBASE-X. 0: Not capable. 1: Capable.	0
0	BASE_R_ABILITY	RO	Device capability to support 10GBASE-R. 0: Not capable. 1: Capable.	1

Table 186. PCS_PKGID1: PCS Package Identifier 1 (3x000E)

Bit	Name	Access	Description	Default
15:0	PKG_ID_MSW	RO	Upper 16 bits of a 32-bit unique PCS package identifier. Bits 3-18 of the device manufacturer's OUI.	0

Table 187. PCS_PKGID2: PCS Package Identifier 2 (3x000F)

Bit	Name	Access	Description	Default
15:0	PKG_ID_LSW	RO	Lower 16 bits of a 32-bit unique PCS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0

Table 188. PCS_10GBASEX_STAT: PCS 10G BASE-X Status (3x0018)

Bit	Name	Access	Description	Default
15:0	BASE_X_STAT	RO	This device does not implement 10GBASE-X.	All zeros

Table 189. PCS_10GBASEX_CTRL: PCS 10G BASE-X Control (3x0019)

Bit	Name	Access	Description	Default
15:0	BASE_X_CTRL	RO	This device does not implement 10GBASE-X.	All zeros

Table 190. PCS_10GBASER_STAT1: PCS 10G BASE-R Status 1 (3x0020)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved.	All zeros
12	BASE_R_RXLCK_STAT	RO	10GBASE-R receive link status. This does not apply during PCS pattern testing. 0: Link down 1: Link up	0
11:3	RESERVED	RO	Reserved.	All zeros
2	PRBS31_ABILITY	RO	PCS PRBS31 pattern test capability. 0: Not capable. 1: Capable.	1
1	HIGH_BER	RO	10GBASE-R PCS high BER status. This does not apply during PCS pattern testing. 0: High BER deasserted. 1: High BER asserted.	0

Table 190. PCS_10GBASER_STAT1: PCS 10G BASE-R Status 1 (3x0020)

Bit	Name	Access	Description	Default
0	BLOCK_LOCK	RO	10GBASE-R PCS block lock status. This does not apply during PCS pattern testing. 0: Not locked. 1: Locked.	0

Table 191. PCS_10GBASER_STAT2: PCS 10G BASE-R Status 2 (3x0021)

Bit	Name	Access	Description	Default
15	BLOCK_LOCK_LATCHED	RO/LL	Latched block lock status. 0: 10GBASE-R PCS does not have block lock. 1: 10GBASE-R PCS has block lock.	1
14	HIGH_BER_LATCHED	RO/LH	Latched high BER status. 0: 10GBASE-R PCS has not reported a high BER. 1: 10GBASE-R PCS has reported a high BER.	0
13:8	BER_CNT	ROCR	Saturating (non-rollover) clear on read BER counter. This does not apply during PCS pattern testing.	All zeros
7:0	ERR_BLK_CNT	ROCR	Saturating (non-rollover) clear on read errored block counter. This does not apply during PCS pattern testing.	All zeros

Table 192. PCS_SEEDA3: PCS Test Pattern Seed A 3 (3x0022)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDA_15_0	RW	Bits 15:0 of the 58-bit seed A test pattern. Used during PCS pseudo-random test.	All zeros

Table 193. PCS_SEEDA2: PCS Test Pattern Seed A 2 (3x0023)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDA_31_16	RW	Bits 31:16 of the 58-bit seed A test pattern. Used during PCS pseudo-random test.	0

Table 194. PCS_SEEDA1: PCS Test Pattern Seed A 1 (3x0024)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDA_47_32	RW	Bits 47:32 of the 58-bit seed A test pattern. Used during PCS pseudo-random test.	0

Table 195. PCS_SEEDA0: PCS Test Pattern Seed A 0 (3x0025)

Bit	Name	Access	Description	Default
15:10	RESERVED	RO	Reserved	0
9:0	TSTPAT_SEEDA_57_48	RW	Bits 57:48 of the 58-bit seed A test pattern. Used during PCS pseudo-random test.	0

Table 196. PCS_SEEDB3: PCS Test Pattern Seed B 3 (3x0026)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDB_15_0	RW	Bits 15:0 of the 58-bit seed B test pattern. Used during PCS pseudo-random test.	0

Table 197. PCS_SEEDB2: PCS Test Pattern Seed B 2 (3x0027)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDB_31_16	RW	Bits 31:16 of the 58-bit seed B test pattern. Used during PCS pseudo-random test.	All zeros

Table 198. PCS_SEEDB1: PCS Test Pattern Seed B 1 (3x0028)

Bit	Name	Access	Description	Default
15:0	TSTPAT_SEEDB_47_32	RW	Bits 47:32 of the 58-bit seed B test pattern. Used during PCS pseudo-random test.	All zeros

Table 199. PCS_SEEDB0: PCS Test Pattern Seed B 0 (3x0029)

Bit	Name	Access	Description	Default
15:10	RESERVED	RO	Reserved	All zeros
9:0	TSTPAT_SEEDB_57_48	RW	Bits 57:48 of the 58-bit seed B test pattern. Used during PCS pseudo-random test.	All zeros

Table 200. PCS_TSTPAT_CTRL: PCS Test Pattern Control (3x002A)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved	All zeros
5	PCS_PRBS31_ANA	RW	Enable PRBS31 test pattern analysis 0: Disable 1: Enable	0
4	PCS_PRBS31_GEN	RW	Enable PRBS31 test pattern generation 0: Disable 1: Enable	0

Table 200. PCS_TSTPAT_CTRL: PCS Test Pattern Control (3x002A) *(continued)*

Bit	Name	Access	Description	Default
3	PCS_TSTPAT_GEN	RW	Enable PCS test pattern generator 0: Disable 1: Enable	0
2	PCS_TSTPAT_ANA	RW	Enable PCS test pattern analyzer 0: Disable 1: Enable	0
1	PCS_TSTPAT_SEL	RW	Select which test pattern to be used during the PCS_TSTPAT_GEN/ANA 0: Pseudo-Random 1: Square Wave (generation only)	0
0	PCS_TSTDAT_SEL	RW	Data to be sent during the pseudo-random pattern test after the loading of seed A or seed B 0: 64-bit encoding for 2 local fault ordered sets 1: 64 zeros	0

Table 201. PCS_TSTPAT_CNT: PCS Test Pattern Error Counter (3x002B)

Bit	Name	Access	Description	Default
15:0	Test error counter	ROCR	Clear on read test pattern error counter. A 32-bit version of this counter is available in 3x8007-3x8008. This counter is a saturating counter. **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	All zeros

Table 202. PCS_USRPAT0: PCS User Test Pattern 0 (3x8000)

Bit	Name	Access	Description	Default
15:0	TSTPAT_USR_15_0	RW	Bits 15:0 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudo-random testing. Active when 3x8005.0 is asserted.	All zeros

Table 203. PCS_USRPAT1: PCS User Test Pattern 1 (3x8001)

Bit	Name	Access	Description	Default
15:0	TSTPAT_USR_31_16	RW	Bits 31:16 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudo-random testing. Active when 3x8005.0 is asserted.	All zeros

Table 204. PCS_USRPAT2: PCS User Test Pattern 2 (3x8002)

Bit	Name	Access	Description	Default
15:0	TSTPAT_USR_47_32	RW	Bits 47:22 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudo-random testing. Active when 3x8005.0 is asserted.	All zeros

Table 205. PCS_USRPAT3: PCS User Test Pattern 3 (3x8003)

Bit	Name	Access	Description	Default
15:0	TSTPAT_USR_63_48	RW	Bits 63:48 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudo-random testing. Active when 3x8005.0 is asserted	All zeros

Table 206. PCS_SQPW_CTRL: PCS Square Wave Pulse Width Control (3x8004)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	All zeros
3:0	SQ_WV_PW	RW	Pulse width of the generated square wave test pattern. This is the number of consecutive low bit times and the number of consecutive high bit times. Only values of 4 through 11 bits are valid.	All zeros

Table 207. PCS_CFG1: PCS Configuration 1 (3x8005)

Bit	Name	Access	Description	Default
15:11	RESERVED	RO	Reserved	All zeros
10	DSCR_DIS	RW	Disable Rx block descrambler 0: Enable 1: Disable	0
9	SCR_DIS	RW	Disable Tx block scrambler 0: Enable 1: Disable	0
8	PCS_XGMII_SRC	RW	Select between XGXS and external XGMII as the source of data for the PCS 0: XGXS is XGMII source 1: External XGMII source	0
7	PHYXS_XGMII_SRC	RW	Select between PCS and external XGMII as the source of data for the XGXS 0: PCS is XGMII source 1: External XGMII source	0
6	XGMII_OE	RW	External XGMII output enable 0: Disable 1: Enable	0

Table 207. PCS_CFG1: PCS Configuration 1 (3x8005) *(continued)*

Bit	Name	Access	Description	Default
5	BLK_CHK_RX_DIS	RW	Disable block error generation when an invalid block sequence is encountered in the Rx path 0: Enable 1: Disable	0
4	BLK_CHK_TX_DIS	RW	Disable block error generation when an invalid block sequence is encountered in the Tx path 0: Enable 1: Disable	0
3	LPBK_F	RW	Enables loopback F (PCS network loopback) 0: Disable 1: Enable	0
2	LPBK_E	RW	Enable loopback E (PCS system loopback) 0: Disable 1: Enable	0
1	RESERVED	RO	Reserved	0
0	USR_PAT_EN	RW	Select the user test pattern in 3x8000 to 3x8003 for psuedo-random test 0: Standard test pattern 1: User test pattern	0

Table 208. PCS_ERR_CNT0: PCS Test Error Counter 0 (3x8007)

Bit	Name	Access	Description	Default
15:0	TSTPAT_ERR_CNT0	RO	Lower 16 bits of the 32-bit test error counter. This counter is a saturating (non-rollover) counter that is cleared upon a consecutive read to 3x8007 and 3x8008. The contents of this register are identical to 3x002B.	All zeros

Table 209. PCS_ERR_CNT1: PCS Test Error Counter 1 (3x8008)

Bit	Name	Access	Description	Default
15:0	TSTPAT_ERR_CNT1	RO	Upper 16 bits of the 32-bit test error counter. This counter is a saturating (non-rollover) counter that is cleared upon a consecutive read to 3x8007 and 3x8008.	All zeros

Table 210. PCS_FIFO_STAT: PCS FIFO Status (3x8009)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	0
3	RX_OFLOW	RO/LH	Rx FIFO overflow status 0: Normal operation 1: Overflow occurred	0

Table 210. PCS_FIFO_STAT: PCS FIFO Status (3x8009) *(continued)*

Bit	Name	Access	Description	Default
2	RX_UFLOW	RO/LH	Rx FIFO underflow status 0: Normal operation 1: Underflow occurred	0
1	TX_OFLOW	RO/LH	Tx FIFO overflow status 0: Normal operation 1: Overflow occurred	0
0	TX_UFLOW	RO/LH	Tx FIFO underflow status 0: Normal operation 1: Underflow occurred	0

Table 211. PCS_TX_ADD_CNT: PCS Tx FIFO Added Idles Counter (3x800C)

Bit	Name	Access	Description	Default
15:0	TX_IDLE_ADD	ROCR	Tx FIFO idle group (||I||) add counter. Increments once for each idle group added to the transmit path for rate compensation.	0

Table 212. PCS_TX_DROP_CNT: PCS Tx FIFO Dropped Idles Counter (3x800D)

Bit	Name	Access	Description	Default
15:0	TX_IDLE_DROP	ROCR	Tx FIFO idle group (||I||) drop count. Increments once for each idle group dropped from the transmit path for rate compensation.	0

Table 213. PCS_RX_ADD_CNT: PCS Rx FIFO Added Idles Counter (3x800E)

Bit	Name	Access	Description	Default
15:0	RX_IDLE_ADD	ROCR	Rx FIFO idle group (||I||) add count. Increments once for each idle group added to the receive path for rate compensation.	All zeros

Table 214. PCS_RX_DROP_CNT: PCS Rx FIFO Dropped Idles Counter (3x800F)

Bit	Name	Access	Description	Default
15:0	RX_IDLE_DROP	ROCR	Rx FIFO idle group (||I||) drop count. Increments once for each idle group dropped from the receive path for rate compensation.	All zeros

Table 215. PCS_TX_SEQERR_CNT: PCS Tx Sequencing Error Counter (3x8010)

Bit	Name	Access	Description	Default
15:0	TX_SEQ_ERR_CNT	ROCR	Tx block sequence error count. Increments once for each Tx block sequence error. Non-saturating (rollover) counter.	All zeros

Table 216. PCS_RX_SEQERR_CNT: PCS Rx Sequencing Error Counter (3x8011)

Bit	Name	Access	Description	Default
15:0	RX_SEQ_ERR_CNT	ROCR	Increments once for each Rx block sequence error	All zeros

Table 217. PCS_TX_BLKERR_CNT: PCS Tx Block Encode Error Counter (3x8012)

Bit	Name	Access	Description	Default
15:0	TX_BLKENC_ERR_CNT	ROCR	Increments once for each Tx block encoding error	All zeros

Table 218. PCS_RX_BLKERR_CNT: PCS Rx Block Decode Error Counter (3x8013)

Bit	Name	Access	Description	Default
15:0	RX_BLKDEC_ERR_CNT	ROCR	Increments once for each Rx block decoding error	All zeros

Table 219. PCS_TX_CHARERR_CNT: PCS Tx Char Encode Error Counter (3x8014)

Bit	Name	Access	Description	Default
15:0	TX_CHARENC_ERR_CNT	ROCR	Increments once for each Tx character encoding error	All zeros

Table 220. PCS_RX_CHARERR_CNT: PCS Rx Char Decode Error Counter (3x8015)

Bit	Name	Access	Description	Default
15:0	RX_CHARDEC_ERR_CNT	ROCR	Increments once for each Rx character decoding error	All zeros

Table 221. PCS_CFG2: PCS Configuration 2 (3xE600)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved	All zeros

Table 221. PCS_CFG2: PCS Configuration 2 (3xE600) *(continued)*

Bit	Name	Access	Description	Default
2	PR58_INV_DIS	RW	Disable the periodic inversion of the psuedo-random test pattern for both transmit and receive paths 0: Enable 1: Disable	0
1	FAULT_TX_SEL	RW	Select error types to trigger a transmit fault 0: FIFO over/underflow condition only 1: Character encoding error, block encoding error, FIFO over/underflow condition	0
0	RX_STAT_SEL	RW	Select contributing logic for receive link status 0: BLOCK_LOCK = 1 1: BLOCK_LOCK = 1 or HIGH_BER = 1	0

Table 222. E-PCS_CTRL1: E-PCS Control 1 (3xE601)

Bit	Name	Access	Description	Default
15:11	RESERVED	RO	Reserved.	All zeros
10:7	SUP_CHAN	RW	Static supervisory channel bits. SUP_MODE must be set to use these overriding bits.	All zeros
6	SUP_MODE	RW	Select supervisory bits to be inserted into the E-PCS frame. 0: TX_MSG. 1: Static SUP_CHAN.	0
5	RESERVED	RW	Factory test only (do not modify this bit group).	0
4	RESERVED	RW	Factory test only (do not modify this bit group).	0
3	RESERVED	RW	Factory test only (do not modify this bit group).	0
2	CORR_ENA	RW	Enable error correction. 0: Disable. 1: Enable.	1
1	RESERVED	RO	Factory test only. Do not modify this bit.	0
0	TX_MSG_RDY	RW	Assert this bit to latch a new TX_MSG (3xE60A-E611) into the transmit buffer. The TX_MSG repeats transmission until this bit is asserted again. 0: Transmit previous TX_MSG. 1: Transmit new TX_MSG.	0

Table 223. EPCS_LSM_CTRL1: E-PCS Link State Machine Control 1 (3xE602)

Bit	Name	Access	Description	Default
15:7	RESERVED	RO	Reserved	0
6	LSM_TX_ENA	RW	Transmit link state machine enable 0: Disable 1: Enable	0
5	LSM_TX_RST	RW	Transmit link state machine restart 0: No action 1: Restart LSM	0

Table 223. EPCS_LSM_CTRL1: E-PCS Link State Machine Control 1 (3xE602)

Bit	Name	Access	Description	Default
4	LSM_TX_HOLD	RW	Transmit link state machine hold 0: Not hold LSM 1: Hold LSM	0
3:0	LSM_RX_R1	RW	Receive link state machine R1 parameter	1111

Table 224. EPCS_LSM_CTRL2: E-PCS Link State Machine Control 2 (3xE603)

Bit	Name	Access	Description	Default
15:0	LSM_TX_D1	RW	Transmit link state machine time-out, D1 parameter	0

Table 225. EPCS_STAT1: E-PCS Status 1 (3xE604)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	0
7:5	LSM_TX_STATE	RO	Current Tx LSM state	0
4	LSM_RX_STAT	RO	Status of Rx framing 0: E-PCS is not framed 1: E-PCS is framed	0
3	RX_MSG_RDY	ROCR	Notification that a new HDLC message has been received 0: No change to HDLC frame 1: New HDLC frame received	0
2:0	LSM_RX_STATE	RO	Current Rx LSM state	0

Table 226. EPCS_CORR_CNT: E-PCS Corrected FEC Error Counter (3xE605)

Bit	Name	Access	Description	Default
15:0	CORR_ERR_CNT	RO	Count of corrected E-PCS frames over the previous second. Counter is reset every second. Counter is not cumulative and does not roll over. Saturating (non-rollover) counter is cleared by assertion of CLR_CNT. Cleared when 3xE601.1 is set.	All zeros

Table 227. EPCS_UCORR_CNT: E-PCS UnCorrected FEC Error Counter (3xE606)

Bit	Name	Access	Description	Default
15:0	UNCORR_ERR_CNT	RO	Count of corrected E-PCS frames over the previous second. Counter is reset every second. Counter is not cumulative and does not roll over. Saturating (non-rollover) counter is cleared by assertion of CLR_CNT. Cleared when 3xE601.1 is set.	All zeros

Table 228. EPCS_TXMSG: E-PCS Tx Message (3xE60A-E611)

Bit	Name	Access	Description	Default
15:0	TX_MSG	RW	128-bit message for in-band transmission to the far end link partner. The 3xE60A is the MSW while 3xE611 is the LSW.	All zeros

Table 229. EPCS_RXMSG: E-PCS Rx Message (3xE612-E619)

Bit	Name	Access	Description	Default
15:0	RX_MSG	RO	128-bit message received from the far end link partner. Frame delineation is not supported, thus higher level software must determine the MSW.	All zeros

Table 230. Factory Test Register (3xE61A)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
2	RESERVED	RW	Factory test only (do not modify this bit group)	0
1	RESERVED	RW	Factory test only (do not modify this bit group)	0
0	RESERVED	RW	Factory test only (do not modify this bit group)	0

Table 231. Factory Test Register (3xE61B)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Factory test only (do not modify this bit group)	0x10
7:0	RESERVED	RW	Factory test only (do not modify this bit group)	0x14

Table 232. Factory Test Register (3xE61C)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 233. Factory Test Register (3xE61D)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
4:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

4.4 Device 4: PHY-XS Registers

The following tables provide settings for the registers related to the PHY-XS.

Table 234. PHYXS_CTRL1: PHY XS Control 1 (4x0000)

Bit	Name	Access	Description	Default
15	SOFT_RST	RWSC	Reset all MMDs 0: Normal operation. 1: Reset	0
14	LPBK_A	RW	Enable PHY XS network loopback (loopback A) 0: Disable 1: Enable	0
13	SPEED_SEL_A	RO	PHY XS speed capability 0: Unspecified 1: Operates at 10 Gbps or above	1
12	RESERVED	RO	Reserved (value always 0, writes ignored)	0
11	LOW_PWR	RW	PHY XS low power mode control 0: Normal operation 1: Low Power	0
10:7	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
6	SPEED_SEL_B	RO	PHY XS Speed capability 0: Unspecified 1: Operates at 10 Gbps or above	1
5:2	SPEED_SEL_C	RO	PHY XS speed selection 1xxx: Reserved x1xx: Reserved xx1x: Reserved 0001: Reserved 0000: 10 Gbps	All zeros
1:0	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros

Table 235. PHYXS_STAT1: PHY XS Status1 (4x0001)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved (ignore when read)	All zeros
7	FAULT	RO	PHY XS fault status. Asserted when either the PHY XS FAULT_RX(4x0008.10) or PHY XS FAULT_TX (4x0008.11) is asserted. 0: No faults asserted 1: Fault(s) asserted	0
6:3	RESERVED	RO	Reserved (ignore when read)	All zeros
2	TX_LNK_STAT	RO/LL	PHY XS transmit link status 0: PHY XS transmit link is down (4x0018.12 = 0) 1: PHY XS transmit link is up (4x0018.12 = 1)	1
1	LOW_PWR_ABILITY	RO	Low power mode support ability 0: Not supported 1: Supported	1
0	RESERVED	RO	Reserved (ignore when read)	0

Table 236. PHYXS_DEVID1: PHY XS Device Identifier 1 (4x0002)

Bit	Name	Access	Description	Default
15:0	DEV_ID_LSW	RO	Upper 16 bits of a 32-bit unique PHY XS device identifier. Bits 3-18 of the device manufacturer's OUI. Device identifier bits 31:16.	0x0007

Table 237. PHYXS_DEVID2: PHY XS Device Identifier 2 (4x0003)

Bit	Name	Access	Description	Default
15:0	DEV_ID_MSW	RO	Lower 16 bits of a 32-bit unique PHY XS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number. Device identifier bits 15:0.	0x0400

Table 238. PHYXS_SPEED: PHY XS Speed Capability (4x0004)

Bit	Name	Access	Description	Default
15:1	RESERVED	RO	Reserved for future speeds (value always 0, writes ignored)	All zeros
0	RATE_ABILITY	RO	PHY XS rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	1

Table 239. PHYXS_DEVPKG1: PHY XS Devices in Package 1 (4x0005)

Bit	Name	Access	Description	Default
15:6	RESERVED	RO	Reserved (ignore when read).	All zeros
5	DTE_XS_PRES	RO	Indicates whether device includes DTS XS. 0: Not present. 1: Present.	0
4	PHY_XS_PRES	RO	Indicates whether device includes PHY XS. 0: Not present. 1: Present.	1
3	PCS_PRES	RO	Indicates whether PCS is present in the package. 0: Not present. 1: Present.	1
2	WIS_PRES	RO	Do not use this bit as the WIS presence indicator. Use 1x0005.2 or 2x0005.2 for that purpose.	0
1	PMD_PMA_PRES	RO	Indicates whether PMA/PMD is present in the package. 0: Not present. 1: Present.	1

Table 239. PHYXS_DEVPKG1: PHY XS Devices in Package 1 (4x0005) *(continued)*

Bit	Name	Access	Description	Default
0	CLS22_PRES	RO	Indicates whether Clause 22 registers are present in the package. 0: Not present. 1: Present.	0

Table 240. PHYXS_DEVPKG2: PHY XS Devices in Package 2 (4x0006)

Bit	Name	Access	Description	Default
15	VS2_PRES	RO	Vendor specific device 2 present 0: Not present 1: Present	0
14	VS1_PRES	RO	Vendor specific device 1 present 0: Not present 1: Present	0
13:0	RESERVED	RO	Reserved (ignore when read)	0

Table 241. PHYXS_STAT2: PHY XS Status 2 (4x0008)

Bit	Name	Access	Description	Default
15:14	DEV_PRES	RO	Reflects the presence of a MMD responding at this address 10: Device responding at this address 11: No device responding at this address 10: No device responding at this address 00: No device responding at this address	10
13:12	RESERVED	RO	Reserved (ignore when read)	All zeros
11	FAULT_TX	RO/LH	Indicates a fault condition on the transmit path. 0: No fault condition on transmit path. (XGXS lanes are aligned, 4x0018.12 = 1.) 1: Fault condition on transmit path. (XGXS lanes are not aligned, 4x0018.12 = 0.) Linked to 1Ex9004.0. Read to either register clears both bits if fault condition no longer exists.	0
10	FAULT_RX	RO/LH	Indicates a fault condition on the receive path 0: No fault condition on receive path. (XAUI_LOL = 0). 1: Fault condition on receive path. XAUI loss of lock (XAUI_LOL = 1). Linked to 1Ex9003.0. Read to either register clears both bits if fault condition no longer exists.	0
9:0	RESERVED	RO	Reserved (ignore when read).	All zeros

Table 242. PHYXS_STAT3: PHY XS Status 3 (4x0018)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved (ignore when read)	All zeros

Table 242. PHYXS_STAT3: PHY XS Status 3 (4x0018) *(continued)*

Bit	Name	Access	Description	Default
12	LANES_ALIGNED	RO	PHY XGXS lane alignment status 0: PHY XS transmit lanes are not aligned 1: PHY XS transmit lanes are aligned	0
11	PATT_ABILITY	RO	PHY XGXS test pattern generation ability 0: PHY XS is not able to generate test patterns 1: PHY XS is able to generate test patterns	1
10	LPBK_ABILITY	RO	PHY XGXS loopback ability 0: PHY XS does not have the ability to perform a loopback function 1: PHY XS has the ability to perform a loopback function	1
9:4	RESERVED	RO	Reserved (ignore when read)	All zeros
3	LANE3_SYNC	RO	PHY XGXS lane 3 synchronization status 0: Not synchronized 1: Synchronized	0
2	LANE2_SYNC	RO	PHY XGXS lane 2 synchronization status 0: Not synchronized 1: Synchronized	0
1	LANE1_SYNC	RO	PHY XGXS lane 1 synchronization status 0: Not synchronized 1: Synchronized	0
0	LANE0_SYNC	RO	PHY XGXS lane 0 synchronization status 0: Not synchronized 1: Synchronized	0

Table 243. PHYXS_TSTCTRL1: PHY XGXS Test Control 1 (4x0019)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved (value always 0, writes ignored)	All zeros
2	TST_PATT_CHK_ENA	RW	PHYXS test pattern checker enable 0: Disable 1: Enable	0
1:0	TST_PATT_CHK_SEL	RW	PHYXS test pattern checker pattern select 111: 2^7 PRBS Pattern 110: Fibre Channel CJPAT 101: Continuous jitter test pattern 100: Continuous random test pattern 011: Disable pattern generator 010: Mixed frequency test pattern 001: Low frequency test pattern 000: High frequency test pattern **Note** The MSB is 4x8000.3	All zeros

Table 244. PHYXS_TSTCTRL2: PHY XS Test Control 2 (4x8000)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros

Table 244. PHYXS_TSTCTRL2: PHY XS Test Control 2 (4x8000) *(continued)*

Bit	Name	Access	Description	Default
4	TST_PATT_GEN_ENA	RW	PHYXS test pattern generator enable 0: Disable 1: Enable	0
3	TST_PATT_MODE	RW	Transmit test pattern checker select bit 2 Use with register 4x0019.1:0	0
2:0	TST_PATT_GEN_SEL	RW	PHYXS test pattern generator select 111: 2^7 PRBS pattern 110: Fibre Channel CJPAT 101: Continuous jitter test pattern 100: Continuous random test pattern 011: Disable pattern generator 010: Mixed frequency test pattern 001: Low frequency test pattern 000: High frequency test pattern	011

Table 245. PHYXS_TSTSTAT: PHY XS Test Pattern Check Status (4x8001)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	All zeros
3	LANE3_PATT_CHK	RO	Lane 3 test pattern check result 0: Pattern check fail 1: Pattern check pass	0
2	LANE2_PATT_CHK	RO	Lane 2 test pattern check result 0: Pattern check fail 1: Pattern check pass	0
1	LANE1_PATT_CHK	RO	Lane 1 test pattern check result 0: Pattern check fail 1: Pattern check pass	0
0	LANE0_PATT_CHK	RO	Lane 0 test pattern check result 0: Pattern check fail 1: Pattern check pass	0

Table 246. PHYXS_CGERR_CTRL: PHY XS Code Group Error Control (4x8002)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	CG_ERR_CNT_CLR	RWSC	Clear code group error counter 0: Normal operation 1: Clear counter	0
3	CG_ERR_CNT_ENA	RW	Enable code group error counter 0: Disable 1: Enable	1

Table 246. PHYXS_CGERR_CTRL: PHY XS Code Group Error Control (4x8002)

Bit	Name	Access	Description	Default
2:0	CG_ERR_CNT_SEL	RW	Select code group error source 111: Reserved 110: Reserved 101: Reserved 100: Cumulative error count on all lanes 011: Error count on lane 3 010: Error count on lane 2 001: Error count on lane 1 000: Error count on lane 0	100

Table 247. PHYXS_CGERR_CNT0: PHY XS Code Group Error Counter 0 (LSW) (4x8003)

Bit	Name	Access	Description	Default
15:0	CG_ERR_CNT_LSW	RO	Code group error counter. Lower 16-bits of the saturating (non-rollover) counter.	All zeros

Table 248. PHYXS_CGERR_CNT0: PHY XS Code Group Error Counter 1 (MSW) (4x8004)

Bit	Name	Access	Description	Default
15:0	CG_ERR_CNT_MSW	RO	Code group error counter. Upper 16-bits of the saturating (non-rollover) counter.	All zeros

Table 249. PHYXS_RDERR_CTRL: PHY XS Disparity Error Counter Control (4x8005)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	RD_ERR_CNT_CLR	RWSC	Clear running disparity error counter 0: Normal operation 1: Clear counter	0
3	RD_ERR_CNT_ENA	RW	Enable running disparity error counter 0: Disable 1: Enable	1
2:0	RD_ERR_CNT_SEL	RW	Select running disparity error source 111: Reserved 110: Reserved 101: Reserved 100: Cumulative error count on all lanes 011: Error count on lane 3 010: Error count on lane 2 001: Error count on lane 1 000: Error count on lane 0	100

Table 250. PHYXS_RDERR_CNT0: PHY XS Disparity Error Counter 0 (LSW) (4x8006)

Bit	Name	Access	Description	Default
15:0	RD_ERR_CNT_LSW	RO	Running disparity error counter. Lower 16-bits of the saturating (non-rollover) counter.	All zeros

Table 251. PHYXS_RDERR_CNT0: PHY XS Disparity Error Counter 1 (MSW) (4x8007)

Bit	Name	Access	Description	Default
15:0	RD_ERR_CNT_MSW	RO	Running disparity error counter. Upper 16-bits of the saturating (non-rollover) counter.	All zeros

Table 252. PHYXS_FIFOERR_CTRL: PHY XS FIFO Error Control (4x8008)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	FIFOERR_CNT_CLR	RWSC	Clear FIFO underflow/overflow error counter 0: Normal operation 1: Clear counter	0
3	FIFOERR_CNT_ENA	RW	Enable FIFO underflow/overflow error counter 0: Disable 1: Enable	1
2:0	FIFOERR_CNT_SEL	RW	Select FIFO underflow/overflow error source 111: Reserved 110: Reserved 101: Reserved 100: Cumulative error count on all lanes 011: Error count on lane 3 010: Error count on lane 2 001: Error count on lane 1 000: Error count on lane 0	100

Table 253. PHYXS_FIFOERR_CNT0: PHY XS FIFO Error Counter 0 (LSW) (4x8009)

Bit	Name	Access	Description	Default
15:0	FIFOERR_CNT_LSW	RO	FIFO underflow/overflow error counter. Lower 16-bits of the saturating (non-rollover) counter.	All zeros

Table 254. PHYXS_FIFOERR_CNT1: PHY XS FIFO Error Counter 1 (LSW) (4x800A)

Bit	Name	Access	Description	Default
15:0	FIFOERR_CNT_MSW	RO	FIFO underflow/overflow error counter. Upper 16-bits of the saturating (non-rollover) counter.	All zeros

Table 255. PHYXS_TPERR_CTRL: PHY XS Test Pattern Error Counter Control (4x800B)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	TP_CNT_CLR	RWSC	Clear test pattern mismatch error counter 0: Normal operation 1: Clear counter	0
3	TP_CNT_ENA	RW	Test pattern mismatch error counter enable 0: Disable 1: Enable	1
2:0	TP_CNT_SEL	RW	Select test pattern mismatch error source 111: Reserved 110: Reserved 101: Reserved 100: Cumulative error count on all lanes 011: Error count on lane 3 010: Error count on lane 2 001: Error count on lane 1 000: Error count on lane 0	100

Table 256. PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 0 (LSW) (4x800C)

Bit	Name	Access	Description	Default
15:0	TP_CNT_LSW	RO	Test pattern mismatch error counter. Lower 16-bits of the saturating (non-rollover) counter. Saturating counter.	All zeros

Table 257. PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 1 (MSW) (4x800D)

Bit	Name	Access	Description	Default
15:0	TP_CNT_MSW	RO	Test pattern mismatch error counter. Upper 16-bits of the saturating (non-rollover) counter. Saturating counter.	All zeros

Table 258. PHYXS_XAUI_CTRL1: PHY XS XAUI Control 1 (4x800E)

Bit	Name	Access	Description	Default
15:14	RESERVED	RO	Reserved.	All zeros
13	LPBK_B	RW	Loopback B enable (PHY XS shallow system). 0: Disable. 1: Enable. High-speed transmitter outputs transmit data. Option to transmit all ones, all zeros, 0x00FF pattern, or XAUI data.	0
12	RX_FIFO_RST	RWSC	Reset PHY XS Rx path FIFOs. 0: Reset FIFOs. 1: Normal operation.	1
11	RESERVED	RO	Factory test only (do not modify this bit group).	1
10	RESERVED	RO	Factory test only (do not modify this bit group).	0
9	RESERVED	RO	Factory test only (do not modify this bit group).	0
8:5	RX_SQUELCH_XAUI	RW	Force receive XAUI data to zero (bit 8 corresponds to lane 3, and bit 5 corresponds to lane 0). 0: Normal operation. 1: Force data to zero.	All zeros
4	RESERVED	RO	Factory test only (do not modify this bit group).	0
3	RESERVED	RW	Factory test only (do not modify this bit group).	0
2	RESERVED	RO	Reserved.	0
1	RESERVED	RO	Reserved.	0
0	RESERVED	RW	Factory test only (do not modify this bit group).	0

Table 259. PHYXS_XAUI_CTRL2: PHY XS XAUI Control 2 (4x800F)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	All zeros
12	RESERVED	RW	Factory test only (do not modify this bit group)	0
11	RESERVED	RW	Factory test only (do not modify this bit group)	0
10	RX_LANE_SWAP	RW	Swaps receive lane 0 with lane 3 and lane 1 with lane 2 0: Enable 1: Disable	1
9	TX_LANE_SWAP	RW	Swaps transmit lane 0 with lane 3 and lane 1 with lane 2 0: Enable 1: Disable	1
8	RESERVED	RW	Factory test only (do not modify this bit group)	0
7	RESERVED	RW	Factory test only (do not modify this bit group)	0
6	RX_INV	RW	Disable XAUI input (receive) data invert 0: Enable 1: Disable	1

Table 259. PHYXS_XAUI_CTRL2: PHY XS XAUI Control 2 (4x800F) *(continued)*

Bit	Name	Access	Description	Default
5	TX_INV	RW	Disable XAUI output (transmit) data invert 0: Enable 1: Disable	1
4	RESERVED	RO	Reserved	0
3	RESERVED	RW	Factory test only (do not modify this bit group)	0
2	LPBK_C	RW	Enable loopback C (XAUI side loopback at XGMII interface) 0: Disable 1: Enable	0
1	LPBK_D	RW	Enable loopback D (XFI side loopback at XGMII interface) 0: Disable 1: Enable	0
0	LPBK_B_76	RW	Must be 0 (legacy bit from the VSC8476)	0

Table 260. PHYXS_RXEQ_CTRL: PHY XS XAUI Rx Equalization Control (4x8010)

Bit	Name	Access	Description	Default
15:12	LANE0_EQ	RW	Equalization setting for XAUI input lane 0 0000: 0 dB 0001: 1.41 dB 0010: 2.24 dB 0011: 2.83 dB 0101: 4.48 dB 0110: 5.39 dB 0111: 6.07 dB 1001: 6.18 dB 1010: 7.08 dB 1011: 7.79 dB 1101: 9.96 dB 1110: 10.84 dB 1111: 11.55 dB	All zeros
11:8	LANE1_EQ	RW	Equalization setting for XAUI input lane 1 Refer to bits [15:12] for settings	All zeros
7:4	LANE2_EQ	RW	Equalization setting for XAUI input lane 2 Refer to bits [15:12] for settings	All zeros
3:0	LANE3_EQ	RW	Equalization setting for XAUI input lane 3 Refer to bits [15:12] for settings	All zeros

Table 261. PHYXS_TXPE_CTRL: PHY XS XAUI Tx Pre-emphasis Control (4x8011)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved.	0
14:13	LANE0_PE	RW	Pre-emphasis setting for XAUI output lane 0. 00: 0 dB. 01: ~2.5 dB. 10: ~6 dB. 11: ~12 dB.	All zeros

Table 261. PHYXS_TXPE_CTRL: PHY XS XAUI Tx Pre-emphasis Control (4x8011)

Bit	Name	Access	Description	Default
12	RESERVED	RO	Reserved.	0
11:10	LANE1_PE	RW	Pre-emphasis setting for XAUI output lane 1. Refer to bits [14:13] for settings.	All zeros
9	RESERVED	RO	Reserved.	0
8:7	LANE2_PE	RW	Pre-emphasis setting for XAUI output lane 2. Refer to bits [14:13] for settings.	All zeros
6	RESERVED	RO	Reserved.	0
5:4	LANE3_PE	RW	Pre-emphasis setting for XAUI output lane 3. Refer to bits [14:13] for settings.	All zeros
3:2	LOS_THRES	RW	LOS threshold setting. 11: 80 mV to 205 mV differential peak-to-peak. 10: 70 mV to 195 mV differential peak-to-peak. 01: 60 mV to 185 mV differential peak-to-peak. 00: 50 mV to 175 mV differential peak-to-peak.	All zeros
1	HS_ENA	RW	Enable XAUI output high swing mode. 0: Disable. 1: Enable.	0
0	RESERVED	RO	Reserved.	0

Table 262. PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012)

Bit	Name	Access	Description	Default
15:7	RESERVED	RO	Reserved	All zeros
6	GLBL_SYNC	RO	PHY XS code group synchronization status 0: At least one lane is not in sync 1: All lanes are in sync	0
5	XS_LOL	RO	PHY XS PLL loss of lock 0: PLL in lock 1: PLL loss of lock **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0
4	RESERVED	RO	Reserved	0
3	LANE3_LOS	RO	Loss of signal status for lane 3 XAUI input 0: Lane 3 signal present 1: Lane 3 loss of signal **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0
2	LANE2_LOS	RO	Loss of signal status for lane 2 XAUI input 0: Lane 2 signal present 1: Lane 2 loss of signal **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0

Table 262. PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012)

Bit	Name	Access	Description	Default
1	LANE1_LOS	RO	Loss of signal status for lane 1 XAUI input 0: Lane 1 signal present 1: Lane 1 loss of signal **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0
0	LANE0_LOS	RO	Loss of signal status for lane 0 XAUI input 0: Lane 0 signal present 1: Lane 0 loss of signal **Note** There is an errata item associated with this register. For more information, see "Errata," page 250.	0

Table 263. PHYXS_RXSD_STAT: PHY XS Rx Signal Detect Status (4xE600)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Factory test only (do not modify this bit group)	0x0001

Table 264. Factory Test Register (4xE601)

Bit	Name	Access	Description	Default
15:9	RESERVED	RO	Reserved	All zeros
8	RESERVED	RW	Factory test only (do not modify this bit group)	0
7:0	RESERVED	RW	Factory test only (do not modify this bit group)	0x01

Table 265. PHYXS_TXPD_CTRL: PHY XS XAUI Tx Power Down Control (4xE602)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	0
14	LANE3_TX_PD	RW	Power down XAUI lane 3 from the system host into the VSC8486 device 0: Powered up 1: Powered down Not changed with lane swap control (4x800F)	0
13	LANE2_TX_PD	RW	Power down XAUI lane 2 from the system host into the VSC8486 device 0: Powered up 1: Powered down Not changed with lane swap control (4x800F)	0
12	LANE1_TX_PD	RW	Power down XAUI lane 1 from the system host into the VSC8486 device 0: Powered up 1: Powered down Not changed with lane swap control (4x800F)	0

Table 265. PHYXS_TXPD_CTRL: PHY XS XAUI Tx Power Down Control (4xE602)

Bit	Name	Access	Description	Default
11	LANE0_TX_PD	RW	Power down XAUI lane 0 from the system host into the VSC8486 device 0: Powered up 1: Powered down Not changed with lane swap control (4x800F)	0
10:9	LPBK_B_CLK	RW	Select which of the four recovered clocks will be used for loopback B (PHY XS shallow system loopback) 11: Lane 3 10: Lane 2 01: Lane 1 00: Lane 0	All zeros
8	LPBK_B_CLKSEL	RW	Enable automatic clock selection for loopback B and select which of the four recovered XAUI receive lane clocks will be used to retime the transmit data 0: Manual select (see bits 10:9) 1: Auto select	1
7:6	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
5:4	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
3:2	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros
1:0	RESERVED	RO	Factory test only (do not modify this bit group)	All zeros

Table 266. PHYXS_RXPD_CTRL: PHY XS XAUI Rx Power Down Control (4xE603)

Bit	Name	Access	Description	Default
15:10	RESERVED	RO	Reserved	All zeros
9	JTAG_CTRL	RW	Disable level shifter at XAUI input receiver 0: Enable 1: Disable	0
8	SYNC_MODE	RW	Selects PHY XS serializer sync mode 0: Fast sync 1: Slow sync	1
7	LANE3_RX_PD	RW	Power down XAUI lane 3 from the VSC8486 device into the system host 0: Powered up 1: Powered down	0
6	LANE2_RX_PD	RW	Power down XAUI lane 2 from the VSC8486 device into the system host 0: Powered up 1: Powered down	0
5	LANE1_RX_PD	RW	Power down XAUI lane 1 from the VSC8486 device into the system host 0: Powered up 1: Powered down	0
4	LANE0_RX_PD	RW	Power down XAUI lane 0 from the VSC8486 device into the system host 0: Powered up 1: Powered down	0

Table 266. PHYXS_RXPD_CTRL: PHY XS XAUI Rx Power Down Control (4xE603)

Bit	Name	Access	Description	Default
3	LANE3_RX_SQU	RW	Force to zero PHY XS Rx lane 3 high-speed data that is output from the VSC8486 device 0: Output normal 1: Output squelched	0
2	LANE2_RX_SQU	RW	Force to zero PHY XS Rx lane 2 high-speed data that is output from the VSC8486 device 0: Output normal 1: Output squelched	0
1	LANE1_RX_SQU	RW	Force to zero PHY XS Rx lane 1 high-speed data that is output from the VSC8486 device 0: Output normal 1: Output squelched	0
0	LANE0_RX_SQU	RW	Force to zero PHY XS Rx lane 0 high-speed data that is output from the VSC8486 device 0: Output normal 1: Output squelched	0

Table 267. Factory Test Register (4xE610)

Bit	Name	Access	Description	Default
15:4	RESERVED	RO	Reserved	All zeros
3:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

4.5 Device 30 (0x1E): NVR and DOM Registers

The following tables provide settings for the registers related to the NVR and DOM.

Table 268. STW_CTRL1: STW Control 1 (1Ex8000)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	All zeros
12:9	RESERVED	RW	Reserved	All zeros
8	STW_MODE	RW	Select the STW controller mode (manual mode is controlled via STW_CTRL2) 0: Automatic 1: Manual	0
7:6	RESERVED	RO	Reserved	All zeros
5	STW_CMD	RW	Command type for automatic mode 0: Read 1: Write	0
4	RESERVED	RO	Reserved	0
3:2	STW_CMD_STATUS	RO	Command status (these bits clear on read, but if a condition persists, the bits maintain their value) 00: Idle 01: Command completed successfully 10: Command in progress 11: Command failed	All zeros

Table 268. STW_CTRL1: STW Control 1 (1Ex8000) *(continued)*

Bit	Name	Access	Description	Default
1:0	STW_EXT_CMD	RW	Extended command; the range of addressing is influenced by STW_MSA_TYPE 00: XENPAK (11-118), XFP (2-57) 01: XENPAK (119-166), XFP (72-111) 10: XENPAK (167-255), XFP (0-127) 11: XENPAK (0-255), XFP (128-255)	All zeros

Table 269. STW_CTRL2: STW Control 2 (1Ex8001)

Bit	Name	Access	Description	Default
15:11	RESERVED	RO	Reserved	All zeros
10	RESERVED	RW	Reserved	0
9	STW_MAN_UPDATE_8002	RW	Latch STW_REGADDR (1Ex8003) into the STW controller 0: Do nothing 1: Update STW controller with STW_REGADDR	0
8	STW_MAN_UPDATE_8003	RW	Latch STW_DEVADDR (1Ex8002) into the STW controller 0: Do nothing 1: Update STW controller with STW_DEVADDR	0
7:6	STW_MAN_STATUS	RO/LH	Instruction status; these bits clear on read, but if a condition persists, the bits maintain their value 00: Idle 01: Instruction completed successfully 10: Instruction in progress 11: Instruction failed	All zeros
5	RESERVED	RW	Factory test only (do not modify this bit group)	0
4	RESERVED	RO	Reserved	0
3	STW_MAN_CMD	RW	Command type for manual mode 0: Read 1: Write	0
2	STW_MAN ACK	RW	Instruct the STW controller to send an ACK after the next data byte 0: Read/Write without an acknowledge 1: Read/Write with an acknowledge	0
1	STW_MAN_STOP	RW	Instruct the STW controller to send a Stop command after the next data byte 0: Read/Write without a STOP command 1: Read/Write with a STOP command	0
0	STW_MAN_START	RW	Instruct the STW controller to send a Start command after the next data byte 0: Read/Write without a START command 1: Read/Write with a START command	0

Table 270. STW_DEVADDR: STW Device Address (1Ex8002)

Bit	Name	Access	Description	Default
15:7	RESERVED	RW	Reserved	All zeros
6:3	STW_DEV_TYPE	RW	Target STW slave device type	All zeros
2:0	STW_ADDR	RW	Target STW slave device address	All zeros

Table 271. STW_REGADDR: STW Register Address (1Ex8003)

Bit	Name	Access	Description	Default
15:0	STW_REG	RW	Intended register address to access within the STW slave device	All zeros

Table 272. STW_CFG1: STW Configuration 1 (1Ex8004)

Bit	Name	Access	Description	Default
15:13	RESERVED	RW	Reserved	All zeros
12	STW_MSA_MODE	RW	MSA register map compliance type; this influences the STW_EXT_CMD selection. 0: XENPAK 1: XFP	0
11	STW_ADDR_MODE	RW	Select the STW device addressing mode 0: 7-bit 1: Reserved	0
10:9	STW_SPEED_MODE	RW	Select the STW bus speed 00: Standard (100 kHz) 01: Fast (400 kHz) 1X: Reserved	All zeros
8:0	RESERVED	RW	Reserved	All zeros

Table 273. NVR Memory Map (1Ex8007-8106)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Consult the XENPAK or XFP specifications for a description of the NVR mapping.	All zeros

Table 274. DOM_RXALRM_CTRL: DOM Rx Alarm Control (1Ex9000)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros

Table 274. DOM_RXALRM_CTRL: DOM Rx Alarm Control (1Ex9000) *(continued)*

Bit	Name	Access	Description	Default
4	FAULT_RX_PMA_ENA	RW	PMA receive local fault enable 0: Disable 1: Enable	1
3	FAULT_RX_PCS_ENA	RW	PCS receive local fault enable 0: Disable 1: Enable	1
2	VEND_SPEC	RO	Vendor Specific	0
1	FLAG_RX_ENA	RW	RX_FLAG enable 0: Disable 1: Enable	0
0	FAULT_RX_PHYXS_ENA	RW	PHY XS receive local fault enable 0: Disable 1: Enable	1

Table 275. DOM_TXALRM_CTRL: DOM Tx Alarm Control (1Ex9001)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	FAULT_TX_PMA_ENA	RW	PMA transmit local fault enable 0: Disable 1: Enable	1
3	FAULT_TX_PCS_ENA	RW	PCS transmit local fault enable 0: Disable 1: Enable	1
2	VEND_SPEC	RO	Vendor specific	0
1	FLAG_TX_ENA	RW	TX_FLAG enable 0: Disable 1: Enable	0
0	FAULT_TX_PHYXS_ENA	RW	PHY XS transmit local fault enable 0: Disable 1: Enable	1

Table 276. DOM_LASI_CTRL: DOM Link Alarm Status Interrupt Control (1Ex9002)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved	All zeros
2	ALARM_RX_ENA	RW	Receive alarm enable 0: Disable 1: Enable	0
1	ALARM_TX_ENA	RW	Transmit alarm enable 0: Disable 1: Enable	0
0	ALARM_LS_ENA	RW	Link status alarm enable 0: Disable 1: Enable	0

Table 277. DOM_RXALRM_STAT: DOM Rx Alarm Status (1Ex9003)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	FAULT_RX_PMA_STAT	RO/LH	PMA receiver local fault 0: No fault asserted 1: Fault asserted See also 1x0008.10	0
3	FAULT_RX_PCS_STAT	RO/LH	PCS receive local fault 0: No fault asserted 1: Fault asserted See also 3x0008.10	0
2	Vendor Specific	RO	Vendor specific	0
1	FLAG_RX_STAT	RO/LH	Receive flag status 0: No fault asserted 1: Fault asserted	0
0	FAULT_RX_PHYXS_STAT	RO/LH	PHY XS receive local fault 0: No fault asserted 1: Fault asserted See also 4x0008.10	0

Table 278. DOM_TXALRM_STAT: DOM Tx Alarm Status (1Ex9004)

Bit	Name	Access	Description	Default
15:5	RESERVED	RO	Reserved	All zeros
4	FAULT_TX_PMA_STAT	RO/LH	PMA transmit local fault status 0: No fault asserted 1: Fault asserted See also 1x0008.11	0
3	FAULT_TX_PCS_STAT	RO/LH	PCS transmit local fault status 0: No fault asserted 1: Fault asserted See also 3x0008.11	0
2	Vendor Specific	RO	Vendor specific	0
1	FLAG_TX_STAT	RO/LH	Transmit flag fault status 0: No fault asserted 1: Fault asserted	0
0	FAULT_TX_PHYXS_STAT	RO/LH	PHY XS transmit local fault status 0: No fault asserted 1: Fault asserted See also 4x0008.11	0

Table 279. DOM_LASI_STAT: DOM Link Alarm Status Interrupt Status (1Ex9005)

Bit	Name	Access	Description	Default
15:3	RESERVED	RO	Reserved	All zeros

Table 279. DOM_LASI_STAT: DOM Link Alarm Status Interrupt Status (1Ex9005)

Bit	Name	Access	Description	Default
2	ALARM_RX_STAT	RO	Receive alarm status 0: No fault asserted 1: Fault asserted	0
1	ALARM_TX_STAT	RO	Transmit alarm status 0: No fault asserted 1: Fault asserted	0
0	ALARM_LS_STAT	RO/LH	Link status alarm status 0: No fault asserted 1: Fault asserted	0

Table 280. DOM_TXFLAG_CTRL: DOM Tx Flag Control (1Ex9006)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Reserved	All zeros
7	TXFLAG_HI_TEMP_ENA	RW	High temperature alarm enable 0: Disable 1: Enable	0
6	TXFLAG_LO_TEMP_ENA	RW	Low temperature alarm enable 0: Disable 1: Enable	0
5:4	RESERVED	RW	Reserved	All zeros
3	TXFLAG_HI_LBIAS_ENA	RW	Laser bias current high alarm enable 0: Disable 1: Enable	0
2	TXFLAG_LO_LBIAS_ENA	RW	Laser bias current low alarm enable 0: Disable 1: Enable	0
1	TXFLAG_HI_TXPWR_ENA	RW	Laser output power high alarm enable 0: Disable 1: Enable	0
0	TXFLAG_LO_TXPWR_ENA	RW	Laser output power low alarm enable 0: Disable 1: Enable	0

Table 281. DOM_RXFLAG_CTRL: DOM Rx Flag Control (1Ex9007)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Reserved	All zeros
7	RXFLAG_HI_RXPWR_ENA	RW	Receive optical power high alarm enable 0: Disable 1: Enable	0
6	RXFLAG_LO_RXPWR_ENA	RW	Receive optical power low alarm enable 0: Disable 1: Enable	0
5:0	RESERVED	RW	Reserved	All zeros

Table 282. DOM Alarm/Warning Thresholds (1ExA000-A027)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 283. DOM Optional Alarm/Warning Thresholds for CWDMs (1ExA048-A05F)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 284. DOM Interfaces (1ExA060-A06D)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 285. Optional Status Bits (1ExA06E)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 286. Extended DOM capability (1ExA06F)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 287. DOM_TXALARM: DOM Tx Alarm Flags (1ExA070)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros

Table 287. DOM_TXALARM: DOM Tx Alarm Flags (1ExA070) *(continued)*

Bit	Name	Access	Description	Default
7	ALARM_HI_XCVRTEMP_STAT	RO	Transceiver temperature high alarm status 0: No alarm asserted 1: Alarm asserted	0
6	ALARM_LO_XCVRTEMP_STAT	RO	Transceiver temperature low alarm status 0: No alarm asserted 1: Alarm asserted	0
5:4	RESERVED	RO	Reserved	All zeros
3	ALARM_HI_LBIAS_STAT	RO	Laser bias current high alarm status 0: No alarm asserted 1: Alarm asserted	0
2	ALARM_LO_LBIAS_STAT	RO	Laser bias current low alarm status 0: No alarm asserted 1: Alarm asserted	0
1	ALARM_HI_TXPWR_STAT	RO	Laser output power high alarm status 0: No alarm asserted 1: Alarm asserted	0
0	ALARM_LO_TXPWR_STAT	RO	Laser output power low alarm status 0: No alarm asserted 1: Alarm asserted	0

Table 288. DOM_RXALARM: DOM Rx Alarm Flags (1ExA071)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7	ALARM_HI_RXPWR_STAT	RO	Receive optical power high alarm status 0: No alarm asserted 1: Alarm asserted	0
6	ALARM_LO_RXPWR_STAT	RO	Receive optical power low alarm status 0: No alarm asserted 1: Alarm asserted	0
5:0	RESERVED	RO	Reserved	All zeros

Table 289. RESERVED (1ExA072-A073)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 290. DOM_TXWARN: DOM Tx Warning Flags (1ExA074)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros

Table 290. DOM_TXWARN: DOM Tx Warning Flags (1ExA074) *(continued)*

Bit	Name	Access	Description	Default
7	WARN_HI_XCVRTEMP_STAT	RO	Transceiver temperature high warning status 0: No warning asserted 1: Warning asserted	0
6	WARN_LO_XCVRTEMP_STAT	RO	Transceiver temperature low warning status 0: No warning asserted 1: Warning asserted	0
5:4	RESERVED	RO	Reserved	All zeros
3	WARN_HI_LBIAS_STAT	RO	Laser bias current high warning status 0: No warning asserted 1: Warning asserted	0
2	WARN_LO_LBIAS_STAT	RO	Laser bias current low warning status 0: No warning asserted 1: Warning asserted	0
1	WARN_HI_TXPWR_STAT	RO	Laser output power high warning status 0: No warning asserted 1: Warning asserted	0
0	WARN_LO_TXPWR_STAT	RO	Laser output power low warning status 0: No warning asserted 1: Warning asserted	0

Table 291. DOM_RXWARN: DOM Rx Warning Flags (1ExA075)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7	WARN_HI_RXPWR_STAT	RO	Receive optical power high warning status 0: No warning asserted 1: Warning asserted	0
6	WARN_LO_RXPWR_STAT	RO	Receive optical power low warning status 0: No warning asserted 1: Warning asserted	0
5:0	RESERVED	RO	Reserved	All zeros

Table 292. RESERVED (1ExA076-A077)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 293. DOM_CWDM: DOM Control and Status (1ExA0C0-A0FF)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros

Table 293. DOM_CWDM: DOM Control and Status (1ExA0C0-A0FF) *(continued)*

Bit	Name	Access	Description	Default
7:0		RW	Refer to the XENPAK or XFP specifications for register details	All zeros

Table 294. DOM_CTRL_STAT: DOM Control and Status (1ExA100)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	All zeros
7:4	RESERVED	RW	Reserved	All zeros
3:2	DOM_CMD_STATUS	RW	This feature is not directly supported	All zeros
1:0	DOM_CMD_UPDATE	RW	This feature is not directly supported	All zeros

Table 295. Factory Test Register (1ExA101-A106)

Bit	Name	Access	Description	Default
7:0	RESERVED	RW	Factory test only (do not modify this bit group)	All zeros

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8486 device.

5.1 DC Characteristics

The following tables show the DC specifications for the VSC8486 device.

Table 296. LVTTL I/O Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4 1.8 1.4 1.1 0.88	V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL}	V	VDDTTL = 3.3 V and I_{OH} = −4 mA VDDTTL = 2.5 V and I_{OH} = −4 mA VDDTTL = 1.8 V and I_{OH} = −2 mA VDDTTL = 1.5 V and I_{OH} = −2 mA VDDTTL = 1.2 V and I_{OH} = −1 mA
Output high voltage, open drain	V_{OH_OD}	3.2 2.4 1.7 1.4 0.9	V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL}	V	VDDTTL = 3.3 V and I_{OH} = 100 µA VDDTTL = 2.5 V and I_{OH} = 100 µA VDDTTL = 1.8 V and I_{OH} = 100 µA VDDTTL = 1.5 V and I_{OH} = 100 µA VDDTTL = 1.2 V
Output low voltage (LVTTL, open drain)	V_{OL}	0.0 0.0 0.0 0.0 0.0	0.5 0.5 0.4 0.2 0.2	V	VDDTTL = 3.3 V and I_{OL} = 4 mA VDDTTL = 2.5 V and I_{OL} = 4 mA VDDTTL = 1.8 V and I_{OL} = 2 mA VDDTTL = 1.5 V and I_{OL} = 2 mA VDDTTL = 1.2 V and I_{OL} = 1 mA
Input high voltage	V_{IH}	2.0 1.7 1.2 1.05 0.85	V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL} V_{DDTTL}	V	VDDTTL = 3.3 V VDDTTL = 2.5 V VDDTTL = 1.8 V VDDTTL = 1.5 V VDDTTL = 1.2 V
Input low voltage	V_{IL}	0.0 0.0 0.0 0.0 0.0	0.8 0.8 0.6 0.45 0.4	V	VDDTTL = 3.3 V VDDTTL = 2.5 V VDDTTL = 1.8 V VDDTTL = 1.5 V VDDTTL = 1.2 V
Input high current	I_{IH}		500	µA	$V_{IH} = V_{DDTTL}$
Input low current	I_{IL}	−50		µA	V_{IL} = 0 V

Note that REFCLKP/N has the exposed center tap (REFTERM), whereas WREFCLKP/N and VREFCLKP/N do not. For more information about reference clock inputs, see "Reference Clock Inputs," page 40.

Table 297. Reference Clock Input Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input voltage	ΔV_{REFCLK}	150		2000	mV	Measured peak-to-peak both sides driven
		300		2000	mV	Measured peak-to-peak single-ended driven
Input common-mode voltage	V_{CM}	700		950	mV	
REFTERM voltage	$V_{REFTERM}$		$0.67 \times V_{DD12TX}$		V	$V_{DD12TX} = 1.2$ V

Table 298. MDIO Electrical Interface Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input high voltage(1)	V_{IH}	0.84		V_{DDTTL}	V	
Input low voltage	V_{IL}	0		0.36	V	
Output high voltage(2)	V_{OH}	1.0		V_{DDTTL}	V	$I_{OH} = -100$ µA
Output low voltage	V_{OL}	0		0.2	V	$I_{OL} = 100$ µA
Output high current during tri-state	I_{OZH}		TBD		mA	$V_I = 1.5$ V
Output low current	I_{OL}	4.0			mA	$V_I = 0.2$ V
Input capacitance	C_{IN}			10	pF	
Bus loading	C_L			470	pF	

1. Input is 3.3 V tolerant.
2. Output is open drain and pulled up to 1.5 V through a 4.7 kΩ resistor.

5.2 AC Characteristics

The following tables show the AC specifications for the VSC8486 device.

5.2.1 10-Gigabit I/O Specifications

The following tables provide the input specifications for 10-gigabit data. They refer to points A and D in the XFI specification, unless specified otherwise.

Table 299. 10-Gigabit Data Input Specifications for Serial Input Performance

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data input swing	ΔV_{SWING}	55		525	mV	Measured peak-to-peak each side (both sides driven)

Table 299. 10-Gigabit Data Input Specifications for Serial Input Performance

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data differential input swing	ΔV_{SWING_DIFF}	55		1050	mV	Measured peak-to-peak both sides driven with no offset applied
Data single-ended input swing	ΔV_{SWING_SE}	55		1050	mV	Measured peak-to-peak single-ended driven with no offset applied
Single-ended input impedance	RZ_{SE_TERM}	40	50	60	Ω	RXIN to RXINCM
Differential input impedance	RZ_{DE_TERM}	80	100	120	Ω	RXIN+ to RXIN–
Differential input return loss	$S11_{DIFF}$		10 See(1)		dB	0.1 GHz to 7.5 GHz 7.5 GHz to 15 GHz
Single-ended input return loss(2)	S11		6		dB	0.1 GHz to 15 GHz
Termination resistor current	I_{TERM}			25	mA	RXIN to RXINCM
RXDATA input common mode	RXINCM		$0.58 \times V_{DD12RX}$		V	

1. Return loss is calculated according to the equation $S11_{DIFF}$(dB) = 10 – 16.6 Log10(f / 7.5 GHz) for f between 7.5 GHz and 15 GHz, with f in GHz.
2. There is an errata item associated with this specification. For more information, see "Errata," page 250.

Figure 59. 10-Gigabit Data Input Compliance Mask

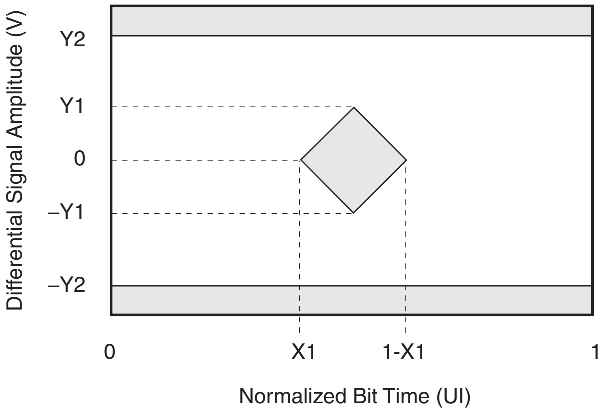


Figure 60. 10-Gigabit Data Input Sinusoidal Jitter Tolerance

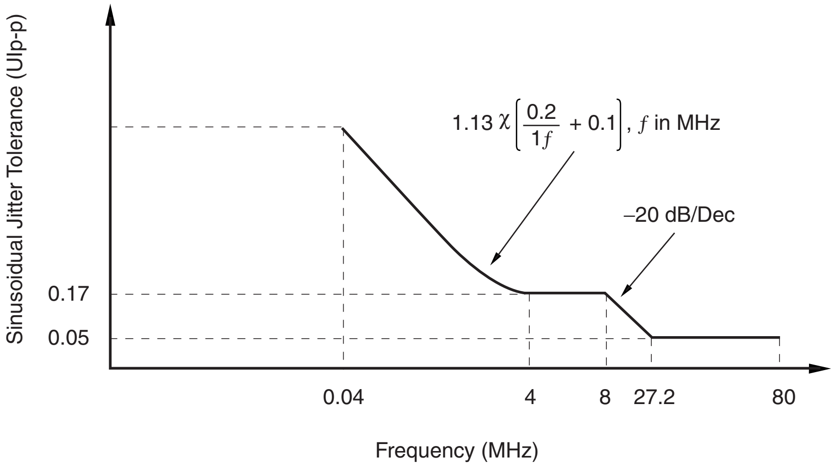


Table 300. 10-Gigabit Data Input Specifications for CRU Performance

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Difference between REFCK frequency (with appropriate multiplier) and 10-gigabit input data frequency	Δf_{REFCLK}	−100	100	ppm	
Total jitter tolerance	TOL_{JIT_P-P}		0.65	UI	Measured peak-to-peak.
Total non-DDJ jitter tolerance	NDD_{JIT_P-P}		0.45	UI	Measured peak-to-peak.
Sinusoidal jitter tolerance	S_J				Measured peak-to-peak. See Figure 60, page 218.
Eye mask (X1)	X1		0.325	UI	See Figure 59, page 217.
Eye mask (Y1)	Y1	55		mV	See Figure 59, page 217.
Eye mask (Y2)	Y2		525	mV	See Figure 59, page 217.

The following tables provide output specifications for 10-gigabit data.

Table 301. 10-Gigabit Data Output Specifications for MUX Performance

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
TXDOUTP/N single-ended output swing at near end	V_{SE_NE}		300		mV	Informative data measured at near end (as specified in XFP MSA) with no de-emphasis enabled. Each side is AC-coupled and terminated 50 Ω to V_{DD12TX}.
TXDOUTP/N single-ended output swing at far end	V_{SE_FE}	90		350	mV	Measured at far end, as specified in SFF-8431.
Common-mode output voltage TXDOUTP/N	V_{CM}		0.9		V	
TXDOUTP/N rise time and fall time	t_R, t_F	24	35		ps	20% to 80% into 50 Ω load.
Single-ended output impedance	TZ_{SE_TERM}	40	50	60	Ω	TXDOUT to V_{DD12TX}.
Differential output impedance	TZ_{DE_TERM}	80	100	120	Ω	TXDOUTP to TXDOUTN.
Differential output return loss	$S22_{DIFF}$		10 See(1)		dB	0.1 GHz to 7.5 GHz. 7.5 GHz to 15 GHz.
Single-ended output return loss	S22		6		dB	0.1 GHz to 15 GHz.

1. Return loss is calculated by equation $S22_{DIFF}$(dB) = 10 – 16.6 Log10(f / 7.5 GHz) for f between 7.5 GHz and 15 GHz, with f in GHz.

Table 302. 10-Gigabit Data Output Specifications for CMU Performance (WAN Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
TXDOUTP/N jitter	JG_{OUT}		0.07	TBD	UI	Measured peak-to-peak. WREFCLK = 622.08 MHz low jitter. Reference clock required.(1)
RXDINP/N jitter tolerance	J_{TOL}	1.5 × SONET jitter mask		TBD		Measured peak-to-peak. Compliant with 1.5 × SONET jitter mask. GR1377-CORE.(2)

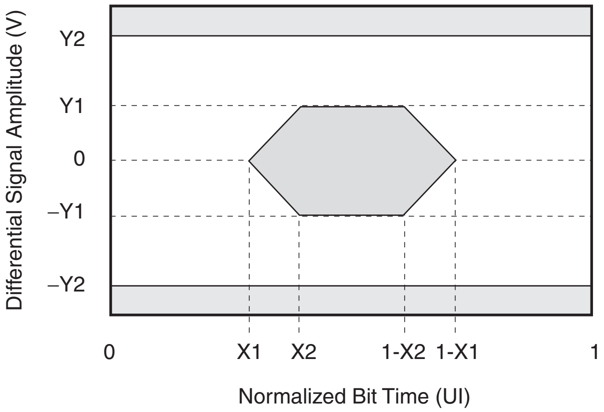
1. For optimal J_G and rise and fall time performance, adjustments might be required to the transmit pre-emphasis or transmit slew rate or both in register 1xE601.
2. Measured 1 dB above minimum RXIN input sensitivity.

Table 303. 10-Gigabit Data Output Specifications for CMU Performance (LAN/SAN Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
TXDOUTP/N deterministic jitter at near end	$DJDOUT_{NE}$		0.22		UI	Informative data measured peak-to-peak at near end (as specified in XFP MSA) with no de-emphasis enabled. Soldered down f = 10.5 GHz.
TXDOUTP/N total jitter at far end	$TJDOUT_{FE}$			0.28	UI	Measured peak-to-peak at far end, as specified in SFF-8431. Soldered down f = 10.5 GHz.
TXDOUTP/N data-dependent jitter at far end	$DJDOUT_{FE}$			0.10	UI	Measured peak-to-peak at far end, as specified in SFF-8431. Soldered down f = 10.5 GHz.
TXDOUTP/N uncorrelated jitter at far end	$UJDOUT_{FE}$			0.023	UI	Measured peak-to-peak at far end, as specified in SFF-8431. Soldered down f = 10.5 GHz.
CLK64P/N jitter generation	JG_{C64}			0.01	UI	Measured peak-to-peak(1). CLK64A and CLK64B in CMU/64 or CMU/66 mode only.
CLK64P/N output swing	ΔV	320		800	mV	Measured peak-to-peak. CLK64A and CLK64B in CMU/64 or CMU/66 mode only.
Eye mask (X1)	X1			0.14	UI	Measured at far end, as specified in SFF-8431. See Figure 61, page 221.
Eye mask (X2)	X2			0.35	UI	Measured at far end, as specified in SFF-8431. See Figure 61, page 221.
Eye mask (Y1)	Y1	90			mV	Measured at far end, as specified in SFF-8431. See Figure 61, page 221.
Eye mask (Y2)	Y2			350	mV	Measured at far end, as specified in SFF-8431. See Figure 61, page 221.

1. JG_{C64} is referenced to 164.35 (161.13) MHz.

Figure 61. 10-Gigabit Data Output Compliance Mask



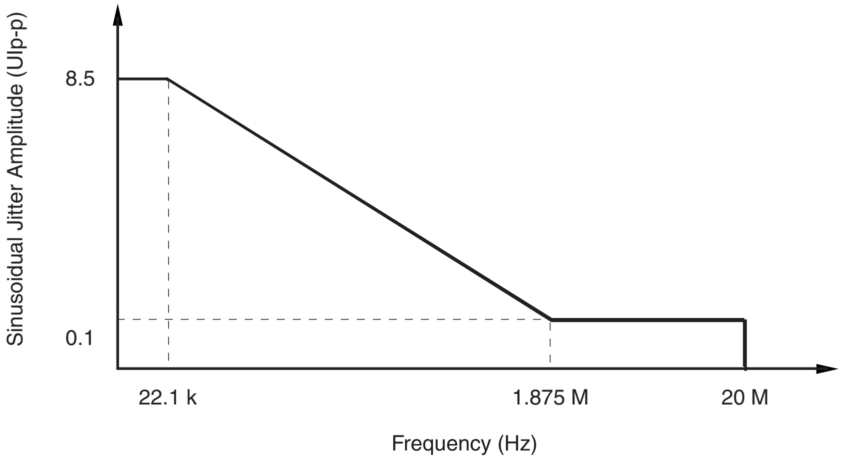
5.2.2 XAUI Specifications

The following table and figure provide XAUI input specifications.

Table 304. XAUI Input Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input baud rate	f	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
Unit interval	UI		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm
Differential input amplitude	V_{IN_DIFF}	75		1600	mV	AC-coupled, measured peak-to-peak each side (both sides driven)
Common-mode input voltage	V_{IN_CM}	0.75		V_{DDA12} – 0.05	V	Midpoints between high and low voltages, measured at DC
Differential return loss	RLI_{DIFF}		10		dB	100 Ω differential reference impedance
Common-mode return loss	RLI_{CM}		6		dB	100 MHz to 2.5 GHz, 25 Ω reference impedance
Differential skew	SK_{DIFF}			75	ps	Between true and complement inputs
Jitter tolerance, total	TOL_{TJ}	0.65			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4
Jitter tolerance, deterministic	TOL_{DJ}	0.37			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4
Jitter tolerance, deterministic plus random jitter	TOL_{DJ+RJ}	0.55			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4

Figure 62. XAUI Receiver Input Sinusoidal Jitter Tolerance



The following table and figure provide XAUI output specifications.

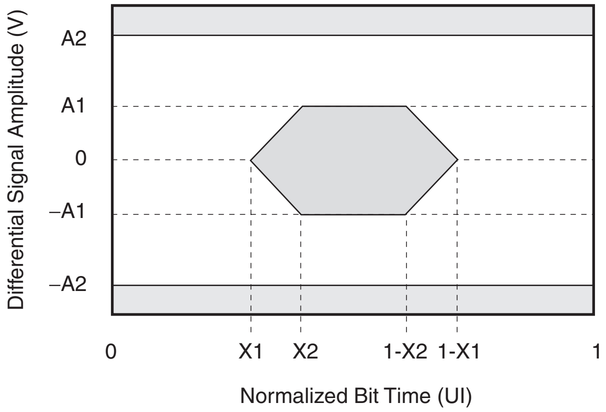
Table 305. XAUI Output Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Output baud rate	f	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
Unit interval	UI		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm.
Differential output voltage	XV_{OUT_DIFF}	400		650	mV	Single-ended, AC-coupled, measured peak-to-peak, both sides driven with no offset applied. HISWNG = 1.
		250		500	mV	Single-ended, AC-coupled, measured peak-to-peak, both sides driven with no offset applied. HISWNG = 0.
Output impedance	Z_{OUT}	40	50	60	Ω	Single-ended.
		80	100	120	Ω	Differential.
Differential output return loss	RLO_{DIFF}		10		dB	100 MHz to 781.25 MHz, reducing 20 dB per decade up to 3.5 GHz. Includes on-chip circuitry, packaging, and off-chip components. 100 Ω test source.
Common-mode output return loss	RLO_{CM}		6		dB	100 MHz to 2.5 GHz over valid output levels. Includes on-chip circuitry, packaging, and off-chip components. 25 Ω test source.
Rise time and fall time	t_R, t_F	60		130	ps	20% for rise time. 80% for fall time.
Total jitter	T_J			0.35	UI	Measured peak-to-peak, no pre-emphasis.

Table 305. XAUI Output Specifications *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Deterministic jitter	DJ			0.17	UI	Measured peak-to-peak, no pre-emphasis.
Eye mask (X1)	X1			0.175	UI	See Figure 63, page 223.
Eye mask (X2)	X2			0.390	UI	See Figure 63, page 223.
Eye mask (A1)	A1	250			mV	See Figure 63, page 223. HISWNG = 0.
		400			mV	See Figure 63, page 223. HISWNG = 1.
Eye mask (A2)	A2			800	mV	See Figure 63, page 223.

Figure 63. XAUI Output Compliance Mask



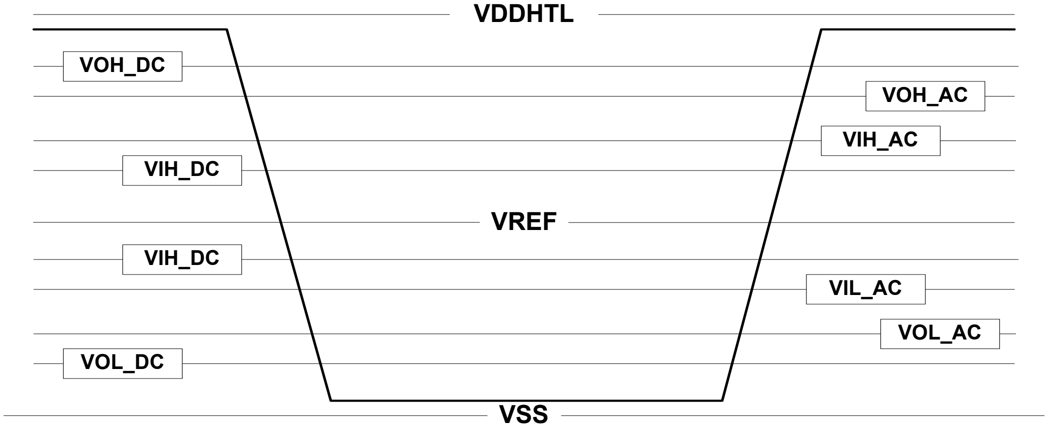
5.2.3 XGMII Specifications

The following table and figure provide XGMII input specificaitons.

Table 306. XGMII Input Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input reference voltage	V_{HVREF}	0.68	0.75	0.9	V	Measured peak-to-peak. AC noise on V_{HVREF} may not exceed 2% V_{HVREF}(DC).
DC input high voltage	V_{IH_DC}	V_{HVREF} + 0.1		V_{DDHTL}	V	
DC input low voltage	V_{IL_DC}	0		V_{HVREF} – 0.1	V	
AC input high voltage	V_{IH_AC}	V_{HVREF} + 0.2			V	
AC input low voltage	V_{IL_AC}			V_{HVREF} – 0.2	V	

Figure 64. XGMII I/O Level Reference Diagram

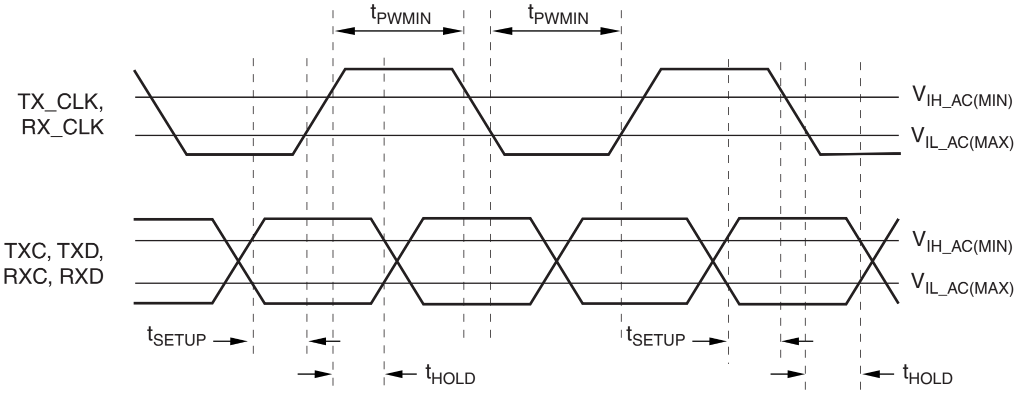


The following table and figure provide XGMII output specificaitons.

Table 307. XGMII Output Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
DC output high voltage	V_{OH}	$V_{DDHTL} - 0.4$		V	I_{OH} = 8 mA (V_{TT} = V_{DDHTL} / 2, R_T = 50 Ω)
DC output low voltage	V_{OL}		0.4	V	I_{OH} = |−8 mA| (V_{TT} = V_{DDHTL} / 2, R_T = 50 Ω)
RXCLK output duty cycle	DC_{RXCLK}	45	55	%	

Figure 65. XGMII Interface Timing Diagram



5.2.4 Timing and Clock Specifications

The following tables show the timing and clock specifications for the VSC8486 device.

Table 308. Reset Timing

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Minimum reset pulse width	T_{RESET}	0.1	TBD	µs	All power supplies are stable.

Table 309. Reference Clock Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
REFCK frequency	f_{REFCLK}	156.25 MHz − 100 ppm	159.37 MHz + 100 ppm	MHz	Pins: REFSEL[1:0] = 00
REFCKP/N duty cycle	DC_{REFCK}	40	60	%	

Table 310. TXCLK and RXCLK Timing Parameters

Parameter	Symbol	Driver	Receiver	Unit
Setup time	t_{SETUP}	960	480	ps
Hold time	t_{HOLD}	960	480	ps
Minimum pulse width	t_{PWMIN}	2.5		ns

Figure 66. Parametric Measurement Setup

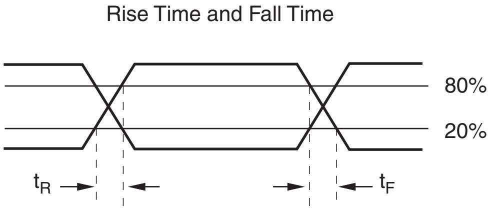


Figure 67. Timing with MDIO Sourced by the Station Management Entity (STA)

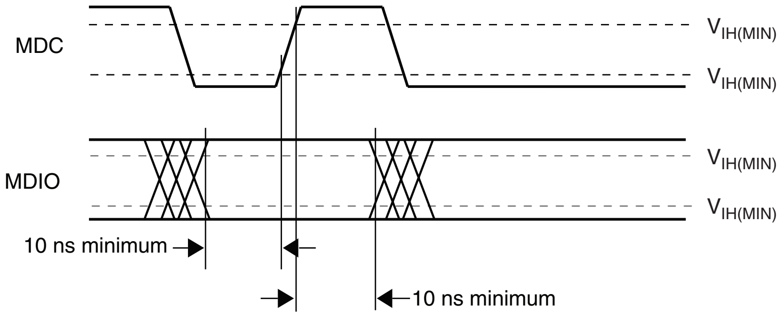
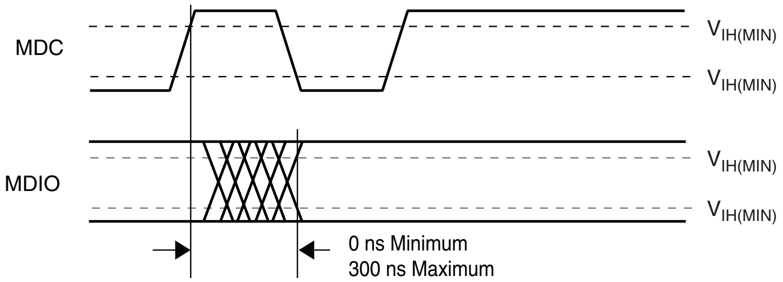


Figure 68. Timing with MDIO Sourced by the MMD



5.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC8486 device. **Note** To ensure that the control pins remain set to the desired configured state when the VSC8486 device is powered up, it is recommended to perform a reset through the reset pin after power-up and after the control pins are steady for 1 ms.

Table 311. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
1.5 V power supply voltage	V_{DDHTL}	1.43	1.5	1.58	V	
1.5 V power supply current	I_{DDHTL}		150		mA	Outputs terminated 50 Ω to V_{REF}, data toggling with 50% duty cycle.
			10		mA	Outputs unterminated, data toggling with 50% duty cycle.
			1		mA	Outputs unterminated, static data.
1.2 V power supply voltage	V_{DD12RX} V_{DD12TX} V_{DDA12} V_{DD12X} $V_{DD12PCS}$	1.14	1.2	1.26	V	
1.2 V power supply current	I_{DD12}		625		mA	V_{DDHTL} = ground. XAUI to 10 gigabit data in LAN mode.
Power consumption at 1.2 V power supply	P_{DD12}		753	924	mW	XAUI to XFI in LAN.
			839	1011	mW	XAUI to XFI in WAN.
TTL I/O power supply voltage	V_{DDTTL}	3.14 2.38 1.71 1.43 1.14	3.3 2.5 1.8 1.5 1.2	3.47 2.63 1.89 1.58 1.26	V	VDDTTL = 3.3 V. VDDTTL = 2.5 V. VDDTTL = 1.8 V. VDDTTL = 1.5 V. VDDTTL = 1.2 V.
TTL I/O power supply current	I_{DDTTL}		3		mA	V_{DDTTL} = 3.3 V, 2.5 V, 1.8 V, 1.5 V.
Operating temperature(1)	T	0		85	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

5.4 Stress Ratings

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 312. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
3.3 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	3.8	V
2.5 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	2.9	V
1.8 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	2.1	V
1.5 V power supply voltage, potential to ground	V_{DDHTL}	–0.5	1.9	V
1.2 V power supply voltage, potential to ground	V_{DD12}	–0.5	1.32	V
DC input voltage	V_I	–0.3	V_{DDTTL}, V_{DDHTL}, or V_{DD12} + 0.3	V
Output current (LVTTL)	I_{O_VDDTTL}	–16	16	mA
Absolute XAUI output voltage	V_{XAUI_ABS}	–0.4	2.3	V
Storage temperature	T_S	-65	150	°C

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

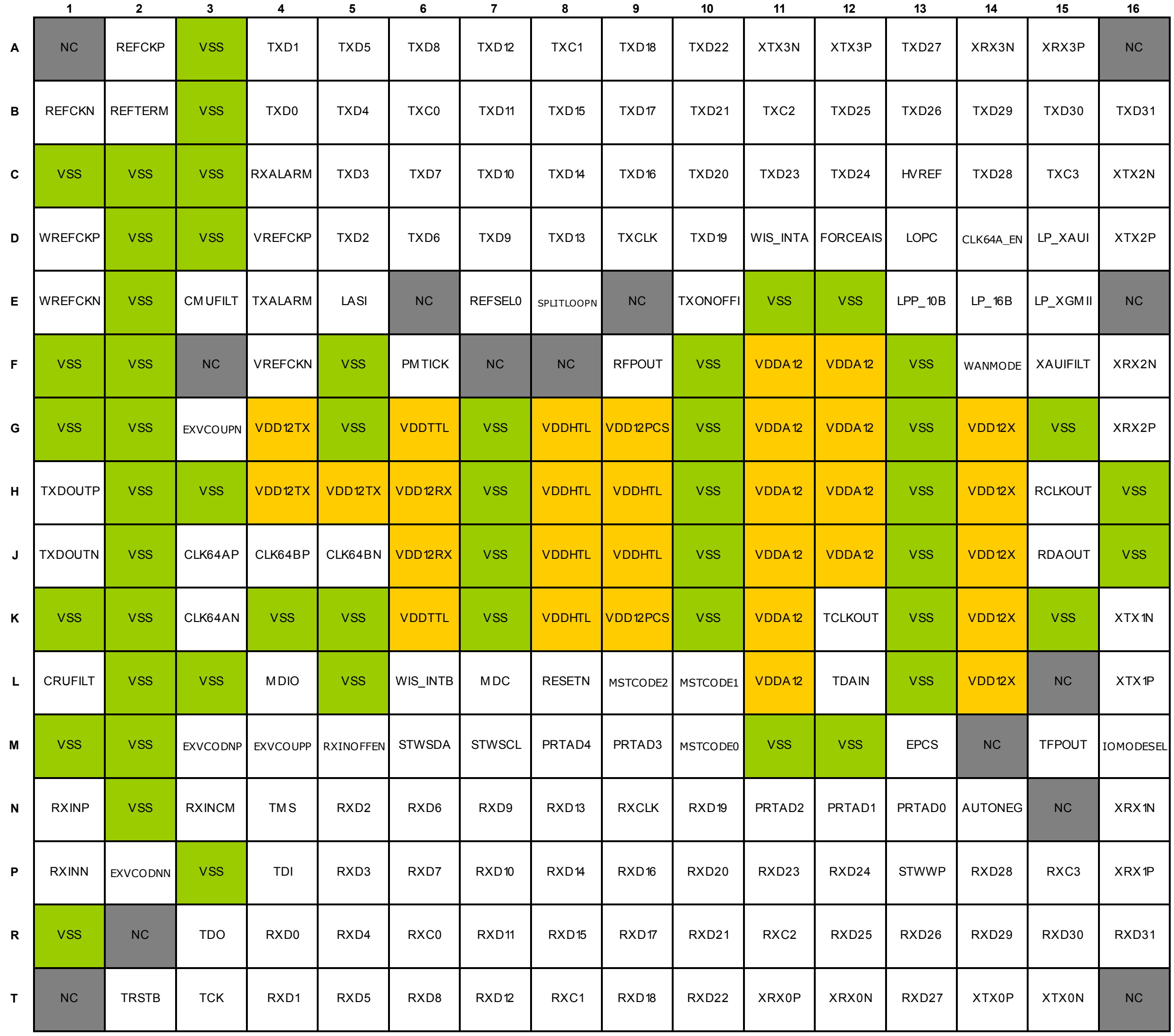
The VSC8486 device has 256 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

6.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8486 device.

Figure 69. Pin Diagram (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	REFCKP	VSS	TXD1	TXD5	TXD8	TXD12	TXC1	TXD18	TXD22	XTX3N	XTX3P	TXD27	XRX3N	XRX3P	NC
B	REFCKN	REFTERM	VSS	TXD0	TXD4	TXC0	TXD11	TXD15	TXD17	TXD21	TXC2	TXD25	TXD26	TXD29	TXD30	TXD31
C	VSS	VSS	VSS	RXALARM	TXD3	TXD7	TXD10	TXD14	TXD16	TXD20	TXD23	TXD24	HVREF	TXD28	TXC3	XTX2N
D	WREFCKP	VSS	VSS	VREFCKP	TXD2	TXD6	TXD9	TXD13	TXCLK	TXD19	WIS_INTA	FORCEAIS	LOPC	CLK64A_EN	LP_XAUI	XTX2P
E	WREFCKN	VSS	CMUFILT	TXALARM	LASI	NC	REFSEL0	SPLITLOOPN	NC	TXONOFFI	VSS	VSS	LPP_10B	LP_16B	LP_XGMII	NC
F	VSS	VSS	NC	VREFCKN	VSS	PMTICK	NC	NC	RFPOUT	VSS	VDDA12	VDDA12	VSS	WANMODE	XAUIFILT	XRX2N
G	VSS	VSS	EXVCOUPN	VDD12TX	VSS	VDDTTL	VSS	VDDHTL	VDD12PCS	VSS	VDDA12	VDDA12	VSS	VDD12X	VSS	XRX2P
H	TXDOUTP	VSS	VSS	VDD12TX	VDD12TX	VDD12RX	VSS	VDDHTL	VDDHTL	VSS	VDDA12	VDDA12	VSS	VDD12X	RCLKOUT	VSS
J	TXDOUTN	VSS	CLK64AP	CLK64BP	CLK64BN	VDD12RX	VSS	VDDHTL	VDDHTL	VSS	VDDA12	VDDA12	VSS	VDD12X	RDAOUT	VSS
K	VSS	VSS	CLK64AN	VSS	VSS	VDDTTL	VSS	VDDHTL	VDD12PCS	VSS	VDDA12	TCLKOUT	VSS	VDD12X	VSS	XTX1N
L	CRUFILT	VSS	VSS	MDIO	VSS	WIS_INTB	MDC	RESETN	MSTCODE2	MSTCODE1	VDDA12	TDAIN	VSS	VDD12X	NC	XTX1P
M	VSS	VSS	EXVCODNP	EXVCOUPP	RXINOFFEN	STWSDA	STWSCL	PRTAD4	PRTAD3	MSTCODE0	VSS	VSS	EPCS	NC	TFPOUT	IOMODESEL
N	RXINP	VSS	RXINCM	TMS	RXD2	RXD6	RXD9	RXD13	RXCLK	RXD19	PRTAD2	PRTAD1	PRTAD0	AUTONEG	NC	XRX1N
P	RXINN	EXVCODNN	VSS	TDI	RXD3	RXD7	RXD10	RXD14	RXD16	RXD20	RXD23	RXD24	STWWP	RXD28	RXC3	XRX1P
R	VSS	NC	TDO	RXD0	RXD4	RXC0	RXD11	RXD15	RXD17	RXD21	RXC2	RXD25	RXD26	RXD29	RXD30	RXD31
T	NC	TRSTB	TCK	RXD1	RXD5	RXD8	RXD12	RXC1	RXD18	RXD22	XRX0P	XRX0N	RXD27	XTX0P	XTX0N	NC

6.2 Pins by Function

This section contains the functional pin descriptions for the VSC8486 device.

6.2.1 XFI 10-Gigabit Data Bus Interface

The following table lists the pins associated with the XFI interface.

Table 313. XFI 10-Gigabit Data Bus Pins

Name	Number	I/O	Type	Description
RXINCM	N3		Analog	Rx 10-gigabit serial data input resistor termination center tap
RXINN	P1	I	CML	Rx 10-gigabit serial data input, complement
RXINP	N1	I	CML	Rx 10-gigabit serial data input, true
TXDOUTN	J1	O	CML	Tx 10-gigabit serial data output, complement
TXDOUTP	H1	O	CML	Tx 10-gigabit serial data output, true

6.2.2 XAUI 10-Gigabit Data Bus Interface

The following table lists the pins associated with the XAUI interface.

Table 314. XAUI 10-Gigabit Data Bus Pins

Name	Number	I/O	Type	Description
XAUIFILT	F15		Analog	XAUI CMU filter capacitor (1 µF) from this pin to ground.
XRX0N	T12	I	CML	XAUI channel 0 serial data input, complement. DL0<N> as specified in IEEE 802.3ae.
XRX0P	T11	I	CML	XAUI channel 0 serial data input, true. DL0<P> as specified in IEEE 802.3ae.
XRX1N	N16	I	CML	XAUI channel 1 serial data input, complement. DL1<N> as specified in IEEE 802.3ae.
XRX1P	P16	I	CML	XAUI channel 1 serial data input, true. DL1<P> as specified in IEEE 802.3ae.
XRX2N	F16	I	CML	XAUI channel 2 serial data input, complement. DL2<N> as specified in IEEE 802.3ae.
XRX2P	G16	I	CML	XAUI channel 2 serial data input, true. DL2<P> as specified in IEEE 802.3ae.
XRX3N	A14	I	CML	XAUI channel 3 serial data input, complement. DL3<N> as specified in IEEE 802.3ae.
XRX3P	A15	I	CML	XAUI channel 3 serial data input, true. DL3<P> as specified in IEEE 802.3ae.
XTX0N	T15	O	CML	XAUI channel 0 serial data output, complement. SL0<N> as specified in IEEE 803.3ae.
XTX0P	T14	O	CML	XAUI channel 0 serial data output, true. SL0<P> as specified in IEEE 803.3ae.
XTX1N	K16	O	CML	XAUI channel 1 serial data output, complement. SL1<N> as specified in IEEE 802.3ae.

Table 314. XAUI 10-Gigabit Data Bus Pins *(continued)*

Name	Number	I/O	Type	Description
XTX1P	L16	O	CML	XAUI channel 1 serial data output, true. SL1<P> as specified in IEEE 802.3ae.
XTX2N	C16	O	CML	XAUI channel 2 serial data output, complement. SL2<N> as specified in IEEE 802.3ae.
XTX2P	D16	O	CML	XAUI channel 2 serial data output, true. SL2<P> as specified in IEEE 803.3ae.
XTX3N	A11	O	CML	XAUI channel 3 serial data output, complement. SL3<N> as specified in IEEE 802.3ae.
XTX3P	A12	O	CML	XAUI channel 3 serial data output, true. SL3<P> as specified in IEEE 802.3ae.

6.2.3 XGMII 10-Gigabit Data Bus Interface

The following table lists the pins associated with the XGMII interface.

Table 315. XGMII 10-Gigabit Data Bus Pins

Name	Number	I/O	Type	Description
HVREF	C13		Analog	HSTL I/O reference input voltage.
RXC0	R6	O	HSTL	XGMII control bit for lane 0 (bits 0–7).
RXC1	T8	O	HSTL	XGMII control bit for lane 1 (bits 8–15).
RXC2	R11	O	HSTL	XGMII control bit for lane 2 (bits 16–23).
RXC3	P15	O	HSTL	XGMII control bit for lane 3 (bits 24–31).
RXCLK	N9	O	HSTL	Double data rate reference for the transfer of RXD<31:0> and RXC<3:0> signals.
RXD0	R4	O	HSTL	XGMII output (lane 0; bit 0).
RXD1	T4	O	HSTL	XGMII output (lane 0; bit 1).
RXD10	P7	O	HSTL	XGMII output (lane 1; bit 2).
RXD11	R7	O	HSTL	XGMII output (lane 1; bit 3).
RXD12	T7	O	HSTL	XGMII output (lane 1; bit 4).
RXD13	N8	O	HSTL	XGMII output (lane 1; bit 5).
RXD14	P8	O	HSTL	XGMII output (lane 1; bit 6).
RXD15	R8	O	HSTL	XGMII output (lane 1; bit 7).
RXD16	P9	O	HSTL	XGMII output (lane 2; bit 0).
RXD17	R9	O	HSTL	XGMII output (lane 2; bit 1).
RXD18	T9	O	HSTL	XGMII output (lane 2; bit 2).
RXD19	N10	O	HSTL	XGMII output (lane 2; bit 3).
RXD2	N5	O	HSTL	XGMII output (lane 0; bit 2).
RXD20	P10	O	HSTL	XGMII output (lane 2; bit 4).
RXD21	R10	O	HSTL	XGMII output (lane 2; bit 5).
RXD22	T10	O	HSTL	XGMII output (lane 2; bit 6).
RXD23	P11	O	HSTL	XGMII output (lane 2; bit 7).
RXD24	P12	O	HSTL	XGMII output (lane 3; bit 0).

Table 315. XGMII 10-Gigabit Data Bus Pins *(continued)*

Name	Number	I/O	Type	Description
RXD25	R12	O	HSTL	XGMII output (lane 3; bit 1).
RXD26	R13	O	HSTL	XGMII output (lane 3; bit 2).
RXD27	T13	O	HSTL	XGMII output (lane 3; bit 3).
RXD28	P14	O	HSTL	XGMII output (lane 3; bit 4).
RXD29	R14	O	HSTL	XGMII output (lane 3; bit 5).
RXD3	P5	O	HSTL	XGMII output (lane 0; bit 3).
RXD30	R15	O	HSTL	XGMII output (lane 3; bit 6).
RXD31	R16	O	HSTL	XGMII output (lane 3; bit 7).
RXD4	R5	O	HSTL	XGMII output (lane 0; bit 4).
RXD5	T5	O	HSTL	XGMII output (lane 0; bit 5).
RXD6	N6	O	HSTL	XGMII output (lane 0; bit 6).
RXD7	P6	O	HSTL	XGMII output (lane 0; bit 7).
RXD8	T6	O	HSTL	XGMII output (lane 1; bit 0).
RXD9	N7	O	HSTL	XGMII output (lane 1; bit 1).
TXC0	B6	I	HSTL	XGMII control bit for lane 0 (bits 0–7).
TXC1	A8	I	HSTL	XGMII control bit for lane 1 (bits 8–15).
TXC2	B11	I	HSTL	XGMII control bit for lane 2 (bits 16–23).
TXC3	C15	I	HSTL	XGMII control bit for lane 3 (bits 24–31).
TXCLK	D9	I	HSTL	Timing reference for the clocking TXD<31:0> and TXC<3:0> signals. Data is sampled using both positive and negative edges of TXCLK.
TXD0	B4	I	HSTL	XGMII input (lane 0; bit 0).
TXD1	A4	I	HSTL	XGMII input (lane 0; bit 1).
TXD10	C7	I	HSTL	XGMII input (lane 1; bit 2).
TXD11	B7	I	HSTL	XGMII input (lane 1; bit 3).
TXD12	A7	I	HSTL	XGMII input (lane 1; bit 4).
TXD13	D8	I	HSTL	XGMII input (lane 1; bit 5).
TXD14	C8	I	HSTL	XGMII input (lane 1; bit 6).
TXD15	B8	I	HSTL	XGMII input (lane 1; bit 7).
TXD16	C9	I	HSTL	XGMII input (lane 2; bit 0).
TXD17	B9	I	HSTL	XGMII input (lane 2; bit 1).
TXD18	A9	I	HSTL	XGMII input (lane 2; bit 2).
TXD19	D10	I	HSTL	XGMII input (lane 2; bit 3).
TXD2	D5	I	HSTL	XGMII input (lane 0; bit 2).
TXD20	C10	I	HSTL	XGMII input (lane 2; bit 4).
TXD21	B10	I	HSTL	XGMII input (lane 2; bit 5).
TXD22	A10	I	HSTL	XGMII input (lane 2; bit 6).
TXD23	C11	I	HSTL	XGMII input (lane 2; bit 7).
TXD24	C12	I	HSTL	XGMII input (lane 3; bit 0).
TXD25	B12	I	HSTL	XGMII input (lane 3; bit 1).
TXD26	B13	I	HSTL	XGMII input (lane 3; bit 2).

Table 315. XGMII 10-Gigabit Data Bus Pins *(continued)*

Name	Number	I/O	Type	Description
TXD27	A13	I	HSTL	XGMII input (lane 3; bit 3).
TXD28	C14	I	HSTL	XGMII input (lane 3; bit 4).
TXD29	B14	I	HSTL	XGMII input (lane 3; bit 5).
TXD3	C5	I	HSTL	XGMII input (lane 0; bit 3).
TXD30	B15	I	HSTL	XGMII input (lane 3; bit 6).
TXD31	B16	I	HSTL	XGMII input (lane 3; bit 7).
TXD4	B5	I	HSTL	XGMII input (lane 0; bit 4).
TXD5	A5	I	HSTL	XGMII input (lane 0; bit 5).
TXD6	D6	I	HSTL	XGMII input (lane 0; bit 6).
TXD7	C6	I	HSTL	XGMII input (lane 0; bit 7).
TXD8	A6	I	HSTL	XGMII input (lane 1; bit 0).
TXD9	D7	I	HSTL	XGMII input (lane 1; bit 1).

6.2.4 Serial Bus Interface

The following table lists the pins associated with the serial bus interface.

Table 316. Serial Bus Interface Pins

Name	Number	I/O	Type	Description
MDC	L7	I	LVTTL	Management data clock. Schmitt trigger.
MDIO	L4	I/O	LVTTL (open drain)	Management data bus bidirectional I/O. Requires external pull-up resistor (nominally 4.7 kΩ).
MSTCODE0	M10	I	LVTTL	Serial two-wire interface master code, bit 0. Can also be used as general purpose input.
MSTCODE1	L10	I	LVTTL	Serial two-wire interface master code, bit 1 or alternate XFP alarm input, internally pulled low. Can also be used as general purpose input.
MSTCODE2	L9	I	LVTTL	Serial two-wire interface master code, bit 2 or alternate XFP alarm input, internally pulled low. Can also be used as general purpose input.
RCLKOUT	H15	O	LVTTL	WIS overhead receive serial data clock.
RDAOUT	J15	O	LVTTL	WIS overhead port receive serial data.
RFPOUT	F9	O	LVTTL	WIS overhead port receive frame pulse.
STWSCL	M7	I	LVTTL	Serial two-wire interface clock. Requires external pull-up resistor nominally 4.7 kΩ.
STWSDA	M6	I/O	LVTTL	Serial input/output data for the serial two-wire (STW) interface. Requires external pull-up resistor, nominally 4.7 kΩ.
STWWP	P13	I	LVTTL	Serial two-wire interface write protect. 0: Enable writes to STW slave. 1: Disable writes to STW slave. Internally pulled up.
TCLKOUT	K12	O	LVTTL	WIS overhead port transmit serial data clock
TDAIN	L12	I	LVTTL	WIS overhead port transmit serial data.

Table 316. Serial Bus Interface Pins *(continued)*

Name	Number	I/O	Type	Description
TFPOUT	M15	O	LVTTL	WIS overhead port transmit frame pulse.

6.2.5 Input and Output Reference Clocks

The following table lists the pins associated with reference clocks.

Table 317. Input and Output Reference Clock Pins

Name	Number	I/O	Type	Description
CLK64A_EN	D14	I	LVTTL	CLK64A enable. 1: CLK64A enabled (default, internally pulled up). 0: CLK64A disabled.
CLK64AN	K3	O	CML	Selectable clock, complement. CMU divided by 64, or CMU divided by 66, or CRU divided by 64, or REFCK. Default is CMU divided by 64. Normally used for XFP reference clock.
CLK64AP	J3	O	CML	Selectable clock, true. CMU divided by 64, or CMU divided by 66, or CRU divided by 64, or REFCK. Default is CMU divided by 64. Normally used for XFP reference clock.
CLK64BN	J5	O	CML	Selectable clock, complement. CMU divided by 64, or CMU divided by 66, or CRU divided by 64, or TEST_CLK. Default is CRU divided by 64 when enabled.
CLK64BP	J4	O	CML	Selectable clock, true. CMU divided by 64, or CMU divided by 66, or CRU divided by 64, or TEST_CLK. Default is CRU divided by 64 when enabled.
REFCKN	B1	I	LVPECL	Reference clock input, complement. Terminated 50 Ω to REFTERM.
REFCKP	A2	I	LVPECL	Reference clock input, true. Terminated 50 Ω to REFTERM.
REFSEL0	E7	I	LVTTL	WAN mode WREFCLK frequency select. 0: 622.08 MHz (default, internally pulled low). 1: 155.52 MHz.
REFTERM	B2	I	LVPECL	Reference clock input termination center tap.
VREFCKN	F4	I	LVPECL	WAN VCO reference clock, complement. The 10-gigabit CMU reference clock for WANMODE. 622.08 MHz VCSO input used in conjunction with external jitter attenuation PLL.
VREFCKP	D4	I	LVPECL	WAN VCO reference clock, true. The 10-gigabit CMU reference clock for WANMODE. 622.08 MHz VCSO input used in conjunction with external jitter attenuation PLL.
WREFCKN	E1	I	LVPECL	WAN reference clock, complement. Can be 155.52 MHz or 622.08 MHz. 622.08 MHz must be used for optimum jitter generation performance.
WREFCKP	D1	I	LVPECL	WAN Reference clock, true. Can be 155.52 MHz or 622.08 MHz. 622.08 MHz must be used for optimum jitter generation performance.

6.2.6 Status and Control

The following table lists the pins that issue status or enable various modes.

Table 318. Status and Control Pins

Name	Number	I/O	Type	Description
AUTONEG	N14	I	LVTTL	Auto-negotiate enable. Adjusts Tx encoder to match Rx input data. 0: Device resets to state set by EPCS pin. 1: Device will auto-negotiate enhanced or standard PCS. Internally pulled low.
EPCS	M13	I	LVTTL	Extended-PCS enable. Sets start-up transmit encoder to E-PCS. 0: Device resets to IEEE standard PCS encoding 64/66B. 1: Device resets to EPCS encoding OIF-CEI “firecode.” Internally pulled low.
FORCEAIS	D12	I	LVTTL	When asserted, forces the receive WIS into an AIS-L state.
IOMODESEL	M16	I	LVTTL	Parallel interface mode selection pin. 0: XGMII (default, internally pulled low). 1: XAUI.
LASI	E5	O	LVTTL (open drain)	Link alarm status interrupt. Logical OR for RXALARM, TXALARM and LSALARM and as enabled by register 1Ex9002. Open-drain output requires external pull-up resistor.
LOPC	D13	I	LVTTL	Loss of optical carrier normally connected to XFP RX_LOS output.
LP_16B	E14	I	LVTTL	Reserved for factory test only. Internally pulled low by default.
LPP_10B	E13	I	LVTTL	Reserved for factory test only. Internally pulled low by default.
LP_XAUI	D15	I	LVTTL	Simultaneous enable for system and network loopback paths B and D, respectively. 0: Normal operation. 1: Loopbacks B and D enabled. Internally pulled low.
LP_XGMII	E15	I	LVTTL	Selects PCS and XGXS data source. 0: PCS source from XGXS, XGXS source from PCS. 1: PCS source from XGMII, XGXS source from XGMII. Internally pulled low.
PMTICK	F6	I	LVTTL	WIS block counter sampling time control.
PRTAD0	N13	I	LVTTL	Port address bit 0 (LOW = 0). Internally pulled down.
PRTAD1	N12	I	LVTTL	Port address bit 1 (LOW = 0). Internally pulled down.
PRTAD2	N11	I	LVTTL	Port address bit 2 (LOW = 0). Internally pulled down.
PRTAD3	M9	I	LVTTL	Port address bit 3 (LOW = 0). Internally pulled low
PRTAD4	M8	I	LVTTL	Port address bit 4 (LOW = 0). Internally pulled low

Table 318. Status and Control Pins *(continued)*

Name	Number	I/O	Type	Description
RESETN	L8	I	LVTTL	Global chip reset. Active LOW. Schmitt trigger. Internally pulled up.
RXALARM	C4	O	LVTTL (open drain)	Logical OR for alarms in register 1Ex9003 and as enabled by register 1Ex9000. Open-drain output requires external pull-up resistor.
RXINOFFEN	M5	I	LVTTL	10-gigabit PMA input receiver DC offset correction loop enable. 0: Disable DC correction loop. 1: Enable DC correction loop. Internally pulled low.
SPLITLOOPN	E8	I	LVTTL	Enable for simultaneous system and network loopback paths J and K, respectively. 1: Normal operation. 0: Loopbacks J and K enabled. Internally pulled high.
TXALARM	E4	O	LVTTL (open drain)	Logical OR for alarms in register 1Ex9004 and as enabled by register 1Ex9001. Open-drain output requires external pull-up resistor. Alternate GPO or Tx link/activity LED driver.
TXONOFFI	E10	I	LVTTL	Transmitter data mute. When set HIGH, transmitter is enabled. When set LOW, transmitter is disabled. Internally pulled up. Internal Schmitt trigger.
WANMODE	F14	I	LVTTL	WAN mode select. 0: LAN mode (default). 1: WAN mode. This can be overridden by setting 1xE605.3=1 and 1xE605.2=0. There is an errata item associated with this pin. For more information, see "Errata," page 250.
WIS_INTA	D11	O	LVTTL (open drain)	WIS interrupt A, part of extended WIS. Open-drain output requires external pull-up resistor. Alternate GPO or LED driver.
WIS_INTB	L6	O	LVTTL (open drain)	WIS interrupt B, part of extended WIS. Open-drain output requires external pull-up resistor. Alternate GPO or LED driver.

6.2.7 Phase Detector Outputs

The following table lists the pins associated with phase detector outputs.

Table 319. Phase Detector Output Pins

Name	Number	I/O	Type	Description
EXVCODNN	P2	O	CML	Internal phase frequency detector down, complement
EXVCODNP	M3	O	CML	Internal phase frequency detector down, true
EXVCOUPN	G3	O	CML	Internal phase frequency detector up, complement
EXVCOUPP	M4	O	CML	Internal phase frequency detector up, true

6.2.8 Phase Lockloop Filter Capacitors

The following table lists the pins associated with phase lockloop filter capacitors.

Table 320. Phase Lockloop Filter Capacitor Pins

Name	Number	I/O	Type	Description
CMUFILT	E3		Analog	CMU filter connect capacitor (1 µF) from this pin to ground
CRUFILT	L1		Analog	CRU filter capacitor (1 µF) from this pin to ground

6.2.9 JTAG Interface

The following table lists the pins that control the JTAG test access port.

Table 321. JTAG Interface Pins

Name	Number	I/O	Type	Description
TCK	T3	I	LVTTL	JTAG test access port test clock input. Internally pulled up.
TDI	P4	I	LVTTL	JTAG test access port test data input. Internally pulled up.
TDO	R3	O	LVTTL	JTAG test access port test data output.
TMS	N4	I	LVTTL	JTAG test access port test mode select input. Internally pulled up.
TRSTB	T2	I	LVTTL	JTAG test access port test logic reset input. Internally pulled up. For TAP controller reset, this input must be pulled low. In normal operation, this pin should be connected to ground.

6.2.10 Power and Ground

The following table lists the pins used for power and ground.

Table 322. Power and Ground Pins

Name	Number	I/O	Description
VDD12PCS	G9 K9	Power	1.2 V power supply (PCS).
VDD12RX	H6 J6	Power	1.2 V power for PMA serial 10-gigabit Rx.
VDD12TX	G4 H4 H5	Power	1.2 V power for PMA serial 10-gigabit Tx.
VDD12X	G14 H14 J14 K14 L14	Power	1.2 V power supply for XAUI I/O.

Table 322. Power and Ground Pins *(continued)*

Name	Number	I/O	Description
VDDA12	F11 F12 G11 G12 H11 H12 J11 J12 K11 L11	Power	1.2 V analog power supply for XAUI I/O.
VDDHTL	G8 H8 H9 J8 J9 K8	Power	HSTL I/O 1.5 V power supply. Left open if XGMII is not used.
VDDTTL	G6 K6	Power	TTL power supply (1.2 V, 1.5 V, 1.8 V, or 3.3 V).
VSS	A3, B3, C1, C2, C3, D2, D3, E2, E11, E12, F1, F2, F5, F10, F13, G1, G2, G5, G7, G10, G13, G15, H2, H3, H7, H10, H13, H16, J2, J7, J10, J13, J16, K1, K2, K4, K5, K7, K10, K13, K15, L2, L3, L5, L13, M1, M2, M11, M12, N2, P3, R1	GND	Ground.

6.3 Pins by Number

This section provides a numeric list of the VSC8486 pins.

A1	NC
A2	REFCKP
A3	VSS
A4	TXD1
A5	TXD5
A6	TXD8
A7	TXD12
A8	TXC1
A9	TXD18
A10	TXD22
A11	XTX3N
A12	XTX3P
A13	TXD27
A14	XRX3N
A15	XRX3P
A16	NC
B1	REFCKN
B2	REFTERM
B3	VSS
B4	TXD0
B5	TXD4
B6	TXC0
B7	TXD11
B8	TXD15
B9	TXD17
B10	TXD21
B11	TXC2
B12	TXD25
B13	TXD26
B14	TXD29
B15	TXD30
B16	TXD31
C1	VSS
C2	VSS
C3	VSS
C4	RXALARM
C5	TXD3
C6	TXD7
C7	TXD10
C8	TXD14
C9	TXD16
C10	TXD20
C11	TXD23
C12	TXD24
C13	HVREF
C14	TXD28
C15	TXC3
C16	XTX2N
D1	WREFCKP
D2	VSS
D3	VSS
D4	VREFCKP
D5	TXD2
D6	TXD6
D7	TXD9
D8	TXD13
D9	TXCLK
D10	TXD19
D11	WIS_INTA
D12	FORCEAIS
D13	LOPC
D14	CLK64A_EN
D15	LP_XAUI
D16	XTX2P
E1	WREFCKN
E2	VSS
E3	CMUFILT
E4	TXALARM
E5	LASI
E6	NC
E7	REFSEL0
E8	SPLITLOOPN
E9	NC
E10	TXONOFFI
E11	VSS
E12	VSS
E13	LPP_10B
E14	LP_16B
E15	LP_XGMII
E16	NC
F1	VSS
F2	VSS
F3	NC
F4	VREFCKN
F5	VSS
F6	PMTICK
F7	NC
F8	NC
F9	RFPOUT
F10	VSS
F11	VDDA12
F12	VDDA12
F13	VSS
F14	WANMODE
F15	XAUIFILT
F16	XRX2N
G1	VSS
G2	VSS
G3	EXVCOUPN
G4	VDD12TX
G5	VSS
G6	VDDTTL
G7	VSS
G8	VDDHTL
G9	VDD12PCS
G10	VSS
G11	VDDA12
G12	VDDA12
G13	VSS
G14	VDD12X
G15	VSS
G16	XRX2P
H1	TXDOUTP
H2	VSS

Pins by number *(continued)*

H3	VSS
H4	VDD12TX
H5	VDD12TX
H6	VDD12RX
H7	VSS
H8	VDDHTL
H9	VDDHTL
H10	VSS
H11	VDDA12
H12	VDDA12
H13	VSS
H14	VDD12X
H15	RCLKOUT
H16	VSS
J1	TXDOUTN
J2	VSS
J3	CLK64AP
J4	CLK64BP
J5	CLK64BN
J6	VDD12RX
J7	VSS
J8	VDDHTL
J9	VDDHTL
J10	VSS
J11	VDDA12
J12	VDDA12
J13	VSS
J14	VDD12X
J15	RDAOUT
J16	VSS
K1	VSS
K2	VSS
K3	CLK64AN
K4	VSS
K5	VSS
K6	VDDTTL
K7	VSS
K8	VDDHTL
K9	VDD12PCS
K10	VSS
K11	VDDA12
K12	TCLKOUT
K13	VSS
K14	VDD12X
K15	VSS
K16	XTX1N
L1	CRUFILT
L2	VSS
L3	VSS
L4	MDIO
L5	VSS
L6	WIS_INTB
L7	MDC
L8	RESETN
L9	MSTCODE2
L10	MSTCODE1
L11	VDDA12
L12	TDAIN
L13	VSS
L14	VDD12X
L15	NC
L16	XTX1P
M1	VSS
M2	VSS
M3	EXVCODNP
M4	EXVCOUPP
M5	RXINOFFEN
M6	STWSDA
M7	STWSCL
M8	PRTAD4
M9	PRTAD3
M10	MSTCODE0
M11	VSS
M12	VSS
M13	EPCS
M14	NC
M15	TFPOUT
M16	IOMODESEL
N1	RXINP
N2	VSS
N3	RXINCM
N4	TMS
N5	RXD2
N6	RXD6
N7	RXD9
N8	RXD13
N9	RXCLK
N10	RXD19
N11	PRTAD2
N12	PRTAD1
N13	PRTAD0
N14	AUTONEG
N15	NC
N16	XRX1N
P1	RXINN
P2	EXVCODNN
P3	VSS
P4	TDI
P5	RXD3
P6	RXD7
P7	RXD10
P8	RXD14
P9	RXD16
P10	RXD20
P11	RXD23
P12	RXD24
P13	STWWP
P14	RXD28
P15	RXC3
P16	XRX1P
R1	VSS
R2	NC
R3	TDO
R4	RXD0
R5	RXD4
R6	RXC0
R7	RXD11
R8	RXD15
R9	RXD17
R10	RXD21
R11	RXC2
R12	RXD25
R13	RXD26

Pins by number *(continued)*

R14	RXD29
R15	RXD30
R16	RXD31
T1	NC
T2	TRSTB
T3	TCK
T4	RXD1
T5	RXD5
T6	RXD8
T7	RXD12
T8	RXC1
T9	RXD18
T10	RXD22
T11	XRX0P
T12	XRX0N
T13	RXD27
T14	XTX0P
T15	XTX0N
T16	NC

6.4 Pins by Name

This section provides an alphabetical list of the VSC8486 pins.

AUTONEG	N14
CLK64A_EN	D14
CLK64AN	K3
CLK64AP	J3
CLK64BN	J5
CLK64BP	J4
CMUFILT	E3
CRUFILT	L1
EPCS	M13
EXVCODNN	P2
EXVCODNP	M3
EXVCOUPN	G3
EXVCOUPP	M4
FORCEAIS	D12
HVREF	C13
IOMODESEL	M16
LASI	E5
LOPC	D13
LP_16B	E14
LP_XAUI	D15
LP_XGMII	E15
LPP_10B	E13
MDC	L7
MDIO	L4
MSTCODE0	M10
MSTCODE1	L10
MSTCODE2	L9
NC	A1
NC	A16
NC	E6
NC	E9
NC	E16
NC	F3
NC	F7
NC	F8
NC	L15
NC	M14
NC	N15
NC	R2
NC	T1
NC	T16
PMTICK	F6
PRTAD0	N13
PRTAD1	N12
PRTAD2	N11
PRTAD3	M9
PRTAD4	M8
RCLKOUT	H15
RDAOUT	J15
REFCKN	B1
REFCKP	A2
REFSEL0	E7
REFTERM	B2
RESETN	L8
RFPOUT	F9
RXALARM	C4
RXC0	R6
RXC1	T8
RXC2	R11
RXC3	P15
RXCLK	N9
RXD0	R4
RXD1	T4
RXD2	N5
RXD3	P5
RXD4	R5
RXD5	T5
RXD6	N6
RXD7	P6
RXD8	T6
RXD9	N7
RXD10	P7
RXD11	R7
RXD12	T7
RXD13	N8
RXD14	P8
RXD15	R8
RXD16	P9
RXD17	R9
RXD18	T9
RXD19	N10
RXD20	P10
RXD21	R10
RXD22	T10
RXD23	P11
RXD24	P12
RXD25	R12
RXD26	R13
RXD27	T13
RXD28	P14
RXD29	R14
RXD30	R15
RXD31	R16
RXINCM	N3
RXINN	P1
RXINOFFEN	M5
RXINP	N1
SPLITLOOPN	E8
STWSCL	M7
STWSDA	M6
STWWP	P13
TCK	T3
TCLKOUT	K12
TDAIN	L12
TDI	P4
TDO	R3
TFPOUT	M15
TMS	N4
TRSTB	T2
TXALARM	E4
TXC0	B6
TXC1	A8
TXC2	B11
TXC3	C15

Pins by name *(continued)*

TXCLK	D9
TXD0	B4
TXD1	A4
TXD2	D5
TXD3	C5
TXD4	B5
TXD5	A5
TXD6	D6
TXD7	C6
TXD8	A6
TXD9	D7
TXD10	C7
TXD11	B7
TXD12	A7
TXD13	D8
TXD14	C8
TXD15	B8
TXD16	C9
TXD17	B9
TXD18	A9
TXD19	D10
TXD20	C10
TXD21	B10
TXD22	A10
TXD23	C11
TXD24	C12
TXD25	B12
TXD26	B13
TXD27	A13
TXD28	C14
TXD29	B14
TXD30	B15
TXD31	B16
TXDOUTN	J1
TXDOUTP	H1
TXONOFFI	E10
VDD12PCS	G9
VDD12PCS	K9
VDD12RX	H6
VDD12RX	J6
VDD12TX	G4
VDD12TX	H4
VDD12TX	H5
VDD12X	G14
VDD12X	H14
VDD12X	J14
VDD12X	K14
VDD12X	L14
VDDA12	F11
VDDA12	F12
VDDA12	G11
VDDA12	G12
VDDA12	H11
VDDA12	H12
VDDA12	J11
VDDA12	J12
VDDA12	K11
VDDA12	L11
VDDHTL	G8
VDDHTL	H8
VDDHTL	H9
VDDHTL	J8
VDDHTL	J9
VDDHTL	K8
VDDTTL	G6
VDDTTL	K6
VREFCKN	F4
VREFCKP	D4
VSS	A3
VSS	B3
VSS	C1
VSS	C2
VSS	C3
VSS	D2
VSS	D3
VSS	E2
VSS	E11
VSS	E12
VSS	F1
VSS	F2
VSS	F5
VSS	F10
VSS	F13
VSS	G1
VSS	G2
VSS	G5
VSS	G7
VSS	G10
VSS	G13
VSS	G15
VSS	H2
VSS	H3
VSS	H7
VSS	H10
VSS	H13
VSS	H16
VSS	J2
VSS	J7
VSS	J10
VSS	J13
VSS	J16
VSS	K1
VSS	K2
VSS	K4
VSS	K5
VSS	K7
VSS	K10
VSS	K13
VSS	K15
VSS	L2
VSS	L3
VSS	L5
VSS	L13
VSS	M1
VSS	M2
VSS	M11
VSS	M12
VSS	N2
VSS	P3
VSS	R1
WANMODE	F14
WIS_INTA	D11
WIS_INTB	L6

Pins by name *(continued)*

WREFCKN	E1
WREFCKP	D1
XAUIFILT	F15
XRX0N	T12
XRX0P	T11
XRX1N	N16
XRX1P	P16
XRX2N	F16
XRX2P	G16
XRX3N	A14
XRX3P	A15
XTX0N	T15
XTX0P	T14
XTX1N	K16
XTX1P	L16
XTX2N	C16
XTX2P	D16
XTX3N	A11
XTX3P	A12

7 Package Information

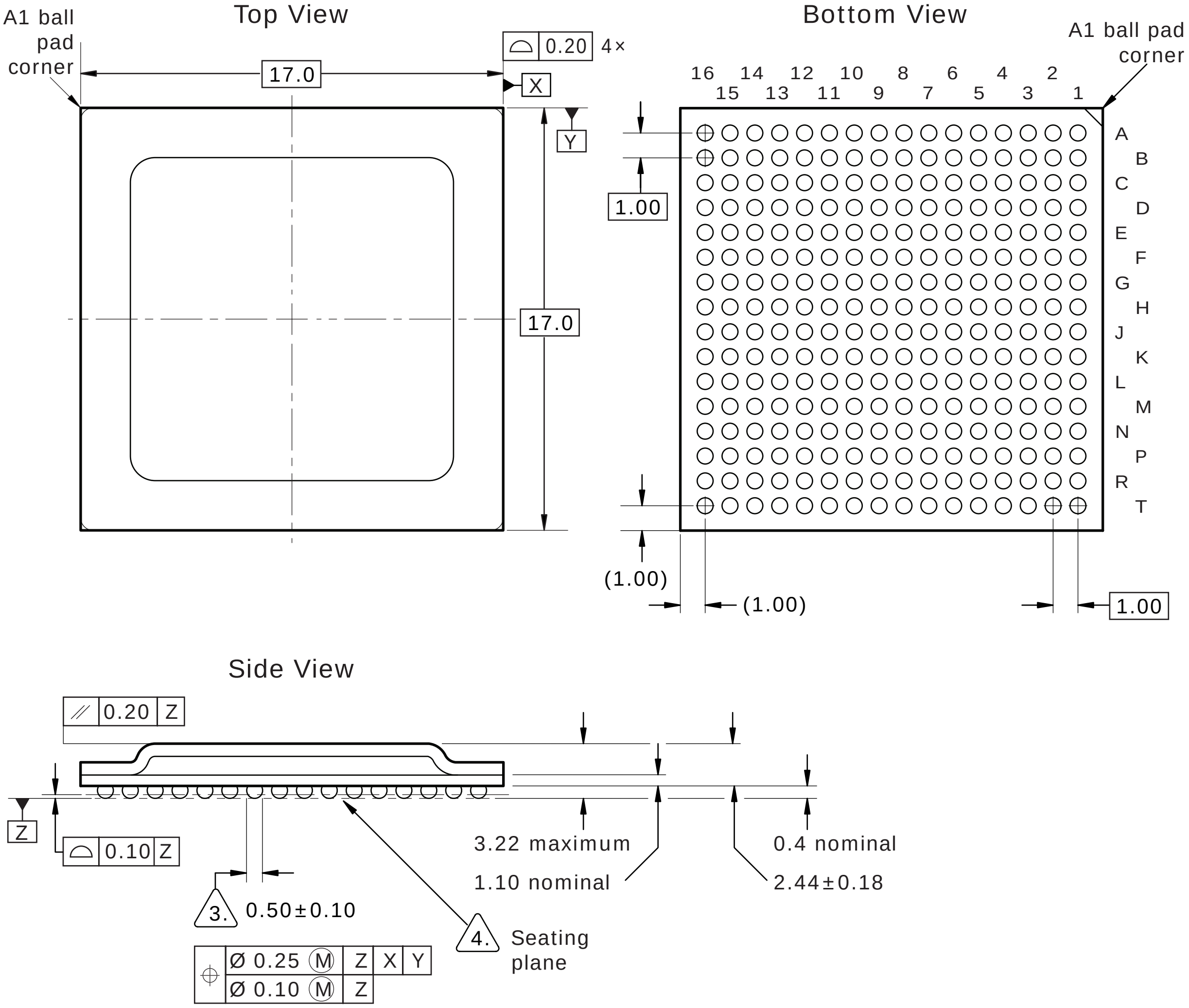
The VSC8486 device is available in two package types. VSC8486SN is a 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 3.22 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC8486XSN.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8486 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8486 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 70. Package Drawing



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. The maximum solder ball matrix size is 16 mm × 16 mm.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 323. Thermal Resistances

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC8486SN	0.9	12	18	16	14
VSC8486XSN	0.9	12	18	16	14

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

7.3 Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. All Vitesse products are rated moisture sensitivity level 4 or better unless specified otherwise. For more information, see the IPC and JEDEC standard.

8 Design Guidelines

This section provides recommended guidelines for designing with the VSC8486 device.

8.1 Power Supply Connection

In XAUI mode, the VSC8486 operates from a single 1.2 V power supply. If XGMII is used, a 1.5 V power supply is required for HSTL I/O only. A 3.3 V LVTTL power supply is used to provide a compatible interface to other devices using low-speed LVTTL I/O. There are no power supply sequence requirements for the VSC8486.

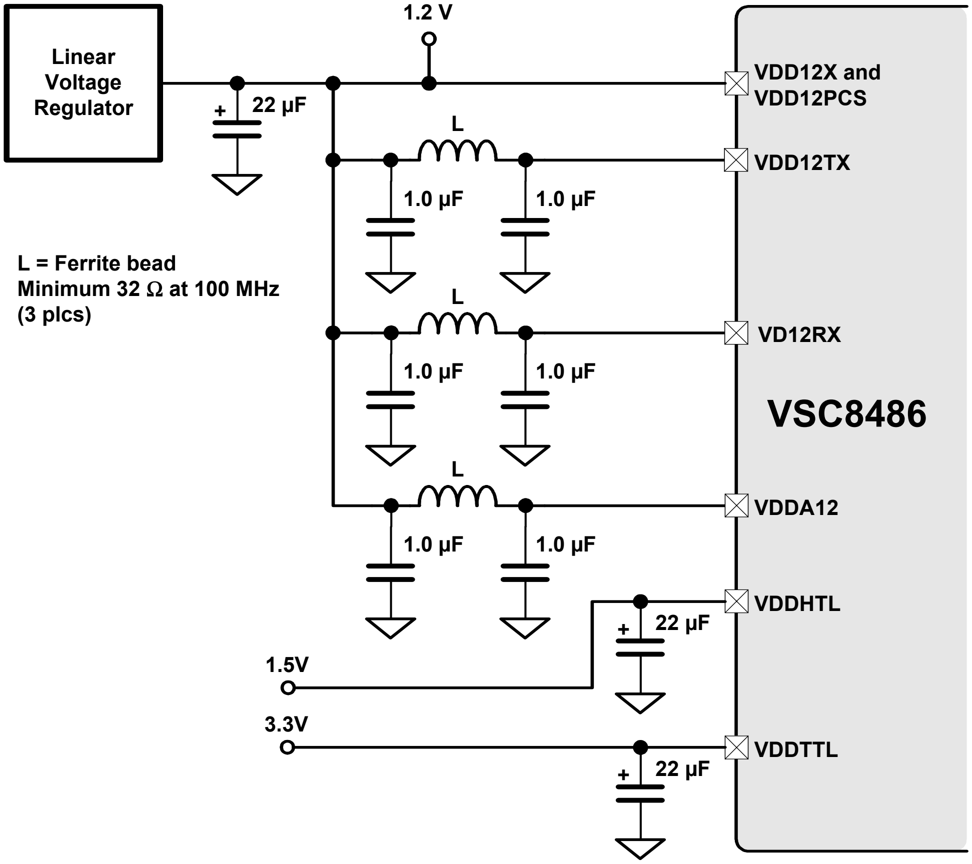
Functional power groups and associated pin locations are summarized in the following table.

Table 324. Power Supply and Pin Locations

Power Supply (DC)	VSC8486 Subsystem	Group Name	Pin Locations	Typical Group Supply Current (LAN Mode)
1.2 V	10-gigabit VCO and Rx PLL	VDD12RX	H6, J6	110 mA
1.2 V	10-gigabit VCO and Tx PLL	VDD12TX	G4, H4, H5	65 mA
1.2 V	XAUI Analog and PLL	VDDA12	F11, F12, G11, G12, H11, H12, J11, J12, K11, L11	70 mA
1.2 V	XAUI	VDD12X	G14, H14, J14, K14, L14	100 mA
1.2 V	PCS	VDD12PCS	G9, K9	220 mA
1.5 V	HSTL I/O	VDDHTL	G8, H8, H9, J8, J9, K8	36 mA
3.3 V	LVTTL I/O	VDDTTL	K6, G6	5 mA
GND		GND	A3, B3, C1, C2, C3, D2, D3, E2, E11, E12, F1, F2, F5, F10, F13, G1, G2, G5, G7, G10, G13, G15, H2, H3, H7, H10, H13, H16, J2, J7, J10, J13, J16, K1, K2, K4, K5, K7, K10, K13, K15, L2, L3, L5, L13, M1, M2, M11, M12, N2, P3, R1	Not applicable

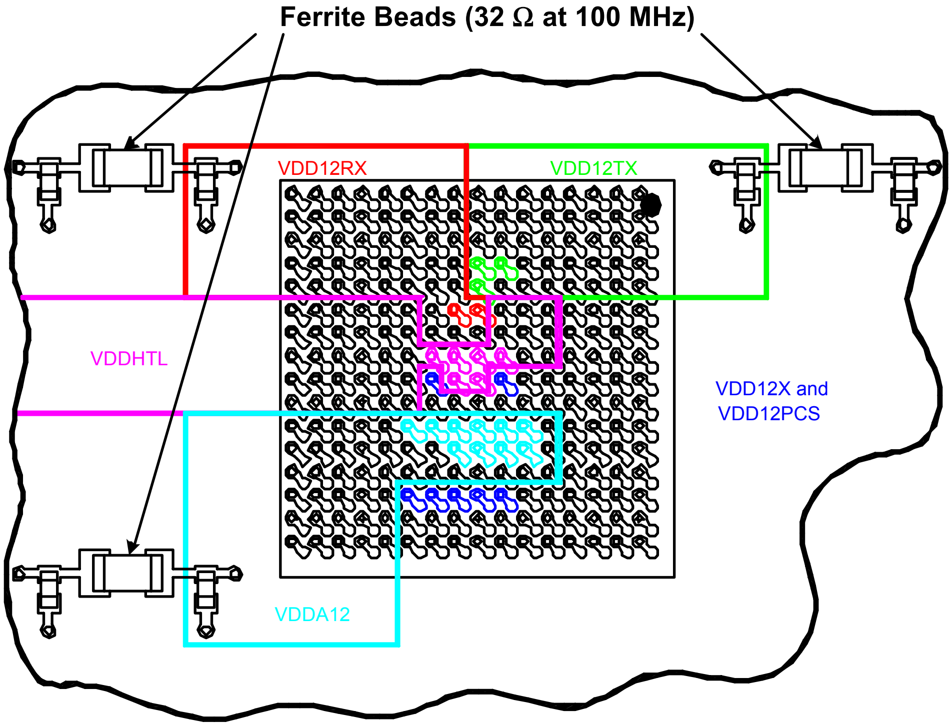
The recommended filter structures for the VSC8486 functional power supply groups are illustrated in the following figure. Although not illustrated, it is recommended each power supply pin have a 0402 size, XR7 dielectric, 0.01 µF ceramic capacitor. Place these capacitors in the pin field, close to the nearest ground pin to minimize connection traces and associated inductance.

Figure 71. Recommended Power Supply Isolation Schematic



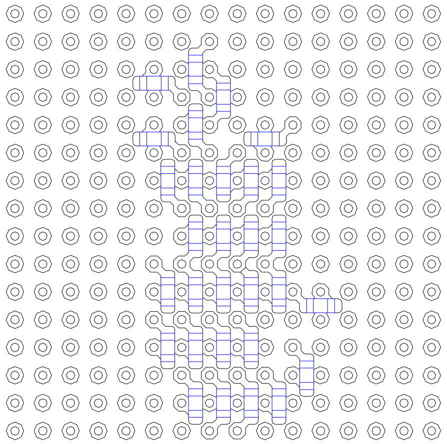
It is recommended to isolate the different 1.2 V power supplies into four different islands on the same PCB layer, as shown in the following figure.

Figure 72. Split Plane Layout Example



The following diagram shows an example of the 0402 size, 0.01 μF decoupling capacitors, located in the pin field.

Figure 73. Decoupling Capacitor Placement Example



9 Errata

This section provides information about the errata for the VSC8486 device. All of the following errata are expected to be resolved in an upcoming revision of the VSC8486 device.

1. For the XGXS test pattern generator, the Fibre Channel CJPAT pattern is only compliant with revision 3.1 of the 10GFC specifications.
2. The REI-P, REI-L, and B2 counters (2x0025, 2x0037, 2x0038, 2x0039, and 2x003A, respectively) might not return to zero after a reset.
3. The B2 and REI-L error counters (2x0037, 2x0038, 2x0039, and 2x003A, respectively) are incorrectly updated. As documented in this datasheet, the registers containing the LSW (2x0037 and 2x0039) are updated upon a read of the registers containing the MSW (2x0037 and 2x0039). Instead, a read of the MSW registers should simply return the LSW value without updating the counter.
4. In the PHY XS receive loss of signal status register (4x8012), the polarity is inverted for bit 5 and bits 3:0. A setting of 0 should indicate a loss of signal for bits 3:0 and a PLL loss of lock for bit 5. A setting of 1 should indicate a signal is present for bits 3:0 and PLL in lock for bit 5.
5. The PMA/WIS system loopback J only works while data is received through the XFI input. If a break in the XFI data link occurs, the loopback J will not function properly.
6. The loss of pointer (LOPP) error flag (2x0021.0) does not assert until after 9 error frames, but it should assert after 8 error frames.
7. As documented in this datasheet, the PCS test pattern counter (3x002B) behaves as a roll-over counter, but it should be a non-rollover counter.
8. The R_TYPE(E) is decoded incorrectly by VSC8486.
9. For MDIO output, there is a delay in the transition from 0 to 1, especially for a 1 followed by several 0's. This delay results from the ESD clamp on VDDMDIO pulling MDIO output to ground. As a possible workaround, use a 500 Ω pull-up resister on MDIO.
10. MDIO write requires one more rising edge. Without this rising edge, the write command will not take effect. As a workaround, add one clock cycle to the end of the write command. **Note** If MDC is constantly running, this is not an issue.
11. In WIS and E-WIS mode, the section trace message (octets J0 and J1) does not increment correctly for 16-byte and 64-byte messages.
12. The pin assignments of the phase detector pins are incorrectly reversed in the device. As documented in this datasheet, the pins for frequency detector down are: EXVCODNN at P2 and EXVCODNP at M3. However, to match the original design, these pins and the pins for frequency detector up (EXVCOUPN at G3 and EXVCOUPP at M4) should be reversed.
13. For the WANMODE pin, the default is internally pulled high.
14. The XAUI LOS feature does not work properly and is currently disabled.

15. The typical value for the single-ended input return loss parameter (S11, 10-Gigabit serial input) is 6 dB, but is currently measured at 4.8 dB. As a workaround, adjust the CRU loop bandwidth at register 1x8000.15:14 and the equalization settings for register 1x8002.14:11.

16. The random jitter for the XAUI output does not meet the IEEE802.3ae recommendation. As a workaround, adjust the de-emphasis level of output to minimize the deterministic jitter, so that the total jitter meets IEEE802.3ae specification.

17. As documented in this datasheet, the default values for register 1x0008 bits 3:1 are 0, but should be 1.

10 Ordering Information

The VSC8486 device is available in two package types. VSC8486SN is a 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 3.22 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC8486XSN.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8486 device.

Table 325. Ordering Information

Part Order Number	Description
VSC8486SN	256-pin FCBGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 3.22 mm maximum height
VSC8486XSN	Lead(Pb)-free (second-level interconnect only), 256-pin FCBGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 3.22 mm maximum height