Marconi
Electronic Devices

Cascade-ALU (Signal Stream™) MA7188

PRELIMINARY INFORMATION

FEATURES

* 16-bit 20MHz ALU with programmable delay of 0 — 31 clock cycles on one input
* 16-function ALU: Add/subtract, absolute value, minimum/maximum selection AND, OR, XOR, XNOR
* Overflow, zero and SGN flags — SGN flag can be used as 17th output bit
* Cascadable for multi-precision arithmetic at 20MHz and to extend the length of programmable delay
* TTL compatible input/output
* Fully static low-power CMOS-SOS
* Standard 68-pin LCC and PGA

APPLICATION

* Cascading MA7180 1-D/2-D convolvers to increase convolution window size and word-lengths
* Combining the outputs of two pipelined systems with the same throughput but different processing latencies
* Fast and low power word-wide ALU for digital signal and image processing applications

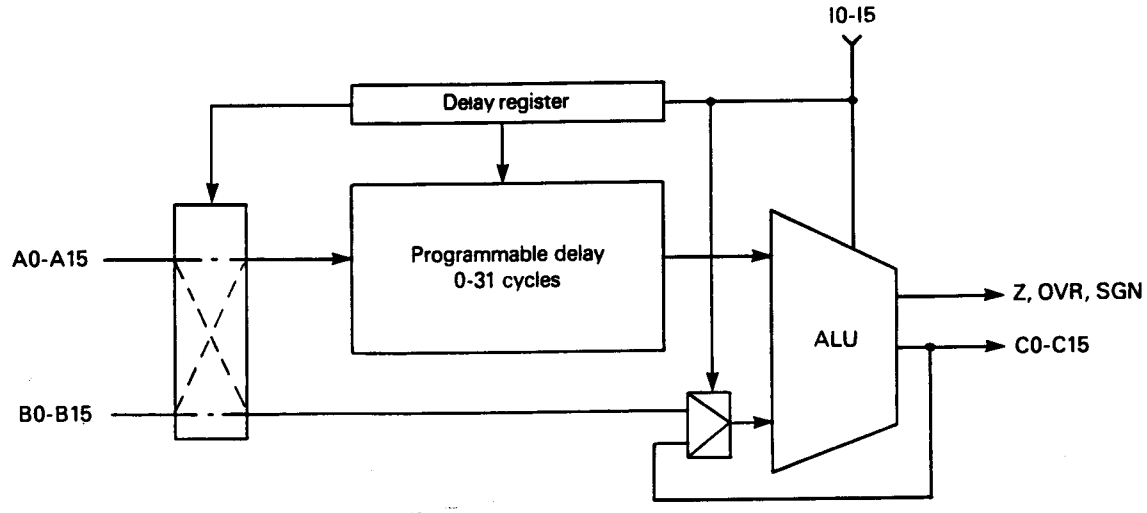
ASSOCIATED DEVICES

* MA7180 1-D/2-D Convolver
* MA7186 Video line buffer
* MA7190 Rank order filter

DESCRIPTION

The MA7188 is a 20MHz 16-bit arithmetic unit with two input ports A and B and an output port C. One of the inputs can be delayed by up to 31 clock cycles prior to ALU operation. This features makes the device very useful in compensating for the difference between the latencies of two pipelined systems, before combining their outputs. The length of the delay can be increased by cascading MA7188 devices or by cascading MA7188 and MA7186. An important application of this latency compensation property is in cascading MA7180 1-D/2-D convolver devices to increase the convolution window size or the wordlengths.

The ALU supports commonly required arithmetic and logic functions. Novel ALU features include absolute value computation and the facility to select the larger or the smaller of the two input operands as the output. Arithmetic overflows can be overcome by using the right shift facility at ALU output. Multiple-precision arithmetic and composite arithmetic operations can be carried out in a single clock cycle using a cascade of devices or in several clock cycles using a single device.



Marconi Electronic Devices Ltd.,
I.C. Division,
Doddington Road,
Lincoln LN6 3LF
Tel. 0522 688121

MEDL
INTEGRATED CIRCUITS

Issue 1 Oct. 87 C106

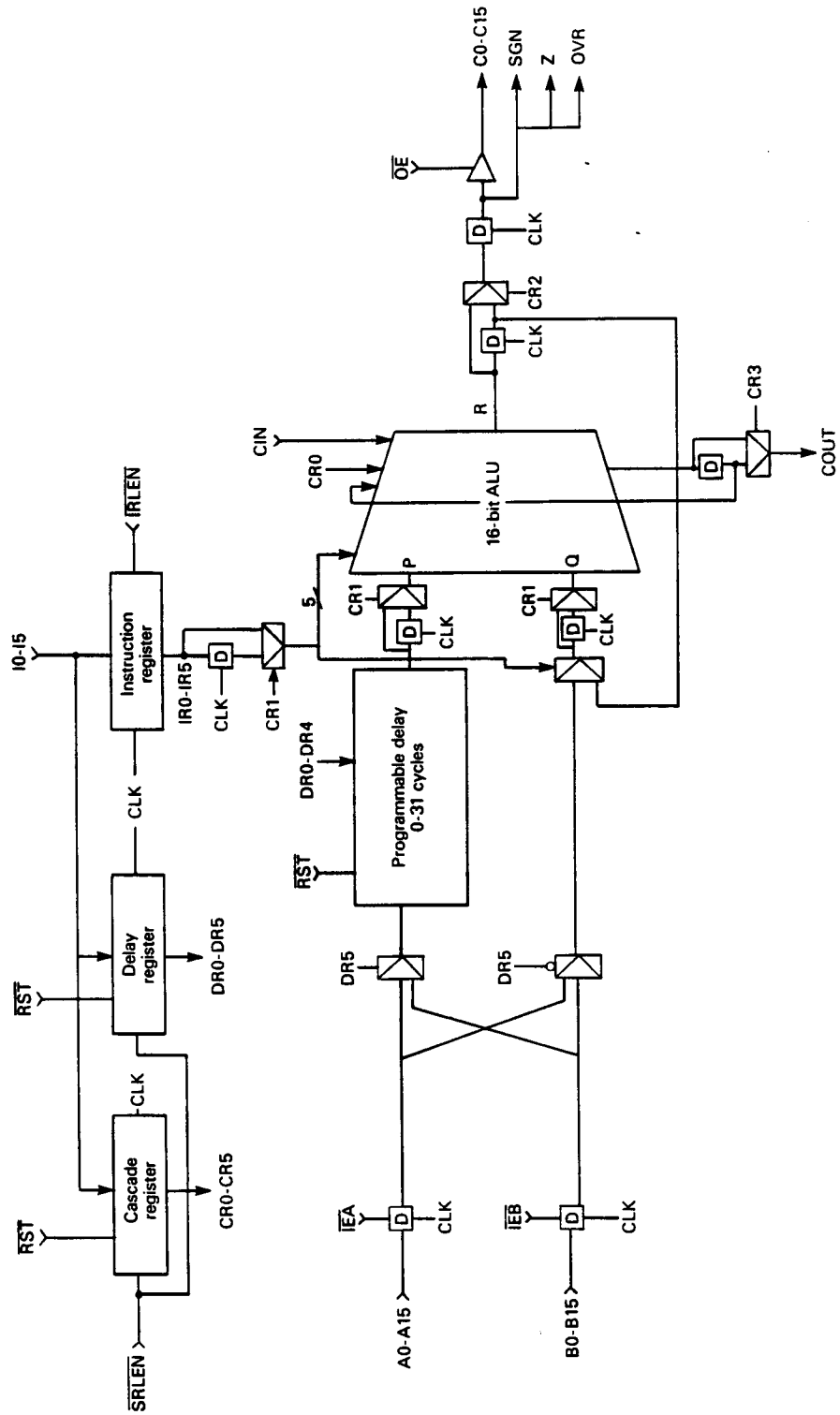


Fig. 1 Functional block diagram of MA7188 Cascade-ALU

MA7188 DETAILED DESCRIPTION

MA7188 is a 16-bit 20MHz arithmetic logic unit. A programmable delay of up to 31 cycles can be applied to either input prior to ALU operation. This programmable delay is very useful for combining the outputs of two pipelined systems with the same throughput but different processing latencies. One of the main applications of this device is in cascading MA7180 1-D/2-D convolvers to increase the convolution window size beyond (3 × 3) or (1 × 9) and data and coefficient wordlengths beyond 10 and 8 bits. A functional block diagram of this device is shown in Figure 1.

The ALU supports the commonly required arithmetic and logic functions. Two novel features of the ALU are absolute value computation and minimum/maximum value selection. The right shift facility is useful for preventing overflows. Alternatively, a 17-bit output can be obtained by using the ALU flag SGN as the 17th bit of the output. Multiple-precision (32-bit, 64-bit) arithmetic can be carried out by cascading devices, with no degradation in the throughput. Multiple-precision arithmetic can also be carried out using a single device in multiple cycles. Absolute value and min/max operations are restricted to 16-bit numbers. The ALU output can be re-cycled as one of the ALU input operands, allowing the implementation of composite operations such as $|P+Q|$ using a single MA7188 device.

Data inputs, outputs and enabling signals

MA7188 has two 16-bit data input ports A0-A15 and B0-B15. The inputs are assumed to be two's complement numbers for arithmetic operations in the ALU.

The inputs A and B are registered on the rising edge of the CLK input, when the input enable signals IEA and IEB are LOW. The inputs A and B are disabled when IEA and IEB are HIGH. These inputs can be disabled only when the length of the programmable delay is zero. Both enable signals IEA and IEB must be held LOW when the length of the programmable delay is non-zero.

The data outputs C0-C15 and the three ALU flags Z, OVR and SGN are available from registers. A new set of outputs will be available following the rising edge of the CLK input. When the output enable signal OE is HIGH the data outputs C0-C15 will be in a high impedance state. The ALU flags are not three-state outputs and are unaffected by the OE input.

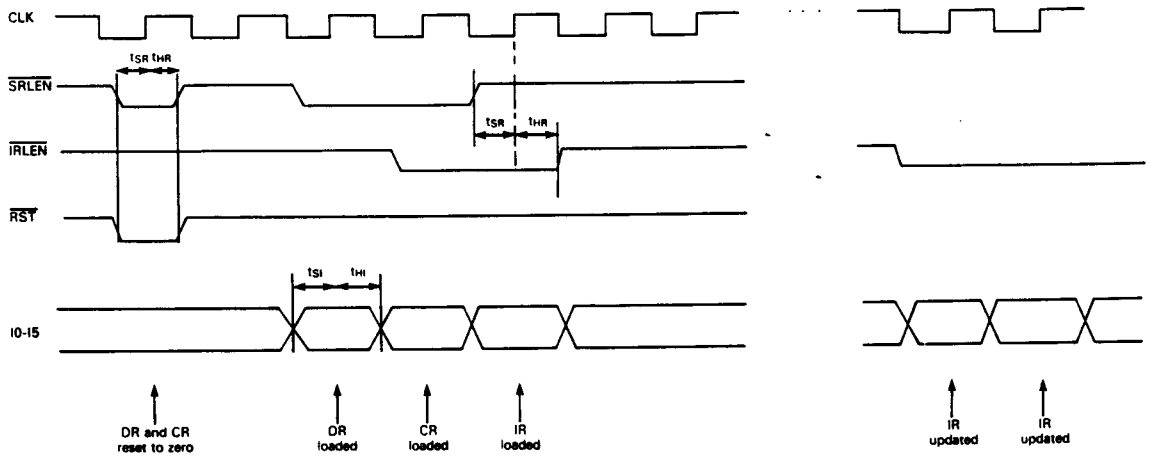
Control registers CR, DR and IR

Three 6-bit control registers, cascade control register CR, delay control register DR and an instruction register IR, are provided to hold the cascade control, programmable delay control and ALU instruction control signals. All three registers are loaded from the 6-bit instruction input port I0-I5 on the rising edge of the CLK input as shown in Figure 2. The register to be loaded is selected using the inputs SRLEN and IRLEN as given by Table 1. Programmable delay and cascade control are static control signals and hence DR and CR can be loaded prior to system operation. After loading CR and DR the SRLEN input may be held HIGH so that the ALU instruction register can, if required, be updated every clock cycle under the control of the IRLEN signal.

The zero-delay and single-chip operating mode is given by zero values in the registers CR and DR (details of the use of these registers are described later). These two registers can be reset to zero by holding the SRLEN and RST signals LOW for a period which includes the rising edge of the CLK input, as shown in Figure 2.

Table 1 Selecting control registers for loading

SRLEN	IRLEN	Control register selected
0	1	Programmable delay control register DR
0	0	Cascade control register CR
1	0	Instruction register IR
1	1	No control registers selected



DR = programmable delay control register CR = cascade control register IR = instruction register

Figure 2 Loading and updating control registers

Programmable delay control

The length of the programmable delay and the input (A or B) to be delayed are determined by the contents of the programmable delay control register DR0-DR5. The five bits DR0-DR4, interpreted as a binary number, specifies the length of the programmable delay in clock cycles. The bit DR5 specifies the input to be delayed. If DR5 = 0 A input is delayed and if DR5 = 1 B input is delayed.

The programmable delay has been implemented using a memory. Hence, after loading the register DR, it is necessary to ensure that this memory is correctly addressed. The simplest method of achieving this is to allow a system initialisation period of 32 or more clock cycles after loading DR and before loading the first data sample (see Figure 3a). This relatively long system initialisation period can be avoided by using the RST input. In this method the first data sample must be loaded in the first clock cycle following the clock cycle in which the system is reset by bringing RST LOW, as shown in Figure 3b. Note that this time in which RST is LOW should include at least one rising edge of the CLK input. It is assumed that the register DR has been loaded prior to bringing RST input LOW (the RST input does not reset the register DR if the SRLEN input is HIGH).

If the length of the programmable delay is N cycles the output of the programmable delay will be undefined for N cycles after applying the first data input. It is not possible to update the register DR whilst preserving the contents of the programmable delay. Hence the device has to be initialised, using any of the two procedures described above, every time the register DR is updated. Any of these procedures need not be followed if the length of the programmable delay is zero. The registers CR and IR can be updated without affecting the programmable delay operation.

Both input enable signals IEA and IEB must be held LOW when the length of the programmable delay is non-zero. The programmable delay is used for latency compensation in pipelined systems and hence input disabling cannot be used in this mode of operation. The input enable signals are useful only when the device is being used as an ALU with the programmable delay length set to zero. The memory used in implementing the programmable delay can be unselected to save power (when the device is not in use) by holding both IEA and IEB signals HIGH. The memory is also unselected when the length of the delay is zero.

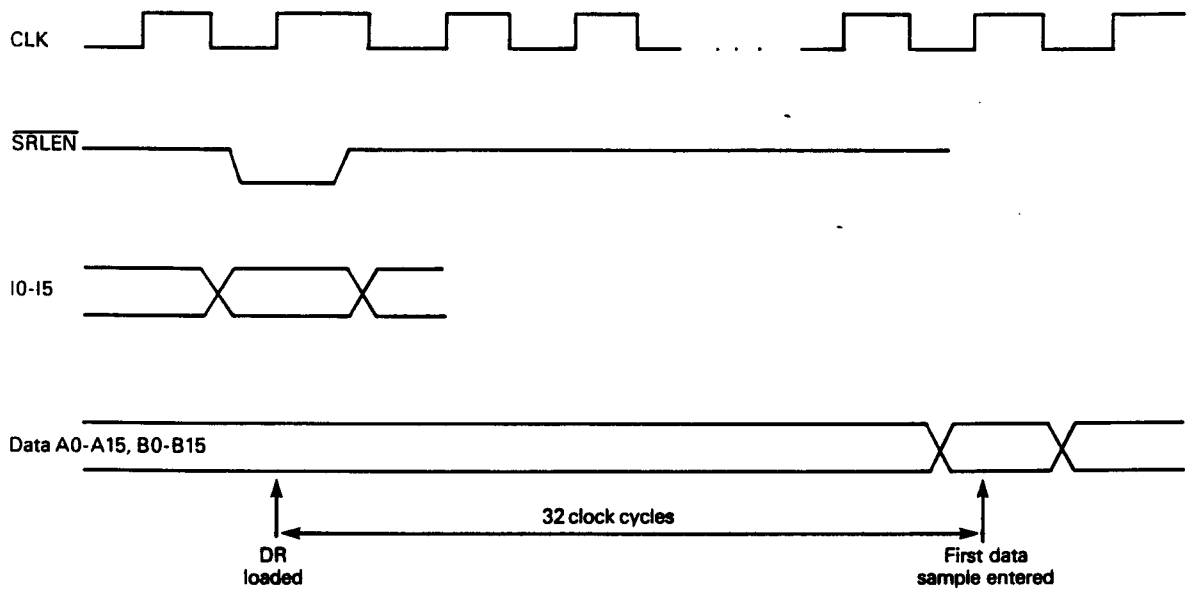


Figure 3a Initialising the programmable delay unit (Method 1)

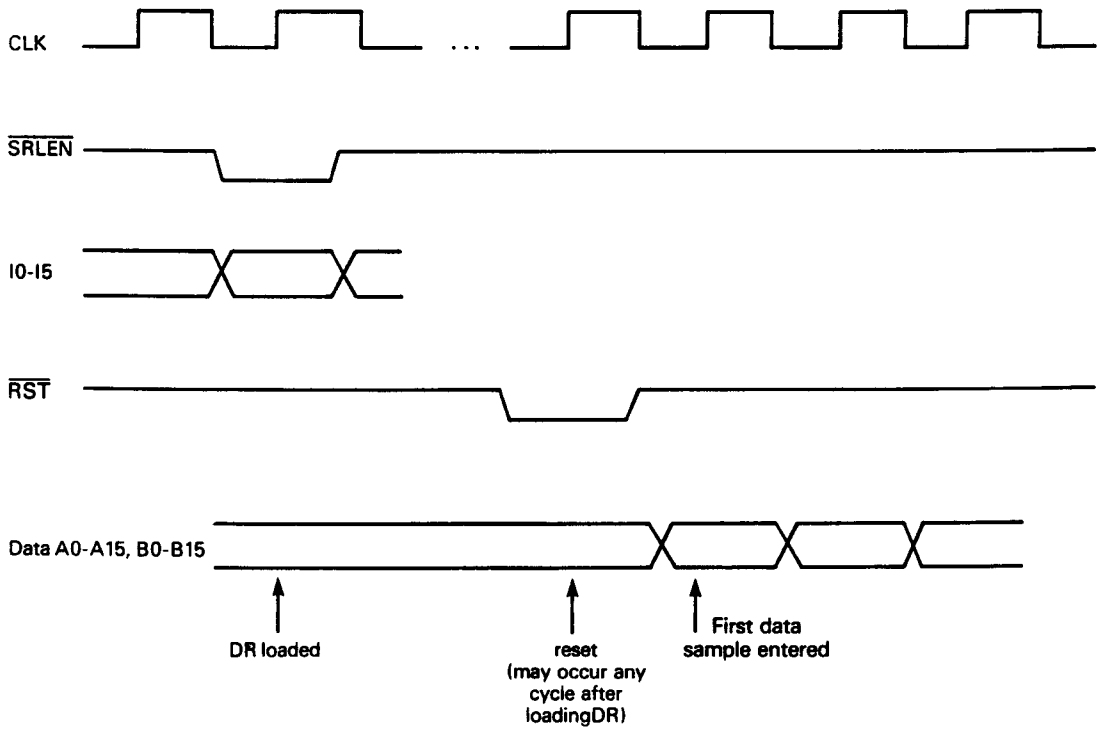


Figure 3b Initialising the programmable delay unit (Method 2)

Cascade control

There are two methods for cascading MA7188 devices, namely, the registered carry method and the ripple-carry method. In the former method the carry input of one device is registered before it is applied to the next most significant device. This is a pipelining technique which allows the 20MHz throughput to be maintained. In the ripple-carry method, the carry output is not registered. Hence the throughput is reduced, but the processing latency remains unaffected. These two cascading techniques are controlled by the first four bits, CR0-CR3, of the CR register. The functions of these signals are given in Table 2 and illustrated in Figure 4. Examples of the use of these control signals for device cascading are shown in Figures 12, 13 and 14. The signals CR4 and CR5 are used for testing and must be set to zero for normal operation.

Table 2 Functions of the cascade control signals

Control signal	Function
CR0	CR0 must be set to 0 for the least significant device and must be set to 1 for all other devices in the cascade. When CR0 = 1 CIN is taken as the carry input to the ALU. When CR0 = 0 the input CIN is disregarded by the ALU.
CR1	If CR1 is set to 1 an additional single clock cycle delay is introduced into the paths of the two operand inputs and the instruction input. If CR1 is set to 0 this additional single clock cycle delay is not introduced.
CR2	If CR2 is set to 1 an additional single clock cycle delay is introduced between the ALU output and the device output C. If CR2 is set to 0 this delay is not introduced.
CR3	If CR3 is set to 0 the carry output COUT is registered. If CR3 is set to 1 COUT is not registered.
CR4, CR5	Used for testing purpose only. Must be set to 0 for normal operation.

ALU operation control

The ALU operations are controlled by the contents of the 6-bit instruction register (IR0-IR5). This register is loaded from the instruction input port I0-I5, on the rising edge of the CLK input, when the IRLEN input is LOW and the SRLEN input is HIGH (refer to Table 1 and Figure 2).

The first four bits of the 6-bit instruction register (IR0-IR3) determine the ALU instruction as given in Table 3. The ALU operations have been defined using internal ALU inputs P and Q since these may not directly correspond to the device inputs A and B.

Absolute value and min/max instructions are two novel features of this ALU. The min instruction selects the smaller of the two input operands as the output. The max instruction selects the larger of the two input operands as the output. For the min and max instructions the SGN flag indicates which of the two inputs has been selected as the output (refer to the description of ALU flags).

Referring to Table 3 it is observed that there are two add instructions and two subtract instructions. For add and subtract operations in category (b) the carry input is taken as the carry output of the previous operation. Hence these instructions are required only when performing multiple-precision arithmetic operations using a single cascade-ALU. The add and subtract instructions in category (b) must be applied in the second and subsequent cycles of this multiple-precision arithmetic operation. For example, to perform a 32-bit addition in two clock cycles using one MA7188, the instruction 1001 is carried out in the first cycle on the 16 l.s.b. inputs and the instruction 0111 is carried out in the second cycle on the 16 m.s.b. inputs.

For arithmetic operations and absolute value operations (categories (a) and (c) of Table 3) the computation result is a 17-bit two's complement number. Hence the arithmetic unit of the ALU always generates a 17-bit result assuming that the two input operands are in two's complement format. This 17th bit of the ALU output is available to the use as the SGN flag. If the SGN flag and C15 are not identical the OVR flag will be set HIGH indicating the presence of an overflow. Overflow can be prevented by shifting the ALU output by one bit towards the least significant bit. IR4 controls this right-shift operation. If IR4 = 1 the 17-bit ALU output is right shifted by one bit and the OVR flag is set LOW. This right shift facility is valid only for arithmetic operations ((a), (b) and (c) of Table 3).

IR5 is used to control the re-cycling of the ALU output to the input port Q of the ALU. If IR5 = 1 the output of the previous clock cycle will be used as input Q of the ALU. This facility is useful for performing composite arithmetic operations such as |P + Q| in two clock cycles using a single device. In the first clock cycle (P + Q) is performed and in the next the absolute value of (P + Q) is obtained. It should be noted that the absolute value instruction is valid only for 16-bit operands. Hence it may be necessary to right shift (P + Q) before absolute value computation.

Table 3 ALU instruction set

	Instruction IR3	IR2	IR1	IR0	Operation	Comments
(a)	1	0	0	1	P + Q	Arithmetic operations
	0	1	0	0	P − Q	
	0	0	1	1	Q − P	
	1	0	0	0	P	
	0	0	1	0	−P	
	1	1	0	1	−Q	
(b)	0	1	1	1	P + Q	Carry output re-cycled internally as the carry input for the next clock cycle
	0	1	0	1	P − Q	
(c)	0	0	0	0	|P|	Absolute value instructions
	1	1	1	1	|Q|	
(d)	1	0	1	1	Min (P, Q)	Selects the smaller or the larger of the two input operands as the output
	1	1	0	0	Max (P, Q)	
(e)	0	0	0	1	P OR Q	Logic operations
	0	1	1	0	P AND Q	
	1	0	1	0	P XOR Q	
	1	1	1	0	P XNOR Q	

ALU flags

MA7188 cascade-ALU produces three status flags Z, OVR and SGN. These flags are available at output from registers, following the rising edge of the CLK input.

Z is the zero flag. A HIGH value on the Z flag indicates that all the ALU outputs are zero.

OVR is the overflow flag. A HIGH value on the OVR flag indicates the presence of an arithmetic overflow in the ALU output. Arithmetic overflows can be prevented using the right-shift facility described under ALU operation control. If a full precision 17-bit output is required SGN flag can be used as the 17th bit of the output.

SGN is the sign flag. The function of this flag depends on the ALU operation. For the ALU operations in categories (a), (b) and (c) the SGN flag is the 17th output bit of the ALU, assuming two's complement input operands. Hence this flag can be used to obtain the true comparison between two operands or to obtain a 17-bit output. For the min/max operations in category (d) of Table 3, the SGN flag indicates which of the ALU inputs has been selected as the output. If SGN flag is HIGH the output is the P input and if SGN flag is LOW the output is the Q input.

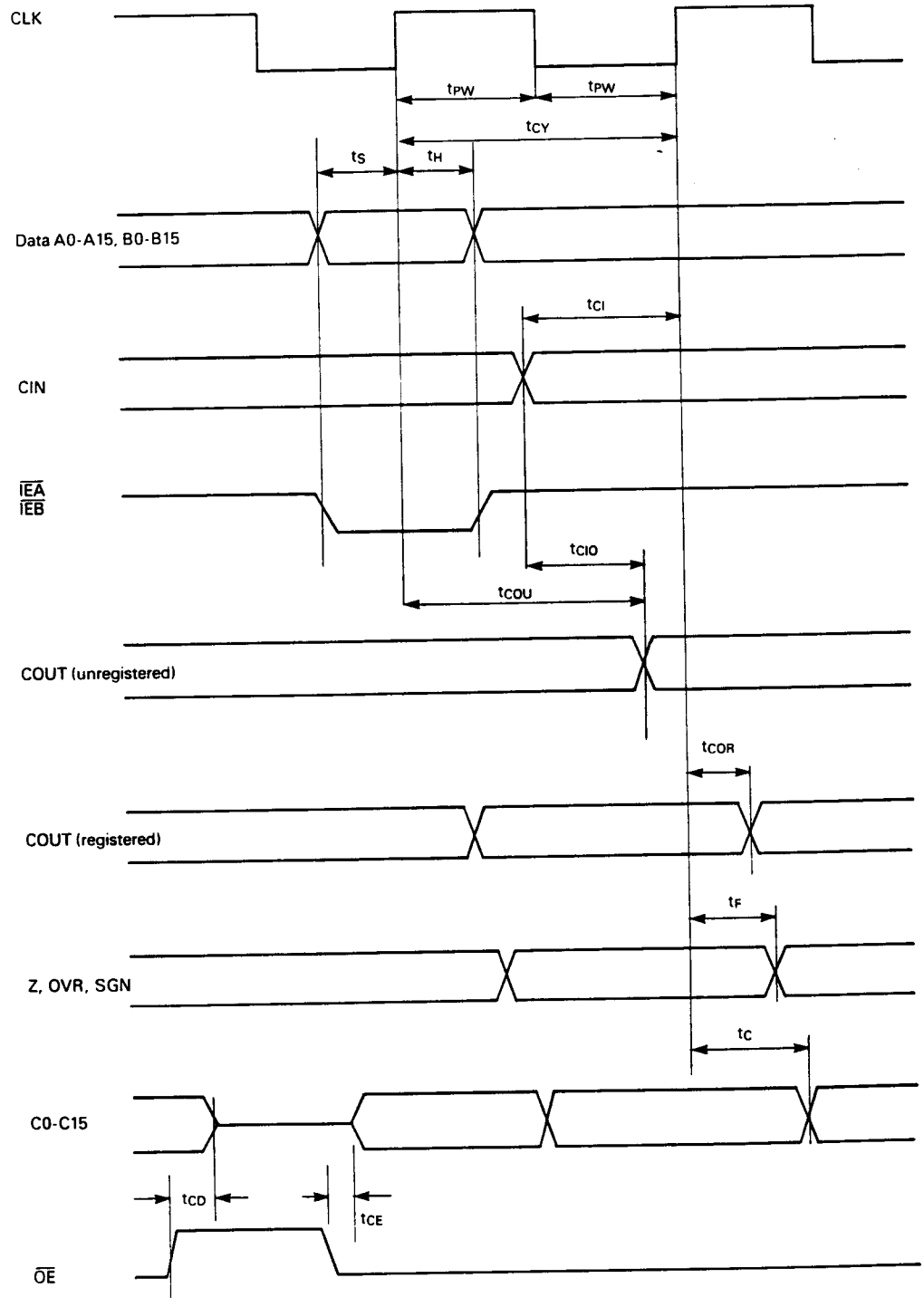


Figure 4 Timing diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max
V_{DD}	Supply Voltage	−0.5V	8V
V_I	Input Voltage	−0.3V	V_{DD} + 0.3V
T_A	Operating Temperature	−55°C	125°C
T_S	Storage Temperature	−65°C	150°C

Stresses above those listed may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING D.C. ELECTRICAL CHARACTERISTICS T_A = −55°C to +125°C, V_{DD} = 5V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	High-level Input Voltage	2.0	–	–	Volts	
V_{IL}	Low-level Input Voltage	–	–	0.8	Volts	
V_{OH}	High-level Output Voltage	2.4	–	–	Volts	V_{DD} = min; I_{OH} = −0.4mA
V_{OL}	Low-level Output Voltage	–	–	0.5	Volts	V_{DD} = min; I_{OL} = 4.0mA
I_{LI}	Input Leakage Current	–	–	10	μA	V_{DD} = max; V_{in} = 0 to V_{DD}
I_{LO}	Output Leakage Current	–	–	10	μA	High Z; V_{DD} = max; V_{out} = 0 to V_{DD}
I_{DD}	Operating Power Supply Current	–	40	60	mA	Output open; V_{IN} = TTL voltage Max clock cycle
I_{DDQ1}	Quiescent Power Supply Current	–	15	25	mA	$V_{in} > V_{IH}$ or $V_{in} < V_{IL}$
I_{DDQ2}	Quiescent Power Supply Current	–	4	25	mA	$V_{in} > V_{DD}$ − 0.2V or $V_{in} < 0.2V$

Note: Typical value measured at V_{DD} = 5.0V and T_A = 25°C

A.C. ELECTRICAL CHARACTERISTICS T_A = −55°C to +125°C, V_{DD} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Figure No.
t_{CY}	Clock period			ns	4
t_{PW}	Clock pulse width			ns	4
t_S	Data set up time			ns	4
t_H	Data hold time			ns	4
t_{SI}	Instruction (I0-I5) set up time			ns	2
t_{HI}	Instruction (I0-I5) hold time			ns	2
t_{SR}	SRLEN, IRLEN and RST set up time			ns	2
t_{HR}	SRLEN, IRLEN and RST hold time			ns	2
t_C	Delay in C output			ns	4

A.C. ELECTRICAL CHARACTERISTICS (continued)

t_{CE}	Enable time for C output			ns	4
t_{CD}	Disable time for C output			ns	4
t_{COR}	Output delay for registered COUT			ns	4
t_{COU}	Output delay for unregistered COUT			ns	4
t_F	Output delay in Z, OVR and SGN flags			ns	4
t_{CIO}	Propagation delay from CIN to unregistered COUT			ns	4
t_{CI}	Set up time for CIN to ensure valid output output following next rising edge of CLK input			ns	4

A.C. CONDITIONS OF TEST

Input pulse level	0 to 3.0 Volts
Input rise and fall times	5ns
Input timing reference levels	1.5 Volts
Output reference levels	1.5 Volts
Output loads	(see Figures 5 and 6)

CAPACITANCE $T_A = 25°C$, $f = 1MHz$

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
CIN	Input capacitance		6	10	pF	V_I = 0V
COUT	Output capacitance		8	12	pF	V_O = 0V

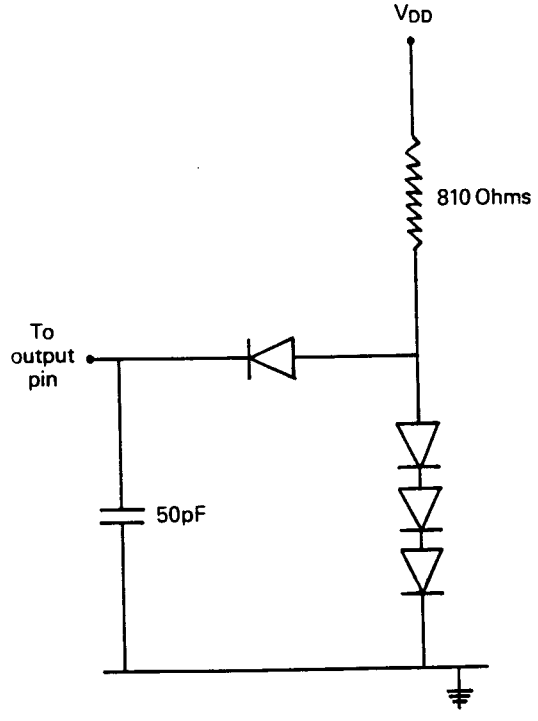


Figure 5 A.C. output test load

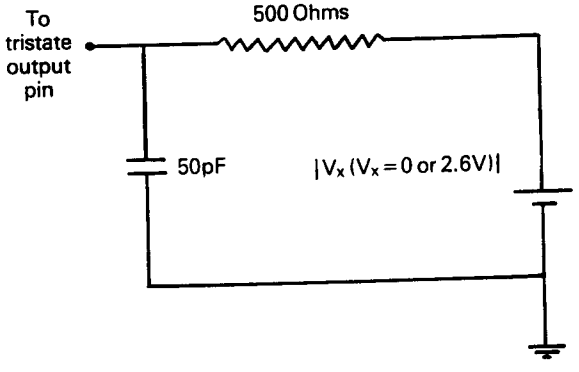


Figure 6 Tristate output delay load

Marconi
Electronic Devices

Cascade-ALU
(Signal Stream™)

MA7188

PRELIMINARY INFORMATION

PIN ASSIGNMENT

Pin No.	Name	I/O	Function
1 - 9	A7 - A15	I	Port A data input
10 - 25	B0 - B15	I	Port B data input
26	COUT	O	Carry output
27	V_{SS}	S	Supply
28 - 43	C15 - C0	O	Port C data output
44	V_{DD}	S	Supply
45	$\overline{OE}$	I	Output enable
46	CLK	I	Clock
47	CI	I	Carry input
48	Z	O	Zero output flag
49	OVR	O	Overflow output flag
50	SGN	O	Sign flag or 17th bit of output
51	$\overline{IEA}$	I	Input enable for A port
52	$\overline{IEB}$	I	Input enable for B port
53 - 58	I5 - I0	I	Instruction input port
59	$\overline{SRLEN}$	I	Control register load enable
60	$\overline{IRLEN}$	I	Control register load enable
61	$\overline{RST}$	I	Reset input
62 - 68	A0 - A6	I	Port A data input

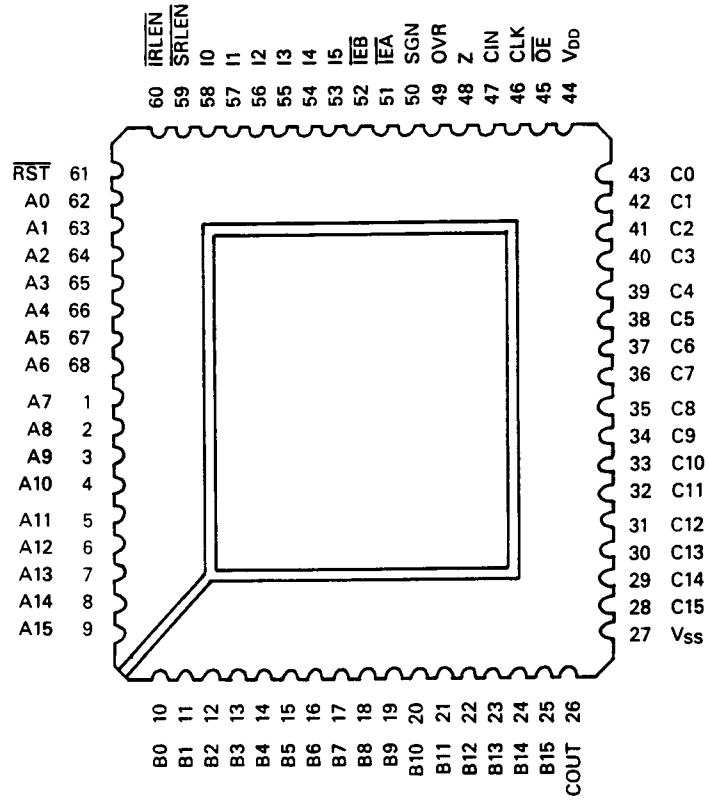


Figure 7 MA7188 cascade-ALU

PIN DESCRIPTION

A0-A15	16-bit data input A inputs are registered on the rising edge of the CLK input, when IEA is LOW.
B0-B15	16-bit data input B inputs are registered on the rising edge of the CLK input, when IEB is LOW.
$\overline{IEA}$	Input enable for the A input Loading of A data inputs is enabled when IEA is LOW and disabled when IEA is HIGH. IEA must be held LOW when the length of the programmable delay is non-zero.
$\overline{IEB}$	Input enable for the B input Loading of B data inputs is enabled when IEB is LOW and disabled when IEB is HIGH. IEB must be held LOW when the length of the programmable delay is non-zero.
I0-I5	6-bit instruction input port These inputs are used to load the instruction register IR, cascade control register CR and the programmable delay control register DR. The register to be loaded is selected using the inputs SRLEN and IRLEN, as given in Table 1. The selected register is loaded on the rising edge of the CLK input.
$\overline{SRLEN}$, $\overline{IRLEN}$	CR, DR and IR control register load enable signals. Active LOW.
$\overline{RST}$	Reset input The programmable delay control register and the cascade control register are reset to zero on the rising edge of the CLK input when both SRLEN and RST are LOW. RST is also used to reset the programmable delay unit as described under programmable delay control.
C0-C15	16-bit three-state data output These outputs are available from a register following the rising edge of the CLK input, provided the output enable input OE is LOW. When the OE is HIGH the outputs are in the high impedance state.
$\overline{OE}$	Output enable control signal. Active LOW.
Z	Zero output flag This flag is HIGH when all 16 ALU outputs are zero. Z is available from a register following the rising edge of the CLK input.
OVR	Overflow output flag This flag is HIGH when there is an arithmetic overflow in the 16-bit output C0-C15. OVR is available from a register following the rising edge of the CLK input.
SGN	Sign flag or the 17th bit of the arithmetic unit output For the arithmetic operations ((a), (b) and (c) of Table 3) this is the 17th bit of the two's complement ALU output. For min/max instructions this flag indicates which of the two input operands to the ALU has been selected as the output. If SGN is LOW then the output is P and if SGN is HIGH then the output is Q. SGN flag is available from a register following the rising edge of the CLK input.
CIN	Unregistered carry input.
COUT	Carry output If the mode control bit CR3 is equal to 0 then CO is available from a register following the rising edge of the CLK input. If CR3 is equal to 1 then CO is an unregistered output.
CLK	System clock input.

Cascade-ALU APPLICATIONS

Latency compensation

One of the main applications of the cascade-ALU is in latency compensation. If it is necessary to combine the outputs of two pipelined systems with the same throughput but different latencies, the programmable delay in the cascade-ALU can be used to compensate for the difference in latencies, as indicated in Figure 8.

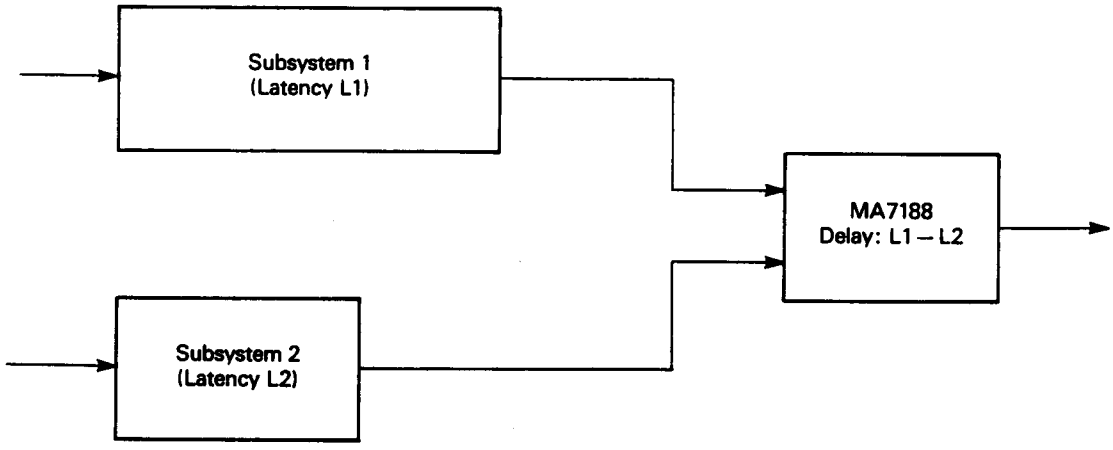


Figure 8 Use of MA7188 for latency compensation

Cascading MA7180 1-D/2-D convolvers

The cascade-ALU is very useful in combining the outputs of MA7180 devices for extending the convolution window size beyond (3 × 3) or (1 × 9) and data and coefficient wordlengths above 10 and 8 bits. Figure 9 shows a 36-stage 1-D convolver designed using four MA7180 devices and three MA7188 devices. Figure 10 shows two possible configurations for a (9 × 9) 2-D convolver using MA7180, MA7186 and MA7188 devices. MA7186 is the video line buffer.

Fast ALU

The cascade-ALU can be used as a fast, low power, word-wide ALU. Absolute value and min/max instructions are particularly useful in digital signal and image processing. The min/max instruction can be used for operations such as hard limiting shown in Figure 11.

Multiple-precision arithmetic

Multiple-precision arithmetic can be performed using a single MA7188 device in multiple clock cycles or using multiple-devices in a single clock cycle. The former method makes use of the re-cycled carry facility and special add/subtract instructions given in Table 3. It is important to note that the absolute value and min/max instructions are limited to 16-bit operations.

Multiple-device, multiple-precision MA7188 systems can be designed using registered-carry or ripple-carry cascade techniques. For 32-bit arithmetic, the former method allows the maximum 20MHz throughput to be maintained. A 32-bit registered carry ALU is shown in Figure 12. To compensate for the delay of the carry bit from one device to another, data inputs and outputs must also be delayed appropriately. This is achieved using the cascade control signals CR0-CR3. The ripple-carry cascading technique results in a reduction in the throughput, but avoids any increase in latency (see Figure 13). Both ripple-carry and registered-carry techniques have been used in the 64-bit ALU shown in Figure 14. The input and output registers and the programmable delay are not shown in the Figures 12, 13 and 14.

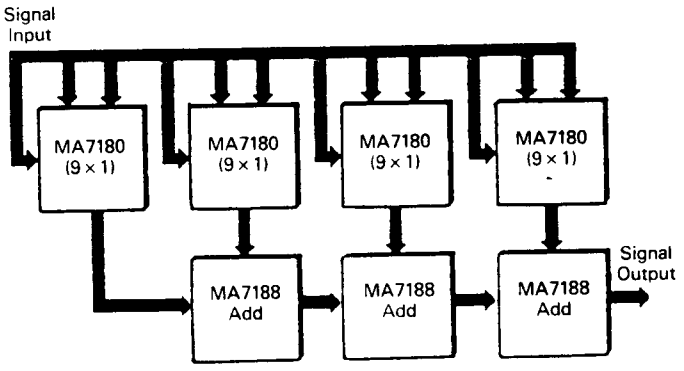


Figure 9 9 (36 x 1) Convolution

Figure 10a (9 x 9) Convolver subsystem

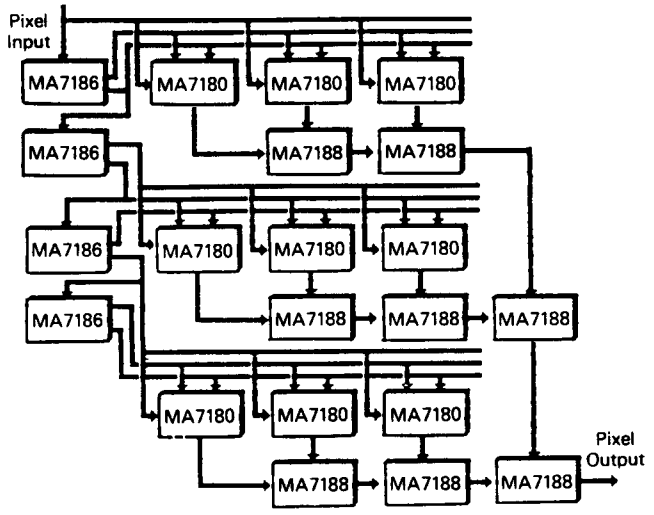
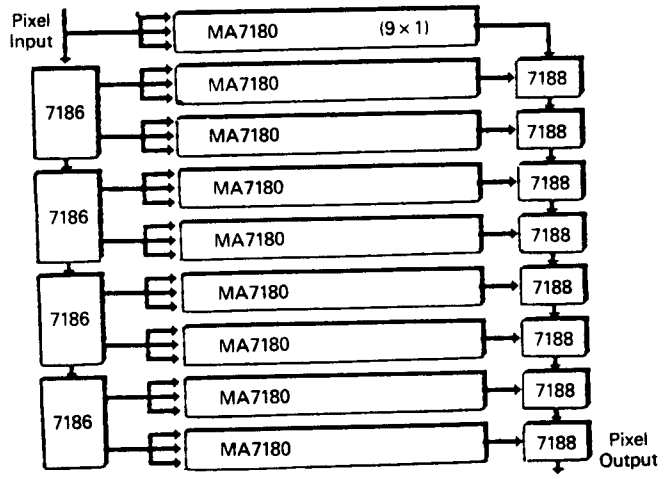


Figure 10b Alternative (9 x 9) Convolver subsystem



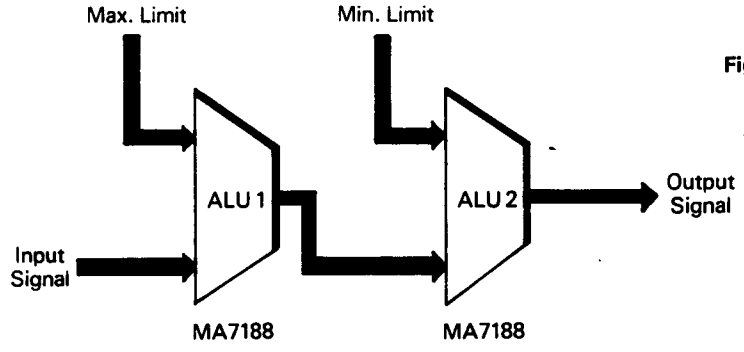


Figure 11

ALU 1 set to Min.
ALU 2 set to Max.

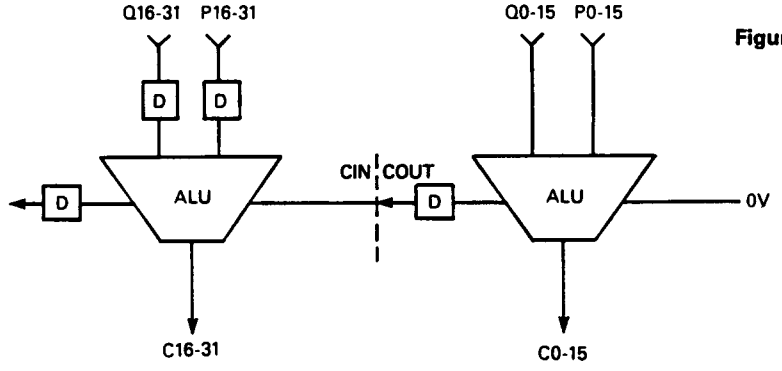


Figure 12

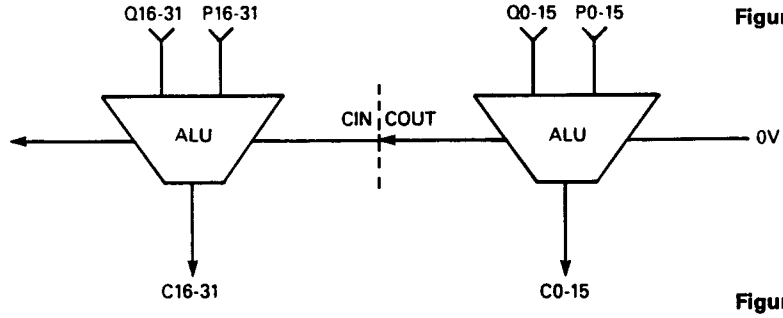


Figure 13

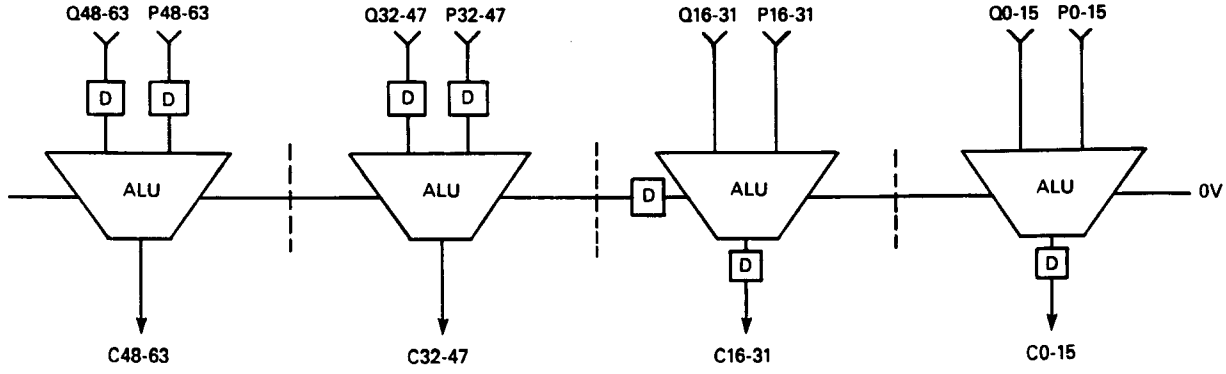
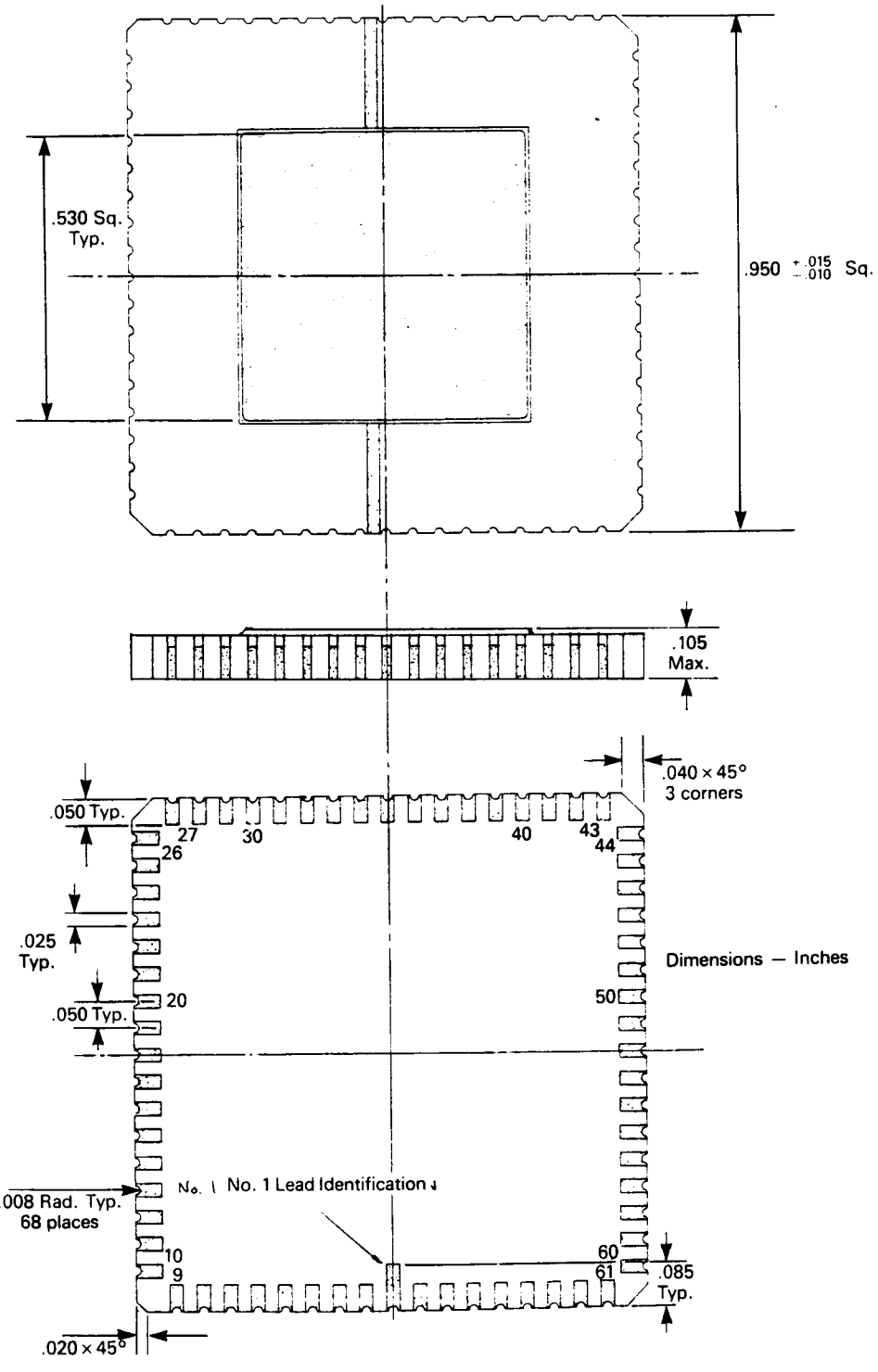


Figure 14

#115



PACKAGE OUTLINE — 68 PIN LEADLESS CHIP CARRIER

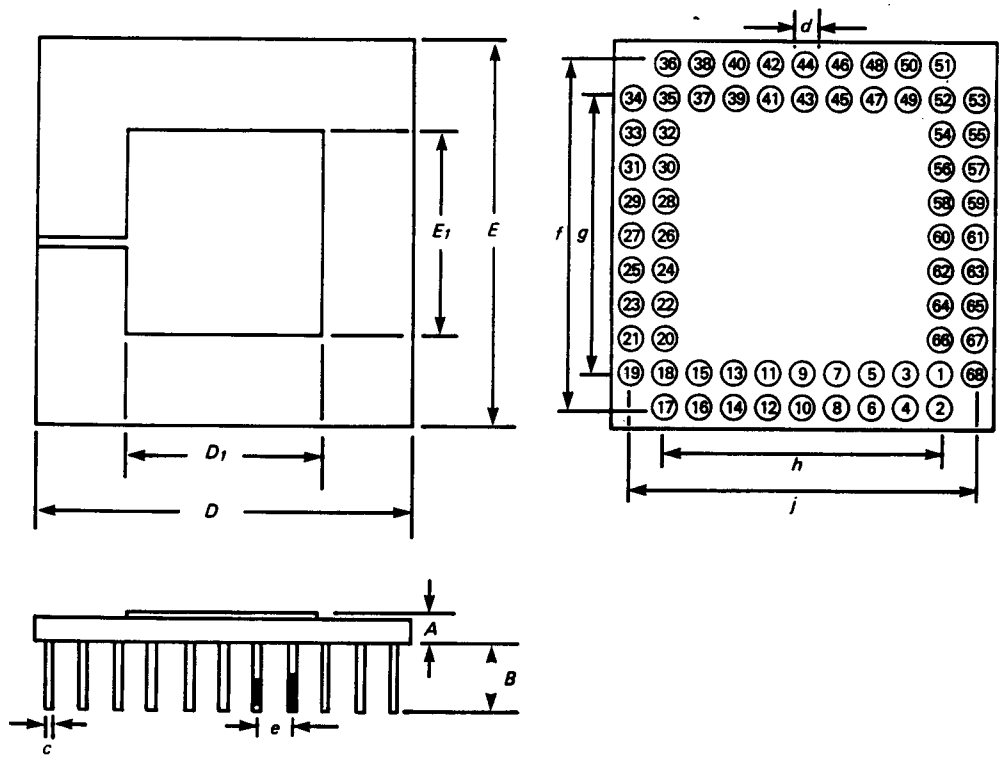
Marconi
Electronic Devices

Cascade–ALU
(Signal Stream™) MA7188

PRELIMINARY INFORMATION

PACKAGE OUTLINE — 68 PIN GRID ARRAY

#196



Symbol	Inches			Millimetres		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.098			2.5
B		0.189			6.8	
c		0.020			0.5	
d		0.055			1.4	
e		0.10			2.54	
E	1.063		1.987	27.6		28.2
E_1			0.529			14.7
D			0.579			16.7
D_1	1.063		1.087	27.6		28.2
f	0.988		1.012	25.1		25.7
g	0.788		0.812	20.29		20.35
h	0.788		0.812	20.29		20.36
j	0.988		1.012	25.1		25.7