

**FEATURES**

- A complete SONET/SDH Transmitter & Receiver
- Complies with Bellcore, ITU/CCITT and ANSI specifications
- Two on-chip PLLs: One for clock generation & another for clock recovery
- SONET framing (defeatable)
- SONET 622.08 Mbit/sec data rates (OC-12)
- Reference frequency of 19.44MHz, 51.84MHz or 77.76MHz
- Compatible with optic modules with and without on-board clock recovery
- TTL/CMOS-compatible parallel I/O
- Differential PECL high-speed serial I/O
- Single +5 volt power supply
- Lock Detect & Frame Detect output
- Compact 100-pin thermally enhanced QFP package
- Typical power dissipation of only 2.8 watts
- Seamless operation with PMC-Sierra's PM5355 S/UNI-622

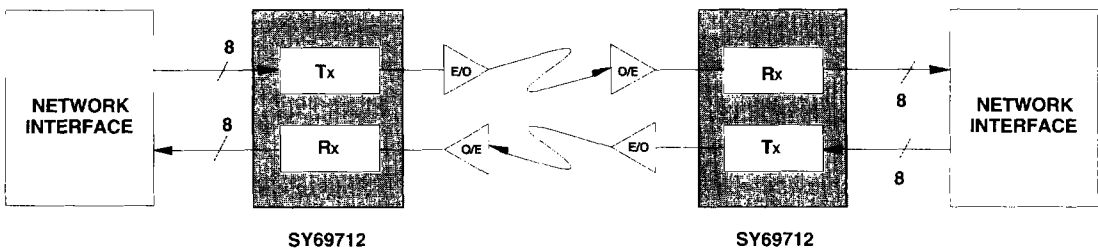
**DESCRIPTION**

Synergy's SY69712 Transceiver with integrated clock recovery contains a fully-integrated SONET OC-12 (622.08 Mbit/s) interface circuit. This device performs all necessary serial-to-parallel and parallel-to-serial conversions per SONET and SDH standards. The SY69712 is manufactured in Synergy's high-performance, highly reliable ASSET technology. It is ideally suited for SONET-based ATM applications.

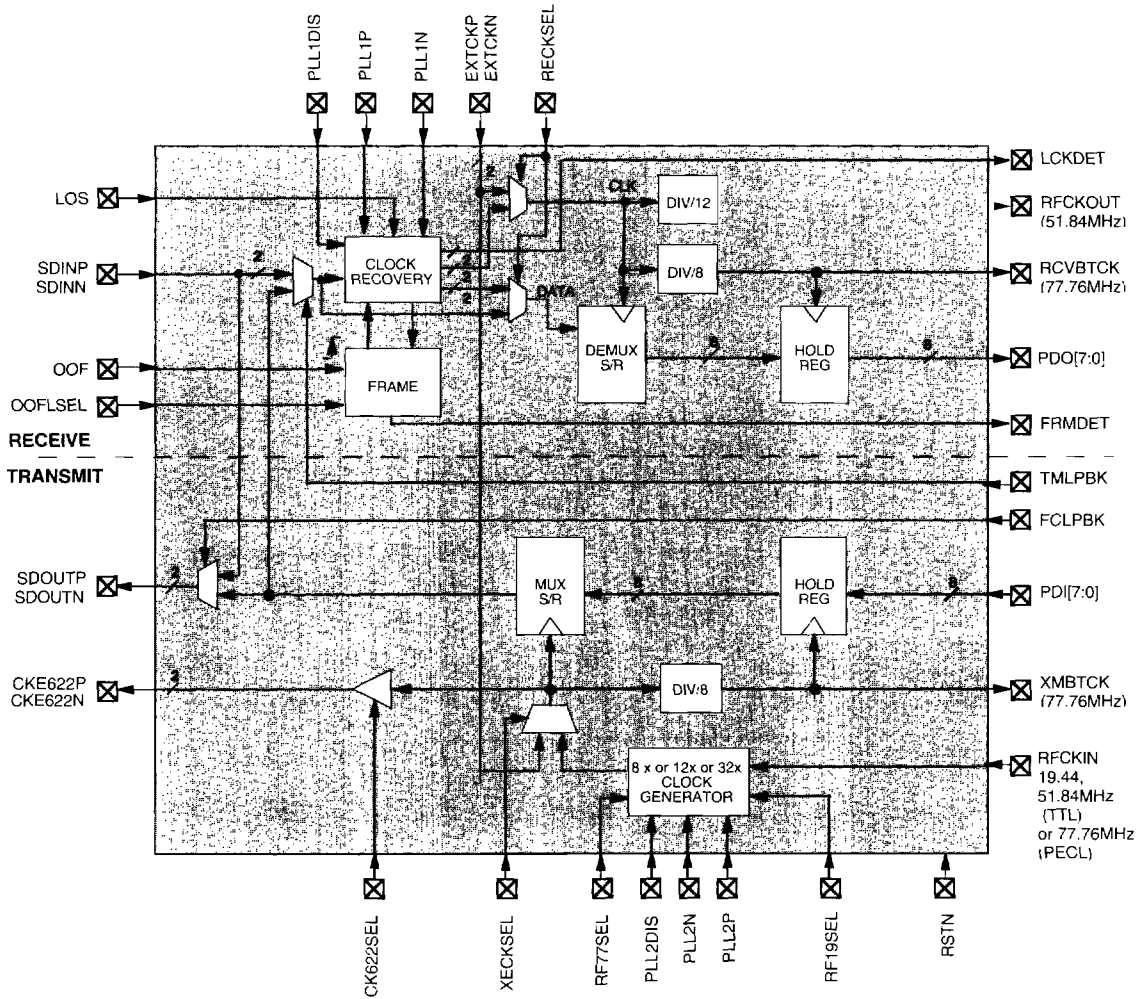
On-chip clock generation is performed by a low-jitter phase-locked loop (PLL), allowing use of the 19.44MHz, 51.84MHz or 77.76MHz clock as a reference. Clock recovery is performed by synchronizing the on-chip VCO directly to the incoming data stream. The SY69712 can also perform SONET/SDH frame detection and alignment on the input data stream.

Compliance with the bit-error rate requirements of the Bellcore, ITU/CCITT and ANSI standards is ensured by Synergy's advanced PLL technology and Positive-ECL (PECL) I/O.

**BLOCK DIAGRAM**

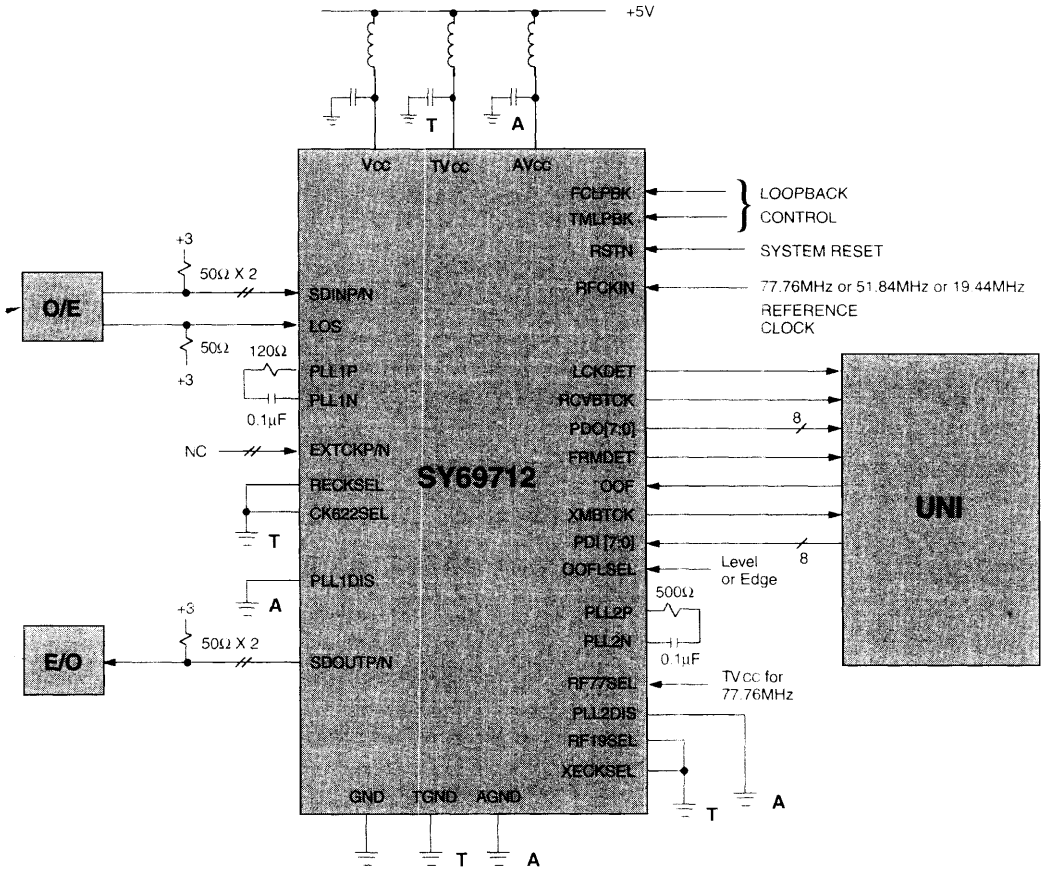


**FUNCTIONAL BLOCK DIAGRAM**

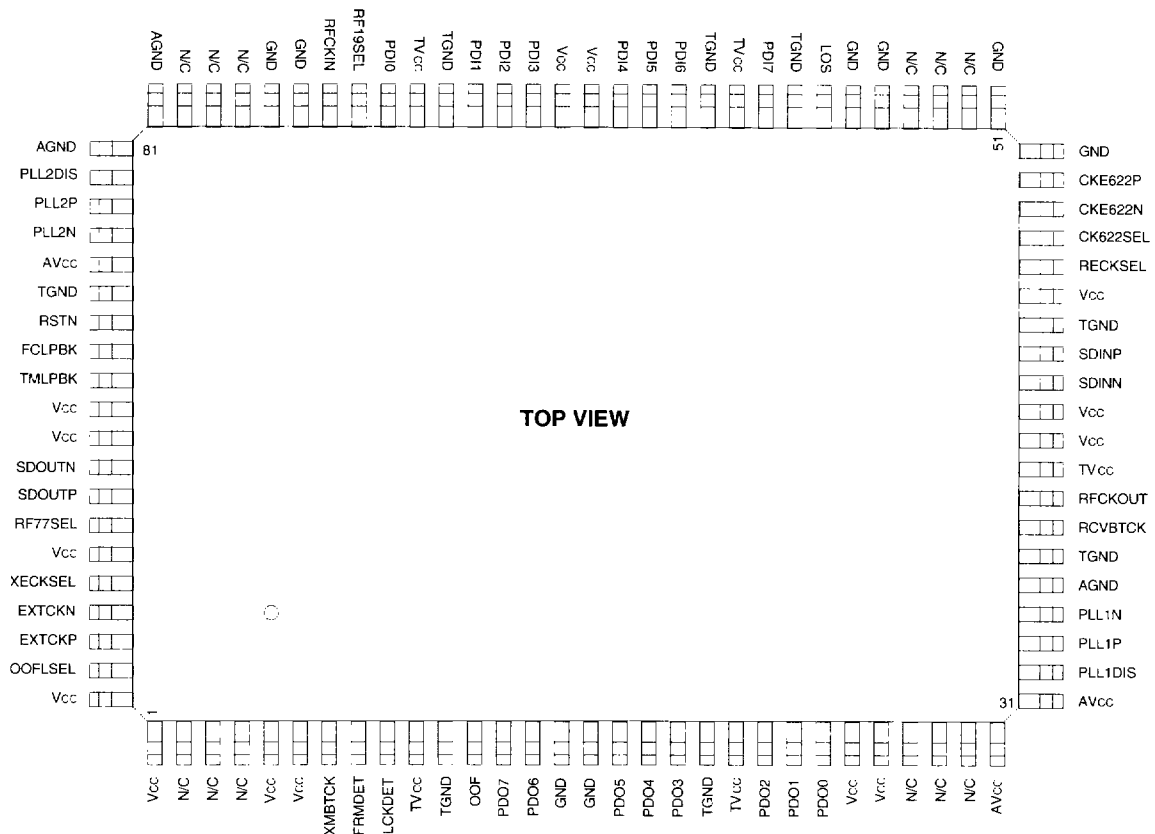


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**SYSTEM CONNECTION DIAGRAM**



**PINOUT**



**2**

**PIN NAMES**

**INPUTS**

**SDINP, SDINN [Serial Data Input]** Differential PECL.  
These pins are normally connected to the optical receiver module. Clock is recovered from the transitions on the SDINP and SDINN inputs.

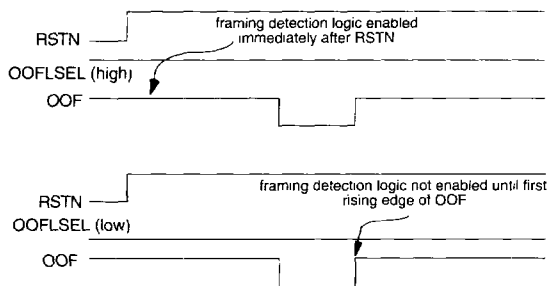
**PDI[7:0] [Parallel Data Input]** TTL.  
A 77.76 Mbyte/s word aligned to the XMBTCK transmit byte clock. PDI7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDI[7:0] is sampled on the rising edge of XMBTCK.

**OOF [Out Of Frame Input]** TTL.  
Signal used to enable/disable the framing pattern detection logic. The framing pattern detection logic is enabled on the rising edge of OOF and remains enabled until frame boundary is detected. OOF is an asynchronous signal with a minimum pulse width of one RCVBTCK period. See OOFSEL signal description.

**OOFSEL [Out of Frame Level]** TTL.  
The purpose of this signal is to determine how the OOF (Out of Frame Input) is treated at power on. If OOFSEL is held low while RSTN is asserted (active low), then the framing pattern detection logic will not be enabled until the first rising edge on OOF after RSTN has gone away (high).

## PIN NAMES (contd.)

If OOFSEL is held high while RSTN is asserted, then the framing pattern detection logic will be enabled as soon as OOF goes high. This means that if OOF is already high during RSTN and remains high (so no rising edge of OOF has occurred), the framing detection logic will still be enabled.



### NOTE:

1. The OOFSEL input only makes a difference at power on. Once the first rising edge of OOF has occurred, the OOF input is treated in exactly the same manner from that point on (whether OOFSEL is high or low). From that point on, the framing detection logic is enabled whenever a low-to-high transition occurs on OOF.

### RFCKIN [Reference Clock Input] TTL/PECL.

Input normally used to generate the XMBTCK. This signal is also used to generate the 'training' frequency for the clock recovery circuit to keep it centered at 622.08MHz in the absence of data coming in on the SDINP, SDINN inputs. The RFCKIN can be either 19.44MHz, 51.84MHz (TTL) or 77.76MHz (PECL, single-ended) and can be selected with RF19SEL and RF77SEL.

### RF77SEL [Reference Clock High Frequency Select Input] TTL.

A low lets the SY69712 default to the RF19SEL pin to determine if this input frequency is 19.44MHz or 51.84MHz. If this pin is high, then the SY69712 will be set for a 77.76MHz (PECL, single-ended) input frequency.

### RF19SEL [Reference Clock Select Input] TTL.

Signal used to select the RFCKIN frequency. A high selects 19.44MHz as the Reference Clock and a low selects 51.84MHz as the Reference Clock. A 51.84MHz or 77.76MHz reference clock should be used in SONET applications.

### LOS [Loss of Signal] PECL.

A single-ended active high input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data Input (SDINP, SDINN) pin will be internally forced to a constant low (zero), LCKDET forced low, and the clock recovery PLL forced to lock to the 622.08MHz clock generated from the RFCKIN. When LOS is low, data on the SDINP, SDINN pins will be processed normally.

### TMLPBK [Terminal Loopback] TTL. (Active Low)

Selects terminal loopback diagnostic mode. When TMLPBK is low, the parallel data presented on PDI[7:0] is looped back via the serial receive side and presented back on the PDO[7:0] along with the recovered clock. Should be high for normal operation.

### FCLPBK [Facility Loopback] TTL. (Active Low)

Selects facility loopback diagnostic mode. When FCLPBK is low, the serial data coming on the SDINP, SDINN pins is routed out via the SDOUTP, SDOUTN pins. Should be high for normal operation.

### RSTN [Master Reset] TTL. (Active Low)

An active low signal that resets the device. Frame detection is disabled after master reset. RSTN must be low for 1 millisecond minimum. Should be HIGH for normal operation.

### PLL1N, PLL1P [Loop Filter 1]

Loop filter pins for the clock recovery PLL.

### PLL2N, PLL2P [Loop Filter 2]

Loop filter pins for the clock synthesis PLL.

### PLL1DIS, PLL2DIS [PLL Disable] TTL.

Normally connected to AGND these inputs can be used to disable the respective PLLs for test purposes. These are active high inputs. i.e. a high on PLL1DIS will disable the clock recovery PLL.

### CK622SEL [622.08MHz Clock Out Select] TTL.

A high on this pin will present the external 622.08MHz clock on the CK622P and CK622N pins. A low disables the output and minimizes noise.

### XECKSEL [Transmit External Clock Select] TTL.

A high on this pin allows the EXTCKP and EXTCKN inputs to be used as the 622.08MHz transmit clock. This is tied to TGND for normal (internal clock recovery) operation.

### RECKSEL [Receive External Clock Select] TTL.

A high on this pin allows the EXTCKP and EXTCKN inputs to be used as recovered clock inputs. This makes it possible to use this device with optical receiver modules that provide on-board clock recovery. This is tied to TGND for normal (internal clock recovery) operation.

### EXTCKP, EXTCKN [External 622.08MHz Clock Input]

Differential PECL.

These pins are normally connected to the optical receiver module that has on-board clock recovery.

## OUTPUTS

### SDOUTP, SDOUTN [Serial Data Output] Differential PECL.

These pins are normally connected to the optical transmitter module.

## PIN NAMES (contd.)

### OUTPUTS (Continued)

#### LCKDET [Lock Detect] TTL.

Active high signal indicating when the internal clock recovery PLL has locked onto the incoming data stream. LCKDET will go high if LOS is low and good data with acceptable run length and transition density is detected on the incoming data stream. LCKDET is an asynchronous output.

#### PDO[7:0] [Parallel Data Output] TTL.

A 77.76 Mbyte/s word aligned to the RCVBTCK receive byte clock. PDO7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDO[7:0] is updated on the falling edge of RCVBTCK.

#### RFCKOUT [Reference Clock Output] TTL.

A 51.84MHz clock provided as a reference clock.

#### RCVBTK [Receive Byte Clock] TTL.

A 77.76MHz clock that is aligned to the PDO7-0 parallel data output. It is a nominally 50% duty cycle clock.

#### XMBTCK [Transmit Byte Clock] TTL.

A 77.76MHz reference clock generated from the RFCKIN pin. It is to be used to coordinate byte transfers for serial transmission. PDI7-0 is sampled on the rising edge of XMBTCK.

#### FRMDET [Frame Detect] TTL.

Indicates SONET frame boundaries in the incoming data stream (SDINP, SDINN). If the framing pattern detection is enabled, with OOF input, FRMDET pulses high for one RCVBTCK cycle when a 48-bit sequence matching the framing pattern is detected on the SDINP, SDINN inputs. FRMDET is updated on the falling edge of RCVBTCLK.

#### CKE622P, CKE622N [622.08 MHz Transmit Clock Output]

Differential PECL.

These pins provide the 622.08MHz transmit clock depending on the state of the CK622SEL pin. When CK622SEL is low the CKE622P will remain high (PECL) and CKE622N will remain low (PECL). These pins can be connected to optical transmit modules that require both data and clock inputs.

#### OTHER

Vcc	ECL +5V
AVcc	Analog +5V
GND	ECL Ground
AGND	Analog Ground
TVcc	TTL +5V
TGND	TTL Ground

#### NOTE:

1. Recommended N/C pins are tied to GND (ECL Ground).

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Rating	Unit
Vcc TVcc, AVcc	Power Supply (GND, TGND, AGND = 0V)	0 to +7	V
Vi	Input Voltage (GND, TGND, AGND = 0V)	0 to Vcc	V
IOUT	Output Current	Continuous	50
		Surge	100
Tj	Junction Temperature Range	0 to +125	°C
Tstore	Storage Temperature Range	-65 to +150	°C

#### NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS<sup>(1), (2), (3)</sup>

VCC = +5V ±5%; VEE = GND = 0V, Tj = 0°C to +125°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>EE</sub>	Internal Operating Current	—	548	—	mA	
I <sub>OUT</sub>	Termination Output Current	—	11	—	mA	50Ω to Vcc -2, 50% duty cycle

#### NOTES:

1. To calculate total power supply current into the Vcc pins:  $I_{cc} = (n \cdot I_{OUT})$ ; where n = number of ECL output pins used (ie, terminated).
2. To calculate total device power dissipation;  $P_D = [I_{EE} \cdot (V_{CC} - V_{EE})] + [n \cdot I_{OUT} \cdot 1.33]^2$ .
3. Average ECL output voltage is calculated as  $VO_{AVG} = (VO_{H(MAX)} + VO_{H(MIN)} + VOL_{(MAX)} + VOL_{(MIN)}) / 4 = 1.33V$ .

### PECL DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = TV<sub>CC</sub> = AV<sub>CC</sub> = 4.75V to 5.25V; GND, TGND, AGND = 0V, T<sub>J</sub> = 0°C to +125°C

Symbol	Parameter	T <sub>J</sub> = 0°C		T <sub>J</sub> = +25°C		T <sub>J</sub> = +65°C		T <sub>J</sub> = +125°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> -1.112	V <sub>CC</sub> -0.897	V <sub>CC</sub> -1.077	V <sub>CC</sub> -0.862	V <sub>CC</sub> -1.025	V <sub>CC</sub> -0.810	V <sub>CC</sub> -0.947	V <sub>CC</sub> -0.732	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.656	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.644	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.620	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.584	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>	V <sub>CC</sub> -1.209	V <sub>CC</sub> -0.888	V <sub>CC</sub> -1.172	V <sub>CC</sub> -0.858	V <sub>CC</sub> -1.125	V <sub>CC</sub> -0.810	V <sub>CC</sub> -1.045	V <sub>CC</sub> -0.738	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.604	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.567	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.520	V <sub>CC</sub> -1.920	V <sub>CC</sub> -1.140	V
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	μA

NOTE:

1. Forcing one input at a time. Apply V<sub>IH</sub> (max) or V<sub>IL</sub> (min) to all other inputs.

### TTL DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = TV<sub>CC</sub> = AV<sub>CC</sub> = 4.75V to 5.25V; GND, TGND, AGND = 0V, T<sub>J</sub> = 0°C to +125°C

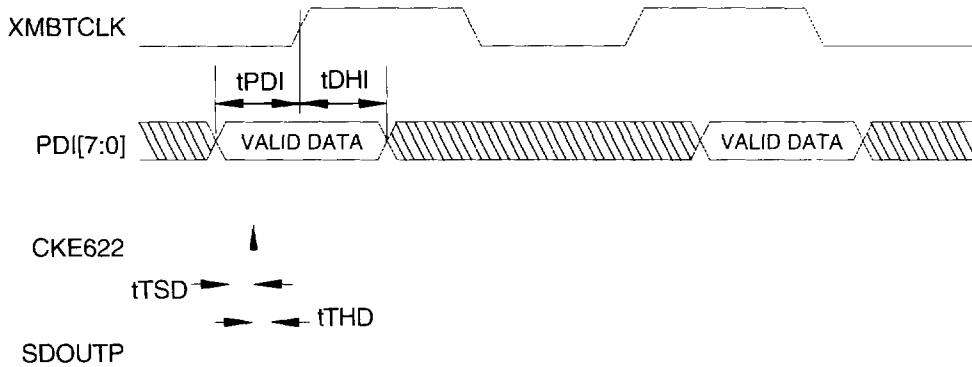
Symbol	Parameter	Min.	Max.	Unit	Condition
V <sub>OH</sub>	Output HIGH Voltage	2.4	—	V	I <sub>OH</sub> = -2mA
V <sub>OL</sub>	Output LOW Voltage	—	0.5	V	I <sub>OL</sub> = 4mA
I <sub>OS</sub>	Output Short Circuit Current	-150	-60	mA	V <sub>OUT</sub> = 0V
V <sub>IH</sub>	Input HIGH Voltage	2.0	—	V	—
V <sub>IL</sub>	Input LOW Voltage	—	0.8	V	—

### AC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = TV<sub>CC</sub> = AV<sub>CC</sub> = 4.75V to 5.25V; GND, TGND, AGND = 0V, T<sub>J</sub> = 0°C to +125°C

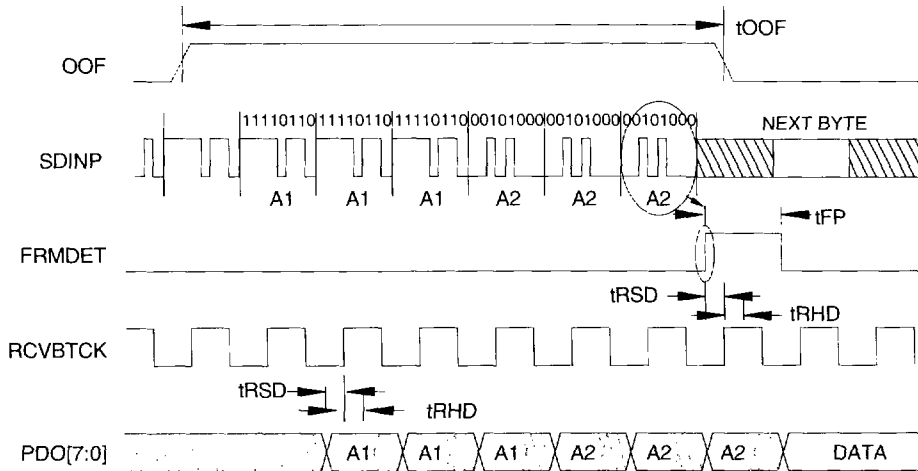
Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency	622.08 ±12%			MHz	Nominal
Reference Clock (RFCKIN) Frequency Tolerance	—	±20	—	ppm	77.76MHz
	—	±20	—	ppm	51.84MHz
	—	±10	—	ppm	19.44MHz
Reference Clock (RFCKIN) Input Duty Cycle	45	—	55	% of UI	
Reference Clock (RFCKOUT) Output Duty Cycle	40	—	60	% of UI	15pF load
Acquisition Lock Time	—	—	15	μsec	
TTL Output Rise/Fall Time	—	—	4	ns	10% to 90% of amplitude, 15pF load
PECL Output Rise/Fall Time	—	—	500	ps	10% to 90%, 50Ω load, 5pF cap
t <sub>PDI</sub> : PDI[7:0] set-up with respect to XMBTCK	1.8	—	—	ns	15pF load
t <sub>DHI</sub> : PDI[7:0] hold time with respect to XMBTCK	1	—	—	ns	15pF load
t <sub>OOF</sub> : OOF pulse width	12.86	—	—	ns	
t <sub>RSO</sub> : PDO[7:0] & FRMDET valid before RCVBTCK	4	—	—	ns	15pF load
t <sub>RHD</sub> : PDO[7:0] & FRMDET valid after RCVBTCK	4	—	—	ns	15pF load
XMBTCK & RCVBTCK Duty Cycle	40	—	60	% of UI	
CKE622 Output Duty Cycle	45	—	55	% of UI	
t <sub>TSD</sub> : SDOUTP valid before CKE622	0.30	—	—	ns	
t <sub>THD</sub> : SDOUTP valid after CKE622	0.30	—	—	ns	
t <sub>RST</sub> : RSTN pulse width	1	—	—	msec	

**TRANSMIT TIMING WAVEFORMS**



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**RECEIVE TIMING WAVEFORMS<sup>(1)</sup>**

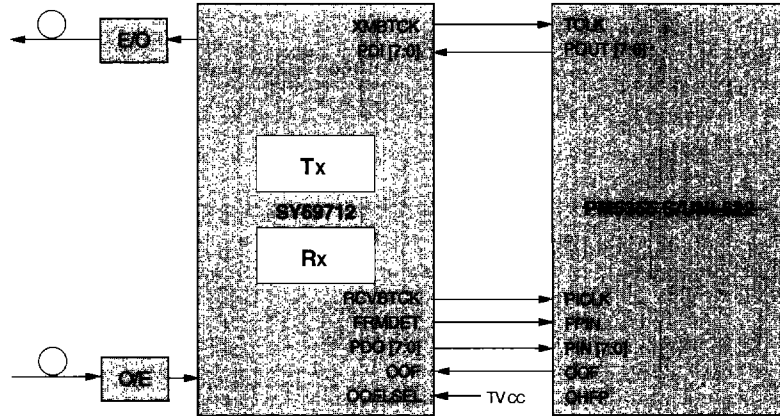


NOTES:

1. The example shown above is for a partial OC-12 framing sequence.

**APPLICATION EXAMPLE**

SY69712 interface with S/UNI-622



**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY69712BC	B100-1	Commercial
SY69712QC	Q100-1	Commercial