

# IEEE-1394 LINK-LAYER CONTROLLER/400M-PHY ONE-CHIP TSB43LV81

SLLS403-December 1999

- Fully Interoperable with FireWire™ Implementation of IEEE-1394 (1995) and IEEE1394.a compliant
  - Interfaces Directly to Texas Instruments TSB11LV01, TSB21LV03 and TSB41LV0X Physical Layer Devices (100/200/400 Mbps) by AUX I/O for more port or Isolation
  - Single 3.3V Supply Operation with 5V Tolerance using 5V bias pins.
  - 400M-PHY One port integrated
  - Automated Read Response for Config-ROM registers
  - Automated Single Retry Protocol and Split Transaction control
  - Support up to 4 initiators by automated Transaction and could support more by firmware(SBP2 Protocol)
  - Management ORB fetch command/Linked Command ORB fetch protocol command/Auto address increment DMA both of direct/indirect addressing(SBP2 Protocol)
  - Automated PageTable Fetch for DataTransfer
  - Automated Status Report to Initiator at End of DMA
  - 8/16Bits asynchronous/synchronous DMA I/F include SCSI and ATAPI like handshake
  - Asynchronous Transmit Data automatic Packetizer DMA/Asynchronous Data Fetch and dePacketizer DMA(Compliant to SBP2 requirements)
  - 8/16bits Data/Address multiplex Microcontroler and 8/16bits separated Data/Address bus
  - 3RAM configuration can support High performance for command exchange and DMA
- |                           |             |
|---------------------------|-------------|
| Asynchronous Command FIFO | : 512 Bytes |
| Config ROM/LOG FIFO       | : 512 Bytes |
| DMA FIFO                  | : 4720Bytes |

## 1. Introduction

### 1.1. Description

The TSB43LV81 provide a high-performance IEEE1394-1995 and IEEE1394.a interface with capability transfer and receive up to 400Mbps proper-formatted packet. The TSB43LV81 have high-performance internal SBP-2 Protocol engine, and it can provide high speed ORB exchange between SBP-2 initiators and own node. That means this TSB43LV81 act as SBP-2 target node. Data packet FIFO has 4096Byte at maximum and Command FIFO has 512Byte at maximum.

The TSB43LV81 can be used for another purpose such as DPP (Direct Printer Protocol) by address sorting for received packet. Address filtering for in coming write request packet can correctly sort data packet that sent by peer DPP devices.

Both two protocols could be existing in this TSB43LV81 in same time, and internal ConfigRom CSR can correctly response for peer Initiator or DPP device.

By above internal high performance feature, external controller can easily make SBP-2 target device and DPP devices.

This document is not intended to serve as tutorial on the 1394, SBP-2, and DPP protocol. User should refer each documentation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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### 1.2. Terminal Assignments

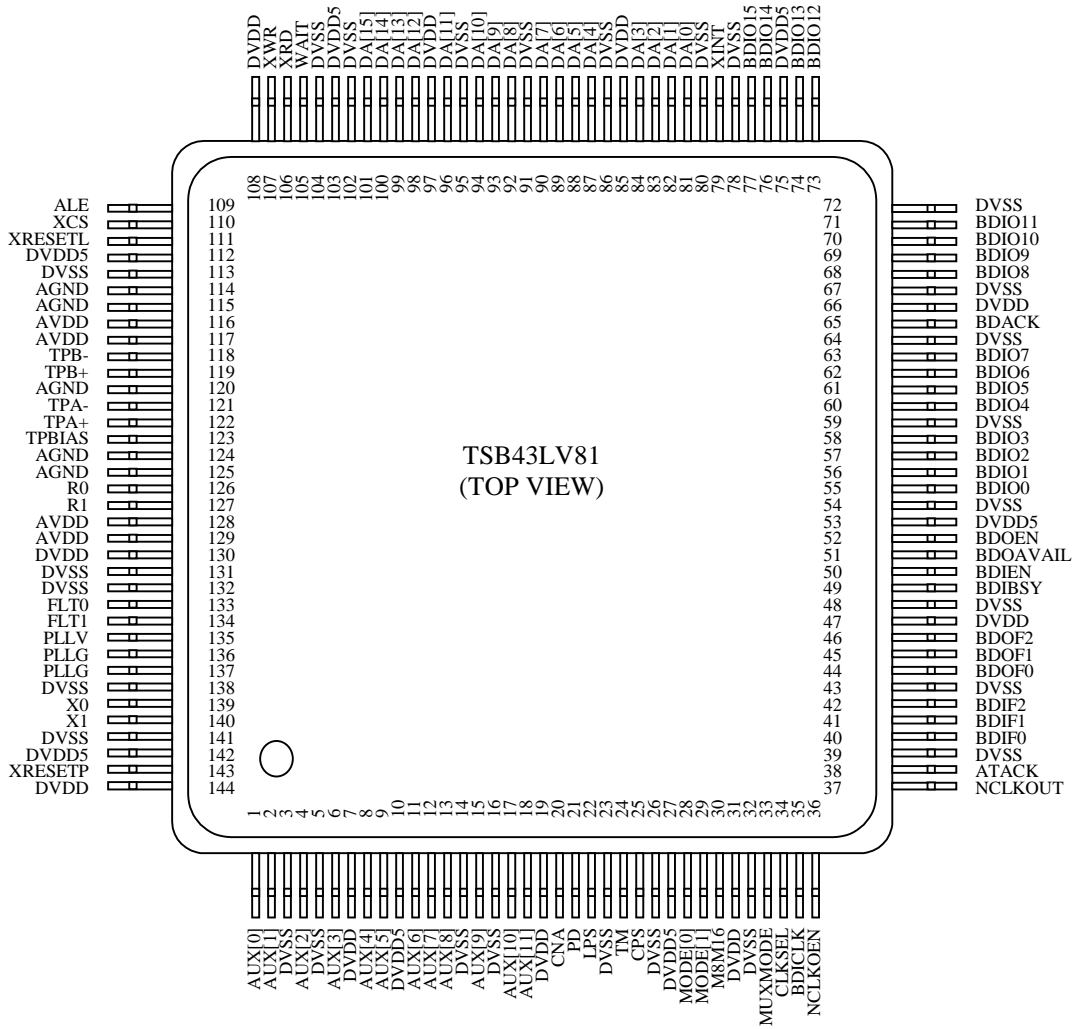


Figure 1-1. Terminal Assignments

### 1.3. Terminal Functions

#### 1.3.1. AUX PIN USAGE vs. MODE[1:0]

The Signals in the AUX vs. MODE are defined as follows:

Both internal LINK and PHY work on NORMAL mode. Only PHY functions on PHY-Mode. Link functions under LINK-Mode.

<b>MODE[1:0]</b>			<b>0 0</b>	<b>0 1</b>	<b>1 0</b>
<b>NAME</b>	<b>PIN</b>	<b>I/O</b>	<b>NORMAL</b>	<b>PHY-MODE</b> (only PHY active)	<b>LINK-MODE</b> (only Link active)
AUX[0] (Note-2)	1	I/O	HiZ	CTL0	D7
AUX[1] (Note-2)	2	I/O	HiZ	CTL1	D6
AUX[2] (Note-2)	4	I/O	HiZ	D0	D5
AUX[3] (Note-2)	6	I/O	HiZ	D1	D4
AUX[4] (Note-2)	8	I/O	HiZ	D2	D3
AUX[5] (Note-2)	9	I/O	HiZ	D3	D2
AUX[6] (Note-2)	11	I/O	HiZ	D4	D1
AUX[7] (Note-2)	12	I/O	HiZ	D5	D0
AUX[8] (Note-2)	13	I/O	Powerclass/CycleIn (Note-1)	D6	CTL1
AUX[9] (Note-2)	15	I/O	Powerclass/CycleIn (Note-1)	D7	CTL0
AUX[10] (Note-2)	17	I	Powerclass/CycleIn (Note-1)	LREQ	SCLK
AUX[11] (Note-2)	18	O	OPEN (pull down)	SCLK	LREQ

Note-1) AUX[8:10] input mean PowerClass [2:0], Internal PHY read this value at Power Up Reset. (input)

Note-2) These input has BUS holder circuit for isolation by cap.

#### 1.3.2. MicroController/MicroProcessor Interface Definition

The Signals in the MicroController/MicroProcessor Interface are defined as follows:

<b>NAME</b>	<b>PIN</b>	<b>I/O</b>	<b>DESCRIPTION</b>
XCS	110	I	Chip select.
ALE	109	I	Address Latch En. Ignored when not DA mux mode.
XRD	106	I	Read cycle Enable.
XWR	107	I	Write cycle Enable.
XINT	79	I/O	Interrupt
XWAIT	105	O	Wait.
ADDR[7:0]	-	I/O	Address (DA[7:0] for 8bits mode, BDIO[15:8] for 16bits parallel mode)
DATA[15:0]	-	I/O	Data (DA [15:8] for 8bits mode DA[15:0] for 16bit mode)
M8M16	30	I	Bit width select. Set HI is 16bit mode.
MUXMODE	33	I	Mode selects. Set HI is Data Address multiplex mode.



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### 1.3.3. MISC

NAME	PIN	I/O	DESCRIPTION
MODE[1:0]	29,28	I	Chip mode select. (NORMAL/PHY/LINK)
XRESETP	143	I	Phy reset. Reset for LINK block.
XRESETL	111	I	Link reset. Reset for PHY block.
TM	24	I	Test mode. Should be Low for all time.

### 1.3.4. Physical Layer Port

The Signals in the Physical Layer Interface are defined as follows:

NAME	PIN	I/O	DESCRIPTION
CPS	25	I	Cable Power Supply
TPBIAS	123	I/O	TPBIAS Output
R1	127	I/O	Current setting resistor
R0	126	I/O	Current setting resistor
TPB-	118	I/O	Twisted pair cable B negative signal
TPB+	119	I/O	Twisted pair cable B positive signal
TPA-	121	I/O	Twisted pair cable A negative signal
TPA+	122	I/O	Twisted pair cable A positive signal
X0	139	I/O	Crystal oscillator
XI	140	I/O	Crystal oscillator
FLT1	134	I/O	PLL filter
FLT0	133	I/O	PLL filter
PD	21	I	Power-down input
CAN	20	O	Cable Not Active output
Contend/LPS	22	I	LPS for PHY Mode, Contend for LINK Mode and Normal Mode

Note: All Pins in this table are reserved for first sample.



### 1.3.5. DMA/BULKY DATA INTERFACE

NAME	PIN	I/O	DESCRIPTION
BDICLK	35	I	DMA clock (note-1)
BDIBSY/BDREQ(SCSI)	49	O	DMA input busy / DMA request
BDIF[2:0]	40,41,42	I	DMA input flag (indicate the order of input data on stream)
BDIEN/BDWR(SCSI)	50	I	DMA input enable
BDIO[15:0]	-	I/O	DMA data (8bit: BDIO[7:0] )
BDOF[2:0]	44,45,46	O	DMA output flag (indicate the order of output data on stream)
BDOEN/BDRD	52	I	DMA output enable
BDOAVAIL/BDRW(SCSI)	51	O	DMA output avail / (DMA R/W indicator at SCSI mode)
NCLKOEN	36	I	BD clock output enable (hi:enable)
CLKSEL	34	I	BD clock select, Set Low use BDICLK Hi : use internal clock (no need to connect BDICLK)
BDACK	65		DMA acknowledge
ATAACK	38	O	ATAPI acknowledge
NCLKOUT	37	O	24.576MHz clock output

note-1) Any frequency is OK. Max freq = 40MHz. It's not required matching same freq to transfer speed.

### 1.3.6. BDIF

8-bit Bulky

BDIF[2:0]	Comment
011	8-bit data except last block on packet
111	8-bit data of last on packet
101	Reset
001	No data

16-bit Bulky

BDIF[2:0]	Comment
011	8-bit data except last block on packet (Upper)
000	8-bit data except last block on packet (Lower)
010	16-bit data except last block on packet
111	8-bit data of last on packet (Upper)
100	8-bit data of last on packet (Lower)
110	16-bit data of last block on packet
101	Reset
001	No data

### 1.3.7. BDOF

BDIF[2:0]	Comment
010	8-bit data except last block on packet
110	8-bit data of last on packet
011	16-bit data except last block on packet
111	16-bit data of last on packet
100	No data

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### 1.3.8. POWER SUPPLIES

NAME	PIN	I/O	DESCRIPTION
DVSS	3,5,14,16,23,26,32,39,43,48,54, 59,64,67,72,78,80,86,91,95,102, ,104,113,131,132,,138,141,		Digital ground
DVDD	7,19,31,47,66,85,97,108,130,14 4,		Digital power supply
DVDD5	10,27,53,75,103,112,142,		5V <sub>V<sub>dd</sub></sub> 5V-tolerant (input 3.3V when not use 5V control signal to input pin)
AGND	114,115,120,124,125		Analog ground
AVDD	116,117,128,129,		Analog power supply
PLLV	135		PLL power supply
PLLG	136,137		PLL ground



**2. Architecture**

**2.1. Block Diagram**

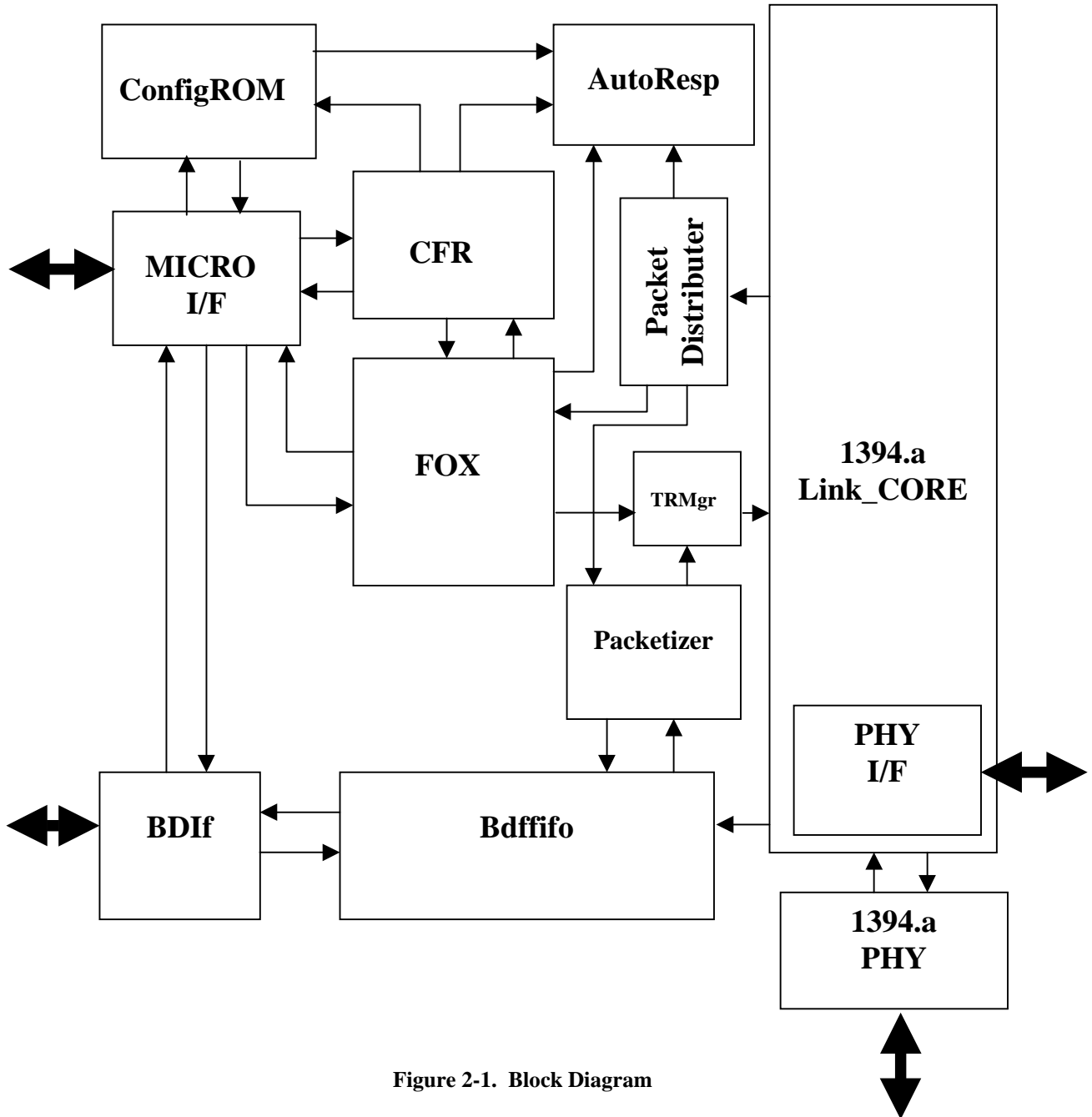


Figure 2-1. Block Diagram

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### **2.1.1. Physical Interface**

The Physical (PHY) interface provides Phy-level service to the LINK layer service. In normal usage, this interface is connected to internal PHY, but this interface module also allows connecting external PHY. This is useful when multiple port PHY or Isolation is required.

### **2.1.2. LINK\_Core (1394.a)**

The LINK\_Core provide LINK layer service such as transmit and receive correctly formatted IEEE1394-1995 and IEEE1394.a Asynchronous packets. Also generate and inspect the 32-bits cyclic redundancy check (CRC). This LINK Core doesn't have capable Isochronous Service.

### **2.1.3. ConfigROM**

The ConfigROM module support Auto Response service for Config ROM read request. And also record transaction history. This module has 528byte of random access memory. ConfigROM provide Configuration ROM that required for IEEE-1212 standard and Host controller can load its data during node initialization. Before all ConfigROM data is loaded, LINK\_Core return Ack\_Tardy to all read requests for this address. Once initialized, ConfigROM is accessible by peer Node read request.

Log module provides transaction history and has loop FIFO architecture.

Hostcontroller can read most recent transaction packet history that transmitted and received by this node.

(Note) Log Mode is disabled when ConfigRom or Status accesses.

Hostcontroller can set each memory size for above two modules. Refer to CFR 0x8C, 0xF8 and 0xFC for more information.

### **2.1.4. AutoResp**

The AutoResp module provide auto packet response service for in-coming request packet.

This AutoResp work for ConfigROM read request, Agent State read request, and error response packet for Un-expected packet. Some sort of auto error response packet could be disable by control bit for various protocols.

### **2.1.5. MICRO I/F**

The MICRO I/F module provides Hostcontroller interface. This module could be accessed by 8/16-bit access both of data address multiplex, 8 bit address data parallel access, and also 16 bit data/8 bit address parallel access when using BDOx line as address line. This interface has Indian programmable access, and allows most MicroController can access CFR easily. Refer to section 3 for more information.

### **2.1.6. CFR**

The CFR(Configuration Resistor) provide most of control bits and also hostcontroller monitor for this node.

Refer to section 3 for more information.

### **2.1.7. FOX**

The FOX module provide Faster ORB exchanger (FOX) function and support Management ORB and also Command block ORB transaction. In SBP-2 protocol, target has to read ORB packet from initiators.

This FOX module automatically read both of Management ORB and Command block ORB from initiator when Initiator requested. Once Management Agent address (CFR 0x48) and other information is set, Hostcontroller does not have to access each packet until getting ORB packet. Linked Command block ORB is automatically fetched each by each and hardware can emulate up to 4 Agents.



This module have 2 FIFO modules for Management ORB and Command block ORB for both of transmit and receive packet. Refer to CFR from 0x44 to 0x6C for more detail.

#### **2.1.8. Packet Distributor**

The Packet Distributor module provides packet routing service for each FIFO module.

When SBP-2 mode, all of request packet and response packet have property and routing to correct FIFO, and also sent to corresponding initiators. When DPP mode, Packet Distributor filtering request packet by its addressing and save it into correct receive FIFO. Refer to CFR definition for more detail.

#### **2.1.9. TRMgr**

The TRMgr(Transaction Manager) module provide transaction control service which control packet transmit Priority between control packet and Data packet. Management is simple first in first type control, so, any packet Transmit request for cable is sent by its order. This module also control split transaction management and busy retry control. If acknowledge packet for the sent packet is any busy code, module retry to send packet until the packet succeed to transmit or busy time out. And also, if acknowledge packet for the sent packet is ack\_pending, then module start split transaction timer and waits response packet. If node did not receive Response packet until split transaction time out limit, then the module set error code and set interrupt.

See CFR specification for more detail.

#### **2.1.10. Packetizer**

The Packetizer module provide packetization for transmit packet. The data stream from BDIF and Bdfifo is split into small packet that meet SBP-2 requirement. Read request or write request header is attached for each packet and each header has correctly incremented destination address. These transaction also do busy retry and split transaction timer control if required. Refer to section for more detail.

The packetizer also provide, AutoPage Table Fetch service, Internal Auto Fetch module send Read Request to page present address each by each, and DMA automatically send Data to requested address that set by Page Table Element. At the end of Packetizer, if entire DMA function is completed successfully, then Status Block Packet is automatically sent by DMA.

#### **2.1.11. Bdfifo**

The Bdfifo module provide data packet FIFO for SBP-2 read response packet and also write request packet. FIFO size is 4736 byte max including received header space, and FIFO size for each Tx and Rx is programmable that set by Hostcontroller via CFR. Refer to CFR definition for more detail.

#### **2.1.12. BDif**

The BDif module provides data interface between external host DMA and internal FIFO (Bdfifo).

Data is also could be read by Micro I/F in some condition if required. This interface has several mode such as 8/16 bit width also asynch/synchronous mode. Refer to Bulky interface section for more detail.



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2.2. System block diagram

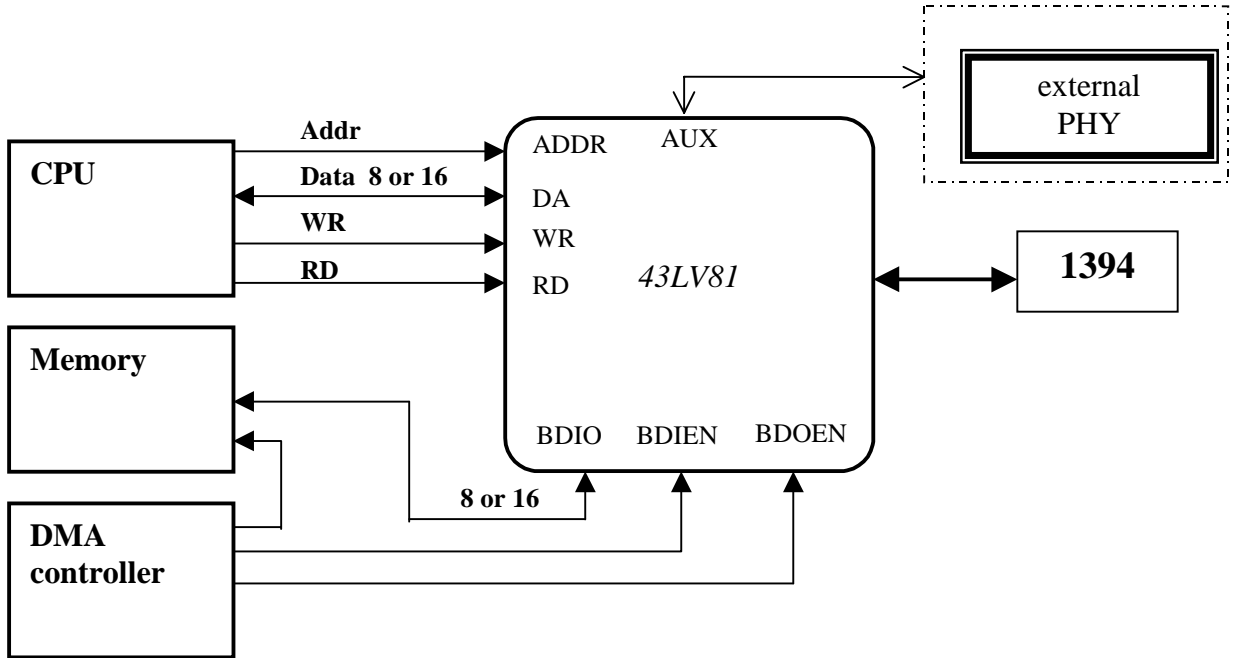


Figure 2-2. System block configuration example1 (Async)

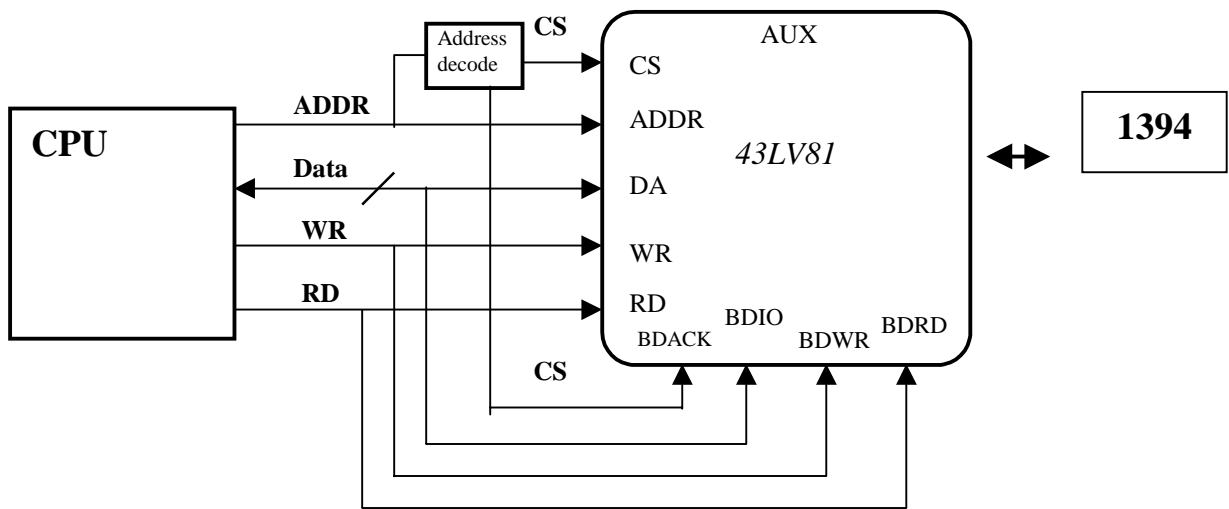


Figure 2-3. System block configuration example2 (SCSI)

### 3. Bit/Byte Order

In this document, the address is big endian and bit 0 is the most significant bit.

MSB																LSB															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
byte0(note)								byte1(note)								byte2(note)								byte3(note)							
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Octlet0(note)																Octlet1(note)															
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
quadlet																															

#### 3.1. Addressing

Addressing in this CFR is in byte. The address is made in the below pin order.

Address[7:0] = ( DA7 , DA6, DA5, DA4, DA3 , DA2, DA1, DA0 )

Note) Write 0xFFFF\_FFFF to 0x00 adder to make Byte Endian swap for this address.

##### 3.1.1. Write access

When the host (MicroController) writes a data on CFR, the quadlet access is only permitted.

It should access with each byte or each octlet but any orders are acceptable.

Example)

Write order for 8 bit access : byte3 -> byte1 -> byte2 -> byte0

: byte0 -> byte1 -> byte3 -> byte2

Write order for 16 bit access : octlet0 -> octlet1

: octlet1 -> octlet0

##### 3.1.2. Read Access

CFR permits the host to read with the byte/octlet access. The host interface brings a quadlet data by the first read of a byte/octlet in a quadlet. If the next read by the host is for the other byte (octlet) in the same quadlet, the host interface shall give the byte (octlet) data in it.

Otherwise, if the next read is for a byte (quadlet) in the other quadlet, the host interface brings the quadlet data newly and shall give a new byte/octlet) data in it.

Example)

Read order for 8 bit access : byte3 -> byte1 -> byte2 -> byte0

: byte0 -> byte1 -> byte3 -> byte2

Read order for 8 bit access : byte1 -> byte1

(These byte1 are read from two different quadlet)



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**3.2. CFR (Configuration Resistor) Definitions**

CFR specification in this datasheet is defined as below example.

MSB										LSB																						
address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Name	reg-1										reg-2																					
Read/Write	R/W										R/O																					
Default	16'h0000										16'hFFFF																					
BusReset	16'h0000										U																					

**Table 3-1. Example CFR Map**

**Read/Write** : "Read or write effect"

- R/O : The host can only read. Write by the host is not effective.
- R/W : The host can read and write.
- W/O : The host can only write. The value read by the host has no meaning.
- S/C : It shall be set as soon as the host writes '1' and then be cleared automatically after being proceeded.
- N/A : The host shall get a meaningless value when it reads from it or writes on it.
- CRW : The host can read or write conditionally.

**Default** : "Default value after a power-on reset"

- BusReset : "Value set after a bus reset"
- U : Unchanged
- A : Automatically set to appropriate value.
- CC : Conditionally changed.

NOTE: For most registers, the initial value after a power-on reset or bus reset is the same.  
 When the initial values differ, the two initial values are explicitly illustrated.

NOTE : If RegRW is set, some CFR bits can be written. But it should not be set in the normal operation as it is test mode for production and other. That shall not be referred to in this specifications.







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	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31																											
0x4C Command Agent	Reserved							Agent_Base_offset																																																			
0x50 Agent Control	AgtNmb		Reserved							USTIEn AgntVld Reserved WrNdID RdNdID					NodeID																																												
0x54 ORB Pointer1	Reserved														ORB_destination_offset_hi																																												
0x58 ORB Pointer2	ORB_destination_offset_lo																																																										
0x5C Agent Status	State0		DrBil0		UnStEn0		Dead0		Rst0		DrBClr0		USEClr0		State1		DrBil1		UnStEn1		Dead1		Rst1		DrBClr1		USEClr1		State2		DrBil2		UnStEn2		Dead2		Rst2		DrBClr2		USEClr2		State3		DrBil3		UnStEn3		Dead3		Rst3		DrBClr3		USEClr3				
0x60 Transaction Timer Control	DTTxEd		DRTxEd		ATTxEd		MTTxEd		CTTxEd		Reserved		ARTxEd		Reserved		DTErr		DRErr		ATErr		MTErr		CTErr		Reserved		ARErr		Reserved		DTRtry		DRRtry		ATRtry		MTRtry		CTRtry		Reserved		ARRtry		Reserved		TimrNo			TxAbrt		HldTr		RlsTr		Reserved	
0x64 Transaction Timer Status1	Destination_ID														Destination_offset_hi																																												
0x68 Transaction Timer Status2	Destination_offset_lo																																																										
0x6C Transaction Timer Status3	TCode			Spd		Tlabel							Retry_Counter					SplitTrTimer																																									
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31																											



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	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0x70 Write First	Write_First																															
0x74 Write Continue	Write_Continue																															
0x78 Write Update	Write_Update																															
0x7C Reserved	Reserved																															
0x80 ARF Data	ARFRead																															
0x84 MRF Data	MRFRead																															
0x88 CRF Data	CRFRead																															
0x8C Configuration ROM Control	Reserved							AR_ConfigROM_Size										Reserved					ConfigROM_Size									
0x90 DMA Control	DMARW	Reserved	DRFEn	DTFEn	DRpktz	DTpktz	DRSpDis	DTSpDis	DheadSel	RconfSinglpkt	LongBlk	QuadSend	QuadBndry	CheckPg	AutoPg	DRPage FetchSize	DTPage FetchSize	Dackpnd	Drespcmp	DTHdls	Dpause	DRStPS	DRHStr	DRDSEL	DTDSEL	DRFCLr	DTFClr					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31



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	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
0x94 Bulky Interface Control	PgBufSiz			MRBufSiz			MTBufSiz			BDAckCtl	Reserved	ATAckCtl	BIBsyCtl	BOAvCtl	BOEnCtl	BIEnCtl	BLECtl	AutoPad	BDODely		BDIDely		BDOMode			Burst		BDIMode			RevPad	BDORst	BDIRst	BDOTris
0x98 DTF/DRF Size	Reserved						DTF_Size						Reserved						DRF_Size															
0x9C DTF/DRF Avail	DTFEmpty	Reserved						DTFAvail						DRFEmpty	BDOAvail	Reserved						DRFThere												
0xA0 DTF/DRF Ack	Reserved						DRAErr	DRxAck			Reserved			DRAVal	Reserved						DTAErr	DTxAck			Reserved			DTAVal						
0xA4 DTF First & Continue	DTF_First & Continue																																	
0xA8 DTF Update	DTF_Update																																	
0xAC DRF Data	DRFRead																																	
0xB0 DTF Control0	DTFCTL0	DTFCTL1	DTFCTL/DIFSx	DTFNdIval	DTFNotify	Reserved	DTFSpd	DTF_Max Payload			PgTblEn	DTF Page Size			DTF_BlockSize/ DTF_BlockCount																			
0xB4 DTF Control1	DTF_BlockCount/DTF_BlockSize																																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		



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	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0xB8 DTF Control2	DTF_destination_ID												DTF_destination_offset_hi																			
0xBC DTF Control3	DTF_destination_offset_lo																												0	0		
0xC0 DRF Control0 (packetizer mode)	DRFCT0	DRFCT1	DRFCT2/DRFSix	DRFNdval	DRFNotify	Reserved	DRFSpd	DRF Max Payload	PgTbIE	DRF Page Size	DRF_BlockSize/ DRF_BlockCount																					
0xC0 DRF Control0 (direct mode)	DRBIdEn	DRSIdEn	DRAdrEn	Reserved																												
0xC4 DRF Control1 (packetizer mode)	DRF_BlockCount/DRF_BlockSize																															
0xC4 DRF Control1 (direct mode)	DRF_destination_Width																															
0xC8 DRF Control2	DRF_destination_ID												DRF_destination_offset_hi																			
0xCC DRF Control3	DRF_destination_offset_lo																												0	0		
0xD0 DRF Header0	DRF_Header0																															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31



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		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	0xD4 DRF Header1	DRF_Header1																															
	0xD8 DRF Header2	DRF_Header2																															
	0xDC DRF Header3	DRF_Header3																															
	0xE0 DRF Tailer	Reserved										Rx_Spd					Reserved					FIFO			Reserved		DRF_TxAck						
	0xE4 DRF Expected Value	DTFPageCount															DRFPageCount																
0xE8	(DhdSel=00) DTx Header0	Reserved										DTxSpd					DTxTlabel					DTxRT			DixTCode		DTxPrio						
	(DhdSel=01) DTx Header0	STAT			RESP			Reserved			AckEirr		Ack			PSTAT			PRESP			Reserved		PAckEirr		PAck							
	(DhdSel=10) DRx Header0	Reserved										DRxSpd					DRxTlabel					DRxRT			DRxTCod e		DRxPrio						
	(DhdSel=11) DRx Header0	STAT			RESP			Reserved			AckEirr		Ack			PSTAT			PRESP			Reserved		PAckEirr		PAck							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31



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		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0xEC	(DhdSel =00) DTx Header1	DTx_destination_ID											DTx_destination_offset_hi																				
	(DhdSel =01) DTx	DTx Page Number											Reserved																				
	(DhdSel =10) DRx Header1	DRx_destination_ID											DRx_destination_offset_hi																				
	(DhdSel =11) DRx	DRx Page Number											Reserved																				
0xF0	(DhdSel =00) DTx Header2	DTx_destination_offset_lo																															
	(DhdSel =01) DTx Header2	DTx Page length											DTx Page table hi																				
	(DhdSel =10) DRx Header2	DRx_destination_offset_lo																															
	(DhdSel =11) DRx Header2	DRx Page length											DRx Page table hi																				
0xF4	(DhdSel =00) DTx Header3	DTx_data_length											DTx_extended_tcode																				
	(DhdSel =01) DTx Header3	DTx page table lo																															
	(DhdSel =10) DRx Header3	DRx_data_length											DRx_extended_tcode																				
	(DhdSel =11) DRx	DRx Page table lo																															





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0x00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Version	Version																												Rev			
Read/Write	R/O																												R/O			
Default	28'h4300_810																												4'h2			
BusReset	U																															

**Table 3-3. CFR map (0x00)**

**Version:** TI device code name of this chip.

**Rev** : Revision of this chip

Note) Write 0xFFFF\_FFFF to make Endian swap for Micro I/F.

0x04	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Misc.	Reserved		C	LKON	LPS	Reserved		Ping_Timer								Root	Reserved				AckErr	ATAck	Reserved		AckVld							
Read/Write	N/A		R/O	S/C	R/W	N/A	R/O								R/O	N/A				R/O	R/O	N/A		R/O								
Default	3'h0		1	0	1	0	9'h0								0	6'h00				0	4'h0	3'h0		0								
BusReset	U		U	U	U	U	9'h0								A	6'h00				0	4'h0	3'h0		0								

**Table 3-4. CFR map (0x04)**

**C** :Bus Manager Capable for PHY.

Refer PHY specification for more detail. This register is active when PHY is ON; even LINK is in Reset State.

**LKON** : Link-On output from PHY.

This register is active when PHY generate LINK\_ON signal; even LINK is in Reset State. This bit is set when PHY detect LINK\_ON Packet, and cleared when write “1”. This bit will be changed during LPS is off.

**LPS** :Link Power Status.

Set this bit to one set internal PHY LPS signal to one.

**Ping\_Timer** :The value of Ping Time.

When Ping Packet transmitted by this node, and received Ping Response, this time is updated.

**Root** :Whether this node is root.



When this node is root, Root shows 1.

When this node is not root or a bus reset is being initiated, Root shows 0.

**AckErr** : "Ack Error"

Whether the last Ack received for the packet transmitted from ATF has any errors.

When the Ack didn't received nor had parity error and length error, AckErr shows 1.

When the Ack has no error or any Ack has not been received yet, AckErr shows 0.

**ATAck** : "Address transmitter acknowledge received"

The last Ack received for the packet transmitted from ATF.

The value is updated each time the Ack is received.

**AckVld** : "Ack Valid"

Whether ATAck has been already read.

When ATAck has not read yet, AckVld shows 1.

When ATAck has already read, AckVld shows 0.

0x08	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Control	IDVal	RxSid	RSIsel	Reserved	Bsy0	TrEn	Reserved	ACArbOn	CncatEn	Reserved	RstTr	Reserved	Reserved	ErrResp	StErpkt	SpTrEn	RetryEn	Ackpnd	Reserved	CyMas	Reserved	CyTmrEn	DMclr	RxUnexp	RUEsel	Prio_Budget						
Read/Write	R/O	R/W	N/A	R/W	N/A	R/W	R/W	N/A	S/C	N/A	R/W			N/A	R/W	N/A	R/W	S/C	R/W	R/W												
Default	0	1	0	0	0	1	0	0	0	0	0	3'h0	0	0	1	1	0	0	1	0	1	0	0	0	6'h0							
BusReset	A	U										U																				

**Table 3-5. CFR map (0x08)**

**IDVal** : "ID valid"

When the information of 0x24 is valid, IDVal shows 1.

**RxSid** : "Received self-identification(self-ID) packets"

When RxSid is set to 1, the self-ID packets generated by Phy during bus initialization are received and placed into DRF or LOG as a single packet.

When RxSid is set to 0, the self-ID packets are not placed anywhere.

**RSIsel** : "Select either Log or DRF to be placed received self-ID packets"

When RSIsel is set to 1 and RxSid is set to 1, the self-ID packets are placed into DRF.

When RSIsel is set to 0 and RxSid is set to 1, the self-ID packets are placed into Log.

**Bsy0** : "Busy control"

Whether the receiver sends Ack\_Busy\_X to all incoming packets.

When Bsy0 is set to 1, Ack\_Busy\_X is sent.



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When Bsy0 is set to 0, Ack\_Busy\_X is sent only when necessary according to the normal busy/retry protocol.

**TrEn** : "Transaction enable"

When TrEn is set to 1, the transmitter arbitrates and sends packets, the receiver receives packets.

When TrEn is set to 0, the transmitter and the receiver is disabled.

**AcArbOn** : "Accelerated arbitration on"

When AcArbOn is set to 1, the accelerated arbitration is enabled.

When AcArbOn is set to 0, the accelerated arbitration is disabled.

caution) This function is not checked yet.

**CncatEn** : "Concatenated transaction enable"

When CncatEn is set to 1, concatenated transaction is supported.

When CncatEn is set to 0, concatenated transaction is not supported.

caution) This function is not checked yet.

**RstTr** : "Reset transaction"

When RstTr is set to 1, the entire transaction in ATF, ARF and AGENT resets synchronously. No effect to DTF and DRF. This bit clears itself to 0 after the reset.

**ErrResp** : "Response for error packets"

When ErrResp is set to 1, the response packets are returned for packets with any errors.

When ErrResp is set to 0, the acknowledge is returned for packets with any errors.

**StErPkt** : "Store error packets"

When StErPkt is set to 1, packets with any errors are stored. Otherwise, packets with any errors is not stored.

**SplTrEn** : "Split transaction enable"

When SplTrEn is set to 1, the timer of ATF attempts split transaction for receiving Ack\_pending and can't transmit any packets till the response packet is received or split-timeout occurs.

When SplTrEn is set to 0, the timer does not wait for the response packet.

**RetryEn** : "Automatic retry enable"

When RetryEn is set to 1, all the transmitter attempts retry automatically for receiving Ack\_Busy\_X, Ack\_Busy\_A or Ack\_Busy\_B.

When RetryEn is set to 0, any transmitters do not retry automatically.

**AckPnd** : "Ack pending enable"

When AckPnd is set to 1, the receiver sends Ack\_pending instead of ack\_complete to the write request packets.

When AckPnd is set to 0, the receiver sends ack\_complete to the write request packet.

Not effect to DRF function

**CyMas** : "Cycle master"

When CyMas is set to 1 and this chip is attached to the root Phy, the cyclemaster function is enable.

When CyMas is set to 0 and this chip is attached to the root Phy, the cyclemaster function is disable.

**CyTmrEn** : "Cycle-timer enable"

When CyTmEn is set to 1, the cycle\_offset field increments.



When CyTmEn is set to 0, the cycle\_offset field does not increment.

**DMclr** : "All the states in DMA block clear"

When DMClr is set to 1, all the states in DMA block are reset synchronously. Before to set DMClr, should clear DTF and DRF also.

This bit clears itself to 0 after that.

**RxUnexp** : "Received the unexpected response packets"

When RxUnexp is set to 1, the unexpected response packets are received and placed into ARF or DRF.

When RxUnexp is set to 0, the unexpected response packets are not received.

**RUEsel** : "Select either ARF or DRF to be placed unexpected response packets"

When RxUnexp is set to 0, RUEsel is invalid.

When RxUnexp is set to 1 and RUEsel is set to 1, the unexpected response packets, the write request packets to read only registers, the read only request packets to write register and the write request for configuration ROM is placed into DRF.

When RxUnexp is set to 1 and RUEsel is set to 0, they are placed into ARF.

**Prio\_Budget** : "Priority budget counter"

Prio\_Budget value loads priority budget counter.

0x0C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Interrupt	Int	PhInt	Breset	CmdSif	Endslf	Phypkt	Reserved		SntRj	PhRRx	IFAcc	HdrErr	TCErr	CySec	Cyst	Reserved	DRHUpdate	FaGap	TxRdy	CyDne	CyPnd	CyLst	CyArbF	Reserved	ATFEnd	ARFRxd	MOREnd	COREnd	DTFEnd	DRFEnd	TxExpr	AgntWr
Read/Write	R/O		S/C			N/A			S/C						N/A			S/C					N/A				S/C					
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-6. CFR map (0x0C)**

**Int** : "Interrupt"

Int contains the value of all interrupt bits and interrupt mask bits ORed logically together.

Inverse of this bit is connected to XINT bit ( pin#70 )

When the logical ORed value of all (INT & MASK) is true, Int shows 1.

When the logical ORed value of all (INT & MASK) is not true, Int shows 0.

**PhInt** : "Phy chip Interrupt"

When the Phy layer signals an interrupt to this Link chip, PhInt becomes 1.

See physical layer specification in detail.

When the host writes "1" on PhInt, it is cleared to 0.



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**Breset** : "Bus reset"

When the Phy layer initializes or detects a bus reset, the Breset becomes 1.

When the host writes "1" on Breset, it is cleared to 0.

**CmdSlf** : "Command reset received"

When the receiver is sent a quadlet write request addressed to the RESET\_START(FFFF\_F000\_000C) CSR register, Cmdrst becomes 1.

When the host writes "1" on Cmdrst, it is cleared to 0.

Command Reset Packet also started into ARF.

**Endslf** : "End of the self-ID process"

When the link layer detects the end of Self-ID process, the Endslf becomes 1.

When the host writes "1" on Endslf, it is cleared to 0.

**Phypkt** : "Phy packet detect"

When the receiver received Phy packet, thePhyPkt become "1".

When the host write "1" on PhyPkt, it is clear to "0". ex)Receive Remote access packet, LinkON packet....

**SntRj** : "Busy acknowledge sent by receiver"

When the receiver is forced to send a Ack\_Busy\_X to a incoming packet because the FIFO overflowed, SntRj becomes 1.

When the host writes "1" on SntRj, it is cleared to 0.

**PhRRx** : "Phy register information received"

When a Phy register value is transferred to the Phy\_Access register from the Phy interface, PhyRRx becomes 1.

When the host writes "1" on PhRRx, it is cleared to 0.

**IFAcc** : "Invalid FIFO Access"

When IFAcc is set, invalid ATF access sequence is violated.

**HdrErr** : "Header error"

When the receiver detects a header CRC error on an incoming packet that may have been addressed to this node, HdrErr becomes 1.

When the host writes "1" on HdrErr, it is cleared to 0.

note) We do not test this function yet.

**TCErr** : "TCode error"

When the transmitter detects an invalid TCode in the data, TCErr becomes 1.

When the host writes "1" on TCErr, it is cleared to 0.

**CySec** : "Cycle second"

When the cycle-second field in the cycle-timer register incremented, CySec becomes 1.

When the host writes "1" on CySec, it is cleared to 0.

**CySt** : "Cycle started"

When the transmitter sends or the receiver receives a cycle-start packets, CySt becomes 1.

When the host writes "1" on CySt, it is cleared to 0.



**DRHUpdate** : "DRF Header Update"

When Host read out DRF data and packet header is been read, this bit is set .

When the Host writes "1" on DRHUpdate, it is clear to 0. This bit is no meaning if DRHStr(0x90) is set.

**FaGap** : "Fair Gap"

When the serial bus has been idle for an arbitration reset gap, FaGap becomes 1.

When the host writes "1" on FaGap, it is cleared to 0.

**TxRdy** : "Transmitter ready"

When the transmitter is idle and ready, TxRdy becomes 1.

When the host writes "1" on TxRdy, it is cleared to 0.

**CyDne** : "Cycle done"

When an arbitration gap is detected on the bus after the transmission or reception of a cycle-start packet, CyDone becomes 1.

When the host writes "1" on CyDne, it is cleared to 0.

**CyPnd** : "Cycle pending"

When Cypnd is set, the cycle timer offset is set to 0 (roll over or reset) and remains set until the isochronous cycle end.

**CyLst** : "Cycle lost"

When the cycle timer rolls over twice without the reception of a cycle-start packet,

CyLst becomes 1.

When the host writes "1" on CyLst, it is cleared to 0.

**CyArbF** : "Cycle arbitration failed"

When the arbitration to send the cycle-start packet fails, CyArbF becomes 1.

When the host writes "1" on CyArbF, it is cleared to 0.

**ATFEnd** : "ATF Transaction End"

When the transmitter completed transmission(received Ack\_comp, Response packet, Timeout), ATFEnd becomes 1.

The host can read the end status from Transaction Timer Control(0x60) and Transaction Timer Status(0x64-0x6C) registers until the next process begins.

When the host writes "1" on ATFEnd, it is cleared to 0.

This bit will be set when receiving response in ARF which sent requesting by itself.

When receiving independent packet in ARF, It'll be set ARFRxd.

**ARFRxd** : "ARF received data"

When the receiver confirms in the ARF, ARFRxd becomes 1. But this bit is not set for Response Packet.

When the host writes "1" on ARFRxd, it is cleared to 0.

**MOREnd** : "Management ORB fetch completed"

When the process of fetching Management ORB is completed, MOREnd becomes 1.

The host can read the end status from Transaction Timer Control(0x60) and Transaction Timer Status(0x64-0x6C) registers until the next process begins.

When the host writes "1" on MOREnd, it is cleared to 0.

**COREnd** : "Command block ORB fetch completed"

When the process of fetching Command block ORB is completed, COREnd becomes 1.

The host can read the end status from Transaction Timer Control(0x60) and



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Transaction Timer Status(0x64-0x6C) registers until the next process begins.  
When the host writes "1" on COREnd, it is cleared to 0.

**DTFEnd** : "DMA transaction from DTF completed"

When the transactions of all blocks from DTF are completed successfully or the transactions of any blocks from DTF are completed with any errors, DTFEnd becomes 1.  
The host can read the end status from Transaction Timer Control(0x60) and Transaction Timer Status(0x64-0x6C) registers until the next process begins.  
When the host writes "1" on DTFEnd, it is cleared to 0.

**DRFEnd** : "DMA transaction from DRF completed"

When the transactions of all blocks from DRF are completed successfully or the transactions of any blocks from DRF are completed with any errors, DRFEnd becomes 1.  
The host can read the end status from Transaction Timer Control(0x60) and Transaction Timer Status(0x64-0x6C) registers until the next process begins.  
When the host writes "1" on DRFEnd, it is cleared to 0.

**TxExpr** : "Transmitter is expired"

When the transmitter fails to transfer the packets, TxExpr becomes 1.  
When the host writes "1" on TxExpr, it is cleared to 0.

**AgntWr** : "Agent is written"

When any registers of any Agents (management/command) is written, AgntWr becomes 1.  
The host can read State, DrBll and UnSEn from Agent\_Status(0x5C) and destinationID and ORB\_offset\_hi from ORB Pointer(0x54, 0x58).  
When the host writes "1" on AgntWr, it is cleared to 0.

0x10	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Interrupt Mask	Int	PhInt	Breset	Cmdrst	Endslf	Phypkt	Reserved	SntRj	PhRRx	IFAcc	HdirErr	TCErr	CySec	Cyst	Reserved	DRHUpdate	FaGap	TxRdy	CyDne	CyPnd	CyLst	CyArbF	Reserved	ATFEnd	ARFRxd	MOREnd	COREnd	DTFEnd	DRFEnd	TxExpr	AgntWr	
Read/Write	R/O	R/W				N/A		R/W				N/A	R/W				N/A		R/W				N/A	R/W								
Default	1	31'h0000_0000																														
BusReset	U	U																														

Table 3-7. CFR map (0x10)

**All R/W bit** : When Each bits is set to 1, it affects Int in Interrupt(0x0c).  
When Each bits is set to 0, it does not.



0x14	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Cycle Timer	Seconds_Count						Cycle_Count										Cycle_Offset															
Read/Write	R/W																															
Default	7'h00						13'h0000										12'h000															
BusReset	U																															

**Table 3-8. CFR map (0x14)**

**Seconds\_Count** : "Cycle seconds count"

Seconds\_Count is incremented When Cycle Count is rolled over. The host also writes the value.

**Cycle\_Count** : "Cycle Count" counting 125 [us]

Cycle\_Count is incremented when Cycle\_Offset is rolled over. The host also writes the value.

**Cycle\_Offset** : "Cycle Offset" counting 40 [ns]

Cycle\_Offset is increment every 40 [ns].The host also writes the value.

0x18	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Diagnostics	IDLIns	IsolDis	BudgEn	Enghl	regRW	AgntStWr	Reserved	AgRdy0	AgRdy1	AgRdy2	AgRdy3	RstAR	RstTrM	Reserved	MAAckconf	Reserved	DisAgentID	DisAR	Budget_Counter				Reserved	MON				TMODE				
Read/Write	R/W						N/A	R/O				S/C	N/A	R/W	N/A	R/W	R/O				N/A	R/W				R/W						
Default	32'h0000_0000																															
BusReset	U						4h'0				U																					

**Table 3-9. CFR map (0x18)**

**IDLIns** : "Idle insert"

NOTE! IDLIns is used in the test mode and should not be set at the normal operation.

**IsolDis** : "Isolate Disable"

When set IsoDis, Phy LINK Interface disable BusHolder.

**BudgEn** : "Budget Counter Enable"



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When this bit is set, internal budget counter is enabled.

**Enghl** :

NOTE! Enghl is used in the test mode and should not be set at the normal operation.

**regRW** : "Register read/write access"

NOTE! regRW is used in the test mode and should not be set at the normal operation.

**AgntStWr** : "Agent write access"

When set Agent Wr, Agent state is Read/Write.

**AgRdy0** : "Agent0 ready"

When AgRdy0 is set to 1, command block agent0 is ready to be written or read.

When AgRdy0 is set to 0, command block agent0 is not ready.

**AgRdy1** : "Agent1 ready"

When AgRdy1 is set to 1, command block agent1 is ready to be written or read.

When AgRdy1 is set to 0, command block agent1 is not ready.

**AgRdy2** : "Agent2 ready"

When AgRdy2 is set to 1, command block agent2 is ready to be written or read.

When AgRdy2 is set to 0, command block agent2 is not ready.

**AgRdy3** : "Agent3 ready"

When AgRdy3 is set to 1, command block agent3 is ready to be written or read.

When AgRdy3 is set to 0, command block agent3 is not ready.

**RstAR** : "Reset autoreponse"

NOTE! RstAR is used in the test mode and should not be set at the normal operation.

**RstTrM** : "Reset transaction manager"

NOTE! RstAR is used in the test mode and should not be set at the normal operation.

**MAAckconf** : "Management Agent Ack conflict"

This bit set 1, "Ack conflict" response will be responded when management agent is busy.

**DisAgentID** : "Disable Agent ID check"

NOTE! DisAgentID is used in the test mode and should not be set at the normal operation.

**DisAR** : "Auto responder Disable"

NOTE! DisAR is used in the test mode and should not be set at the normal operation.

**Budget\_Counter** : "Budget Counter Value"

This field specifies the current value of internal budget counter.

**MON** : "Monitor select"

NOTE! MON is used in the test mode and should not be set at the normal operation.

**TMODE** : "Test mode"

NOTE! TMODE is used in the test mode and should not be set at the normal operation.



0x1C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Monitor	State_Monitor																															
Read/Write	R/O																															
Default	State dependent																															
BusReset	A																															

**Table 3-10. CFR map (0x1C)**

**State\_Monitor** : "State monitor"

NOTE! The state machine monitor for production test. Read value is beyond of this specifications.

0x20	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Phy Access	Rdpy	Wrpy	Reserved	PhyRgAd				PhyRgData				Reserved				PhyRxAd				PhyRxData												
Read/Write	S/C	N/A	S/C				N/A				R/O				R/O																	
Default	32'h000_0000																															
BusReset	U																															

**Table 3-11. CFR map (0x20)**

**RdPy** : "Read Phy register"

When RdPy is set to 1, Link sends a read register request with the address equal to PhyRdAd to the Phy. This bit is cleared when request is sent.

**WrPy** : "Write Phy register"

When WrPy is set to 1, Link sends a write register request with the address equal to PhyRdAd to the Phy. This bit is cleared when request is sent.

**PhyRgAd** : "Phy-register address"

The addresses of the Phy register to be accessed when either WrPy or RdPy is 1.

**PhyRgData** : "Phy-register data"

The data to be written to the Phy register when WrPy is 1.



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**PhyRxAd** : "Phy-register-received address"  
 The addresses of Phy register from which PhyRxData came.

**PhyRxData** : "Phy-register-received data"  
 The data of Phy register addressed by PhyRxAd.

0x24	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
BusReset	BusNumber				NodeNum				BRFErr_Code				NodeSum				CFRContID															
Read/Write	R/W				R/O				R/O				R/O				R/O															
Default	10'h3FF				6'h3F				4'h00				6'h01				6'h3F															
BusReset	U				A																											

**Table 3-12. CFR map (0x24)**

**BusNumber** : "Bus number"  
 Link uses BusNumber as BusID.  
 When a bus reset completes, BusNumber is set to an appropriate value. The host may write BusNumber.

**NodeNum** : "Node number"  
 Link uses NodeNum as NodeID.  
 When a bus reset completes, NodeNum is set to an appropriate value. The host may write NodeNum.

**BRFErr\_Code** : "Error code in bus reset"  
 When a bus reset occurs, BRFErr\_Code is set to the appropriate value.  
 If BRFErr\_Code is not zero, the host should initiate a bus reset again. The code table is below.

- 0000 No Error
- 0001 last self ID port status is not all children
- 0010 Phy id is sequence error. ( not have correct order )
- 0011 inverted-quadlet is not the reverse of preceding quadlet
- 0100 Phy id sequence error (two gaps in Phy IDs')
- 0101 Phy id sequence error (arbitration reset gap in Phy IDs')
- 0110 Phy id within self ID packet does not match
- 0111 quadlet/inverted-quadlet sequence error
- 1000 first 2 bits does not match either 01 or 10.
- 1111 At least one SelfID packet has different GAP count.

**NodeSum** : "Number of node in this 1394 topology"  
 When a bus reset occur, NodeSum is set to the appropriate value.



**CFMContID** : "Node ID of IRM"

When a bus reset occurred, CFMContID is set to the appropriate value.

0x28	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Time Limit	SplitTimeOut											RetryInterval					RtryLmt			ORBTime												
Read/Write	R/W																															
Default	16'h0320											8'h08					4'hE			4'h0												
BusReset	U																															

**Table 3-13. CFR map (0x28)**

**SplitTimeOut** : "Split transaction time-out"

SplitTimeOut limits the time waiting for the response packet.

If the response packet has not received when the split transaction timer exceeds the SplitTimeOut period, the transaction failed. Unit is one Iso cycle (125us)

**RetryInterval** : "Retry interval time"

RetryInterval defines the time from receipt of Ack\_Busy\_X to retransmission. Unit is one Iso cycle (125us)

**RtryLmt** : "Retry limit"

RtryLmt limits the number of times the transmitter retries.

If RtryLmt is 0, the transmitter shall not attempt retransmission of busied packet.

Otherwise, it shall retransmit the packet RtryLmt times or until receipt of other acknowledgements than Ack\_Busy\_X.

**ORBTime** : "Time waited by timer to fetch command block ORB"

The timer to fetch command block ORB waits for ORBTime period before beginning to transmit the read request packet, unit is one Iso cycle (125us)



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0x2C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ATF Status	ATFFul	ATFAFI	Reserved				ATFAEm	ATFEmp	Reserved											ATFClr	Reserved				ATF_Size							
Read/Write	R/O		N/A				R/O		N/A											S/C	N/A				R/W							
default	0	0	4'h00				0	1	11'h00											0	4'h00				8'h0D							
BusReset	0	0	U				0	1	U											C	U				U							

**Table 3-14. CFR map (0x2C)**

**ATFFul** : "ATF full flag"

While ATF is full, ATFFul shows 1.

While ATF is not full, ATFFul shows 0.

**ATFAFI** : "ATF almost-full flag"

While ATF can accept one more write, ATFAFI shows 1. Otherwise, ATFAFI is 0.

**ATFAEm** : "ATF almost-empty flag"

While ATF has only one quadlet in it, ATFAEm shows 1. Otherwise, ATFAEm shows 0.

**ATFEmp** : "ATF empty flag"

While ATF is empty, ATFEmp shows 1. Otherwise, ATFEmp shows 0.

**ATFClr** : "ATF clear control bit"

When ATFClr is set, ATF is cleared. This bit clears itself after the clear.

**ATF\_Size** : "ATF size control bits"

ATF\_Size is equal to the ATF size number in quadlet.



0x30	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ARF Status	ARFFul	ARFAFI	Reserved				ARFAEm	ARFEmp	ARFThere						ARFCD	Reserved			ARFClr	Reserved				ARF_Size								
Read/Write	R/O		N/A				R/O						N/A			S/C	N/A				R/W											
Default	0	0	4'h00				0	1	8'h00						0	0	0	0	4'h0				8'h0D									
BusReset	0	0	U				0	1	8'h00						0	U	C	U				U										

**Table 3-15. CFR map (0x30)**

**ARFFul:** "ARF full flag"

While ARF is full, ARFFul shows 1.

While ARF is not full, ARFFul shows 0.

**ARFAFI:** "ARF almost-full flag"

While ARF can accept one more write, ARFAFI shows 1. Otherwise, ARFAFI is 0.

**ARFAEm:** "ARF almost-empty flag"

While ARF has only one quadlet in it, ARFAEm shows 1. Otherwise, ARFAEm shows 0.

**ARFEmp:** "ARF empty flag"

While ARF is empty, ARFEmp shows 1. Otherwise, ARFEmp shows 0.

**ARFThere:** "ARF there"

ARF has ARFThere quadlet.

**ARFCD:** "ARF control bit"

When the first quadlet of a packet is being read from the ARF Data(0x80) register, ARFCD shows 1.

**ARFClr:** "ARF clear control bit"

When ARFClr is set, ARF is cleared. This bit clears itself after the clear.

**ARF\_Size:** "ARF size control bits"

ARF\_Size is equal to the ARF size number in quadlet.



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0x34	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
MTQ status	MTQFul	Reserved						MTQEmp	Reserved											MTQClr	Reserved											
Read/Write	R/O	N/A						R/O	N/A											S/C	N/A											
Default	0	6'h00						1	11'h000											0	12'h000											
BusReset	0	U						1	U											C	U											

**Table 3-16. CFR map (0x34)**

**MTQFul** : "MTQ full flag"  
 While MTQ is full, MTQFul shows 1.  
 While MTQ is not full, MTQFul shows 0.

**MTQEmp** : "MTQ empty flag"  
 While MTQ is empty, MTQEmp shows 1. Otherwise, MTQEmp shows 0.

**MTQClr** : "MTQ clear control bit"  
 When MTQClr is set, MTQ is cleared. This bit clears itself after the clear.

0x38	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
MRF Status	MRFFul	MRFAFI	Reserved				MRFAEm	MRFEmp	MRFTHere								MRFCd	Reserved	MRFClr	Reserved												
Read/Write	R/O		N/A						R/O								N/A		S/C	N/A												
Default	0	0	4'h0				0	1	8'h00								0	0	0	0	12'h00											
BusReset	0	0	U				0	1	8'h00								0	U	C	U												

**Table 3-17. CFR map (0x38)**

**MRFFul**: "MRF full flag"  
 While MRF is full, MRFFul shows 1.  
 While MRF is not full, MRFFul shows 0.

**MRFAFI**: "MRF almost-full flag"  
 While MRF can accept one more write, MRFAFI shows 1. Otherwise, MRFAFI is 0.



**MRFAEm:** "MRF almost-empty flag"

While MRF has only one quadlet in it, MRFAEm shows 1. Otherwise, MRFAEm shows 0.

**MRFEmp:** "MRF empty flag"

While MRF is empty, MRFEmp shows 1. Otherwise, MRFEmp shows 0.

**MRFThere:** "MRF there"

MRF has MRFThere quadlet.

**MRFCd:** "MRF control bit"

When the first quadlet of a packet is being read from the MRF Data(0x84) register, MRFCd shows 1.

**MRFClr** : "MRF clear control bit"

When MRFClr is set, MRF is cleared. This bit clears itself after the clear.

0x3C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CTQ status	CTQFul	CTQAFI	Reserved			CTQ1Av	CTQAEmp	CTQEmp	Reserved											CTQClr	Reserved			CTQ_Size								
Read/Write	R/O		N/A			R/O			N/A											S/C	N/A	R/W										
Default	0	0	3'h0			1	0	1	11'h000											0	4'h0			8'h0F								
BusReset	0	0	U			1	0	1	U											C	U			U								

**Table 3-18. CFR map (0x3C)**

**Note: Provide only 3quadlets only**

**CTQFul** : "CTQ full flag"

While CTQ is full, CTQFul shows 1.

While CTQ is not full, CTQFul shows 0.

Note: (CTQ – 1) size will be displayed.

**CTQAFI:** "CTQ almost-full flag"

While CTQ can accept one more write, CTQAFI shows 1. Otherwise, CTQAFI is 0.

Caution: It'll be set 0 after writing 3 quadlets.

**CTQ1Av:** "CTQ 1-available flag"

CTQ can accept one more packet.

**CTQAEmp:** "CTQ almost-empty flag"

While CTQ has only one quadlet in it, CTQAEmp shows 1. Otherwise, CTQAEmp shows 0.



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Caution: It'll be set 0 after writing 2 quadlets.

**CTQEmp:** "CTQ empty flag"

While CTQ is empty, CTQEmp shows 1. Otherwise, CTQEmp shows 0.

**CTQClr** : "CTQ clear control bit"

When CTQClr is set, CTQ is cleared. This bit clears itself after the clear.

**CTQ\_Size:** "CTQ size control bits"

CTQ\_Size is equal to the CTQ size number in quadlet.

0x40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CRF status	CRFFul	CRFAFI	Reserved				CRFAEm	CRFEmp	CRFThere								CRFCD	Reserved			CRFClr	Reserved				CRF_Size						
Read/Write	R/O		N/A				R/O								R/O	N/A			S/C	N/A				R/W								
Default	0	0	4'h0				0	1	8'h00								0	0	0	0	4'h0				8'h40							
BusReset	0	0	4'h0				0	1	8'h00								0	0	0	C	4'h0				U							

**Table 3-19. CFR map (0x40)**

**CRFFul:** "CRF full flag"

While CRF is full, CRFFul shows 1.

While CRF is not full, CRFFul shows 0.

**CRFAFI:** "CRF almost-full flag"

While CRF can accept one more write, CRFAFI shows 1. Otherwise, CRFAFI is 0.

**CRFAEm:** "CRF almost-empty flag"

While CRF has only one quadlet in it, CRFAEm shows 1. Otherwise, CRFAEm shows 0.

**CRFEmp:** "CRF empty flag"

While CRF is empty, CRFEmp shows 1. Otherwise, CRFEmp shows 0.

**CRFThere:** "CRF there"

CRF has CRFThere quadlet.

**CRFCD:** "CRF control bit"

When the first quadlet of a packet is being read from the CRF Data(0x88) register, CRFCD shows 1.

**CRFClr:** "CRF clear control bit"



When CRFClr is set, CRF is cleared. This bit clears itself after the clear.

**CRF\_Size:** "CRF size control bits"

CRF\_Size is equal to the CRF size number in quadlet.

caution) It's not transmitted data when setting number to CRF\_Size less than CORB\_Size+3 quadlets.

0x44	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ORB Fetch Control	MagtVld	MagtBsy	Reserved	MShtFmt	MORB_Prior				CORB_Size								CAG0Vld	CAG1Vld	CAG2Vld	CAG3Vld	DrBSnp	DrBFtEn	CnxFtEn	CShtFmt	CAG0QRdy	CAG1QRdy	CAG2QRdy	CAG3QRdy	CORB_Prior			
Read/Write	R/W	N/A	R/W														S/C				R/W											
Default	0	0	0	1	4'h0				8'h08								0	0	0	0	1	1	1	1	0	0	0	0	4'h0			
BusReset	U																															

**Table 3-20. CFR map (0x44)**

**MagtVld :** "Management\_Agent register valid"

When MagtVld is set to 1, the Management\_Agent\_offset in Management\_Agent(0x48) is valid.

And if the management fetch agent receives the block write request addressed to the MANAGEMENT\_AGENT register.

the management ORB shall be fetched automatically and placed into MRF.

When MAGtVld is set to 0, the Management\_Agent\_offset is invalid.

**MagtBsy :** "Management\_Agent register busy"

When block write request addressed to the Management\_Agent register, this bit set to "1".

The block write request addressed to the MANAGEMENT\_AGENT register shall be rejected with the conflict response or the conflict acknowledgement, when this bit is set.

When the host writes "0" on MAgtBsy, it is cleared to 0.

When MAgtBsy is set to 0, the management agent can accept the block write request.

**MShtFmt :** "Management ORB in short format in MRF"

When MShtFmt is set to 1, the receiver transforms the received packets containing a fetched management ORB into short format and places into MRF.

When MShtFmt is set to 0, the receiver shall place the received packets containing a fetched management ORB into MRF as it is.

**MORB\_Prior :** "Management ORB transmission priority"

The read request packet to fetch a management ORB has MORB\_Prior in the priority filed.

**CORB\_size :** "Command block ORB size"



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Command block ORBs whose size is CORB\_size shall be fetched. Unit is quadlet.

**CAG0Vld** : "Register of command block agent0 valid"

When CAG0Vld is set to 1, The Agent\_base\_offset in Command\_Agent(0x4C) is valid.

If NodeID is assigned to agent0 by writing on Agent Control(0x50), the command block agent0 can receive write/read requests.

When the block write request addressed to the ORB\_POINTER register, the command block ORB shall be fetched automatically and be placed into CRF.

Otherwise, if NodeID is not assigned to agent0, the agent0 rejects any requests.

When CAgTVld is set to 0, the Command\_block\_Agent\_offset is invalid.

**CAG1Vld** : "Register of command block agent1 valid" See CAG0Vld.

**CAG2Vld** : "Register of command block agent2 valid" See CAG0Vld.

**CAG3Vld** : "Register of command block agent3 valid" See CAG0Vld.

**DrBSnp** : "Enable to snoop about the packet fetched by doorbell"

When DrBSnp is set to 1 and doorbell is rung, command block agent fetch the whole command block ORB and put it into CRF. When DrBSnp is set to 0 and doorbell is rung, command block agents fetch the only next ORB field and does not put it into FIFO, and be displayed ORB address at 0x54,58 .

**DrBFtEn** : "Ring the doorbell enable to fetch Command block ORB"

When DrBFtEn is set to 1 and the command block agents receive the quadlet write request addressed to the DOORBELL register, the command block ORB shall be fetched automatically and placed into CRF. Either DrBll0 - DrBll3 in Agent Status(0x5C) shall be also set to 1.

When DrBFtEn is set to 0 and the command block agents receive it, the command block ORB shall not be fetched automatically.

Either DrBll0 - DrBll3 in Agent Status(0x5C) is just set to 1.

caution) do not change setting during operation.

**CnxFtEn** : "Next command block ORB fetch enable"

When CnxFtEn is set to 1 and the receiver receives a command block ORB whose the next\_ORB field is not null, the next command block ORB shall be fetched automatically.

When CnxFtEn is set to 0 and the receiver does so, the next command block ORB shall not be fetched automatically.

**CShtFmt** : "Command block ORB in short format in CRF"

When CShtFmt is set to 1, the receiver transforms the received packets containing a fetched command block ORB into short format and places into CRF.

When CShtFmt is set to 0, the receiver shall place the received packets containing a fetched command block ORB into CRF as it is.

**CAG0Rdy** : "Command block agent 0 is ready to fetch the command block ORB"

When command block agent gets ready to fetch the command block ORB, this bit is set to 1, When the host writes '1' on CAG0Rdy, it is cleared to 0 and the agent fetches the command block ORB and put it into CRF.

**Cag1Rdy** : "Command block agent 0 is ready to fetch the command block ORB"

See Cag0Rdy.



**Cag2Rdy** : "Command block agent 0 is ready to fetch the command block ORB"  
 See Cag0Rdy.

**Cag3Rdy** : "Command block agent 0 is ready to fetch the command block ORB"  
 See Cag0Rdy.

**CORB\_Prior** : "Command block ORB transmission priority"  
 The read request packet to fetch a command block ORB has CORB\_Prior in the priority filed.

0x48	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Management Agent	Reserved								Management_Agent_offset																							
Read/Write	N/A								R/W																							
Default	8'h00								24'h00_4000																							
BusReset	U																															

**Table 3-21. CFR map (0x48)**

**Management\_Agent\_offset** : "Management agent offset"  
 This contains the offset in quadlet from FFFF\_F000\_0000 [byte] to the base address of the MANAGEMETN\_AGENT register.  
 It shall not be less than 00\_4000.

0x4C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Command Agent	Reserved								Agent_base_offset																								
Read/Write	N/A								R/W																								R/O
Default	8'h00								21'h000_802																								3'h0
BusReset	U																																

**Table 3-22. CFR map (0x4C)**

**Agent\_base\_offset** : "Agent base offset"



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This contains the offset in quadlet from FFFF\_F000\_0000 [byte] to the base address of the command block agent0 register.

Agent\_base\_offset shall not be less than 00\_4000 and .

The base address of registers that each command block agent has is specified as the followings:

$$\begin{aligned} \text{Agent0[byte]} &= \text{FFFF\_F000\_0000} + \text{Agent\_base\_offset[quadlet]} * 3'b100 \\ \text{Agent1[byte]} &= \text{Agent0} + 6'h20 \\ \text{Agent2[byte]} &= \text{Agent1} + 6'h20 \\ \text{Agent3[byte]} &= \text{Agent2} + 6'h20 \end{aligned}$$

Management offset address shall not be a)less than 0xFFFFF0010000, b) reserved address for COMMAND\_BLOCK\_AGENT.

The Unit in this CFR 0x48: Management\_Agent\_Offset field is in quadlet. Therefore, Managemant Agent Address 0xFFFFFFFF0011000 should be represented as 0x04400 in this input field with the offset address.

0x50	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Agent Control	AgtNmb		Reserved									USTIEn	AgntVld	Reserved	WrNdID	RdNdID	NodeID															
Read/Write	R/W		N/A									R/W	S/C	N/A	S/C	R/W																
Default	0	0	9'h000									0	0	0	0	0	15'hFFFF															
BusReset	U											0		U																		

**Table 3-23. FR map (0x50)**

**AgtNmb** : "The number of command block agent"

The host can read the ORBPointer register of Agt\_Nmb from ORB Pointer1(0x54) and ORB Pointer2 (0x58) registers. Also this number is used to set NODE-ID for each AGENT.

**USTIEn** : "UnsolicitedStatusEn tlabel control enable"

When USTIEn is set to 1 and the host writes a packet with tlabel (tl=3'b111+2b'AgntNub+1b'X) on Write First(0x70), either UnSEn0-UnSEn3 in 0x5C shall be cleared automatically.

When USTIEn is set to 0 and the host writes a packet with tlabel (tl=3'b111+2b'AgntNub+1b'X) on Write First(0x70), UnSEn0 - UnSEn3 shall not be cleared automatically.

**AgntVld** : "valid NodeID for Agent"

When Agntvld is set to "1" with Agent Number, then NodeID corresponding to Agent is valid, This bit is automatically cleared at Bus reset.

**WrNdID** : "Write NodeID of each agent"

When WrNdID is set to 1 and AgtNmb and Agent\_NodeID are set to certain values, the command block agent of AgtNmb is assigned to Agent\_NodeID.



This bit is cleared after this assignment.

**RdNdID** : "Read NodeID of each agent"

When RdNdID is set to 1 and AgtNmb is set to a certain value, the host can read the NodeID assigned to the command block agent of AgtNmb from Agent\_NodeID. This bit is cleared after read.

**NodeID** : "NodeID assigned to the each agent"

The NodeID to be assigned to the command block agent of AgtNmb when WrNdID is set to 1. Agent\_NodeID represents the NodeID assigned to the command block agent of AgtNmb after RdNdID is set to 1.

BusReset does not effect Agent\_Node\_IDs.but Agent become not ready after BusReset, So Host have to write NodeID for Agent again after BusReset to activate Agent.

0x54	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ORB Pointer1	Reserved																ORB_destination_offset_hi															
Read/Write	N/A																R/O															
Default	32'h0000_0000																															
BusReset	0																															

**Table 3-24. CFR map (0x54)**

**ORB\_destination\_offset\_hi** : "ORB destination offset hi in ORBPointer"

The destination offset hi part of ORB POINTER register that is contained the agent indicated by Agent\_Number in Agent Control.

(Note) The value of register returns to default value when initiator which is being log in resets agent.

0x58	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ORB Pointer2	ORB_destination_offset_lo																															
Read/write	R/O																															
Default	32'h0000_0000																															
BusReset	0																															

**Table 3-25. CFR map (0x58)**



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**ORB\_destination\_offset\_lo** : "ORB destination offset low in ORBPointer"

The destination offset low part of ORB POINTER register that is contained the agent indicated by Agent\_Number in Agent Control.

(Note) The value of register returns to default value when initiator which is being log in resets agent.

0x5C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31																								
Agent Status	State0		DrBll0		UnStEn0		Dead0		Rst0		DrBClr0		USEClr0		State1		DrBll1		UnStEn1		Dead1		Rst1		DrBClr1		USEClr1		State2		DrBll2		UnStEn2		Dead2		Rst2		DrBClr2		USEClr2		State3		DrBll3		UnStEn3		Dead3		Rst3		DrBClr3		USEClr3	
Read/Write	R/O		S/C		S/C		S/C		R/O		S/C		S/C		R/O		S/C		S/C		S/C		R/O		S/C		R/O		S/C		S/C		S/C		S/C		S/C		S/C		S/C		S/C													
Default	32'h0000_0000																																																							
BusReset	0																																																							

**Table 3-26. CFR map (0x5C)**

**State0** : "State of the command block agent 0"  
 State0 shows the state of each command block agent 0.

**DrBll0** : "DoorBell variable of the command block agent 0"  
 When the DOORBELL register receives quadlet write request, DrBll0 becomes 1.  
 When the host writes 1 on a DrBClr0, DrBll0 are cleared to 0.

**UnStEn0** : "Unsolicited Status Enable variable of the command block agent 0"  
 When the UNSOLICITED\_STATUS\_ENABLE register receives quadlet write request, the UnStEn0 becomes 1.  
 If USTIE in Agent Control(0x50) is set to 1, the transmission of packet with tlabel 6'h0F clears UnStEn0.  
 Or when the host writes 1 on a USEClr0, USEClr0 is cleared to 0.

**Dead0** : "Dead state control bit"  
 When Dead0 is set to 1, State0 is set to 2'h3.  
 Dead0 clears itself after that.

**Rst0** : "Reset state control bit"  
 When Rst0 is set to 1, State0 is set to 2'h0.  
 Rst0 clears itself after that.

**DrBClr0** : "DoorBell variable clear bit"  
 When DrBClr0 is set to 1, DrBll0 is cleared to 0.  
 DrBClr0 clears itself after that.

**USEClr0** : "Unsolicited Status Enable variable clear bit"  
 When USEClr0 is set to 1, USEClr0 is cleared to 0.



USEClr0 clears itself after that.

There are four command block agents, which has the respective State, DrBll and UnStEn, variables and Dead, Rst, DrBClr and USEClr bits.

0x60	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Transaction Timer Control	DTTxEd	DRTxEd	ATTxEd	MTTxEd	CTTxEd	Reserved	ARTxEd	Reserved	DTErr	DRErr	ATErr	MTErr	CTErr	Reserved	ARErr	Reserved	DTRtry	DRRtry	ATRtry	MTRtry	CTRtry	Reserved	ARRtry	Reserved	TimrNo				TxAbrt	HldTr	Rlsr	Reserved
Read/ Write	R/O				N/A	R/O	N/A	R/O				N/A	R/O	N/A	R/O				N/A	R/O	N/A	R/W				S/C				N/A		
Default	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4'h0				0	0	0	0
BusReset	1	1	1	1	1	0	1	0	U	U	0	0	0	0	0	0	0	0	0	0	0	0	0	4'h0				0	0	0	0	

**Table 3-27. CFR map (0x60)**

**DTTxEd** : "DTF transaction end"

When the transaction from DTF has completed, DTTxEd becomes 1.

When the transaction from DTF begins, DTTxEd becomes 0.

**DRTxEd** : "DRF transaction end"

When the transaction from DRF has completed, DRTxEd becomes 1.

When the transaction from DRF begins, DRTxEd becomes 0.

**ATTxEd** : "ATF transaction end"

When the transaction from ATF has completed, ATTxEd becomes 1.

When the transaction from ATF begins, ATTxEd becomes 0.

**MTTxEd** : "MTQ transaction end"

When the transaction from MTQ has completed, MTTxEd becomes 1.

When the transaction from MTQ begins, MTTxEd becomes 0.

**CTTxEd** : "CTQ transaction end"

When the transaction from CTQ has completed, CTTxEd becomes 1.

When the transaction from CTQ begins, CTTxEd becomes 0.

**ARTxEd** : "Autoresponse transaction end"

When the autoresponse transaction has completed, ARTxEd becomes 1.

When the autoresponse transaction begins, ARTxEd becomes 0.

**DTErr**: "DTF transaction err"

If the transaction from DTF ends with any errors, DTErr becomes 1.

Otherwise, if it ends with no error, DTErr remains 0.



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When the transaction from DTF begins, DTErr is cleared to 0.

**DRErr**: "DRF transaction err"

If the transaction from DRF ends with any errors, DRErr becomes 1.

Otherwise, if it ends with no error, DRErr remains 0.

When the transaction from DRF begins, DRErr is cleared to 0.

**ATErr**: "ATF transaction err"

If the transaction from ATF ends with any errors, ATErr becomes 1.

Otherwise, if it ends with no error, ATErr remains 0.

When the transaction from ATF begins, ATErr is cleared to 0.

**MTErr**: "MTQ transaction err"

If the transaction from MTQ ends with any errors, MTErr becomes 1.

Otherwise, if it ends with no error, MTErr remains 0.

When the transaction from MTQ begins, MTErr is cleared to 0.

**CTErr** : "CTQ transaction err"

If the transaction from CTQ ends with any errors, CTErr becomes 1.

Otherwise, if it ends with no error, CTErr remains 0.

When the transaction from CTQ begins, CTErr is cleared to 0.

**ARErr** : "Autoreponse transaction err"

If the autoreponse transaction ends with any errors, ARErr becomes 1.

Otherwise, if it ends with no error, ARErr remains 0.

When the autoreponse transaction begins, ARErr is cleared to 0.

**DTRtry** : "DTF retry"

When the transaction from DTF begins retrying because of receiving Ack\_Busy\_X, DTRtry becomes 1.

When the retransaction from DTF ends because of receiving the other acknowledgements,

a retry time-out or a bus reset, DTRtry becomes 0.

**DRRtry** : "DRF retry"

When the transaction from DRF begins retrying because of receiving Ack\_Busy\_X, DRRtry becomes 1.

When the retransaction from DRF ends because of receiving the other acknowledgements,

a retry time-out or a bus reset, DRRtry becomes 0.

**ATRtry** : "ATF retry"

When the transaction from ATF begins retrying because of receiving Ack\_Busy\_X, ATRtry becomes 1.

When the retransaction from ATF ends because of receiving the other

acknowledgements, a retry time-out or a bus reset, ATRtry becomes 0.

**MTRtry** : "MTQ retry"

When the transaction from MTQ begins retrying because of receiving

Ack\_Busy\_X, MTRtry becomes 1.

When the retransaction from MTQ ends because of receiving the other acknowledgements,

a retry time-out or a bus reset, MTRtry becomes 0.

**CTRtry** : "CTQ retry"



When the transaction from CTQ begins retrying because of receiving Ack\_Busy\_X, CTRtry becomes 1.  
 When the retransaction from CTQ ends because of receiving the other acknowledgements,  
 a retry time-out or a bus reset, CTRtry becomes 0.

**ARRtry** : "Autoresponse retry"

When the autoresponse transaction begins retrying because of receiving Ack\_Busy\_X, ARRtry becomes 1.  
 When the autoresponse retransaction ends because of receiving the other acknowledgements,  
 a retry time-out or a bus reset, ARRtry becomes 0.

**TimrNo** : "Number of transaction timer"

When the host writes on TimerNo, the timer indicated in TimerNo is selected.  
 TimerNo affects TxAbort, HldRtr and reading from Transaction Timer Status1-3(0x64-0x6C).  
 The definition is the following.

- 4h0 : The timer of transmission from DTF
- 4h1 : The timer of transmission from DRF
- 4h2 : The timer of transmission from ATF
- 4h3 : The timer of transmission from MTQ
- 4h4 : The timer of transmission from CTQ
- 4h6 : The timer of autorsponse(AR) transmission

**TxAbrt** : "Transaction abort"

When TxAbrt is set to 1, the transmission of the timer indicated in TimrNo is aborted.  
 TxAbrt clears itself after it's aborted.  
 Note) DTErr(0x60) will be set 1 when abort DTF transaction.

**HldTr** : "Hold transmission"

When HldTr is set to 1, the transmission of TimerNo is held. RlsTr clears itself after it's held.  
 If both HldTr and RlsTr are set to 1 at the same time, HldTr is ignored.  
 Note) It's necessary to set this bit to 1 when writing ATQ.ATF,MTQ,CTQ. Then transmit packet by set RlsTr.

**RlsTr** : "Release transmission"

When RlsTr is set to 1, the transmission of TimerNo is released.  
 RlsRtr clears itself after it's released.

0x64	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Transaction Timer Status1	Destination_ID															Destination_offset_hi																
Read/ Write	R/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-28. CFR map (0x64)**



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**Destination\_ID** : "TimerNo's transmitting destination ID"

The timer of TimerNo is transmitting or has transmitted the packet to Destination\_ID in the last transaction.

**Destination\_offset\_hi** : "TimerNo's transmitting destination offset high"

The timer of TimerNo is transmitting or has transmitted the request packet to Destination\_offset\_hi in the last transaction.

0x68	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Transaction Timer Status2	Destination_offset_lo																															
Read/ Write	R/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-29. CFR map (0x68)**

**Destination\_offset\_lo** : "TimerNo's transmitting destination offset low"

The timer of TimerNo is transmitting or has transmitted the request packet to Destination\_offset\_low in the last transaction.

0x6C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Transaction Timer Status3	TCode				Spd		Tlabel				Retry_ Counter				SplitTrTimer																	
Read/ Write	R/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-30. CFR map (0x6C)**

**TCode** : "TimerNo's transmitting TCode"

The packet that the timer of TimerNo is transmitting or has transmitted TCode in the last transaction.

**Spd** : "TimerNo's transmitting speed"

The timer of TimerNo is transmitting or has transmitted the packet last with Spd in the last transaction.



**Label** : "TimerNo's transmitting label"

The packet that the timer of TimerNo is transmitting or has transmitted has Label in the last transaction.

**Retry\_Counter** : "TimerNo's transmitting retry counter"

The timer of TimerNo is retransmitting or has retransmitted the packet Retry\_Counter times in the last transaction.

**SplitTrTimer** : "TimerNo's transmitting split transaction timer"

If the timer of TimerNo is waiting or has waited for the response packet for SplitTrTimer period in the last transaction.

0x70	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Write First	Write_First																															
Read/Write	W/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-31. CFR map (0x70)**

**Write\_First** : "Write first quadlet of the packet to ATF, MTQ or CTQ"

This write only register provides the host with the capability to write the first quadlet of an transmit packet to transmitting FIFO.

When the host writes the first quadlet of the packet here, the value of label and TCode decide which FIFO(ATF,MTQ or CTQ) the written packet is delivered to.

0x74	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Write Continue	Write_Continue																															
Read/Write	W/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-32. CFR map (0x74)**



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**Write\_Continue** : "Write any other quadlet than first and last quadlet to ATF, MTQ or CTQ"  
 This write only register provides the host with the capability to write the quadlet of an transmit packet - except the first and last quadlet - to transmitting FIFO which is decided when the host writes on Write First(0x70).

0x78	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Write Update	Write_Update																															
Read/Write	W/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-33. CFR map (0x78)**

**Write\_Update** : "Write last quadlet of the packet"  
 This write only register provides the host with the capability to write the last quadlet of an transmit packet to transmitting FIFO which is decided when the host writes on Write First(0x70).

0x80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ARF Data	ARFRead																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-34. CFR map (0x80)**

**ARFRead** : "ARF data read access register"  
 This read only register provides the host with the capability to read the data quadlet of an received packet from ARF. Each read outputs the next quadlet from ARF. If ARF is empty, the last valid value is read.



0x84	0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
MRF Data	MRFRead																																
Read/Write	R/O																																
Default	32'h0000_0000																																
BusReset	32'h0000_0000																																

**Table 3-35. CFR map (0x84)**

**MRFRead** : "MRF data read access register"

This read only register provides the host with the capability to read the data quadlet of an received packet from MRF. Each read outputs the next quadlet from MRF. If MRF is empty, the last valid value is read.

0x88	0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
CRF Data	CRFRead																																
Read/Write	R/O																																
Default	32'h0000_0000																																
BusReset	32'h0000_0000																																

**Table 3-36. CFR map (0x88)**

**CRFRead** : "CRF data read access register"

This read only register provides the host with the capability to read the data quadlet of an received packet from CRF. Each read outputs the next quadlet from CRF. If CRF is empty, the last valid value is read.

0x8C	0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
Configuration ROM Control	Reserved				AR_CSR_Size								Reserved				CSR_Size																
Read/Write	N/A				R/W				R/O				N/A				R/W				R/O												
Default	5'h00				9'h00				0 0				5'h00				9'h00				0 0												
BusReset	U												0 0				U												0 0				

**Table 3-37. CFR map (0x8C)**

**AR\_CSR\_Size** : "Size autoresponded in Configuration ROM"



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AR\_CSR\_Size is equal to the byte size number responded automatically in the ConfigROM.  
AR\_CSR\_Size should be less than 0x20C.

**CSR\_Size** : "Size of Configuration ROM"  
CSR\_Size is equal to the ConifgROM size number in byte.  
AR\_CSR\_Size should be less than 0x400.

0x90	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
DMA Control	DMARW	Reserved	DRFEn	DTFEn	DRPktz	DTPktz	DRSpDis	DTSpDis	DheadSel	RconfSnglPkt	LongBlk	QuadSend	QuadBndry	CheckPg	AutoPg	DRPage FetchSiz	DTPPage FetchSiz	Dackpnd	Drescomp	DTHdls	Dpause	DRStPS	DRHStr	DRDSEL	DTDSel	DRFCir	DTFCir						
Read/Write	R/W	N/A	R/W							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	S/C
Default	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	001	001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
BusReset	0	0	U	0	U	U	U	U	U										U														

**Table 3-38. CFR map (0x90)**

**DMARW** : "DMA Read/Write"  
This bit controls the DMA input/output mode control for particular bus mode.  
When DMARW is set to 1, DMA is used for input. (memory → 43LV81)  
When DMARW is set to 0, DMA is used for output. (43LV81 → memory)

**DRFEn** : "DRF enable"  
When DRFEn is set to 1, DRF is enabled to receive data.  
When DRFEn is set to 0, DRF is disabled to receive data.  
When DRFEn is set to 0, DRF is to be DPP(direct print protocol) mode. Then direct mode field enable on 0xC0, 0XC4.

**DTFEn** : "DTF enable"  
When DTFEn is set to 1, DTF is enabled to transmit data.  
When DTFEn is set to 0, DTF is disabled to transmit data.  
This bit is Active only DTPkt=0. Automatically cleared, when BusReset is occurred.

**DRPktz** : "DRF Packetizer enable"  
When DRPktz is set to 1, the DRF Packetizer is ready to start to transmit read request packets.  
When DRPktz is set to 0, it is not ready to do so.

**DTPktz** : "DTF Packetizer enable"  
When DTFpktz is set to 1, the DTF Packetizer is ready to start to transmit write request packets.  
When DTPktz is set to 0, it is not ready to do so.



**DRSpDis:** "DRF Packetizer split transaction disable"

When DRSpDis is set to 0, the DRF Packetizer waits for the response packet if the transaction is acknowledged with Ack\_pending.

When DRSpDis is set to 1, the DRF Packetizer doesn't wait for it even if the transaction is acknowledged with Ack\_pending.

**DTSpDis :** "DTF Packetizer split transaction disable"

When DTSpDis is set to 0, the DTF Packetizer waits for the response packet if the transaction is acknowledged with Ack\_pending.

When DTSpDis is set to 1, the DTF Packetizer doesn't wait for it even if the transaction is acknowledged with Ack\_pending.

**DheadSel :** "DTx header select"

00: write request header

01: DTF Packetizer status

10: read request header

11: DRF Packetizer status

**RconfSnglpkt :** "Receive confirm for each single packet"

When RconfSnglpkt is set to 1, each quadlet read from DRF reflect the value of DRF status. Otherwise DRF status is updated for every "packet" received.

**LongBlk :** "Long block size"

When LngBlk is set to 1, the Packetizer uses long block size. Effect to Block size and Block count field in 0xB0,0xB4.

When LongBlk is set to 1, it will be swapped Block\_size(0xB0) field and Block\_count(0xB4) field.

**Quad Boundary:**

When this bit is set to one, Packetizer aligns quadlet address boundary in the first request packet.

Caution) This function is not checked yet.

**CheckPg:** " Check Page table "

When this bit is set to one, page table entry consistency is checked. If any error is observed, page fault interrupt is initiated.

**QuadSend :**

When this bit is set to one, Packetizer translate 4byte block request to quadlet request packet.

(When sending 4 byte request, quad request will be used on setting 1. 4byte block request will be used on setting 0)

**AutoPg:** "AutoPaging"

When this bit is set to one, auto paging function is enabled. Page table read requests are automatically initiated accordingly.

**DTPageFetch size, DRF page Fetch size:**

This field specifies the number of page table entry to be read requested by single read request packet.

$2^{(DxPageFetchSize+3)}$  bytes will be fetched by single read request.

Caution) Must set value less than 4 due to destroy status buffer area.

**DRRespComplete:**

When DRAck complete is zero and this bit is one, complete\_response is automatically set by AutoResponder.



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### **DackPnd:**

When this bit is set to zero, write ack\_complete acknowledges request to BDIFfifo. rather than ack-pending.

### **DTHdIs** : "DTF Header insert mode"

When DTHdIs is set to 1, DTx Head0-3(0xE8-0xF4) is inserted as the header of data transmitted from DTF. In this mode the chip expects the data processor to load the DTF with pure data that contains no header. When DTHdIs is set to 0, the chip expects DTF to contain completely formatted 1394 packets.

### **Dpause** : "DRF pause"

When Dpause is set to 1, the transfer of the packet in DRF is paused after DRF RxHead0-3(0xD0-0xDC) and DRF RxTailor(0xE0) is updated.

When Dpause is set to 0, the transfer of the packet in DRF is continued after DRF RxHead0-3(0xD0-0xDC) and DRF RxTailor(0xE0) is updated.

### **DRStPS** : "DRF sets Dpause automatically"

When DRStPS is set to 1, Dpause is set to 1 automatically after a packet is delivered to data processor via BDIF. When DRStPS is set to 0, Dpause is not done so.

### **DRHStr** : "DRF Header strip mode"

When DRHSty is set to 1, the header is stripped from the packet and only data payload is delivered to the data processor. The stripped header is copied to DRF RxHead0-3(0xD0-0xDC) and DRF RxTailor(0xE0).

### **DRDSel** : "DRF receiving data destination select"

When DRDSel is set to 1, the received packets are transferred to the data processor by the way of the Bulky Data Interface(BDif).

When DRDSel is set to 0, the host has read access to DRF by reading received data from DRF Data(0xAC).

### **DTDSel** : "DTF transmitting data source select"

When DTDSel is set to 1, the data processor has written access DTF by the way of the BDif.

When DTDSel is set to 0, the host has write access to DTF by writing transmitted data on DTF First(0xA4) and DTF Cont&Up(0xA8).

### **DRFClr** : "DRF clear control bit"

When DRFClr is set to 1,data in DRF is cleared.

This bit clears itself after the clear.

### **DTFClr** : "DTF clear control bit"

When DTFClr is set to 1, data in DTF is cleared.

This bit clears itself after the clear.



0x94	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Bulky Interface Control	PgBufsiz			MTRBufsiz			MTTBufsiz			BDAcKctl	Reserved	ATAcKctl	BIBsyCtl	BOAvCtl	BOEnCtl	BIEnCtl	BLECtl	AutoPad	BDODely		BDIDely		BDOMode		Burst		BDIMode			RcvPad	BDORst	BDIRst	BDOTris
Read/Write	R/W			R/W			R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W		R/W		s/c			R/W					
Default	7			5			5			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1
BusReset	U			U			U			U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	0	0	0	U	

**Table 3-39. CFR map (0x94)**

**PgBufsiz** : "Specifies Pagetable fetch buffer size" (\*note-1)  
This is page ram size. Fetched page element will be stored here.

table is,

PgBufsiz	Size (quadlet)
0	0
1	2
2	4
3	8
4	10
5	12
6	14
7	16

Example.

If 0x90 bit19-21 is 2. Page element read size is  
 $2^{(2+3)}=32$  ( byte ) = 8 quadlet

in this case, Page-requester send 32 byte read request to initiator and store that data into page ram, so, PgBufsiz is 3 in this case.



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**MTRBufSiz:** "Specifies DRF status block buffer" (\*note-1)  
MTRBufSiz is number of quadlet for status Fifo use to DRF DMA.  
table is,

MTRBufSiz	Size (quadlet)
0	0
1	2
2	4
3	6
4	8
5	10
6	12
7	14

**MTTBufSiz :** "Specifies DTF status block buffer" (\*note-1)  
MTTBufSiz is number of quadlet for status Fifo use to DTF DMA.  
table is,

MTTBufSiz	Size (quadlet)
0	0
1	2
2	4
3	6
4	8
5	10
6	12
7	14

note-1) RAM size is followed by following calculation.

$$\mathbf{ARConfigSize + STSiz + STSiz + MTTsiz + MTRsiz + LOGSize = 126 \text{ quadlet}}$$

**ATAckCtl:** "Active high control for ATAck terminal"

When AckCtl is set to 1, the ATAck is active high.

When AckCtl is set to 0, the ATAck is active low.

**BDAckCtl:** "Active high control for BDAck terminal"

When BDMacKctl is set to 1, the BDAck is active high.

When BDMacKctl is set to 0, the BDAck is active low.

**BIBsyCtl :** "Active high control for BDIBUSY terminal"

When BIBsCtl is set to 1, the BDIBUSY is active high.

When BIBstl is set to 0, the BDIBUSY is active low.

**BOAvCtl :** "Active high control for BDOAVAIL terminal"

When BOAvCtl is set to 1, the BDOAVAIL is active high.

When BOAvCtl is set to 0, the BDOAVAIL is active low.



**BOEnCtl** : "Active high control for BDOEN terminal"

When BOEnCtl is set to 1, the BDOEN is active high.

When BOEnCtl is set to 0, the BDOEN is active low.

**BIEnCtl** : "Active high control for BDIEN terminal"

When BIEnCtl is set to 1, the BDIEN is active high.

When BIEnCtl is set to 0, the BDIEN is active low.

**BLECtl** : "BD Data little endian control"

Set to one set the DMA port Little Ending Mode.

**AutoPad**: "Automatic padding"

Set this bit to 1, set automatic padding for entire data block.

If this bit is 0, write to DMA must add padding bytes for each DMA block.

**BDODely** : "BDO Delay"

BDO Delay time

**BDIDely** : "BDI Delay"

BDI Delay inserts clock interval by each quadlet write to DMA.

BDIBUSY is negated for the duration specified by BDIDelay value.

**BDOMode** : "BDMODE"

See the below table.

**Burst** : "Burst Mode"

When this bit is set to 1, Asynchronous DMA bus work as burst mode.

**BDIMode** : "BDIMODE"

See the below table.

BDI mode	BDO mode	description	input control	output control	in/out select
000	00	8bit parallel input/ 8bit parallel output	BDIEN Sync	BDOEN Sync	N/A
001	01	8bit parallel input/ 8bit parallel output	BDIEN Async	BDOEN Async	N/A
010	01	8bit bi-directional in/out	BDIEN Async	BDOEN Async	N/A
011	10	8bit bi-directional in/out	BDIEN Sync	BDIEN Sync	CFR or BDOEN
100	11	8bit bi-directional in/out scsi mode	BDIEN Async	BDOEN Async	CFR
101	01	16bit bi-directional in/out	BDIEN Async	BDOEN Async	N/A
110	10	16bit bi-directional in/out	BDIEN Sync	BDIEN Sync	CFR or BDOEN
111	11	16bit bi-directional in/out scsi mode	BDIEN Async	BDOEN Async	CFR

**Table 3-40. BDI/BDO mode**

**RcvPad** : "Received data padding bits through to the BDif"

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Data must be written through to the BDif in quadlet multiples.  
 If a packet does not end on a quadlet boundary, zeros are padded to the last quadlet automatically.  
 When RcvPad is set to 1, 1394 is allowed to pad bits through to the BDif.  
 The BDif does not strip the zeros inserted into received packets prior to transferring them to the BDif.  
 When RcvPad is set to 0, 1394 is not allowed to do so.

**BDORst** : "BDO logic reset"  
 When BDORst is set to 1, BDO logic is reset.  
 This bit clears itself. Recommend to do reset when edit 0x94.

**BDIRst** : "BDI logic reset"  
 When BDIRst is set to 1, BDI logic is reset.  
 This bit clears itself. Recommend to do reset when edit 0x94.

**BDOTris** : "BDO tri-state"  
 When BDOTris is set to 1, BDO data bus is forced high-impedance state.  
 Effective to BDIO[15:8] only. (not effect to BDREQ)

0x98	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF/DRF Size	Reserved				DTF_Size				Reserved				DRF_Size																			
Read/Write	N/A				R/W				N/A				R/W																			
Default	6'h00				10'h000				6'h00				10'h040																			
BusReset	6'h00				U				6'h00				U																			

**Table 3-41. CFR map (0x98)**

**DTF\_Size** : "DTF size control bits"  
 DTF\_Size is equal to the DTF size number in 4 quadlets.

**DRF\_Size** : "DRF size control bits"  
 DRF\_Size is equal to the DRF size number in 4 quadlets.



0x9C	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF/DRF Avail	DTFEmpty	Reserved					DTFAvail										DRFEmpty	BDOAvail	Reserved					DRFThere								
Read/Write	R/O	N/A					R/O										R/O	R/O	N/A					R/O								
Default	1	5'h00					10'h000										1	1	5'h00					10'h000								
BusReset	1	5'h00					U										U	U	5'h00					U								

**Table 3-42. CFR map (0x9C)**

**DTFEmpty :**

DTFEmpty specifies the status of DTF status.

**DTFAvail :** "DTF available flag"

DTF has space available for DTFAvail quadlets. (Display remaining size by quadlet)

**DRFEmpty :**

DRFEmpty specifies the status of DRF status.

**BDOAvail :**

Reflect the status of BDOAvail output. (Caution: This bit is not equal to BDOAVAIL output because BDOAVAIL output is allowed to the BOAvlCtl. )

**DRFThere :** "DRF there flag"

DRF has DRFThere quadlets.

0xA0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF/DRF Ack	Reserved							DRAErr	DRxAck				Reserved	DRAVal	Reserved							DTAErr	DtxAck				Reserved	DTAVal				
Read/Write	N/A							R/O				N/A	R/O	N/A							R/O				N/A	R/O						
Default	7'h0							0	4'h0				3'h0	0	7'h0							0	4'h0				3'h0	0				
BusReset	7'h0							0	4'h0				3'h0	0	7'h0							0	4'h0				3'h0	0				

**Table 3-43. CFR map (0xA0)**



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**DRAErr** : "DRF Ack error"  
 Whether the last Ack received for the read request packet for DRF has any errors.  
 When the Ack didn't receive nor had parity error and length error, AckErr shows 1.  
 When the Ack has no error or any Ack has not been received yet, AckErr shows 0.

**DRxAck** : "DRF transmitter acknowledge received"  
 The last Ack received for read request packet for DRF.  
 The value is updated each time the Ack is received.

**DRAVal** : "DRF Ack Valid"  
 Whether DRxAck has been already read.  
 When DRxAck has not read yet, DRAVal shows 1.  
 When DRxAck has already read, DRAVal shows 0.

**DTAErr** : "DTF Ack error"  
 Whether the last Ack received for the packet transmitted from DTF has any errors.  
 When the Ack didn't receive nor had parity error and length error, AckErr shows 1.  
 When the Ack has no error or any Ack has not been received yet, AckErr shows 0.

**DtxAck** : "DTF transmitter acknowledge received"  
 The last Ack received for the packet transmitted from DTF.  
 The value is updated each time the Ack is received.

**DTAVal** : "DTF Ack Valid"  
 Whether DtxAck has been already read.  
 When DtxAck has not read yet, DTAVal shows 1.  
 When DtxAck has already read, DTAVal shows 0.

0xA4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF First & Continue	DTF_First & Continue																															
Read/Write	W/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-44. CFR map (0xA4)**

**DTF\_First & Continue** : "Write any other quadlets than last quadlet of the packet to DTF"  
 This write only register provides the host with the capability to write the quadlets of an transmit packet - except the last quadlet - to DTF.



0xA8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF Update	DTF_Update																															
Read/Write	W/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-45. CFR map (0xA8)**

**DTF\_Update** : "Write last quadlet of the packet to DTF"  
This write only register provides the host with the capability to write the last quadlet of an transmit packet to DTF.

0xAC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Data	DRFRead																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	32'h0000_0000																															

**Table 3-46. CFR map (0xAC)**

**DRFRead** : "DRF data read access register"  
This read only register provides the host with the capability to read the data quadlet of an received packet from DRF. Each read outputs the next quadlet from DRF. If DRF is empty, the last valid value is read.



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0xB0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF Control0	DTFCTL0	DTFCTL1	DTFClr/DRFst	DTFNdIdval	DTFNofity	Reserved	DTF Spd	DTF Max Payload				PgTblEn	DTF Page Size	DTF_BlockSize/ DTF_BlockCount																		
Read/Write	R/W	R/W	R/O	R/W	N/C	R/W	R/W				R/W	R/W	R/W																			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BusReset	*1	U	U	U	U	U	U				U	U																				

**Table 3-47. CFR map (0xB0)**

Note) All bits of this register is N/A when DTpktz=0 in 0x90.

\*1 depend on current condition.

**DTFctl** : "DTF Packetizer transmit control"

Meaning of read value.

DTFCTL0	DTFCTL1	
0	0	IDLE
1	0	BUSY
1	1	PEND
0	1	PAGEFAULT

Effect to write value.

DTFCTL0	DTFCTL1	
0	0	No operation
1	0	Start/Restart
1	1	Init-start
0	1	Abort

**DTFClr/DTFStx** : "DTF clear control bit" (write)"/"DTFStatus Transmit"(read)

When DTFClr is set to "1", Data in DTF is cleared.

This bit clears itself after DTF cleared. Should not assert when DTFctl = busy.

When this bit used for read it specifies whether current transaction is status transfer or not.

Caution) DTF\_dest\_ID(0xB8) data is required to set.

**DTFSt** : "DTF Packetizer Transfer Status" (read)

DTFSt represents DTF is transferring Transaction status data.

**DTFNdIdval** : "DTF NODE Id Valid"

represents Node ID in DTF Destination Id is valid. Writing to DTF destination Id Register sets this bit, and cleared by bus reset.



note) This bit will be cleared after bus reset. And this bit should be 1 when re-setting destination ID on 0xB8 again.

**DTFNotify** : "DTF Notify"

When this bit is set to one, Transaction status data is transferred following DTF data transfer.

**DTFSpd** : "DTF transaction speed"

DTFSpd specifies the speed used by the DTF Packetizer.

- 2'b00 : 100Mbps/s
- 2'b01 : 200Mbps/s
- 2'b10 : 400Mbps/s
- 2'b11 : Not valid

**DTFMaxPayload** : "DTF transfer maximum payload"

DTFMaxPayload is the maximum data transfer length that the DTF Packetizer requests in a single write transaction.

The maximum data transfer length is specified as  $2^{(DTFMaxPayload + 2)}$ .(byte)

**PgTblEn** : "Page table enable"

This bit control fetching of PgTblEn.

When PgTblEn is set to 1, enable page table enable fetch.

When PgTblEn is 0 and AutoPg is set 1, disable page table fetch.

DTF\_destination\_offset\_hi and DTF\_destination\_offset\_lo data point for page table address when PgTblEn is set 1.

When PgTblEn is 0, DTF\_destination\_offset\_hi and DTF\_destination\_offset\_lo are data area.

**DTFPageSize**: "DTF transmit page size"

DTFPageSize specifies the underlying page size of data buffer memory.

Any one request packet is not permitted to cross a page boundary.

DTFPageSize value of zero indicates that the underlying page size is not specified. Otherwise, the page size is  $2^{(DTFPageSize + 8)}$ .

**DTF\_BlockSize/DTF\_BlockCount**: "DTF transmit block size in byte / DTF transmit block count"

When LngSiz in DMA Control(0x90) is set to 0, this value shows DTF\_BlockSize.

When LngSiz is set to 1, it showed DTF\_BlockCount.

DTFBlockSize specifies the transmitted blocksize value.

DTF\_BlockCount specifies the number of transmitted blocks. DTF\_BlockCount is decremented during transmission automatically.

0xB4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF Controll	DTF_BlockCount/DTF_BlockSize																												0			
Read/Write	R/W																												N/A			
Default	30'h0000_00																												00			
BusReset	30'h0000_00																												00			

Table 3-48. CER map (0xB4)



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**DTF\_BlockCount/DTF\_BlockSize:** "DTF transmit block count / DTF transmit block size in byte"  
 When LongBlk in DMA Control(0x90) is set to 1, it showed DTF\_BlockSize.  
 When LongBlk is set to 0, this value shows DTF\_BlockCount.

0xB8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF Control2	DTF_destination_ID										DTF_destination_offset_hi																					
Read/Write	R/W										R/W																					
Default	16'h0000										16'h0000																					
BusReset	U										U																					

**Table 3-49. CFR map (0xB8)**

**DTF\_destination\_ID :** "DTF transferred destination ID"  
 DTF\_destination\_ID specifies transfer destination ID.

**DTF\_destination\_offset\_hi:** "DTF transferred destination start offset high"  
 DTF\_destination\_offset\_hi specifies transfer destination offset high.

0xBC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF Control3	DTF_destination_offset_lo																													0	0	
Read/Write	R/W																													N/A		
Default	30'h0000_0000																													0	0	
BusReset	U																													0	0	

**Table 3-50. CFR map (0xBC)**

**DTF\_destination\_offset\_lo :** "DTF transfer destination start offset low"  
 DTF\_destination\_offset\_lo specifies transfer destination offset low.



0xC0 (packetizer mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control0	DRFCTL0	DRFCTL1	DRFClr/DRFst	DRFNdIdval	DRFNofity	Reserved	DRF Spd	DRF Max Payload				PgTblEn	DRF Page Size	DRF_BlockSize/ DRF_BlockCount																		
Read/ Write	R/W	R/W	R/O	R/W	N/C	R/W	R/W				R/W		R/W																			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BusReset	*1	U	U	U	U	U	U				U		U																			

**Table 3-51. CFR map (0xC0)**

Note) When DRPktz is set to “1” in “0x90”,this table is used.

\*1 depend on current condition.

**DRFCtl** : "DRF Packetizer transmit control"

Meaning of read value.

DRFCTL0	DRFCTL1	
0	0	IDLE
1	0	BUSY
1	1	PEND
0	1	PAGEFAULT

Effect to write value.

DRFCTL0	DRFCTL1	
0	0	No operation
1	0	Start/Restart
1	1	Init-start
0	1	Abort

**DRFClr/DRFStx** : "DRF clear control bit"(write)/"DRF status transmit"(read)

When DRFClr is set to “1”,all state in DRF and Data in DRF and Bulky data buffer is cleared.

This bit clears itself after DRF cleared.

Should not assert when DRFCtl = busy.

When this bit used for read it specifies whether current transaction is status transfer or not.

**DRFst** : "DRF Packetizer Transfer Status" (read)

DRFst represents DRF is transferring Transaction status data.

**DRFNdIdval** : “DRF NODE Id Valid”

represents Node ID in DRF Destination Id is valid. Writing to DRF destination Id Register sets this bit, and cleared by



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bus reset.

note) This bit will be cleared after bus reset. And this bit should be 1 when re-setting destination ID on 0xC8 again.

### **DRFNotify** : "DRF Notify"

When this bit is set to one, Transaction status data is transferred following DRF data transfer.

### **DRFSpd** : "DRF transaction speed"

DRFSpd specifies the speed used by the DRF Packetizer.

2'b00 : 100Mbits/s

2'b01 : 200Mbits/s

2'b10 : 400Mbits/s

2'b11 : Not valid

### **DRFMaxPayload**: "DRF transfer maximum payload"

DRFMaxPayload is the maximum data transfer length that the DRF Packetizer requests in a single read transaction.

The maximum data transfer length is specified as  $2^{(DRFMaxPayload + 2)}$ .

### **PgTblEn** : "Page table enable"

This bit control fetching of PgTblEn.

When PgTblEn is set to 1, enable page table enable fetch.

When PgTblEn is 0 and AutoPg is set 1, disable page table fetch.

DRF\_destination\_offset\_hi and DRF\_destination\_offset\_lo data point for page table address when PgTblEn is set 1.

When PgTblEn is 0, DRF\_destination\_offset\_hi and DRF\_destination\_offset\_lo are data area.

### **DRFPageSize**: "DRF receive page size"

DRFPageSize specifies the underlying page size of data buffer memory.

Any one request packet is not permitted to cross a page boundary.

DRFPageSize value of zero indicates that the underlying page size is not specified.

Otherwise, the page size is  $2^{(DRFPageSize + 8)}$ .

### **DRF\_BlockSize/DRF\_BlockCount**: "DRF receive block size in byte / DRF receive block count"

When LngSiz in DMA Control(0x90) is set to 0, this value shows DRF\_BlockSize.

When LngSiz is set to 1, it showed DRF\_BlockCount.

DRFBlockSize specifies the received blocksize value.

DRF\_BlockCount specifies the number of received blocks. DRF\_BlockCount is decremented during reception automatically.



0xC0 (direct mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control0	DRFBIdEn	DRFSIdEn	DRFAdrEn	Reserved																												
Read/Write	R/W			N/A																												
Default	0	0	0	29'h0000_0000																												
BusReset	U			U																												

**Table 3-52. CFR map (0xC0)**

Note) When DRPktz is set to “0” in “0x90”,this table is used.

**DRFBIdEn** : "DRF bus id check enable"  
 Enables Bus Id check for write request routing control.  
 caution) Valid only during DRFAdrEn=1

**DRFSIdEn** : "DRF source id check enable"  
 Enables Source Id check for write request routing control.  
 caution) Valid only during DRFAdrEn=1

**DRFAdrEn** : "DRF address enable"  
 Enables write request routing function.  
 In this mode write request packet with destination address within the area specified by DRF Control0/1/2 address is stored in DRF.  
 caution) It's accepted to setting illegal qty which stick out areas. But would not work correct.

	0xC0(DRFBIdEn,DRFSIdEn,DRFAdrEn)							
	000	001	010	011	100	101	110	111
All match packet	ARF	DRF	ARF	DRF	ARF	DRF	ARF	DRF
unmatch source_ID	ARF	DRF	ARF	ARF	ARF	DRF	ARF	ARF
unmatch address	ARF	ARF	ARF	ARF	ARF	ARF	ARF	ARF



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0xC4 (packetizer mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control1	DRF_BlockCount/DRF_BlockSize																															
Read/Write	R/W																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-53. CFR map (0xC4)**

**DRF\_BlockCount/DRF\_BlockSize:** "DRF receive block size in byte / DRF receive block count"  
 When LngSiz in DMA Control(0x90) is set to 1, this value shows DRF\_BlockSize.  
 When LngSiz is set to 0, it showed DRF\_BlockCount.  
 DRFBlockSize specifies the received blocksize value.  
 DRF\_BlockCount specifies the number of received blocks. DRF\_BlockCount is decremented during reception automatically.

0xC4 (direct mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control1	DRF_destination_Width																															
Read/Write	R/W																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-54. CFR map (0xC4)**

Note) When DRAdrEn is set to "1" in "0xC0",this table is used.

**DRF\_destination\_Width :** "DRF destination width"  
 DRF\_destination\_Width specifies the address depth to routing write request packet to DRF.

Caution) there is a limit to the value  $FFFF\ FFFF > DRF\_destination\_Width + DRF\_destination\_offset\_lo$



0xC8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control2	DRF_destination_ID											DRF_destination_offset_hi																				
Read/Write	R/W											R/W																				
Default	16'h0000											16'h0000																				
BusReset	U											U																				

**Table 3-55. CFR map (0xC8)**

**DRF\_destination\_ID** : "DRF receive destination ID"  
DRF\_destination\_ID specifies transferred destination ID.

**DRF\_destination\_offset\_hi**: "DRF receive destination offset start high"  
DRF\_destination\_offset\_hi specifies transferred destination offset high.

0xCC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Control3	DRF_destination_offset_lo																														0	0
Read/Write	R/W																														N/A	N/A
Default	30'h0000_0000																														0	0
BusReset	U																														0	0

**Table 3-56. CFR map (0xCC)**

**DRF\_destination\_offset\_lo**

**o** : "DRF receive destination start offset low"  
DRF\_destination\_offset\_lo specifies transferred destination offset low.



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0xD0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Header0	DRF_Header0																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-57. CFR map (0xD0)**

**DRF\_Header0** : "First quadlet of received packet header in DRF"  
 When DRHStr in DMA Control(0x90) is set to 1, the host can read the first header quadlet of a received packet header after the header has been copied into DRF Header0.

0xD4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Header1	DRF_Header1																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-58. CFR map (0xD4)**

**DRF\_Header1** : "Second quadlet of received packet header in DRF"  
 When DRHStr in DMA Control(0x90) is set to 1, the host can read the first header quadlet of a received packet header after the header has been copied into DRF Header1.

0xD8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Header2	DRF_Header2																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-59. CFR map (0xD8)**



**DRF\_Header2** : “Third quadlet of received packet header in DRF”

When DRHStr in DMA Control(0x90) is set to 1, the host can read the first header quadlet of a received packet header after the header has been copied into DRF Header2.

0xDC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Header3	DRF_Header3																															
Read/Write	R/O																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-60. CFR map (0xDC)**

**DRF\_Header3** : “Forth quadlet of received packet header in DRF”

When DRHStr in DMA Control(0x90) is set to 1, the host can read the first header quadlet of a received packet header after the header has been copied into DRF Header3.

0xE0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRF Tailor	Reserved										Rx_Spd		Reserved						FII0		Reserved				DRF_TxAck							
Read/Write	N/A										R/O		N/A						R/O		N/A				R/O							
Default	14'h000										0 0		6'h00						0 0		4'h0				4'h0							
BusReset	14'h000										U		6'h00						U		4'h0				U							

**Table 3-61. CFR map (0xE0)**

**Rx\_Spd** : "DRF receive speed"

Rx\_Spd specifies the speed that DRF receives a response packet with.

2'b00 : 100Mbps/s

2'b01 : 200Mbps/s

2'b10 : 400Mbps/s

2'b11 : Not valid

**FII0** : "The number of fill zero byte"

The FII0 specifies the number of zero-fill bytes in the last quadlet of the packet data payload.



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2'b00 : no zero fill bytes.  
 2'b01 : 3 zero fill byte.  
 2'b10 : 2 zero fill bytes.  
 2'b11 : 1 zero fill bytes.

**DRF\_TxAck** : "DRF send Ack"  
 DRF\_TxAck specifies the sent acknowledgement after receiving the packet.

4'b0000 : Reserved  
 4'b0001 : Ack\_complete  
 4'b0010 : Ack\_pending  
 4'b0011 : Reserved  
 4'b0100 : Ack\_Busy\_X  
 4'b0101 : Ack\_Busy\_A  
 4'b0110 : Ack\_Busy\_B  
 4'b1011 : Ack\_Tardy  
 4'b1100 : Ack\_Conflict\_Error  
 4'b1101 : Ack\_Data\_Error  
 4'b1110 : Ack\_Type\_Error  
 4'b1111 : Ack\_Address\_Error

0xE4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTF/DRF Page count	DTF Page Count										DRF Page Count																					
Read/Write	R/W										R/W																					
Default	0										0																					
BusReset	U										U																					

**Table 3-62. CFR map (0xE4)**

**DTF /DRF Page Count :**  
 DTF/DRF Page count specifies the number of page table entry to be fetched during data transfer. Any number other than zero is valid value. This number is decremented following page fetch action.  
 note) Displaying data decrements during work.



DhdSel=00 0xE8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head0	Reserved										DTxSpd	DTxTlabel					DTxRT	DtxTCode					DTxPrio									
Read/ Write	N/A										R/ O	R/O					R/ O	R/O					R/O									
Default	14'h0000										0 1	6'h00					0 0	4'h1					4'h0									
BusReset	14'h0000										U	U					U	U					U									

**Table 3-63. CFR map (0xE8)**

**DTxSpd** : "DTF/DRF transaction speed code"

DTxSpd represents the speed code with which request packet is been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTxTlabel** : "DTF/DRF transaction tlabel"

DTxTlabel represents the transaction tlabel of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTxRT** : "DTF/DRF transmit retry code"

DTxRT represents the transaction retry code of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DtxTCode** : "DTF/DRF transmit tCode"

DtxTCode represents the transaction tCode of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.  
 When DRPktz is enabled, DtxTCode is set to 4'h1 automatically.

**DTxPrio** : "DTF/DRF transmit priority"

DTxPrio represents the transaction priority of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.



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DhdSel=00 0xEC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head1	DTx_destination_ID																DTx_destination_offset_hi															
Read/ Write	R/O (Note)																R/O (Note)															
Default	16'h0000																16'h0000															
BusReset	U																U															

**Table 3-64. CFR map (0xEC)**

Note)R/W when DTPktz = "0".

**DTx\_destination\_ID** : "DTF/DRF transmit destination ID"

DTx\_destination\_ID represents destination ID where the request packet is been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTx\_destination\_offset\_hi** : "DTF/DRF transmit destination offset high"

DTx\_destination\_offset\_hi represents destination ID where the request packet is been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=00 0xF0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head2	DTx_destination_offset_lo																															
Read/ Write	R/O (Note)																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-65. CFR map (0xF0)**

Note) R/W when DTPktz = "0".

**DTx\_destination\_offset\_lo** : "DTF/DRF transmit destination offset low"

DTx\_destination\_offset\_lo represents the destination ID where the request packet is been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.



DhdSel=00 0xF4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head3	DTx_data_length																DTx_extended_tcode															
Read/ Write	R/O (Note)																R/O (Note)															
default	16'h0008																16'h0000															
BusReset	U																U															

**Table 3-66. CFR map (0xF4)**

Note) R/W when DTPktz = "0".

**DTx\_data\_length** : "DTF/DRF transmit data length"

DTx\_data\_length represents data length of the request packet been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTx\_extended\_tcode** : "DTF/DRF transmit extended tCode"

DTx\_extended\_tcode represents the extended tCode of the request packet been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=01 0xE8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head0	STAT				RESP				Reserved		AckErr	Ack				PSTAT				PRESP				Reserved		PAckErr	PAck					
Read/ Write	R/O				R/O				N/A		R/O	R/O				R/O				R/O				N/A		R/O	R/O					
Default	4'h0				4'h0				3'h0		0	4'h0				4'h0				4'h0				3'h0		0	4'h0					
BusReset	*1				U				U		U	U				*1				U				U		U	U					

**Table 3-67. CFR map (0xE8)**

\*1 Depend on previous status.

**RESP** :

Specified status response received.

**AckErr** : "Ack Error"

Whether the last Ack received for the packet transmitted from DTF has any errors.

When the Ack didn't received nor had parity error and length error, AckErr shows 1.



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When the Ack has no error or any Ack has not been received yet, AckErr shows 0.

#### **ACK :**

Specified Ack code received.

#### **STAT :** "DTF transaction complete state"

DTF\_State is the state that transaction from DRF complete.

- 4'h0 : The request block transaction from DRF completed successfully
- 4'h1 : The packet received Ack-pending and fall in split transaction.
- 4'h2 : The acknowledgement except Ack\_complete, Ack\_Busy\_X and Ack\_pending was returned to the request packet
- 4'h3 : Reserved
- 4'h4 : The transaction was stopped because of page table fetch problem.
- 4'h5 : Reserved
- 4'h6 : Reserved
- 4'h7 : The request packet was transmitted Retry\_Limit times
- 4'h8 : Reserved
- 4'h9 : Reserved
- 4'hA: The response packet was received but rCode is not complete
- 4'hB: The response packet was not received in Split\_Time
- 4'hC: The request packet was stop to send because of a bus reset
- 4'hD: The request packet was removed because of RstTr or Clear
- 4'hE: Reserved
- 4'hF: Reserved

#### **PSTAT :**

Specified page status code received as above lists.

#### **PRESP :**

Specified page status response received.

#### **PAckErr** : "Pagetable Ack Error"

Whether the last Ack received for the pagetable request.

When the Ack didn't received nor had parity error and length error, AckErr shows 1.

When the Ack has no error or any Ack has not been received yet, AckErr shows 0.

#### **PACK :**

Specified page Ack code received.



DhdSel=01 0xEC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head1	Page Number																Reserved															
Read/ Write	R/O																N/A															
Default	0																0															
BusReset	U																0															

**Table 3-68. CFR map (0xEC)**

**Page Number** : "Page number"

Page number specifies the current page number used during current packetization. It is incremented by one, each time when Packetizer fetches new page table. This number is cleared to zero when Packetizer starts from initial state.

DhdSel=01 0xF0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head2	Page length																Page table hi															
Read/ Write	R/O																R/O															
Default	0																0															
BusReset	U																U															

**Table 3-69. CFR map (0xF0)**

**Page length** : "page length"

PageLength field specifies the current page table value used during current packetization.

**Page table hi** : "page table hi"

Page Table hi field specifies the current page table value used during current packetization.



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DhdSel=01 0xF4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DTx Head3	page table lo																															
Read/ Write	R/O																															
default	0																															
BusReset	U																															

**Table 3-70. CFR map (0xF4)**

**Page table lo** : "page table lo"

Page Table lo field specifies the current page table value used during current packetization.

DhdSel=10 0xE8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRx Head0	Reserved										DRxSpd	DRxTlabel				DRxRT	DRxTCode				DRxPrio											
Read/ Write	N/A										R/O	R/O				R/O	R/O				R/O											
Default	14'h0000										0 1	6'h00				0 0	4'h1				4'h0											
BusReset	14'h0000										U	U				U	U				U											

**Table 3-71. CFR map (0xE8)**

**DRxSpd** : "DTF/DRF transaction speed code"

DTxSpd represents the speed code with which request packet is been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DRxTlabel** : "DTF/DRF transaction tlabel"

DTxTlabel represents the transaction tlabel of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DRxRT** : "DTF/DRF transmit retry code"

DTxRT represents the transaction retry code of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DRxTCode** : "DTF/DRF transmit tCode"

DtxTCode represents the transaction tCode of the request packet been transmitting from FIFO.  
 DHdSel in DMA Control(0x90) selects either DTF or DRF.



When DRPktz is enabled, DtxTCode is set to 4'h1 automatically.

**DRxPrio** : "DTF/DRF transmit priority"

DTxPrio represents the transaction priority of the request packet been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=10 0xEC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRx Head1	DRx_destination_ID																DRx_destination_offset_hi															
Read/ Write	R/O (Note)																R/O (Note)															
Default	16'h0000																16'h0000															
BusReset	U																U															

**Table 3-72. CFR map (0xEC)**

Note)R/W when DTPktz = "0".

**DTx\_destination\_ID** : "DTF/DRF transmit destination ID"

DTx\_destination\_ID represents destination ID where the request packet is been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTx\_destination\_offset\_hi** : "DTF/DRF transmit destination offset high"

DTx\_destination\_offset\_hi represents destination ID where the request packet is been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=10 0xF0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRx Head2	DRx_destination_offset_lo																															
Read/ Write	R/O (Note)																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-73. CFR map (0xF0)**

Note) R/W when DTPktz = "0".

**DTx\_destination\_offset\_lo** : "DTF/DRF transmit destination offset low"

DTx\_destination\_offset\_lo represents the destination ID where the request packet is been transmitting from FIFO.



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DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=10 0xF4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DRx Head3	DRx_data_length															DRx_extended_tcode																
Read/ Write	R/O (Note)															R/O (Note)																
default	16'h0008															16'h0000																
BusReset	U															U																

**Table 3-74. CFR map (0xF4)**

Note) R/W when DTPktz = "0".

**DTx\_data\_length** : "DTF/DRF transmit data length"

DTx\_data\_length represents data length of the request packet been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

**DTx\_extended\_tcode** : "DTF/DRF transmit extended tCode"

DTx\_extended\_tcode represents the extended tCode of the request packet been transmitting from FIFO.

DHdSel in DMA Control(0x90) selects either DTF or DRF.

DhdSel=11 0xE8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
DRx Head0	STAT				RESP				Reserved		AckErr		Ack				PSTAT				PRESP				Reserved		PAckErr		PAck				
Read/ Write	R/O				R/O				N/A		R/O		R/O				R/O				R/O				N/A		R/O		R/O				
Default	4'h0				4'h0				3'h0		0		4'h0				4'h0				4'h0				3'h0				0		4'h0		
BusReset	*1				U				U		U		U				*1				U				U		U		U				

**Table 3-75. CFR map (0xE8)**

**STAT** :

Specified status code received as following lists.

**RESP** :

Specified status response received.



**ACK :**

Specified Ack code received.

**STATE :** "DRF packetizer transaction complete state"

DTF\_State is the state that transaction from DRF complete.

- 4'h0 : The request block transaction from DRF completed successfully
- 4'h1 : The packet received Ack-pending and fall in split transaction.
- 4'h2 : The acknowledgement except Ack\_complete, Ack\_Busy\_X and Ack\_pending was returned to the request packet
- 4'h3 : Reserved
- 4'h4 : The transaction was stopped because of page table fetch problem.
- 4'h5 : Reserved
- 4'h6 : Reserved
- 4'h7 : The request packet was transmitted Retry\_Limit times
- 4'h8 : Reserved
- 4'h9 : Reserved
- 4'hA: The response packet was received but rCode is not complete
- 4'hB: The response packet was not received in Split\_Time
- 4'hC: The request packet was stop to send because of a bus reset
- 4'hD: The request packet was removed because of RstTr or Clear
- 4'hE: Reserved
- 4'hF: Reserved

**PSTAT :**

Specified page status code received as above lists.

**PRESP :**

Specified page status response received.

**PACK :**

Specified page Ack code received.

DhdSel=11 0xEC	0	1	2	3	4	5	6	7	8	9	0	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
DRx Head1	Page Number												Reserved																		
Read/ Write	R/W												N/A																		
Default	0												0																		
BusReset	U												0																		

**Table 3-76. CFR map (0xEC)**

**Page Number** : "Page number"

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0xF8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31				
Log/ROM Control (XLOG = 0)	LogATF	LogARF	LogMAgent	LogMTQ	LogMRF	LogAgent	LogCTQ	LogCRF	LogDTFRq	LogDTFRs	LogDRFRq	LogDRFRs	LogARROM	LogRetry	ShortLog	LogClr	XLOG	ROMValid	LogCD	LogFull	LogThere OR ROMAddr															
Read/Write	R/W													N/A	R/W	S/C	R/W	R/O	R/O // R/W										N/A							
Default	30'h0000_0000																														0	0				
BusReset	U																																			

**Table 3-79. CFR map (0xF8)**

**LogATF** : "Record packets transmitted from ATF on LOG"

When LogATF is set to 1, packets transmitted from ATF shall be recorded on Log.

When LogATF is set to 0, packets transmitted from ATF shall not be done.

**LogARF** : "Record packets placed into ARF on LOG"

When LogARF is set to 1, packets placed into ARF shall be recorded on Log.

When LogARF is set to 0, packets placed into ARF shall not be done.

**LogMAgent** : "Record packets accessed to management agent on LOG"

When LogMAgent is set to 1, packets accessed to management agent shall be recorded on Log.

When LogMAgent is set to 0, packets placed into MRF shall not be done.

**LogMTQ** : "Record packets transmitted from MTQ on LOG"

When LogMTQ is set to 1, packets transmitted from MTQ shall be recorded on Log.

When LogMTQ is set to 0, packets transmitted from MTQ shall not be done.

**LogMRF** : "Record packets placed into MRF on LOG"

When LogMRF is set to 1, packets placed into MRF shall be recorded on Log.

When LogMRF is set to 0, packets placed into MRF shall not be done.

**LogAgent** : "Record packets accessed to command block agent on LOG"

When LogAgent is set to 1, packets accessed to command agent shall be recorded on Log.

When LogAgent is set to 0, packets placed into MRF shall not be done.

**LogCTQ** : "Record packets transmitted from CTQ on LOG"

When LogCTQ is set to 1, packets transmitted from CTQ shall be recorded on Log.

When LogCTQ is set to 0, packets transmitted from CTQ shall not be done.

**LogCRF** : "Record packets placed into CRF on LOG"

When LogCRF is set to 1, packets placed into CRF shall be recorded on Log.

When LogCRF is set to 0, packets placed into CRF shall not be done.

**LogDTFRq** : "Record write request packets transmitted from DTF on LOG"

When LogDTFRq is set to 1, write request packets transmitted from DTF shall be recorded on Log.



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When LogDTFRq is set to 0, they shall not be done.

**LogDTFRs** : "Record write response packets received by the DTF on LOG"

When LogDTFRs is set to 1, write response packets received by DTF shall be recorded on Log.

When LogDTFRs is set to 0, they shall not be done.

**LogDRFRq** : "Record read request packets transmitted by DRF on LOG"

When LogDRFRq is set to 1, read request packets transmitted by DRF shall be recorded on Log.

When LogDRFRq is set to 0, they shall not be done.

**LogDRFRs** : "Record read response packets received into DRF on LOG"

When LogDRFRs is set to 1, read response packets received into DRF shall be recorded on Log.

When LogDRFRs is set to 0, they shall not be done.

**LogARROM** : "Record auto-response packet from Configuration ROM on LOG"

When LogARROM is set to 1, auto-response packets including data read from Configuration ROM shall be recorded on Log.

When LogARROM is set to 0, they shall not be done.

**LogRetry** : "Record Retry Packet"

When LogRetry is set to 1, retry packet shall be recorded on Log.

When LogRetry is set to 0, they shall not be done.

**ShortLog** : "Short format log"

When ShortLog is set to 1, packets in general format shall be recorded on Log.

When ShortLog is set to 0, packets in short format shall be recorded on Log.

**LogClr** : "Log clear control bit"

When LogClr is set to 1, Log is cleared.

This bit clears itself after the clear.

**XLOG** : "Select Log data or ConfigROM data"

When XLOG is set to 1, the data read from Log Data( 0xFC ) is ConfigROM data.

When XLOG is set to 0, the data read from Log Data( 0xFC ) is Log data.

note) After XLOG set to 0, please clear LOG using LogClr bit.

**ROMValid** : "Configuration ROM valid"

When ROMValid is set to 1, the data in Configuration ROM is valid.

The receiver shall return Ack\_pending for all quadlet read requests addressed to this Configuration ROM and the respective quadlet read response packets shall be transmitted automatically.

When ROMValid is set to 0, the data in Configuration ROM is invalid.

The receiver will return Ack\_Tardy for all quadlet read requests addressed to this Configuration ROM.

**LogCD** : "Log control bit"

When the first or the last quadlet of a packet is being read from

Log Data(0xFC), LogCD shows 1. Otherwise, LogCD shows 0.

**LogFull** : "Log Full"

When LogFull shows 1, Log is full.

Otherwise, Log is not full.



**LogThere/ROMAddr** : "Log available flag / Address of Configuration ROM"

When XLOG is set to 1, LogThere/ROMAddr is ROMAddr mode.

ROMAddr is the address accessed by the host in Configuration ROM.

When XLOG is set to 0, LogThere/ROMAddr is LogThere mode.

Log has space available for LogThere quadlets.

0xF8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Log/ROM Control (XLOG=1)	DTFSt	DRFSt	Reserved													XLOG	ROMValid	Reserved	Adder													
Read/Write	R/W	R/W	N/A													R/W	R/W	R/O	R/W													
Default	0	0	14'h0000_0000													0	0															
BusReset			U													U	U															

**Table 3-80. CFR map (0xF8)**

**DTFSt** : "DTF status Block access mode"

When DTFSt is set to 1, Adder in this field and 0xFC menu access address and Data for DTF status block.

**DRFSt** : "DRF status Block access mode"

When DRFSt is set to 1, Adder in this field and 0xFC menu access address and Data for DRF status block.

**XLOG** : "Select Log data or ConfigROM data"

When XLOG is set to 1, the data read from Log Data( 0xFC ) is ConfigROM data.

When XLOG is set to 0, the data read from Log Data( 0xFC ) is Log data.

**ROMValid** : "Configuration ROM valid"

When ROMValid is set to 1, the data in Configuration ROM is valid.

The receiver shall return Ack\_pending for all quadlet read requests addressed to this Configuration ROM and the respective quadlet read response packets shall be transmitted automatically.

When ROMValid is set to 0, the data in Configuration ROM is invalid.

The receiver will return Ack\_Tardy for all quadlet read requests addressed to this Configuration ROM.

**Adder**:

Where address for DTF/DRF status Block and config ROM Write/Read.

Caution) Do not read within beyond the limit of writing area.



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0xFC	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Log Data	LogRead/ROMAccess																															
Read/Write	CRW																															
Default	32'h0000_0000																															
BusReset	U																															

**Table 3-81. CFR map (0xFC)**

**LogRead/ROMAccess** : "Log data read access register/Configuration ROM data read access register"  
 Meaning in this field is determined as bellow.

XLOG	DTFSt	DRFst	LogRead/ROMAccess field
0	X	X	LogRead Access
1	0	0	Config Rom access
1	1	0	DTF status Block access
1	0	1	DRF status Block access
1	1	1	NA

note)

Do not access (Read/Write) datas exceeding input packet quantities.



**4. TSB43LV81 Data Formats**

The data formats for transmission and reception for data are shown in the following sections. The transmit formats describe the expected organization of data presented to the TSB43LV81 at the host-bus interface. The received formats describe the data formats that the TSB43LV81 presents to the host-bus interface.

**4.1. Generic Asynchronous Transmit (ATF Interface to TSB43LV81)**

Generic Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. Packet transmission with ATF will be written with below format. As with other packet transmissions, it is accessed through CFR (0x70~0x78) address.

**4.1.1. Generic Quadlet Transmit**

The quadlet-transmit format is shown in Figure 2. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The fourth quadlet is data used only for write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Reserved										spd		tlabel			rt		tCode			prior											
destination ID										Destination_Offset_high																					
destination_offset_Low																															
quadlet data																															

**Figure 2. Generic Transmit Format of Packet with quadlet data**

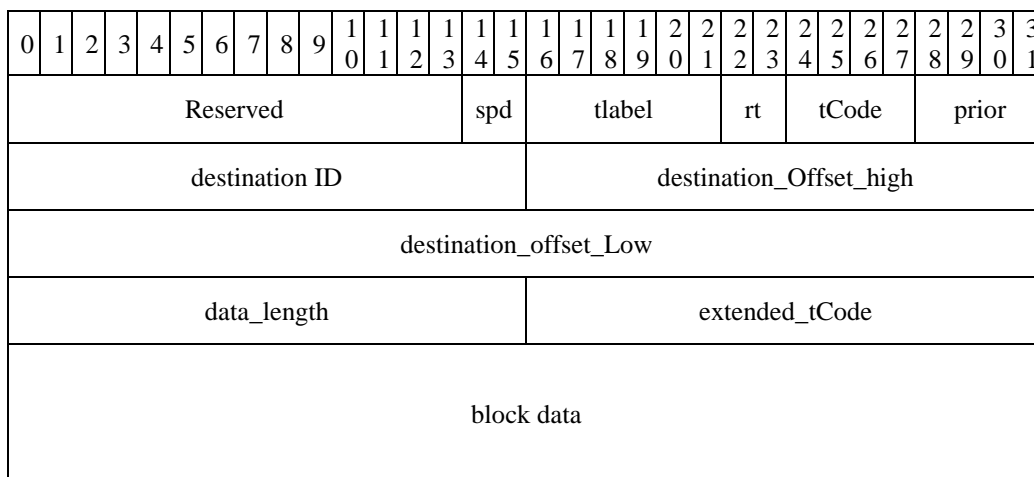


**Table 4-1. Quadlet-Transmit Format**

<b>FIELD NAME</b>	<b>DESCRIPTION</b>
Spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
Tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet. This tlabel must be set except 10_xxxx, 11_xxxx, 01_xxxx which is Block Read Request handling.
Rt	The retry code for this packet is : 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
Tcode	tCode is the transaction code for this packet. (see Table 6-10 of IEEE-1394 standard)
Prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
DestinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of this packet.
Destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination nodes address space. This address must be quadlet aligned (modulo 4).
quadlet data	For write requests and read responses, this field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.

**4.1.2. Generic Block Transmit**

The block-transmit format is shown in Figure 3. The first quadlet contains packet-control information. The second and third quadlets contain the 64-bit address. The first 16 bits of the fourth quadlet contains the dataLength field. The remaining 16 bits represent the extended\_tCode field. (See Table 6-11 of the IEEE-1394 standard for more information on extended\_tCodes.) The block data, if any, follows the extended\_tCode.



**Figure 3. Generic Transmit Format of Packet with block data**



**Table 4-2. Block-Transmit Format Functions**

FIELD NAME	DESCRIPTION
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet. This tlabel must be set except 10_xxxx, 11_xxxx, , 01_xxxx which is Block Read Request handling.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet (see Table 6-10 of IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.
block data	The data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.

**4.2. Generic Asynchronous Receive (TSB43LV81 to ARF Interface)**

Transmission packets from ATF are generally received to ARF. ARF also receives request packets from other nodes, except packets to AGENT. Received packets will be stored in ARF FIFO as below.

**4.2.1. Generic Quadlet Receive**

The quadlet-receive format is shown in Figure 4. The first quadlet is a packet token and contains packet-control information.. The first 16 bits of the second quadlet contains the destination bus and node number, and the remaining 16 bits contain packet-control information. The first 16 bits of the third quadlet contains the bus and node number of the source, and the remaining 4 bits of the third contain packet-control information. The fifth quadlet contains data that was used by write requests and read responses. For read requests and write responses, the quadlet data field is omitted.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
status				Reserved												spd		Reserved												Ack	
Destination ID																tlabel				rt		tCode		prior							
Source ID																rCode				Reserved											
Reserved																															
quadlet data																															

**Figure 4. Generic Received Format of Packet with quadlet data**

**Table 4-3. Quadlet-Receive Format Functions**

FIELD NAME	DESCRIPTION
status	Received packet will go into each Rx FIFO with each status. Each status are shown as below.
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
Ack	This field holds the acknowledge sent by the receiver for this packet. (See Table 6-13 of the IEEE-1394 standard).
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	TCode is the transaction code for this packet. (See Table 6-9 of the IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
rCode	This field is the response code for this packet. (See Table 6-11 of the IEEE-1394 standard).
quadlet data	For write requests and read responses, this field holds the transferred data. For write responses and read requests, this field is not present.

<status>

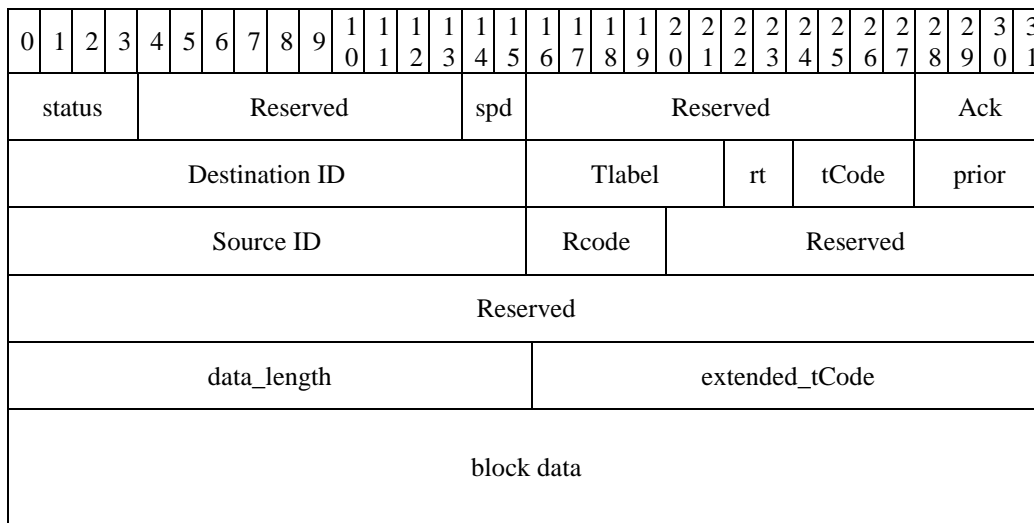
- 4'h0 : Ack\_comp was returned to the request packet  
Transaction is terminated by SplitEn =1 in case of receiving Ack\_Pnd for request packet on ATF.
- 4'h1 : The packet, which does not require any acknowledgement, was transmitted
- 4'h2 : The acknowledgement except Ack\_comp, Ack\_Busy\_X and Ack\_Pnd was returned to the request packet. Ack\_Pnd received for Response packettransmit on ATF/
- 4'h3 : Ack was not returned to the request packet  
long acknowledge receive, short acknowledge receive, acknowledge parity error.
- 4'h4 : No next packet on CTQ due to fetched packet which next ORB is Invalid
- 4'h5 : Nex request packet is set up to CTQ because fetched packet which having next ORB pointer.
- 4'h6 : Reserved
- 4'h7 : Retry time out due to retry count exceed Retry\_limit value.
- 4'h8 : CTQ: no request packet in CTQ due to received packet which has invalid NextORB or CnxFtEn=0.  
MTQ: response packet  
ATF: response packet by split transaction request
- 4'h9 : Request packet for getting nextORB is setup to CTQ
- 4'hA : The response packet was received but rCode is not complete
- 4'hB : Reserved
- 4'hC : Reserved
- 4'hD : Reserved
- 4'hE : Reserved
- 4'hF : Received except response packet. (expect split transaction response)



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**4.2.2. Generic Block Receive**

The block-receive format is shown in Figure 5. The first 16 bits of the second quadlet contain the bus and node number of the destination node, and the last 16 bits contain packet-control information. The first 16 bits of the third quadlet contain the bus and node number of the source node, and the last 16 bits of the third quadlet and all of the fourth quadlet contain the 48-bit, quadlet-aligned destination offset address. All remaining quadlets contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted.



**Figure 5. Generic Received Format of Packet with block data**

**Table 4-4. Block-Receive Format Functions**

<b>FIELD NAME</b>	<b>DESCRIPTION</b>
status	Received packet will go into each Rx FIFO with each status. Each status are shown as below.
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
Ack	This field holds the acknowledge sent by the receiver for this packet. (See Table 6-13 of the IEEE-1394 standard).
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	TCode is the transaction code for this packet. (See Table 6-9 of the IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
rCode	This field is the response code for this packet. (See Table 6-11 of the IEEE-1394 standard).



data-length	For write request, read responses, and locks, this field indicates the number of bytes being transferred. For read requests, this field indicates the number of bytes of data to be read. A write-response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.
block data	For write requests and read responses, this field holds the transferred data. For write responses and read requests, this field is not present.

<status>

- 4'h0 : Ack\_comp was returned to the request packet  
Transaction is terminated by SplitEn =1 in case of receiving Ack\_Pnd for request packet on ATF.
- 4'h1 : The packet, which does not require any acknowledgement, was transmitted
- 4'h2 : The acknowledgement except Ack\_comp, Ack\_Busy\_X and Ack\_Pnd was returned to the request packet. Ack\_Pnd received for Response packettransmit on ATF/
- 4'h3 : Ack was not returned to the request packet  
long acknowledge receive, short acknowledge receive, acknowledge parity error.
- 4'h4 : No next packet on CTQ due to fetched packet which next ORB is Invalid
- 4'h5 : Nex request packet is set up to CTQ because fetched packet which having next ORB pointer.
- 4'h6 : Reserved
- 4'h7 : Retry time out due to retry count exceed Retry\_limit value.
- 4'h8 : CTQ: no request packet in CTQ due to received packet which has invalid NextORB or CnxFtEn=0.  
MTQ: response packet  
ATF: response packet by split transaction request
- 4'h9 : Request packet for getting nextORB is setup to CTQ
- 4'hA : The response packet was received but rCode is not complete
- 4'hB : Reserved
- 4'hC : Reserved
- 4'hD : Reserved
- 4'hE : Reserved
- 4'hF: Received except response packet. (expect split transaction response)

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**4.3. DTF/DRF packet format**

4.3.1. DRF Packet format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
status				Reserved												spd		Reserved												Ack	
Destination ID														Tlabel				rt		tCode				prior							
Source ID														Rcode				Reserved													
Reserved																															
data_length																extended_tCode															
block data																															

**Figure 6. DRF Packet format with block data**

**Table 4-5. Block-Receive Format Functions**

FIELD NAME	DESCRIPTION
status	Received packet will go into each Rx FIFO with each status. Each status are shown as below.
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
Ack	This field holds the acknowledge sent by the receiver for this packet. (See Table 6-13 of the IEEE-1394 standard).
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	TCode is the transaction code for this packet. (See Table 6-9 of the IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
sourceID	This is the node ID of the sender of this packet.
rCode	This field is the response code for this packet. (See Table 6-11 of the IEEE-1394 standard).
data-length	For write request, read responses, and locks, this field indicates the number of bytes being transferred. For read requests, this field indicates the number of bytes of data to be read. A write-

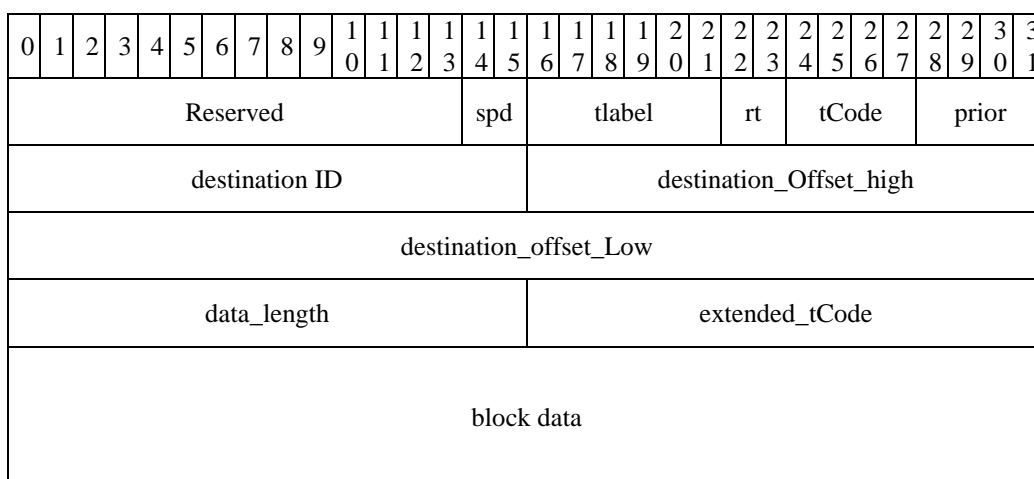


	response packet does not use this field. Note that the number of bytes does not include the head, only the bytes of block data.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.
block data	For write requests and read responses, this field holds the transferred data. For write responses and read requests, this field is not present.

<status>

- 4'h0 : The request block transaction from DRF completed successfully
- 4'h1 : The packet received Ack-pending and fall in split transaction.
- 4'h2 : The acknowledgement except Ack\_complete, Ack\_Busy\_X and Ack\_pending was returned to the request packet
- 4'h3 : Reserved
- 4'h4 : The transaction was stopped because of page table fetch problem.
- 4'h5 : Reserved
- 4'h6 : Reserved
- 4'h7 : The request packet was transmitted Retry\_Limit times
- 4'h8 : Reserved
- 4'h9 : Reserved
- 4'hA: The response packet was received but rCode is not complete
- 4'hB: The response packet was not received in Split\_Time
- 4'hC: The request packet was stop to send because of a bus reset
- 4'hD: The request packet was removed because of RstTr or Clear
- 4'hE: Reserved
- 4'hF: Reserved

#### 4.3.2. DTF packet format



**Figure 7. DTF Packet Format with block data**



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**Table 4-6. Block-Transmit Format Functions**

<b>FIELD NAME</b>	<b>DESCRIPTION</b>
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet. This tlabel must be set 01_xxxx which is Block Read Request handling.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet (see Table 6-10 of IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
destination OffsetHigh, destination OffsetLow	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
dataLength	The number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.
block data	The data to be sent. If dataLength is 0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in byte 0 of the first quadlet.



**4.4. Phy Packet common format**

The format of the transmitted Phy configuration packet is shown in Figure 6. The Phy configuration packet transmit contains two quadlets, which are loaded into the ATF. The first quadlet is written to address 70h. The second quadlet is written to address 78h. The 00E0h in the first quadlet tells the LINK that this is the Phy configuration packet. The 'Eh' is then replace with 0h before the packet is transmitted to the Phy interface.

There is a possibility of a false header error on receipt of a Phy configuration packet. If the first 16 bits of a Phy configuration packet happen to match the destination identifier of a node (bus number and node number), the TSB41LV81 issues a header error since the node misinterprets the Phy configuration packet as a data packet addressed to the node.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31														
0	0	root_ID						R	T	gap_cnt						0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0													
Logical inverse of first quadlet																1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

**Figure 6. Phy Configuration Format**

**Table 4-5. Phy Configuration Format Functions**

FIELD NAME	DESCRIPTION
00	This field is the Phy configuration packet identifier.
root_ID	This field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	This field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new Phy configuration packet is received.

A Phy configuration packet with R = 0, and T = 0 is reserved and is ignored when received .



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**4.5. PHY other packet formats**

**4.5.1. Link-On packet**

Reception of the following cable PHY packet shall cause a PH\_EVENT.indication on LINK\_ON.

0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	3	3		
0	1	phy_ID						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Logical inverse of first quadlet																															

FIELD NAME	DESCRIPTION
Phy_ID	Physical node identifier of the destination of this packet.

**4.5.2. PHY configuration packet**

It is possible to configure Serisal Bus performance in the following ways.

- A) Optimize the gap\_count used by all nodes to a smaller value (appropriate to the actual worst case round-trip delay between any two nodes); and
- B) Force a paticular node to be the root after the next bus initialization (for instance, to insure that the root is cycle master capable).

Both of these actions shall be effect for all nodes (including the originator) by means of PHY configuration packet show bellow. The PH\_CONTROL.request service affects only the local node and is not recommended for changes to either gap\_count or force\_root.

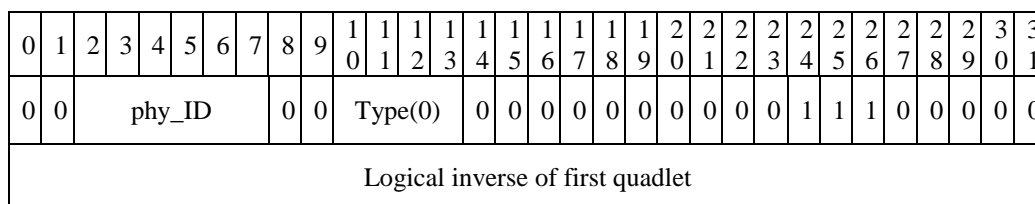
0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	3	3		
0	0	Root_ID						R	T	gap_count						0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Logical inverse of first quadlet																																



FIELD NAME	DESCRIPTION
root_ID	This field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T	When T is set, the PHY_CONFIGURATION.gap_count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	This field contains the new value for PHY_CONFIGURATION.gap_count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new Phy configuration packet is received.
Phy_ID	Physical node identifier of the destination of this packet.

#### 4.5.3. PING packet

The reception of the cable PHY packet shall cause the node identified by phy\_ID to transmit self\_ID packet(s) that reflect the current configuration and status of the PHY. Because of other actions, such as the receipt of a PHY configuration packet, the self-ID packet transmitted may differ from that of the most recent self-identify process.



FIELD NAME	DESCRIPTION
Phy_ID	Physical node identifier of the destination of this packet.
Type	Extended PHY packet type (zero indicates ping packet)

A PHY shall transmit a self-ID packet within RESPONSE\_TIME after the receipt of a ping packet.



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**4.5.4. Remote access packet**

The reception of the cable PHY packet shall cause the node identified by phy\_ID to read the selected PHY register and subsequently return a remote reply packet that contains the current value of the PHY register,

0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
0	0	phy_ID				0	0	Type		page		port			reg		1	1	1	0	reserved										
Logical inverse of first quadlet																															

FIELD NAME	DESCRIPTION
Phy_ID	Physical node identifier of the destination of this packet.
Type	Extended PHY packet type 1 Register read ( base register ) 5 Register read ( paged register )
Page	This field corresponds to the Page_select field in the PHY registers. The register read behaves as if Page_select was set to this value.
Port	This field corresponds to the Port_select field in the PHY registers. The register read behaves as if Port_select was set to this value.
reg	This field, in combination with page and port, specifies the PHY register. If type indicates a read of the base PHY registers reg directly addresses one of the first eight PHY registers. Otherwise the PHYregister address is $1000_2 + \text{reg}$ .

**4.5.5. Remote command packet**

The reception of the cable PHY packet shall request the node identified by phy\_ID to perform the operation specified and subsequently return a remote confirmation packet.

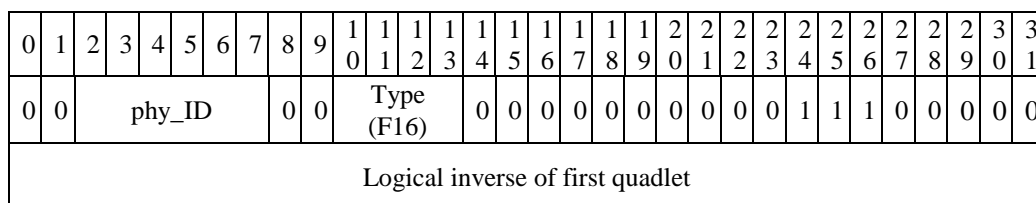
0	1	2	3	4	5	6	7	8	9	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3
0	0	phy_ID				0	0	Type(8)		0	0	0	port			0	0	0	1	1	1	0	cmnd								
Logical inverse of first quadlet																															



FIELD NAME	DESCRIPTION
Phy_ID	Physical node identifier of the destination of this packet.
Type	Extended PHY packet type (8 indicates command packet)
Port	This field selects one of the PHY's ports.
cmnd	Command: 0: NOP 1: Transmit TX_DISABLE_NOTIFY then disable port 2: Initiate suspend (I.e., become a suspend initiator) 4: Clear the port's Fault bit to zero 5: Enable port 6: Resume port

#### 4.5.6. Resume packet

The reception of the cable PHY packet shall cause any node to commence resume operations for all PHY ports that are both connected and suspended. This is equivalent to setting the resume variable TRUE for each of these ports. The resume packet is broadcast; there is no reply.



FIELD NAME	DESCRIPTION
Phy_ID	Physical node identifier of the destination of this packet.
Type	Extended PHY packet type (F16 indicates resume packet)



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**4.6. MTQ/CTQ Asynchronous Transmit (ATF Interface to TSB43LV81)**

MTQ/CTQ Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. Packet transmission with MTQ/CTQ will be written with below format. As with other packet transmissions, it is accessed through CFR (0x70~0x78) address. tlabel and tCode attached to a packet direct each request and response packet to appropriate FIFO. In IEEE1394, a response packet needs to have the same tlabel as its request packet. With this rule, TSB43LV81 assigns the response packet from the initiator to each Receive FIFO.

**4.6.1. MTQ/CTQ Format**

Packets transmitted from MTQ/CTQ are the same as Block Read Request in write format to ATF. However, as stated in previous section, this has to be a Block Read Request with the specified tlabel. The quadlet-transmit format is shown in Figure 6. The first quadlet contains packet control information. The second and third quadlets contain the 64-bit, quadlet-aligned address. The data\_length of packet transmitted from MTQ should be set 32bytes alone.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Reserved										spd		tlabel			rt		tCode			prior											
destination ID										destination_Offset_high																					
destination_offset_Low																															
data_length																extended_tCode															

**Figure 7. MTQ/CTQ Transmission Block Read Packet Format**

**Table 4-6. Block-Transmit Format Functions**

<b>FIELD NAME</b>	<b>DESCRIPTION</b>
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet. This tlabel must be set 10_xxxx in case of using MTQ and must be set 11_xxxx in case of CTQ.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	TCode is the transaction code for this packet (see Table 6-10 of IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
destinationID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.

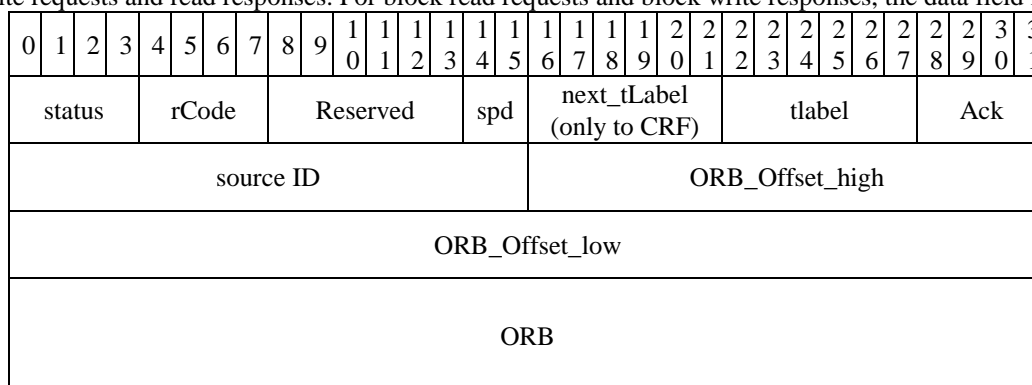


destination Offset_high, destination Offset_low	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4). The upper four bits of the destination OffsetHigh field are used as the response code for lock-response packets and the remaining bits are reserved.
data-length	The number of bytes of data to be transmitted in the packet. The data_length of packet transmitted from MTQ should be set 32bytes alone.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.

#### 4.6.2. MRF/CRF Format

ORB format is stored with ORB pointer address. Setting MShtFmt and CShtFmt on CFR/ORB Fetch Control (0x44) will record ORB in shortened format. This enables FIFO to be used effectively and speed up read access.

MRF/CRF received short format is shown in Figure 8. The first quadlet contains packet-control information. The first 16 bits of the second quadlet contain the bus and node number of source, and the last 16 bits of the third quadlet and all of the fourth quadlet contain the 48-bit, quadlet-aligned ORB offset address. All remaining quadlets contain data that is used only for write requests and read responses. For block read requests and block write responses, the data field is omitted.

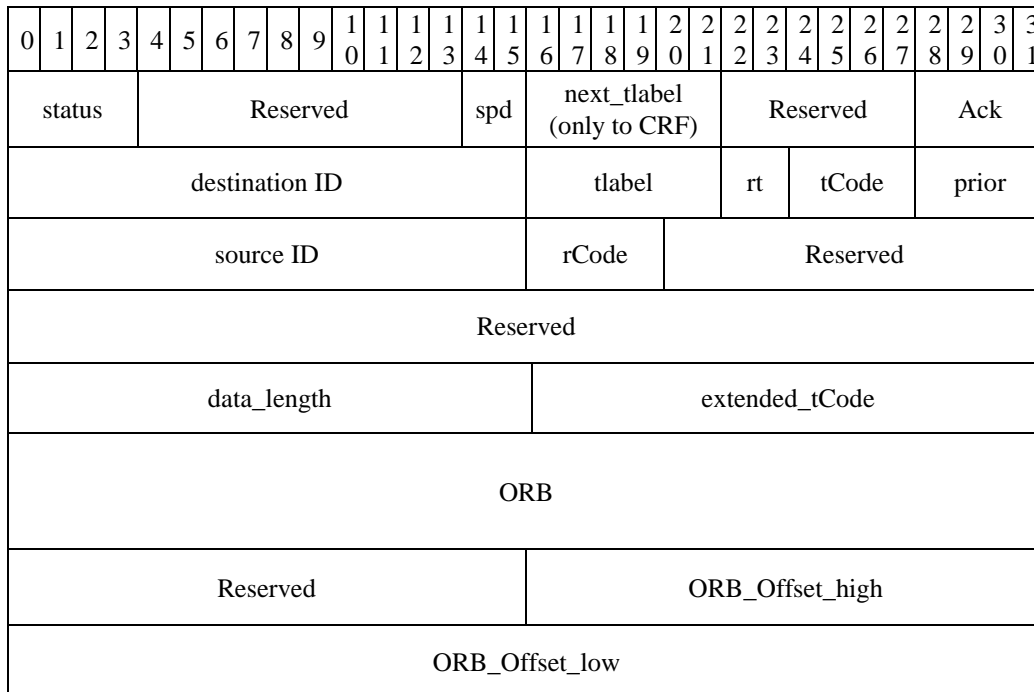


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**Table 4-7. Block-Receive Short Format Functions**

FIELD NAME	DESCRIPTION
status	Received packet will go into each Rx FIFO with each status. Each status is shown as below.
rCode	This field is the response code for this packet. (See Table 6-11 of the IEEE-1394 standard).
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
next_tlabel	LINK command automatically generate request packet to fetch next command block ORB. This is tlabel for next packet. When not generate its automatically request packet, this is 6'b00_0000. (Note.) next_tlabel is only to CRF.
tlable	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
Ack	This field holds the acknowledge sent by the receiver for this packet. (See Table 6-13 of the IEEE-1394 standard).
sourceID	This is the node ID of the sender of this packet.
ORB_Offset_high ORB_Offset_low	These fields are ORB destination offset address that fetched from Initiator.
ORB	This is ORB pointer data that fetched from Initiator.



**Figure 9. MRF/CRF Received Long Format (ORB)**



**Table 4-8. Block-Receive Long Format Functions**

FIELD NAME	DESCRIPTION
status	Received packet will go into each Rx FIFO with each status. Each status is shown as below.
spd	This field indicates the speed at which this packet is to be sent. 00 = 100 Mb/s, 01 = 200 Mb/s, and 10 = 400 Mb/s, and 11 is undefined for this implementation.
next_tlabel	LINK command automatically generate request packet to fetch next command block ORB. This is for next packet. When not generate its automatically request packet, this is 6'b00_0000. Note.) next_tlabel is only to CRF.
Ack	This field holds the acknowledge sent by the receiver for this packet. (See Table 6-13 of the IEEE-1394 standard).
destination ID	This is the concatenation of the 10-bit bus number and the 6-bit node number that forms the node address to which this packet is being sent.
tlabel	This field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This is used to pair up a response packet with its corresponding request packet.
rt	The retry code for this packet is 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.
tCode	tCode is the transaction code for this packet (see Table 6-10 of IEEE-1394 standard).
prior	The priority level for this packet. For cable implementation, the value of the bits must be zero. For backplane implementation, see clause 5.4.1.3 and 5.4.2.1 of the IEEE-1394 standard.
source ID	This is the node ID of the sender of this packet.
rCode	This field is the response code for this packet. (See Table 6-11 of the IEEE-1394 standard).
data_length	The number of bytes of data to be transmitted in the packet.
extended_tCode	The block extended_tCode to be performed on the data in this packet. See Table 6-11 of the IEEE-1394 standard.
ORB	This is ORB pointer data that fetched from Initiator.
ORB_Offset_high / low	These fields are ORB destination offset address that fetched from Initiator.

<status>

4'h0 : Ack\_comp was returned to the request packet

4'h1 : The packet which does not require any acknowledgement was transmitted

4'h2 : The acknowledgement except Ack\_comp, Ack\_Busy\_X and Ack\_Pnd was returned to the request packet

4'h3 : Ack was not returned to the request packet

4'h4 : Doorbell was rung and the response packet was received.

The packet is not queued to fetch next command block ORB

4'h5 : Doorbell was rung and the response packet was received

The packet is queued to fetch next command block ORB

4'h6 : Reserved

4'h7 : The request packet was transmitted Retry\_Limit times

4'h8 : ORBPointer was written and the response packet was receive. The packet is not queued to fetch next command block because next\_ORB\_offset field is null or CnxFtEn(0x44) is 0

4'h9 : ORBPointer was written and the response packet was received

The packet is queued to fetch next command block ORB

4'hA : The response packet was received but rCode is not complete

4'hB : The response packet was not received in Split\_Time

4'hC : The request packet was removed because of a bus reset

4'hD : The request packet was removed because of RstTr or Clear

4'hE : Reserved

4'hF : Reserved.



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### 4.7. Status Block Set-up

TSB43LV81 can send Status block packet to initiator when DMA successfully completed to write/read entire amount of data. The contents of status block packet should be loaded before starting DMA. This function is Active only when the Notify bit is set. Below is basic Status Block format.

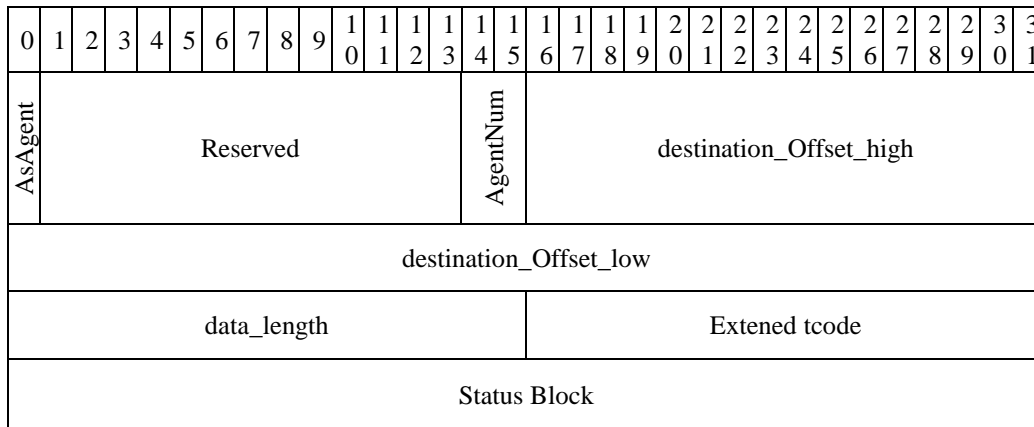


Figure 10. Status Block Format

Table 4-8. Status Block Format Functions

FIELD NAME	DESCRIPTION
AsAgent	Associates corresponding Agent for this transaction. The only difference between associated and non associated is when status transfer is not successful. The agent status specified by agent number is fall into dead state. Setting AsAgent=0 is Activate.
AgentNum	Specifies the agent number associated by this transaction.
Destination Offset_high, destination Offset_low	The concatenation of these two fields addresses a quadlet in the destination node's address space. This address must be quadlet aligned (modulo 4) and address of status FIFO at Initiator.
Data_length	The number of bytes of status block size is transmitted in the packet.
Status Block	SBP-2 Status block. Refereed to SBP-2 standard.

To load Status Block Packet into Internal RAM

- 1.) Set Size of Status Block FIFO  
0x94, MTXBufSiz bit is FIFO Size of status block. To set 8 quadlet of entire status block packet (for example, write 0x06 to this field). This field should be half size of status block packet in quadlet.
- 2.) Set internal RAM to status write mode  
0xF8, DTFST/DRFST bit can enable to access Status FIFO. Set on of them, then host can access to Status FIFO.
- 3.) Write Status Block packet  
Host can write Status Block Packet through 0xFC. Request writing in 0xFC will process its address automatically.
- 4.) Active Status Block  
Set Notify bit enable to send Status Block Packet. Notify bit is located at both of DTF and DRF control.



**5. Configuration ROM setup**

TSB43LV81 can have CSR ConfigROM as stated in IEEE1212 up to 528bytes. And it can auto-respond to Quadlet Read Request.

Below is a basic ConfigROM structure for typical SBP-2 target device. Each system has a different structure and this is for reference only.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
4				0x11				ROM CRC																							
0x3133439 (ASCII "1394")																															
Node Options (0x00FF_2000)																															
Node_vender_ID																								Chip_ID_hi							
Chip_ID-low																															
4				Root directory CRC																											
0x03				module_vender_ID																											
0x81				Test lead offset																											
0x0C				node_capability ( 0x00_83C0 )																											
0xD1				Unit directory offset																											
7							Unit directory CRC																								
0x12				unit spec ID ( 0x00_609E )																											
0x13				unit sw version ( 0x01_0483 )																											
0x38				command set spec ID																											
0x39				command_set																											
0x54				csr_offset ( 0x00_4000 )																											
0x3A				Logical unit characteristics ( 0x00_0A08 )																											
0x14				Device type and LUN ( 0 )																											

**Figure 10. ConfigROM base structure (reference SBP-2 DRAFT)**



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After power is on, write number of bytes written in ConfigROM into AR\_ConfigROM\_Size on CFR/Config ROM Control (0x8C). Value between ConfigROM address (FFFF\_F000\_0400) and this will be subject for ConfigROM Autoreponse. If content of ConfigROM does not exceed 528Bytes, write value of AR\_ConfigROM\_Size to ConfigROM\_Size. If it is more than 528Bytes, write total ConfigROM size into ConfigROM\_Size. As stated previously, HOST needs to transact response for ConfigROM larger than AR\_ConfigROM\_Size.

Next, HOST will load ConfigROM to TSB43LV81 by CFR / XLOG Control (0xF8) and CFR/Log Data (0xFC). First, set XLOG bit to make LogData accessible to ROM. And write 0x400 into ROMAddr, which is to write data for ConfigROM address FFFF\_F000\_0400 into ROMAccess. Repeat writing in LogRead will process its address automatically and will write ConfigROM data in order. To check data, write start address to ROMAddr, then read ROMAccess.

(Note: ConfigROM\_Size does not exceed 1024 Bytes)

Then, clear XLOG bit on CFR/XLOG Control (0xF8), and at the same time, set ROMValid to indicate ConfigROM is valid. If this ROMValid were not set, LINK would respond Ack\_Tardy for Ack to ConfigROM read request.



## 6. Internal Agent Operation for Initiator

This section describes what internal Command Block Fetch Agent act for various accesses by Initiators. Command Block Agent registers are located in CSR address that set by Agent Base offset (0x4C) and each Command block Agent is separated by 0x20 offset.

### 6.1. Internal Agent Transaction for Write Request from Initiator

When each Active Agent Register receive Write request, Internal Agent operates various behavior. Agent state transaction is shown in Table 6-1.

**Table 6-1. Agent Transaction for Write Request from Initiator**

State	Register	Err/Comp <sup>§1</sup>	Action <sup>§2</sup>	Agent Transaction <sup>§3</sup>
RESET	AGENT_STATE	<i>type_error</i>	<i>pending</i>	Auto-resp
	AGENT_RESET	complete	-	-
	ORB_POINTER	complete	Write <sup>1</sup> and CTQ <sup>2</sup>	ACTIVE
	DOORBELL	complete	DrBll <sup>3</sup> = 1	-
	UNSOLICITED_STATE_ENABLE	complete	UnStEn <sup>4</sup> = 1	-
ACTIVE	AGENT_STATE	<i>type_error</i>	<i>pending</i>	Auto-resp
	AGENT_RESET	complete	Reset Agent State	RESET
	ORB_POINTER	<i>conflict_error</i>	-	-
	DOORBELL	complete	DrBll <sup>3</sup> = 1	-
	UNSOLICITED_STATE_ENABLE	complete	UnStEn <sup>4</sup> = 1	-
SUSPENDED	AGENT_STATE	<i>type_error</i>	<i>pending</i>	Auto-resp
	AGENT_RESET	complete	Reset Agent State	RESET
	ORB_POINTER	complete	Write <sup>1</sup> and CTQ <sup>2</sup>	ACTIVE
	DOORBELL	complete	DrBll <sup>3</sup> = 1 <sup>5</sup>	-
	UNSOLICITED_STATE_ENABLE	complete	UnStEn <sup>4</sup> = 1	-
DEAD	AGENT_STATE	<i>type_error</i>	<i>pending</i>	Auto-resp
	AGENT_RESET	complete	Reset Agent State	RESET
	ORB_POINTER	complete	-	-
	DOORBELL	complete	DrBll <sup>3</sup> = 1	-
	UNSOLICITED_STATE_ENABLE	complete	UnStEn <sup>4</sup> = 1	-
Any State	Reserved Agent Area	pending <sup>6</sup>	Stored in ARF	-

§ 1 If it's possible to write AGENT\_STATE Register, Internal Agent returns Ack\_complete. (Setting AckPnd, Agent returns Ack\_pending)  
If it's impossible to write AGENT\_STATE Register, Internal Agent returns acknowledge which follows table 6-2.

§ 2 Agent Operation

§ 3 Agent State Transaction by Write Request

1 Update ORB Pointer Register



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- 2 Loading Read Request Packet in CTQ
- 3 This field shows DrBll of Agent Status Register (0x5C) .
- 4 This field shows UnStEn of Agent Status Register (0x5C).
- 5 If DrBFtEn(ORB Fetch Control 0x44 ) is set to ‘1’, loading Read Request Packet in CTQ again.
- 6 Returned Ack\_pending

**Table 6-2. Response to unexpected**

StErPkt	ErrResp	Ack to Initiator	Response Packet to Initiator and other Actions
1	0	ack_complete	Received packet shall be stored in ARF
0	1	ack_pending	The packet which has resp_type_error or resp_conflict_error shall be sent to Initiator
0	0	ack_type_error or ack_conflict_error	-

**6.2. Internal Agent Transaction for Read Request from Initiator**

**Table 6-3. Agent Transaction for Read Request from Initiator**

Register	Ack and Response Packet
AGENT_STATE	ack_pending Read Response (resp_complete)
AGENT_RESET	ack_type_error <sup>7</sup>
ORB_POINTER	ack_pending Read Response (resp_complete)
DOORBELL	ack_type_error <sup>7</sup>
UNSOLICITED_STATE_ENABLE	ack_type_error <sup>7</sup>
Reserved Agent Area	ack_pending stored in ARF

<sup>7</sup> Ack and Response packet is controlled by StErPkt and ErrResp setting (Control Register 0x80)

**6.3. Controlling Command ORB Fetch Request**

CAftSt of ORB Fetch Control Register (0x44) is set to 1 when each Agent is ready for writing Read Request to CTQ. When host writes ‘1’ to CAftSt, Read Request is loaded to CTQ and CAftSt is set to ‘0’.

**Table 6-4. ORB Fetch Control**

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0x44 ORB Fetch Control	MagtVld	MagtBsy	Reserved	MShftFmt	MORB_ Prior				CORB_ Size								CAG0Vld	CAG1Vld	CAG2Vld	CAG3Vld	DrBISnp	DrBFtEn	CnxFtEn	CShtFmt	CAG0Qrdy	CAG1Qrdy	CAG8Qrdy	CAG3Qrdy	CORB_ Prior			



**6.4. Agent Behavior by write to DOORBELL Register**

**Table 6-5. DOORBELL Special Functions**

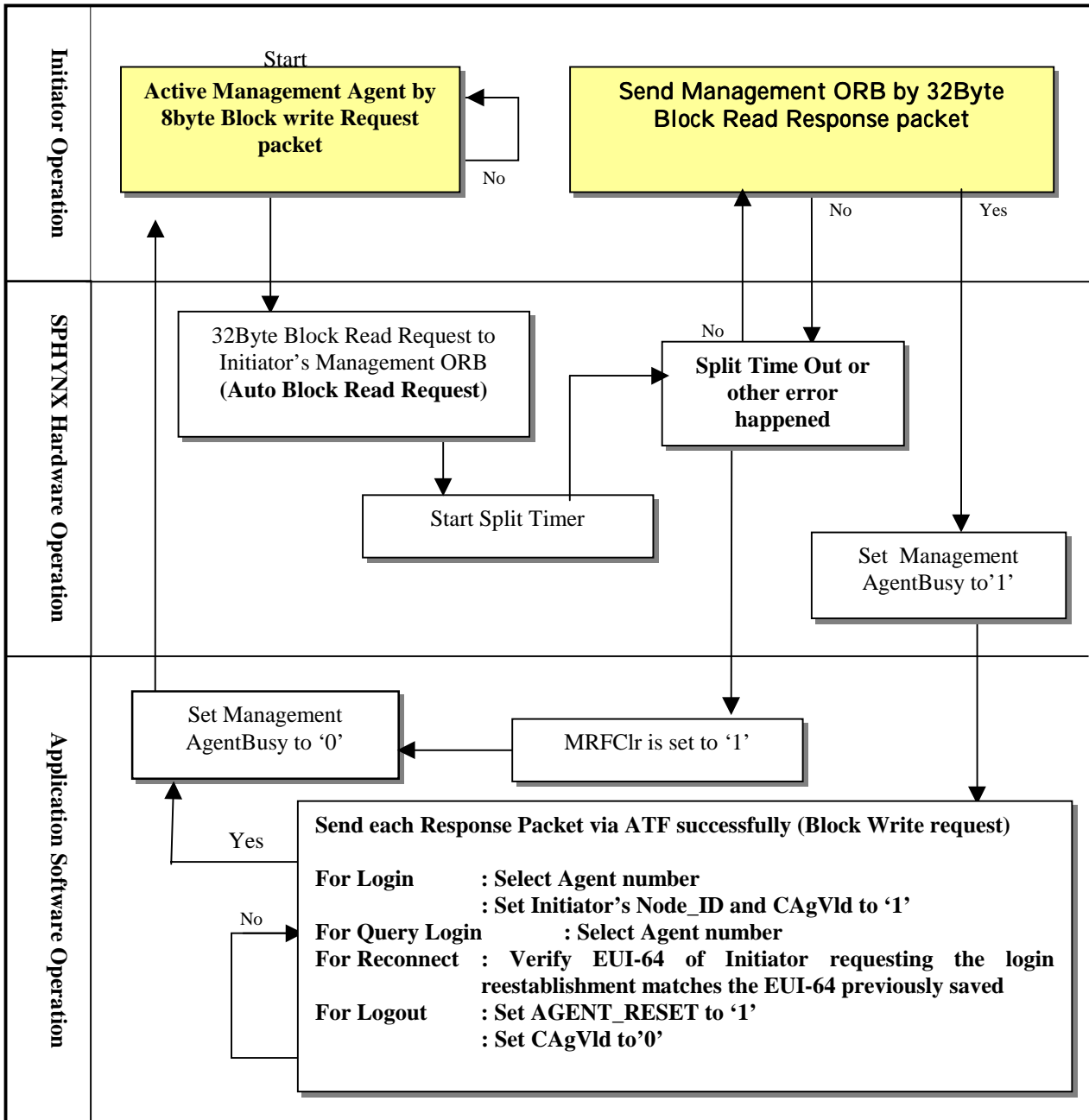
<b>DrBlSnP</b>	<b>DrBFtEn</b>	<b>ORB fetch Operation when DOORBELL is written</b>
X	0	AgentWrInt(0x0C) occurs and DrBlI(0x5C) becomes '1'.
0	1	Fetching only next_ORB field of previous ORB Block. No stored in CRF. And fetching Command_ORB. This packet is stored in CRF.
1	1	Fetch previous ORB Block. Stored it in CRF and Fetch Command ORB included in it from the address
1	0	Reserved

This list effect on CShFmt(0x44) = 1 only.

**7. Typical ORB Fetch Command Operation**

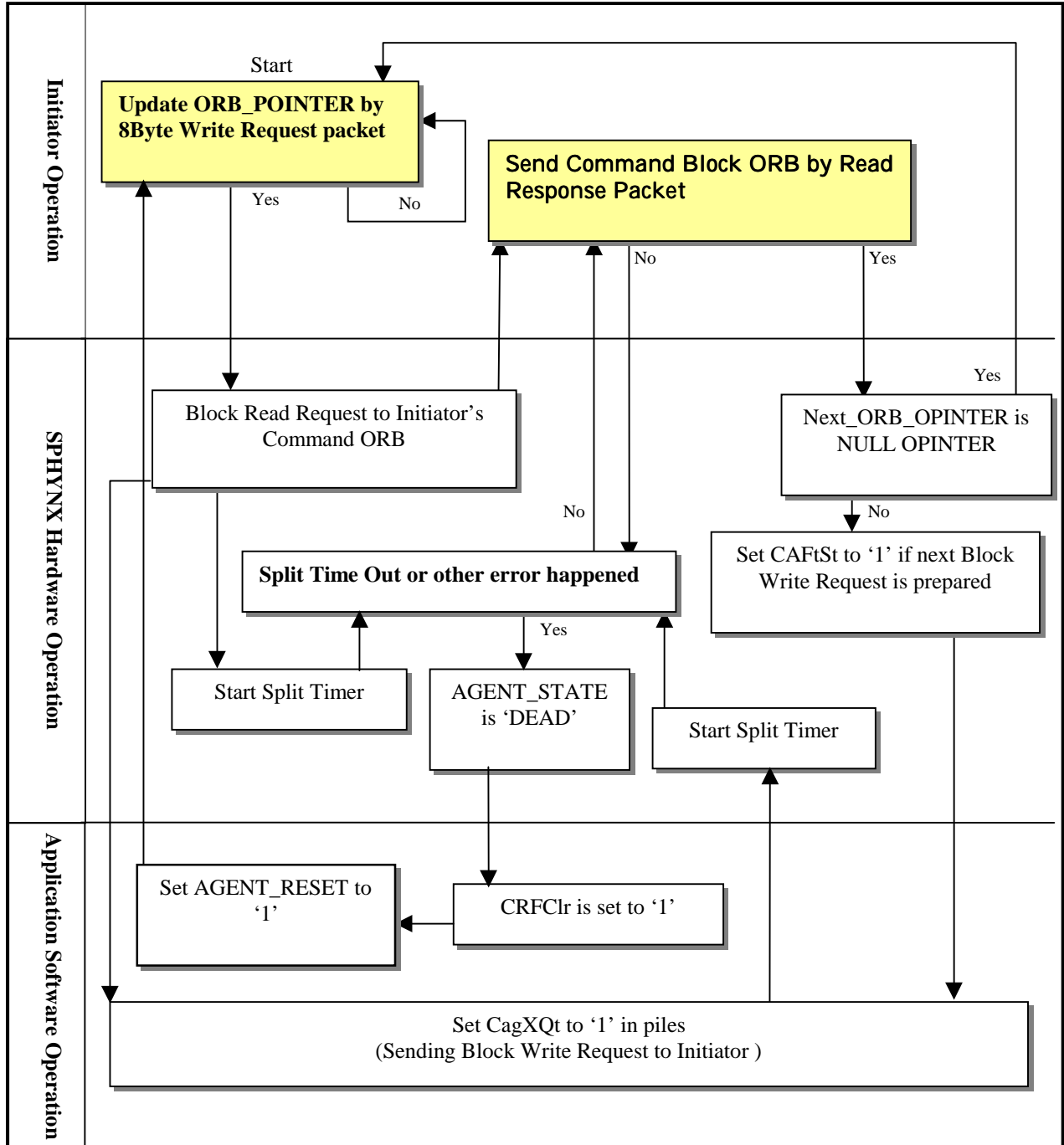
**7.1. Typical ORB Management ORB Fetch Command Operation**

**Typical Management ORB Fetch Command Operation**



7.2. Typical Command ORB Fetch Command Operation

Typical Command ORB Fetch Command Operation



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**8. Ack and Response Packet for Request Packet**

**8.1. Management Agent**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1	
Write	except 8 byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)	
	8byte block write	MRFFULL = 1 MagtBsy = 1	resp_conflict_error	ack_pending (auto resp by confl error)	ack_pending (stored in ARF)
		MRFFULL = 1 MagtBsy = 0	busy_ack	ack_pending (auto resp by confl error)	ack_pending (stored in ARF)
		MRFFULL = 0 MagtBsy = 1	resp_conflict_error	ack_pending (auto resp by confl error)	ack_pending (stored in ARF)
		MRFFULL = 0 MagtBsy = 0	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
Read	except 8 byte	ack_type_error	ack_pending	ack_pending (stored in ARF)	
	subsystem is in use	busy_ack	<-	<-	
	8 byte block read	ack_pending (auto response)	<-	<-	
Other		ack_type_error	Ack_pending (auto resp by type error)	ack_pending (stored in ARF)	

Note) This table is only valid when MagtVld is set.

**8.2. Command Agent AGENT\_STATE**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	any	ack_type_error	ack_pending (auto resp by type error)	ack_pending(stored in ARF)
Read	except 4byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending(stored in ARF)
	Subsystem is in use	busy_ack	<-	<-
	quad read	ack_pending (auto response)	<-	<-
	4byte block read	ack_pending (auto response)	<-	<-
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending(stored in ARF)

Note) This table is only valid when CagtVld is set.

Note) ErrResp is CFR 0x08 , bit14

StErPkt is CFR 0x08 , bit15



**8.3. Command Agent AGENT\_RESET**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	except 4 byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
	quad write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
	4 byte block write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
Read	any	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)

Note) This table is only valid when CagtVld is set.

**8.4. Command Agent ORB pointer**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	except 8 byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
	Active 8byte block write	ack_conflict_error	ack_pending (auto resp by conflict error)	ack_pending (stored in ARF)
	8 byte block write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
Read	except 8byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
	subsystem is in busy 8byte block read	ack_busy/	<-	<-
	8byte Block read	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)

Note) This table is only valid when CagtVld is set.



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**8.5. Command Agent DOOR\_BELL**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	except 4 byte	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
	system in busy (Ackpnd)	ack_complete	<-	<-
		ack_busy	<-	<-
	quad write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
4 byte block write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-	
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)

Note) This table is only valid when CagtVld is set.

**8.6. Command Agent UNSOLISITED\_STATUS\_ENABLE**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	other	Ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
	system in busy (Ackpnd)	ack_complete	<-	<-
		ack_busy	<-	<-
	quad write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-
4 byte block write	ack_complete/ ack_pending (depended on cfr setting. Responed by response Packetl later.)	<-	<-	
Read		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)

Note) This table is only valid when CagtVld is set.



**8.7. Command Agent reserved area**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	except 4 byte	ARF	<-	<-
	ARF is full	busy_ack	<-	<-
	quad write	ARF	<-	<-
	4 byte block write	ARF	<-	<-
Read	except 4 byte	ARF	<-	<-
	ARF is full	busy_ack	<-	<-
	quad read	ARF	<-	<-
	4 byte block read	ARF	<-	<-
Other		ARF	<-	<-

Note) This table is only valid when CagtVld is set.

**8.8. RAM ROM (Destination Address : from ( FFFF\_F000\_0400 to (FFFF\_F000\_0400 + AR\_ConfigRom\_Size))**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	any	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
Read	subsystem is busy	busy_ack	<-	<-
	quad read	ack_pending (auto response)	<-	<-
	block read	ack_pending (auto response)	<-	<-
Other		ack_type_error	ack_pending (stored in ARF) (auto resp by type error)	ack_pending (stored in ARF)



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**8.9. ARF ROM (Destination Address : from (FFFF\_F000\_0400 + AR\_ConfigRom\_Size) to (FFFF\_F000\_0400 + ConfigRom\_Size)**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	any	ack_type_error	ack_pending(stored in ARF)	ack_pending(stored in ARF)
Read	ready & subsystem is busy	ack_pending(stored in ARF)	<-	<-
	quad read	ack_pending(stored in ARF)	<-	<-
	block read	ack_pending(stored in ARF)		
Other		ack_type_error	ack_pending(stored in ARF)	ack_pending(stored in ARF)

**8.10. Out side of ROM configure (Destination Address : from FFFF\_F0000\_0400 + ConfigRom\_Size) to FFFF\_F000\_0800))**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	any	ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)
Read	ready & subsystem is busy	ack_address_error	busy_ack	<-
	quad read/ block read	ack_address_error	ack_pending (auto resp by address error)	ack_pending (stored in ARF)
Other		ack_type_error	ack_pending (auto resp by type error)	ack_pending (stored in ARF)

**8.11. Others**

		ErrResp/StErPkt=0/0	ErrResp/StErPkt =1/0	ErrResp/StErPkt =x/1
Write	any	ack_complete (stored in ARF)	<-	<-
Read	any	ack_pending (stored in ARF)	<-	<-
Other	any	ack_pending (stored in ARF)	<-	<-



**9. DMA Interface**

**9.1. mode setting**

BDOMode and BDIMode register setting on CFR will determine DMA interface transaction mode.

MODE	BDI MODE	BDO MODE	TRANSACTION	INPUT CONTROL	OUTPUT CONTROL
A	0 0 0	0 0	8 bit parallel input/ parallel output	BDIEN Synchronism	BDOEN Synchronism
B	0 0 1	0 1	8 bit parallel input/ parallel output	BDIEN Asynchronism	BDOEN Asynchronism
C	0 1 0	0 1	8 bit bi-directional inout	BDIEN Asynchronism	BDOEN Asynchronism
D	0 1 1	1 0	8 bit bi-directional inout	BDIEN & BDOEN Synchronism	BDIEN & /BDOEN Synchronism
E	1 0 0	1 1	8 bit bi-directional inout	BDIEN & BDOEN Asynchronism	BDIEN & /BDOEN Asynchronism
F	1 0 1	0 1	16 bit bi-directional inout	BDIEN Asynchronism	BDOEN Asynchronism
G	1 1 0	1 0	16 bit bi-directional inout	BDIEN & BDOEN Synchronism	BDIEN & /BDOEN Synchronism
H	1 1 1	1 1	16 bit bi-directional inout	BDIEN & BDOEN Asynchronism	BDIEN & /BDOEN Asynchronism

**Figure 9-1. DMA mode setting**

Below data is for 8 bit bus DMA interface.

MSB		LSB					
7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B
D	D	D	D	D	D	D	D
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0

**Figure 9-2 BDIO (8bit)**

MSB		LSB					
7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B
D	D	D	D	D	D	D	D
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
1	1	1	1	1	1	9	8
5	4	3	2	1	0		

**Figure 9-3. BDO (8bit)**

For 16-bit bus DMA interface, combine BDIO and BDO to make 16-bit signal as below.



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MSB					LSB										
1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	
5	4	3	2	1	0										
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
5	4	3	2	1	0										

Figure 9-4. BDIO (16bit)

### Mode A

Input: BDIO

Output: BDO

Use BDIO for 8-bit request data input. Use BDO for 8-bit response data output.

Data will be input synchronously with BDICLK and will be written when BDIEN is true and BDIBUSY is false.

Data will be output synchronously with BDICLK and will be updated when BDOEN is true and BDOAVAIL is false.

### Mode B

Input: BDIO

Output: BDO

Use BDIO for 8-bit request data input. BDO is used for 8-bit response data output.

Data will be written asynchronously by BDIEN input.

Data output will be updated asynchronously by BDOEN input. When BDOEN is false BDO will be high impedance.

### Mode C

Input: BDIO

Output: BDIO

Use BDIO for 8-bit data input/output.

Data will be output synchronously with BDICLK by BDIEN input, and will be updated when both BDOEN and BDOAVAIL are true.

### Mode D

Input: BDIO

Output: BDIO

Use BDIO for 8-bit data input/output.

Specify data input/output with BDOEN. If BDOEN is true the mode is input, if it is false the mode is output.

Data will be input synchronously with BDICLK, and will be written when BDIEN is true and BDIBUSY is false. Data will be output synchronously with BDICLK, and will be updated when both BDIEN and



BDOAVAIL are true.

#### Mode E

Input: BDIO

Output: BDIO

Use BDIO for 8bit data input/output.

Specify data input/output with BDOEN. If BDOEN is true, the mode is input. If it's false, the mode is output.

Data will be written asynchronously with BDIEN input.

Data output will be updated asynchronously with BDOEN input. When BDOEN is false, BDO is high impedance.

#### Mode F

Input: BDIO, BDO

Output: BDIO, BDO

Use BDIO and BDO combined for 16-bit data input/output.

Data will be written asynchronously with BDIEN input.

Data output will be updated asynchronously with BDOEN input.

#### Mode G

Input: BDIO, BDO

Output: BDIO, BDO

Use BDIO and BDO combined for 16-bit data input/output.

BDOEN controls data input or output. When BDOEN is true, it is input mode. When it is false, it is output mode.

Data will be input synchronously with BDICLK, and updated when BDIEN is true and BDIBUSY is false.

Data will be output synchronously with BDICLK, and updated when both BDOEN and BDOAVAIL are true.

#### Mode H

Input: BDIO, BDO

Output: BDIO, BDO

Use BDIO and BDO combined for 16-bit data input/output.

BDOEN controls data input or output. When BDOEN is true, it is input mode. When it is false, it is output mode.

Data input will be written asynchronously with BDIEN input.

Data output will be updated asynchronously with BDOEN input.

#### Setting active signal

Polarity of BDIBUSY, BDOAVAIL, BDOFEN and BDIFEN is determined by BIBsyCtl, BOAvCtl, BOEnCtl and BIEnCtl register (0x90,bit12, 13,14,15) respectively. For each register 1 means active high, and 0 means active low.

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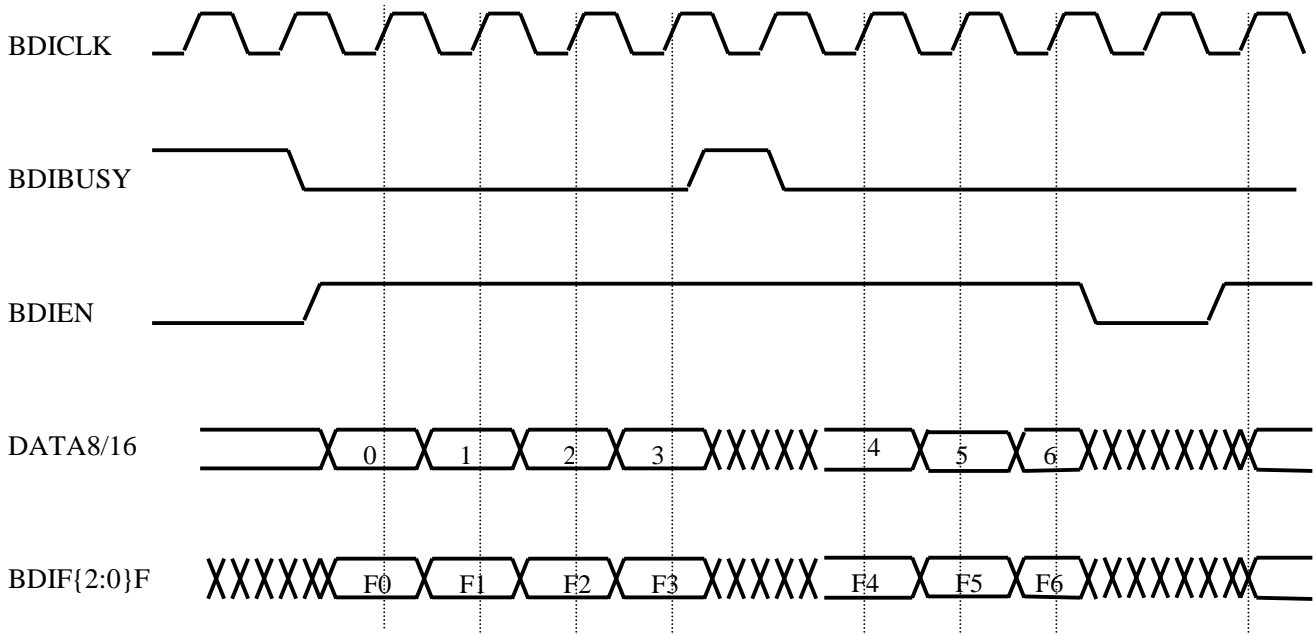
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### 9.2. Request transmission

#### 9.2.1. Synchronous mode

In this mode, data will be written synchronously with BDICLK input.



Data will be written when BDIBUSY is false and BDIEN is true.  
 BDIF2~0 is an attribute flag for a packet, and each means:

#### 8-bit Bulky

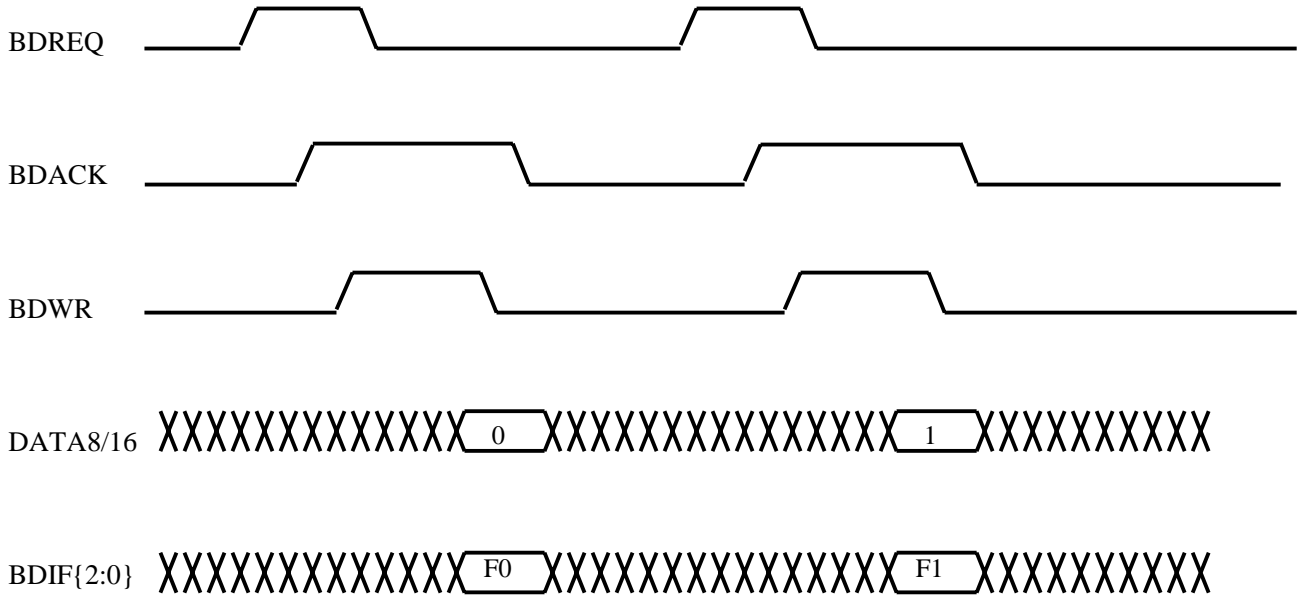
BDIF[2:0]	Comment
011	8-bit data except last block on packet
111	8-bit data of last on packet
101	Reset
001	No data

#### 16-bit Bulky

BDIF[2:0]	Comment
011	8-bit data except last block on packet (Upper)
000	8-bit data except last block on packet (Lower)
010	16-bit data except last block on packet
111	8-bit data of last on packet (Upper)
100	8-bit data of last on packet (Lower)
110	16-bit data of last block on packet
101	Reset
001	No data



9.2.2. Asynchronous SCSI mode



The data needs to be guaranteed by BDWR negated edge. Also, BDACK needs to be asserted after confirming BDREQ input is false.

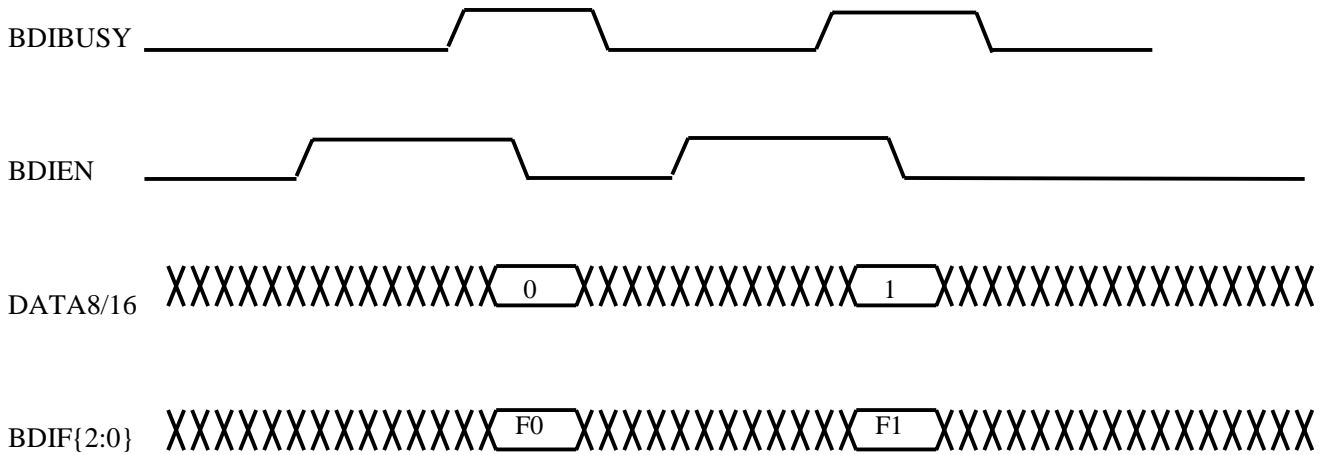
16 bit bus data write can not bestride over 32-bit boundary.

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### 9.2.3. Asynchronous handshake mode



The data needs to be guaranteed by BDIEN negedge. Also, BDIEN needs to be asserted after confirming BDIBUSY input is false.

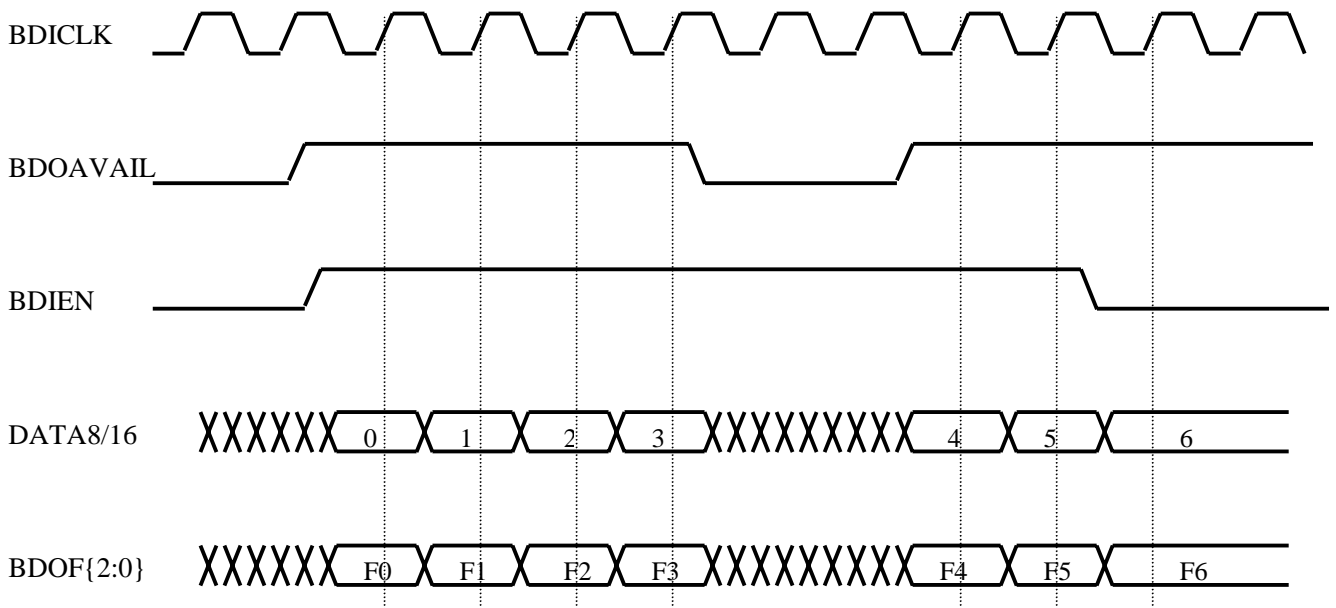
16 bit bus data write can not bestride over 32-bit boundary.



**9.3. Receiving**

9.3.1. Synchronous mode

In this mode, data receipt will be recognized synchronously with BDICLK input, when both BDOEN and BDOAVAIL are true.



It takes maximum a little over 100 ns per 1QW.  
 For faster DMA port frequency, wait cycles needs to be added to every 1QW.

Frequency	wait for 16 bit bus / wait for 8 bit bus	
40MHz	3wait	1wait
36MHz	2wait	no wait
33MHz	2wait	no wait
25MHz	1wait	no wait
18MHz	no wait	no wait

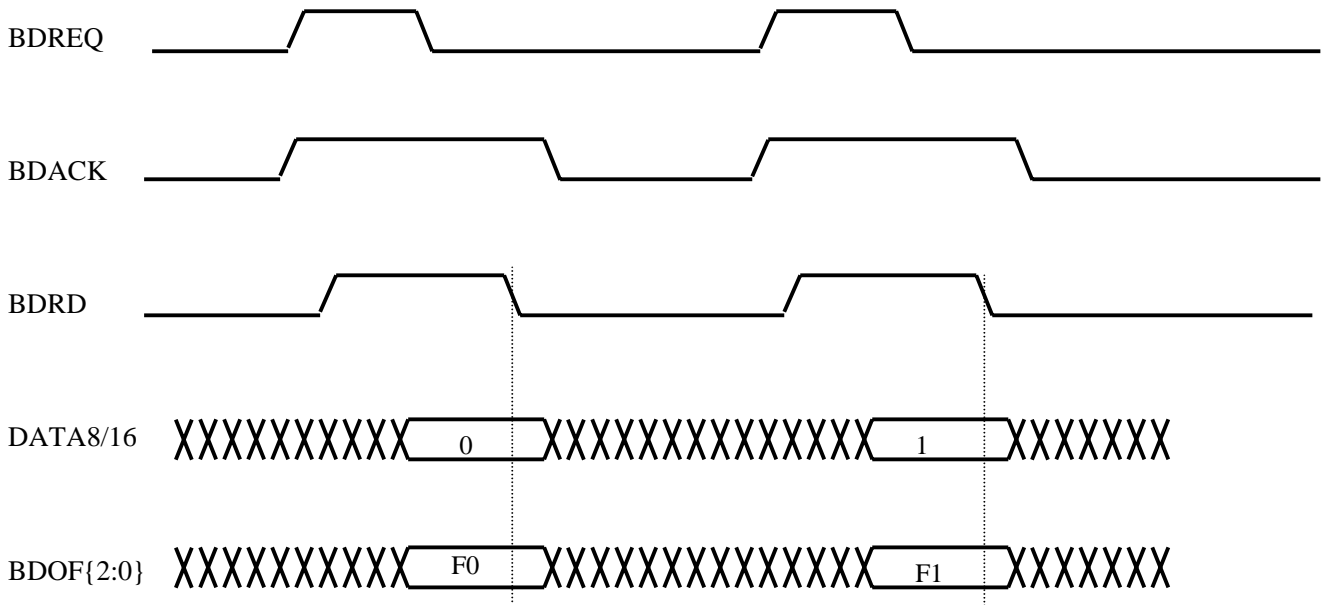
Specify number of waits to be added (0~3) with BDODelay on CFR.



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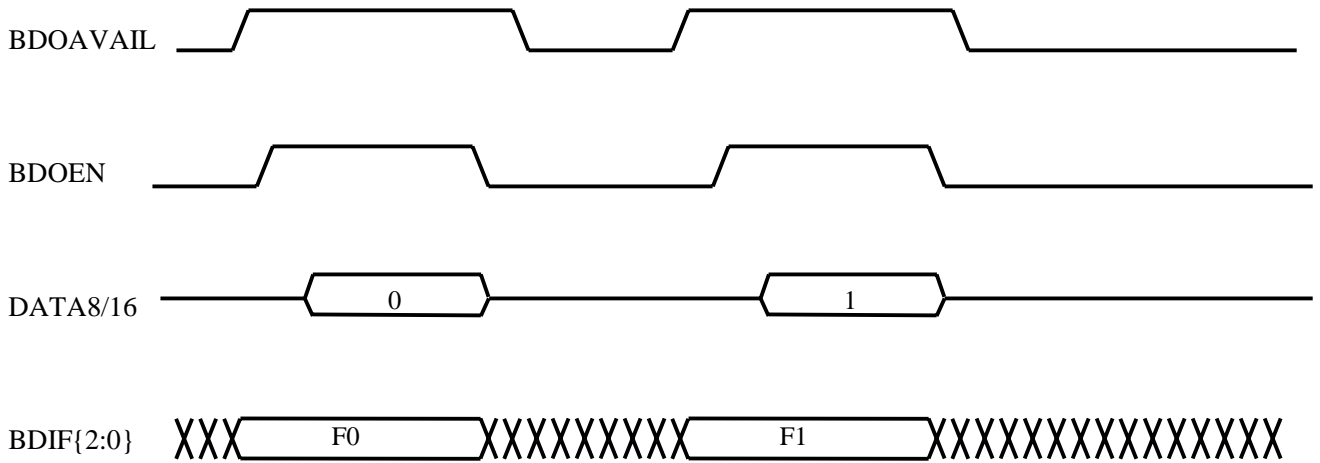
---

9.3.2. Asynchronous SCSI mode



In this mode, data will be output as BDRD negedge.  
 Specify number of waits to be added 0 with BDODelay on CFR.

9.3.3. Asynchronous handshake mode



The data should be output by repeating BDOEN negate and assert. Also, BDOEN needs to be asserted after confirming BDOAVAIL input is true.

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### 9.4. Endianness

When BLtCtl (0x94,bit11) is 1, data from DMA interface will be received in Little Endian mode. The difference between Little Endian and Big Endian are described below.

The example is for outputting below 1394 quadlet data packets.

D0	D1	D2	D3
----	----	----	----

Data are to be output in below order. And, for 1, 2 and 3 byte data, every padded data will be deleted before output.

8 bit mode

#### Big Endian Byte Ordering

4 byte data	D0⇒D1⇒D2⇒D3	
3 byte data	D0⇒D1⇒D2	D3 is Padding data
2 byte data	D0⇒D1	D2 & D3 are Padding data
1 byte data	D0	D1, D2 & D3 are Padding data

#### Little Endian Byte Ordering

4 byte data	D3⇒D2⇒D1⇒D0	
3 byte data	D2⇒D1⇒D0	D3 is Padding data
2 byte data	D1⇒D0	D2 & D3 are Padding data
1 byte data	D0	D1, D2 & D3 are Padding data

16 bit mode

#### Big Endian Byte Ordering

4 byte data	{D0,D1}⇒{D2,D3}	
3 byte data	{D0,D1}⇒{D2,0x00}	D3 is Padding data
2 byte data	{D0,D1}	D2 & D3 are Padding data
1 byte data	{D0,0x00}	D1, D2 & D3 are Padding data

#### Little Endian Byte Ordering

4 byte data	{D3,D2}⇒{D1,D0}	
3 byte data	{D2,D1}⇒{0x00,D0}	D3 is Padding data
2 byte data	{D1,D0}	D2 & D3 are Padding data
1 byte data	{0x00,D0}	D1, D2 & D3 are Padding data



### 9.5. Reference clock

DMA interface can use either internal clock or external clock as a reference clock.

When CLKSEL terminal is 0, it uses an external clock that is input through BDICLK pin.

When CLKSEL terminal is 1, it uses internal 24.976MHz clock.

Internal clock will be output through NCLK terminal by setting CLKOE signal to 0. When CLKOE signal is 1, NCLK terminal will be kept as high impedance.

### 9.6. Clearing DMA interface data

To clear DMA interface data, write 1 on DTFClr (0x90, bit31) and DRFClr (0x90, bit30).

It takes 2~3BDIClk for the data to be cleared after the micro controller writes the order.

### 9.7. Resetting DMA interface

To reset DMA interface, write 1 on BDORst (0x94, bit29) and BDIRst (0x94, bit30).

It takes 2~3BDIClk for the interface to be reset after the micro controller writes the order.

### 9.8. Suspending BDO output

To suspend BDO output, set 1 on BDOTris (0x94, bit31).

Under 8-bit synchronous mode, BDO is in Output State.

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### 10. Electrical Characteristics

#### 10.1. Absolute Maximum Ratings Over Free-Air Temperature Range

Supply voltage range, $V_{CC}$ (5-V tolerant TTL terminals)	-0.5V to 5.5V
Input voltage range, $V_I$ (5-V tolerant TTL terminals)	-0.5V to $V_{CC} + 0.5V$
Output voltage range, $V_O$ (TTL terminals)	-0.5V to $V_{CC} + 0.5V$ (4.6V maximum)
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 2)	$\pm 20$ mA
Operating free-air temperature range, $T_A$	0 to 70
Storage temperature range, $T_{STG}$	-65 to 150

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE:

1. This parameter applies to external input and bidirectional buffers without hysteresis.  $V_I > V_{CC}$  does not apply to fail-safe terminals. For 5-V tolerant and universal PCI use  $V_O > V_{CC} 5V$ .
2. This parameter applies to external input and bidirectional buffers without hysteresis.  $V_O > V_{CC}$  does not apply to fail-safe terminals. For 5-V tolerant and universal PCI use  $V_O > V_{CC} 5V$ .

#### 10.2. Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		3	3.3	3.6	V
Supply voltage, $V_{dd5V}$ (5V)		4.5	5	5.5	V
Output voltage, $V_O$	LVC MOS terminals	0		$V_{CC}$	V
High-level input voltage, $V_{IH}$	LVC MOS terminals	$0.7V_{CC}$		$V_{CC}$ ( $V_{dd5V}$ )	V
Low-level input voltage, $V_{IL}$	LVC MOS terminals	0		$0.2V_{CC}$	V
Clock frequency	BCLK			40	MHz
	SCLK			50	
Operating free-air temperature, $T_A$		0		70	
Virtual junction temperature range, $T_J$		0		115	
Differential input voltage, $V_{ID}$	Cable inputs, during data reception	118		260	mV
	Cable inputs, during arbitration	168		265	
Common-mode input voltage, $V_{IC}$	TPB cable inputs, Source power node	0.4706		2.515	V
	TPB cable inputs, Non-source power node	0.4706		$2.015^\dagger$	
Power-up reset time, $t_{pu}$	/RESET input	2			msec
Receive input jitter	TPA, TPB cable inputs, S100 operation			$\pm 1.08$	nsec
	TPA, TPB cable inputs, S200 operation			$\pm 0.5$	
	TPA, TPB cable inputs, S400 operation			$\pm 0.315$	



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Receive input skew	Between TPA and TPB cable inputs, S100 operation	±0.8	nsec
	Between TPA and TPB cable inputs, S200 operation	±0.55	
	Between TPA and TPB cable inputs, S400 operation	±0.5	

**10.3. electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)**

10.3.1. driver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Differential output voltage	56 Ω, See Figure 1	172		265	mV
I <sub>DIFF</sub>	Driver Difference current, TPA+, TPA-, TPB+, TPB-	Drivers enabled, speed signaling off	-1.05*		1.05*	mA
I <sub>SP</sub>	Common mode speed signaling current, TPB+, TPB-	S200 speed signaling enabled	-4.84▼		-2.53▼	mA
I <sub>SP</sub>	Common mode speed signaling current, TPB+, TPB-	S400 speed signaling enabled	-12.4▼		-8.10▼	mA
V <sub>OFF</sub>	Off state differential voltage	Drivers disabled, See Figure 1			20	mV

\* Limits defined as algebraic sum of TPA+ and TPA- driver currents. Limits also apply to TPB+ and TPB- algebraic sum of driver currents.

▼ Limits defined as absolute limit of each of TPB+ and TPB- driver currents.

10.3.2. receiver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Z <sub>ID</sub>	Differential impedance	Drivers disabled	10	14		kΩ
					4	pF
Z <sub>IC</sub>	Common mode impedance	Drivers disabled	20			kΩ
					24	pF
V <sub>TH-R</sub>	Receiver input threshold voltage	Drivers disabled	-30		30	mV
V <sub>TH-CB</sub>	Cable bias detect threshold, TPB cable inputs	Drivers disabled	0.6		1.0	V
V <sub>TH+</sub>	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V <sub>TH-</sub>	Negative arbitration comparator threshold voltage	Drivers disabled	-168		-89	mV



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$V_{TH-SP200}$	Speed signal threshold	TPBIAS-TPA common mode voltage, drivers disabled	49	131	mV
$V_{TH-SP400}$	Speed signal threshold	TPBIAS-TPA common mode voltage, drivers disabled	314	396	mV

### 10.3.3. device

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_O$	TPBIAS output voltage		1.665		2.015	V

### 10.3.4. switching characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Jitter, transmit	Between TPA and TPB			$\pm 0.15$	ns
	Skew, transmit	Between TPA and TPB			$\pm 0.10$	ns
$t_r$	TP differential rise time, transmit	10% to 90%, At 1394 connector	0.5		1.2	ns
$t_f$	TP differential fall time, transmit	90% to 10%, At 1394 connector	0.5		1.2	ns
$t_{su}$	Setup time, CTL0, CTL1, D0-D7, LREQ to SYSCLK	50% to 50%, At 1394 connector	5			ns
$t_h$	Hold time, CTL0, CTL1, D0-D7, LREQ after SYSCLK	50% to 50%, At 1394 connector	TBD			ns
$t_d$	Delay time, SYSCLK to CTL0, CTL1, D0-D7	50% to 50%, At 1394 connector	2		11	ns



**10.4. Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub> High-level output voltage		I <sub>OH</sub> = -8mA ‡	V <sub>CC</sub> - 0.6			V
		I <sub>OH</sub> = -4mA §	V <sub>CC</sub> - 0.6			
V <sub>OL</sub> Low-level output voltage		I <sub>OL</sub> = 8 mA ‡	0.4			V
		I <sub>OL</sub> = 4 mA §	0.4			
I <sub>IL</sub> Low-level input current		V <sub>I</sub> = GND	± 1			µ A
" ¢		V <sub>I</sub> = GND				µ A
" £		V <sub>I</sub> = GND				µ A
" ®		V <sub>I</sub> = GND				µ A
I <sub>IH</sub> High-level input current		V <sub>I</sub> = V <sub>CC</sub>	± 1			µ A
" ¢		V <sub>I</sub> = V <sub>CC</sub>				µ A
" £		V <sub>I</sub> = V <sub>CC</sub>				µ A
" ®		V <sub>I</sub> = V <sub>CC</sub>				µ A
I <sub>OZ</sub> High-impedance-state output current		V <sub>I</sub> = V <sub>CC</sub> or GND	± 20			µ A
V <sub>IT+</sub> positive-going threshold voltage		TTL compatible	1.8			V
V <sub>IT-</sub> Negative-going threshold voltage		TTL compatible	0.8			V
V <sub>hys</sub> Hysteresis (V <sub>it+</sub> - V <sub>it-</sub> ) ©		TTL compatible	0.30		0.70	V
I <sub>CC</sub> Supply current		TTL compatible	150			mA
C <sub>i</sub> Input capacitance	Input terminals	V <sub>CC</sub> = 3.3V, T <sub>A</sub> = 25	5			pF
	Bidirectional terminal		13			
C <sub>o</sub> Output capacitance				8		

- † All typical values are at V<sub>CC</sub> = 3.3V and T<sub>A</sub> = 25C
- ‡ Terminals: output terminals of 1-15 and 37-77 pin
- § Terminals: All other outputs
- © Terminals: All pins except 1-15, 109-111, 143.
- ¢ with Bus holder
- £ with pull up
- ® with pull down



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### 10.5. AC specification for Micro interface

#### 10.5.1. [ DA ]

Title	Item	Min	Max	Unit
tsu_da	Addr/Data setup	5		[ns]
th_data	Addr/Data hold	5		[ns]
ten1_da	Enable after XRD low		15	[ns]
ten2_da	Disable after XRD hi	2	10	[ns]
tdr_da	data read time		210 (260-note1)	[ns]
twr_da	data write time	40	80	[ns]

Note1: access time for DRF use this value

#### 10.5.2. [XRD]

Title	Item	Min	Max	Unit
tsu_xrd	ALE to XRD	40		[ns]
tw_xrd	pulse width	160		[ns]

#### 10.5.3. [ XWR ]

Title	Item	Min	Max	Unit
tsu_xwr	ALE to XWR	40		[ns]
tw_xwr	pulse width	160		[ns]

#### 10.5.4. [ ALE ]

Title	Item	Min	Max	Unit
tw_ale	pulse width	30		[ns]
t_cy	wait after last XRD or XWR	100		[ns]

#### 10.5.5. [ XCS ]

Title	Item	Min	Max	Unit
tsu_xcs	set up	5		[ns]
th_xcs	hold	5		[ns]

#### 10.5.6. [ WAIT ]

Title	Item	Min	Max	Unit
td_wait	delay from XRD	TBD	TBD	[ns]
tw_wait	width	40	TBD	[ns]



**10.6. Phy-Interface Timing Requirements Over Operating Free-Air Temperature Range (See Note1)**

PARAMETER		MIN	MAX	UNIT
T <sub>c2</sub>	Cycle time,SCLK (see Figure X-1)	20.347	20.343	ns
T <sub>w2(H)</sub>	Pulse duration, SCLK high (see Figure X-1)	9		ns
T <sub>w2(L)</sub>	Pulse duration, SCLK low (see Figure X-1)	9		ns
T <sub>su5</sub>	Setup time, D0-D7 valid before SCLK↑ (see Figure X-3)	6		ns
T <sub>h5</sub>	Hold time, D0-D7 invalid after SCLK↑ (see Figure X-3)	1		ns
T <sub>su6</sub>	Setup time, CTL0-CTL1 valid before SCLK↑ (see Figure X-3)	6		ns
T <sub>h6</sub>	Hold time, CTL0-CTL1 invalid after SCLK↑ (see Figure X-3)	1		ns

NOTE1: These parameters are not production tested.

**Phy-Interface Characteristics Over Operating Free-Air Temperature Range, CL=45pF(unless otherwise noted) (See Note1)**

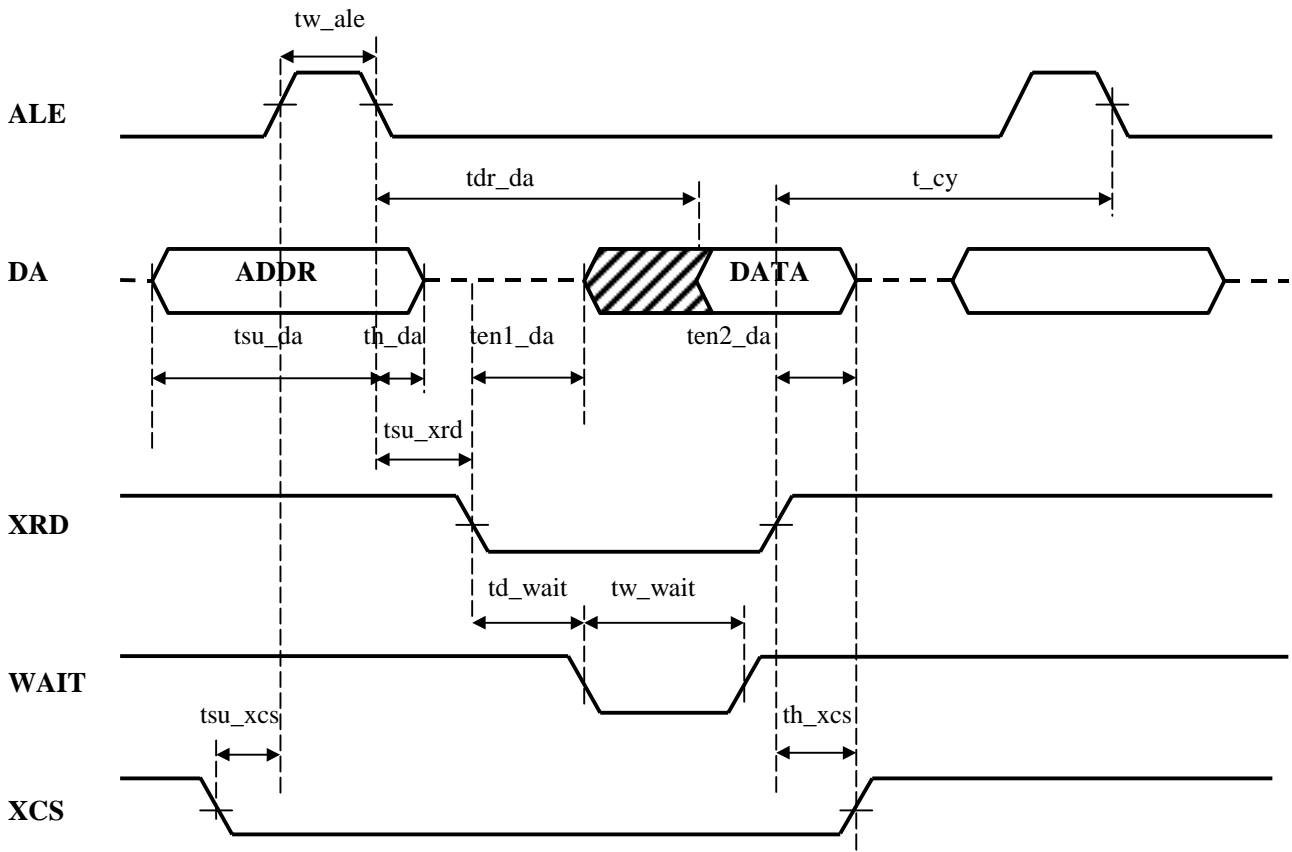
PARAMETER		MIN	MAX	UNIT
T <sub>d5</sub>	Delay time, SCLK↑ to D0-D7 valid	3	11	ns
T <sub>d6</sub>	Delay time, SCLK↑ to D0-D7↑↓	3	11	ns
T <sub>d7</sub>	Delay time, SCLK↑ to D0-D7 invalid	3	11	ns
T <sub>d8</sub>	Delay time, SCLK↑ to CTL0-CTL1 valid	3	11	ns
T <sub>d9</sub>	Delay time, SCLK↑ to CTL0-CTL1↑↓	3	11	ns
T <sub>d10</sub>	Delay time, SCLK↑ to CTL0-CTL1 invalid	3	11	ns
T <sub>d11</sub>	Delay time, SCLK↑ to LREQ↑↓	3	11	ns

NOTE1: These parameters are not production tested.



**11. Parameter Measurement Information**

**11.1. Micro Interface timing diagram**



**Figure 11-1. MUX Mode Read Cycle**

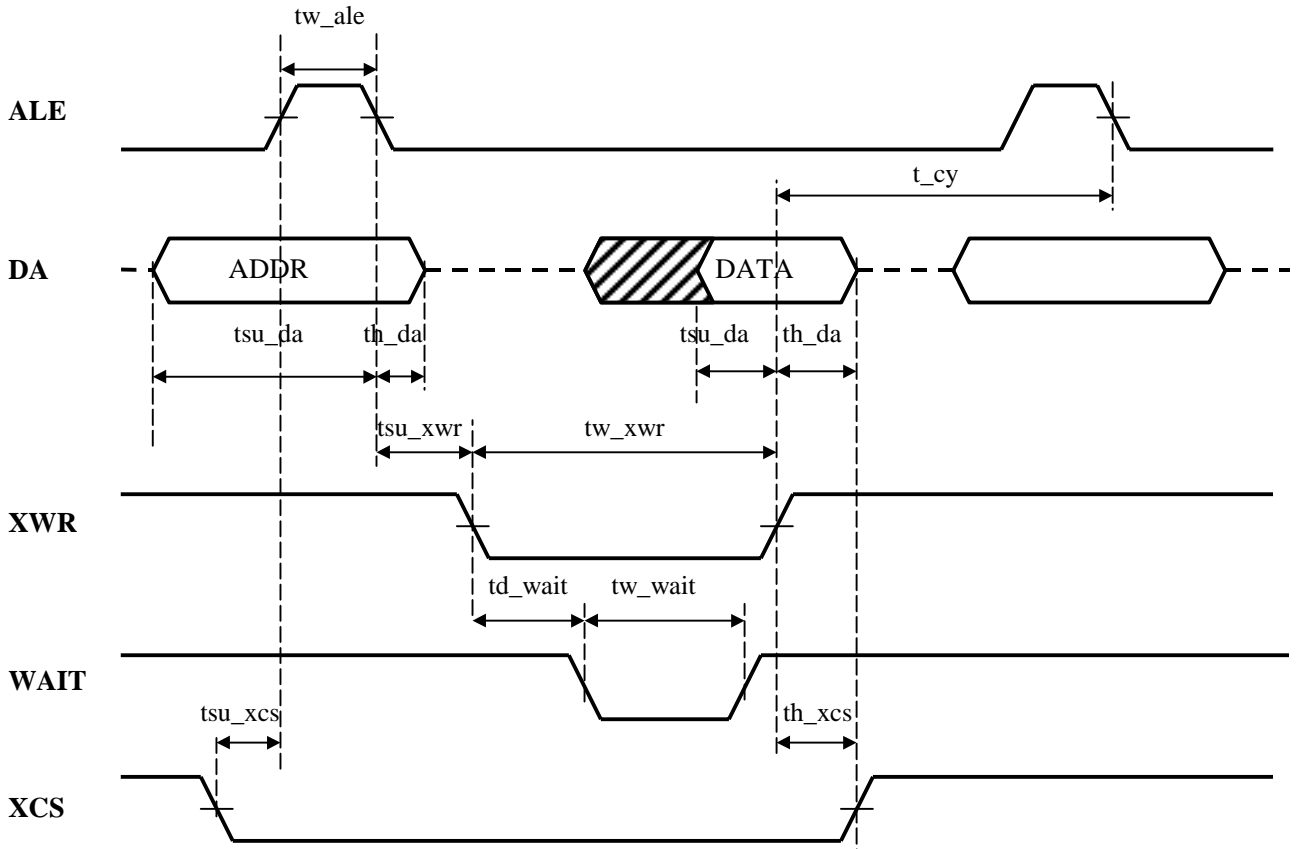


Figure 11-2. MUX Mode Write Cycle

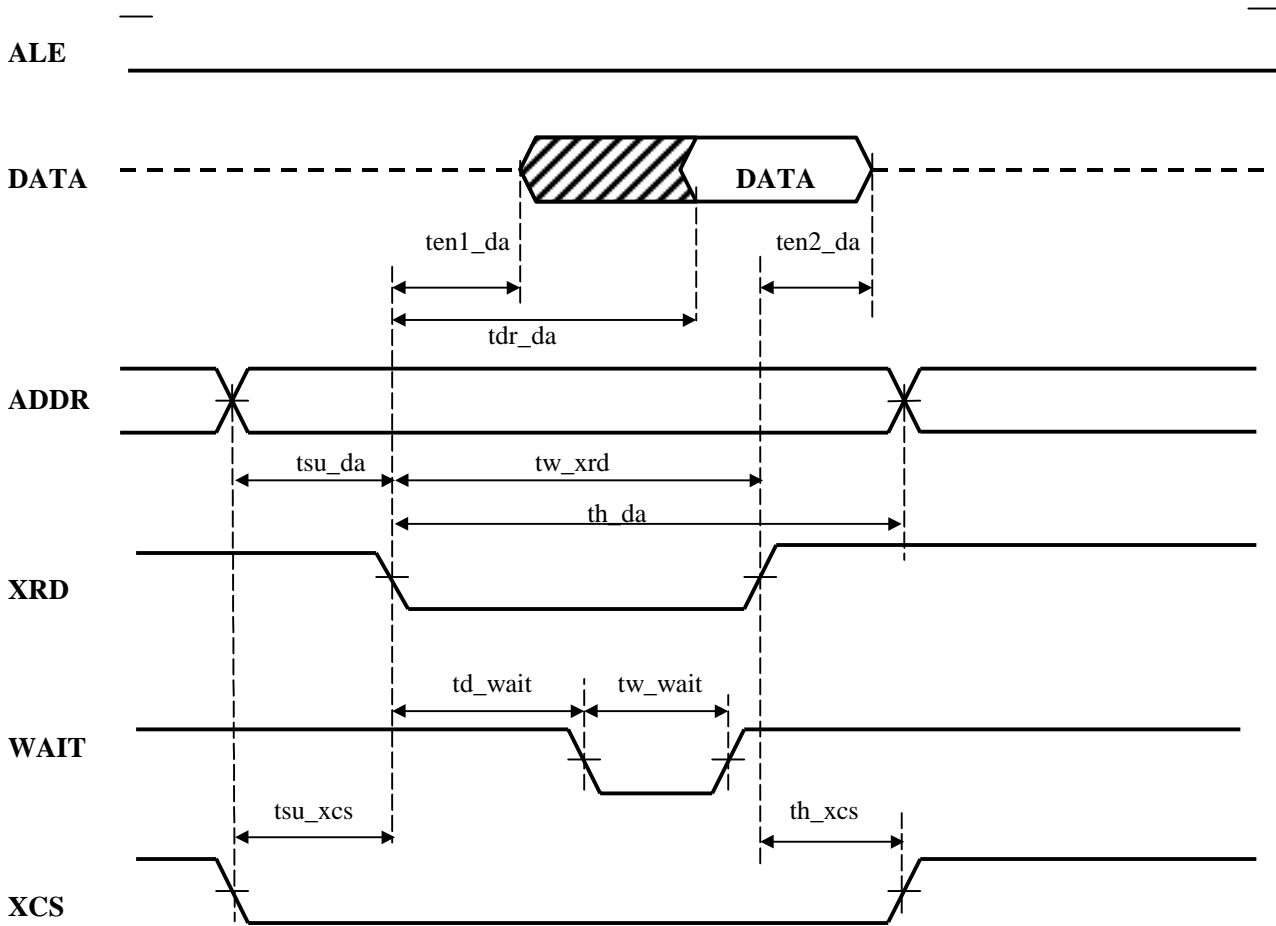
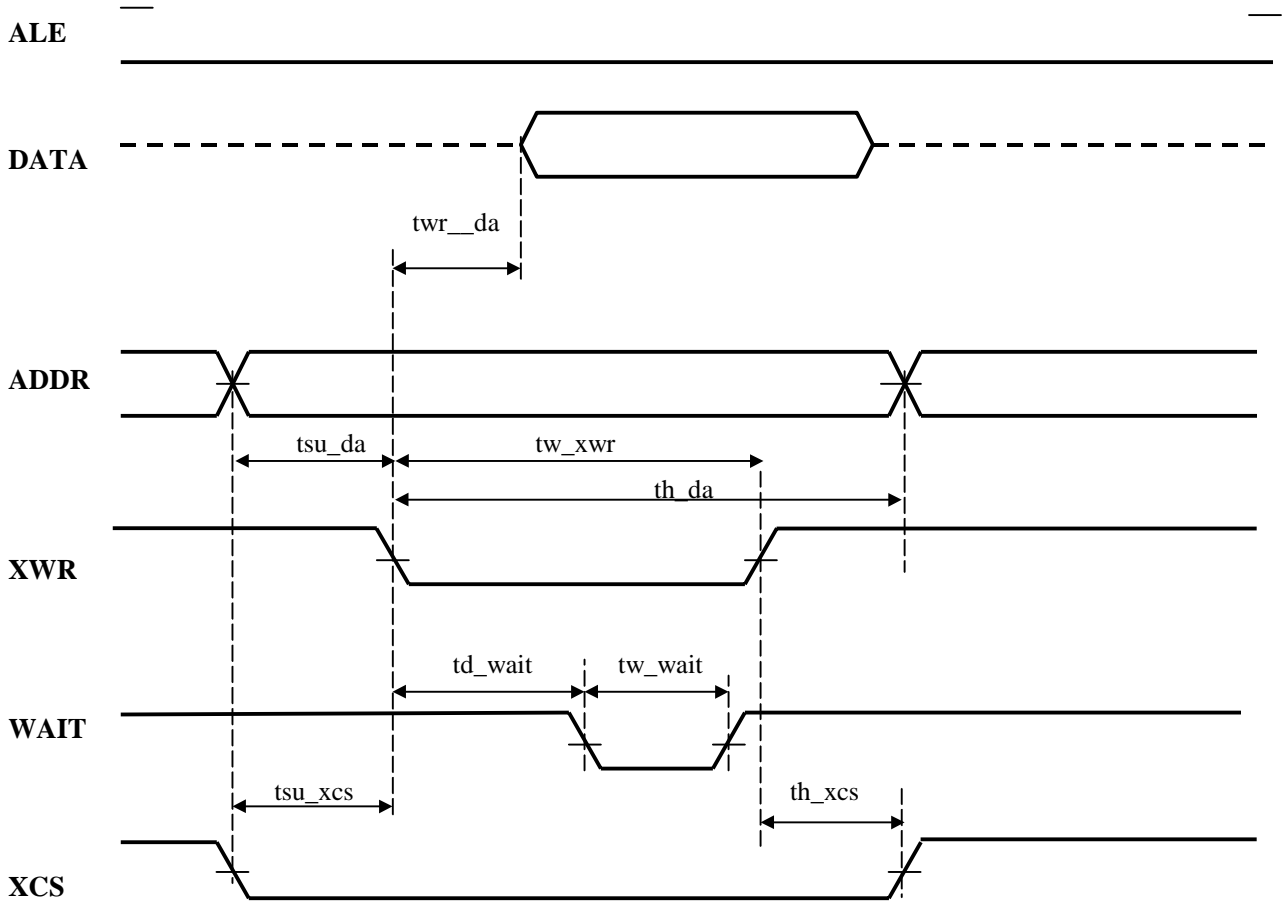


Figure 11-3. PARA Mode Read Cycle



**Figure 11-4. PARA Mode Write Cycle**

NOTE:

M8M16 mode	DATA[7:0]	ADDR[7:0]
8 bit Mode	DA[15:8]	DA[7:0]
16 bit Mode	DA[15:0]	BDIO[15:8] DA[7:0] ( mux mode )

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**11.2. Bulky Interface**

11.2.1. Sync mode

Title	Item	min	max	unit
Tbdoav	BDOAVAIL output delay	2	15	ns
Tbdibsy	BDIBUSY output delay	5	17	ns
Tbd	Data output delay	5	17	ns
TSubdi	BDIFEN/BDOFEN input setup	8		ns
THObdi	BDIFEN/BDOFEN input hold	2		ns
TSubd	Data input setup	8		ns
THObd	Data input hold	2		ns

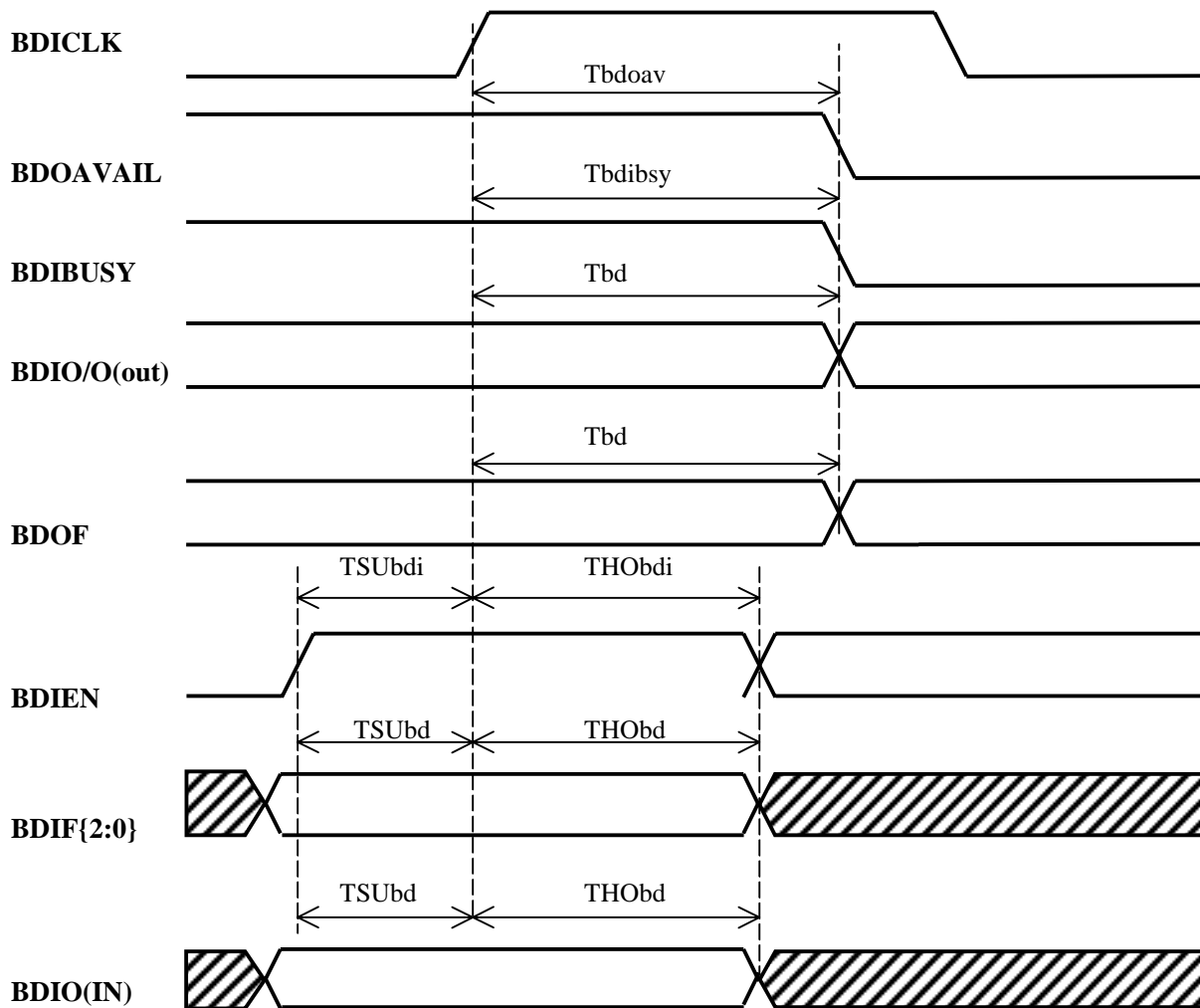


Figure 11-5. Sync Mode



11.2.2. Async mode

Title	Item	min	max	unit
Tabdien on	BDIEN pulse width on	Tcyc		ns
Tabdien off	BDIEN pulse width off	Tcyc		ns
Tcyc	Cycle time	25		ns

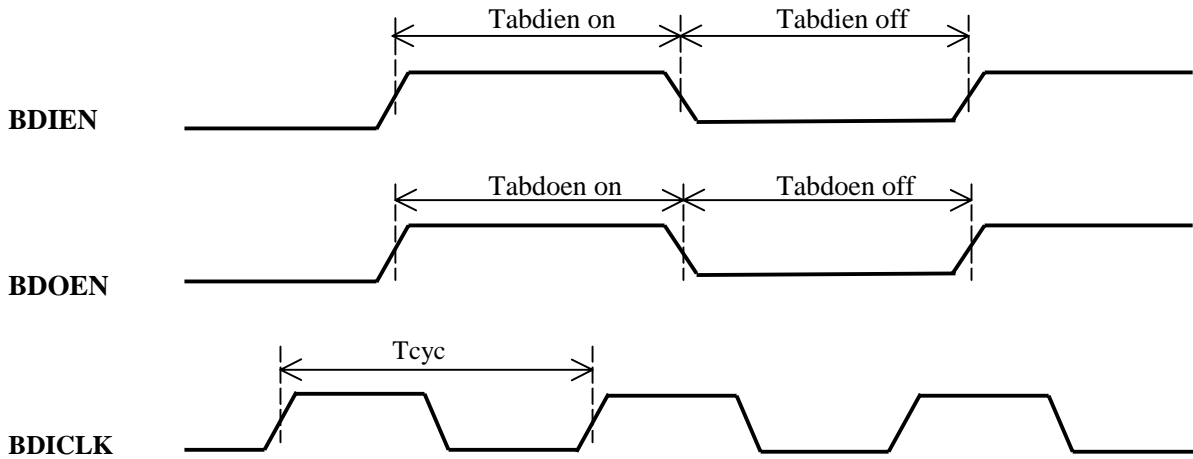


Figure 11-6. Async

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Title	Item	min	max	unit
TSUabd	data input setup	6		ns
THOabd	data input hold	2		ns
Tabdibsy0	BDIBUSY delay 0		11	ns
Tabdibsy1	BDIBUSY delay 1	3		ns
Tabdoav0	BDOAVAIL delay 0		11	ns
Tabdoav1	BDOAVAIL delay 1	3		ns
Tabdoen	BDData output enable	3	11	ns
Tabdodis	BDData output disable	3	11	ns

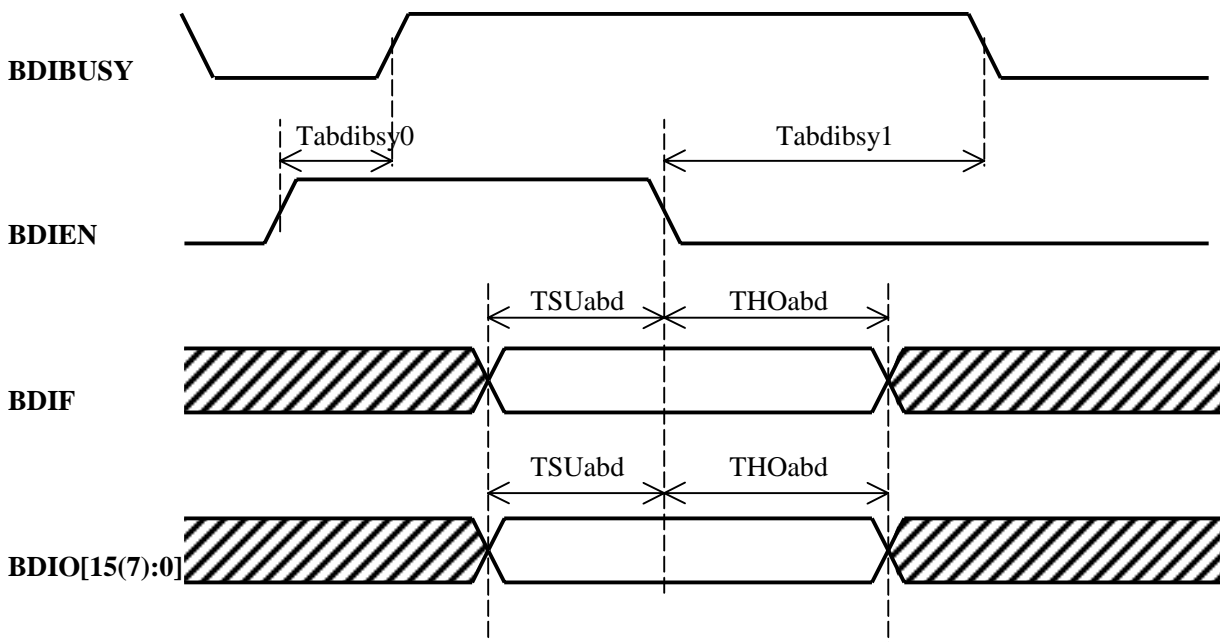


Figure 11-7 . ASYNC Handshake Mode WRITE

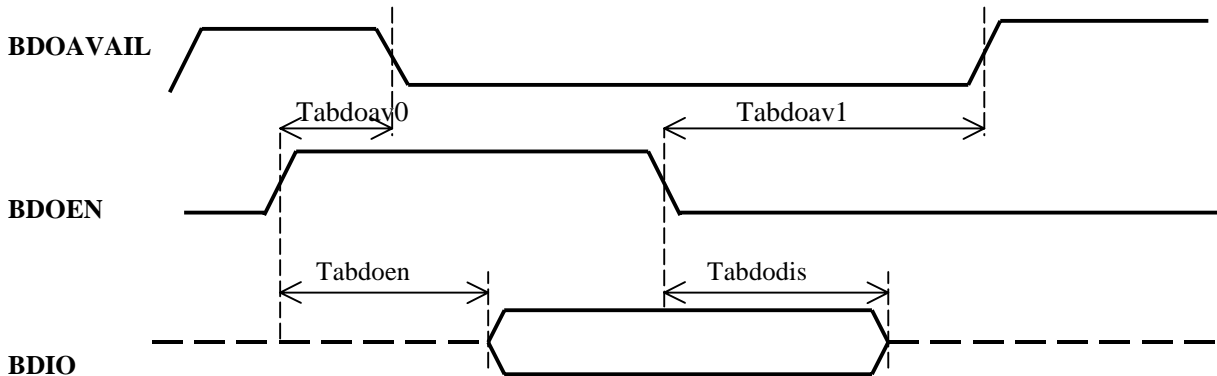


Figure 11-8 . ASYNC Handshake mode READ



Title	Item	min	max	unit
Tbbdibsy	BDIBUSY delay		2T+8	ns
TSUabbd	BDData input setup	6		ns
THOabbd	BDData input hold	2		ns
Tabbdoav	BDOAVAIL		2T+8	ns
Tabbdoen	BDData output enable	3	11	ns
Tabbdodis	BDData output disable	3	11	ns

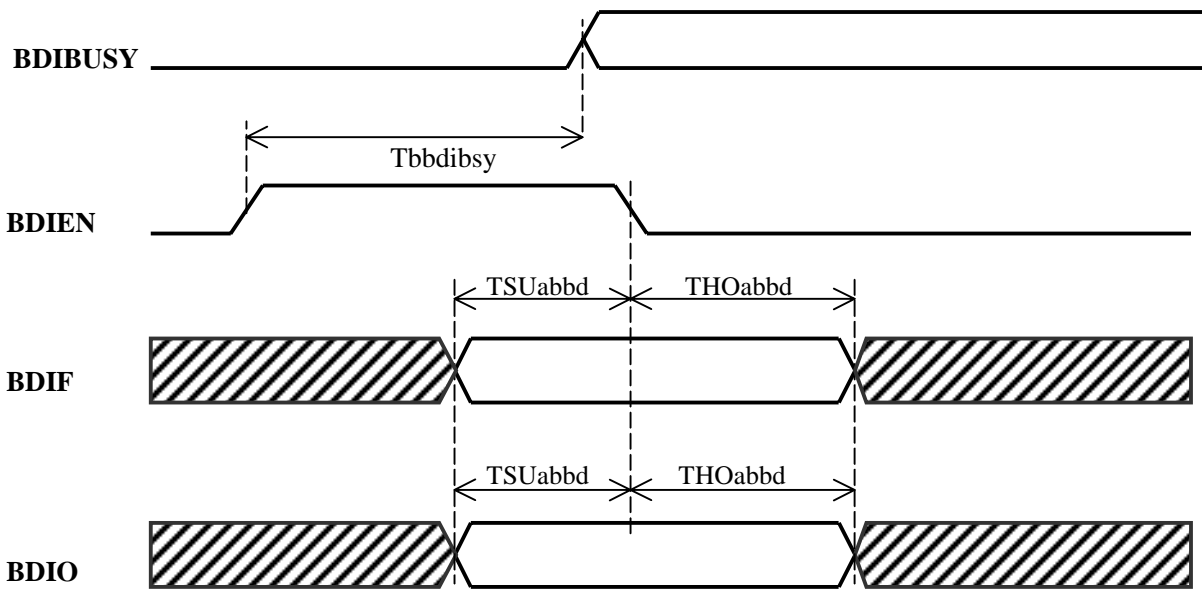


Figure 11-9. ASYNC Burst Mode WRITE

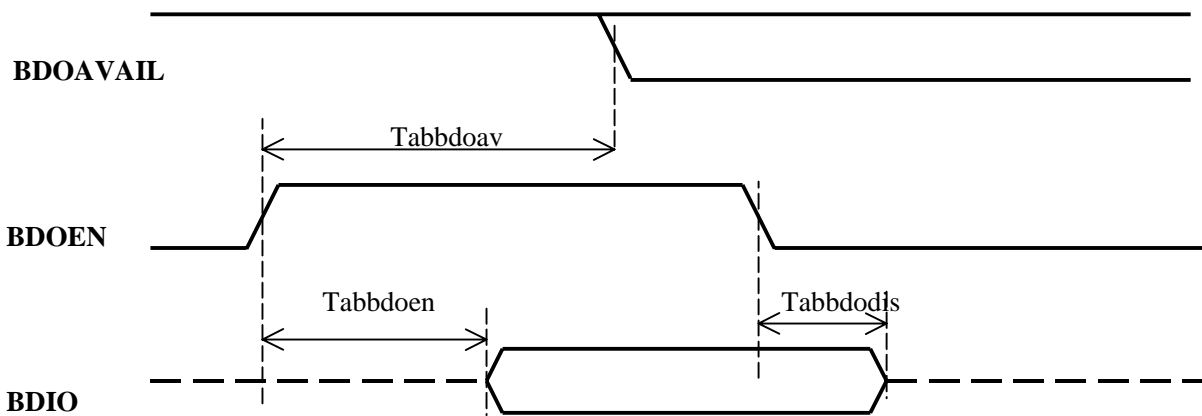


Figure 11-10. Async Burst Mode READ



Title	Item	min	max	unit
Tsbbdreq	BDREQ delay		2T+8 (T: 1BDICLK cycle)	ns
Tsbrw0	BDACK to BRWR/RD	0		ns
Tsbrw1	BRWR/RD to BDACK	0		ns
TSUsbbd	SCSI Data input setup	6		ns
THOsbbd	SCSI Data input hold	2		ns
Tsbbdoen	SCSI Data output enable	3	11	ns
Tsbbdodis	SCSI Data output disable	3	11	ns

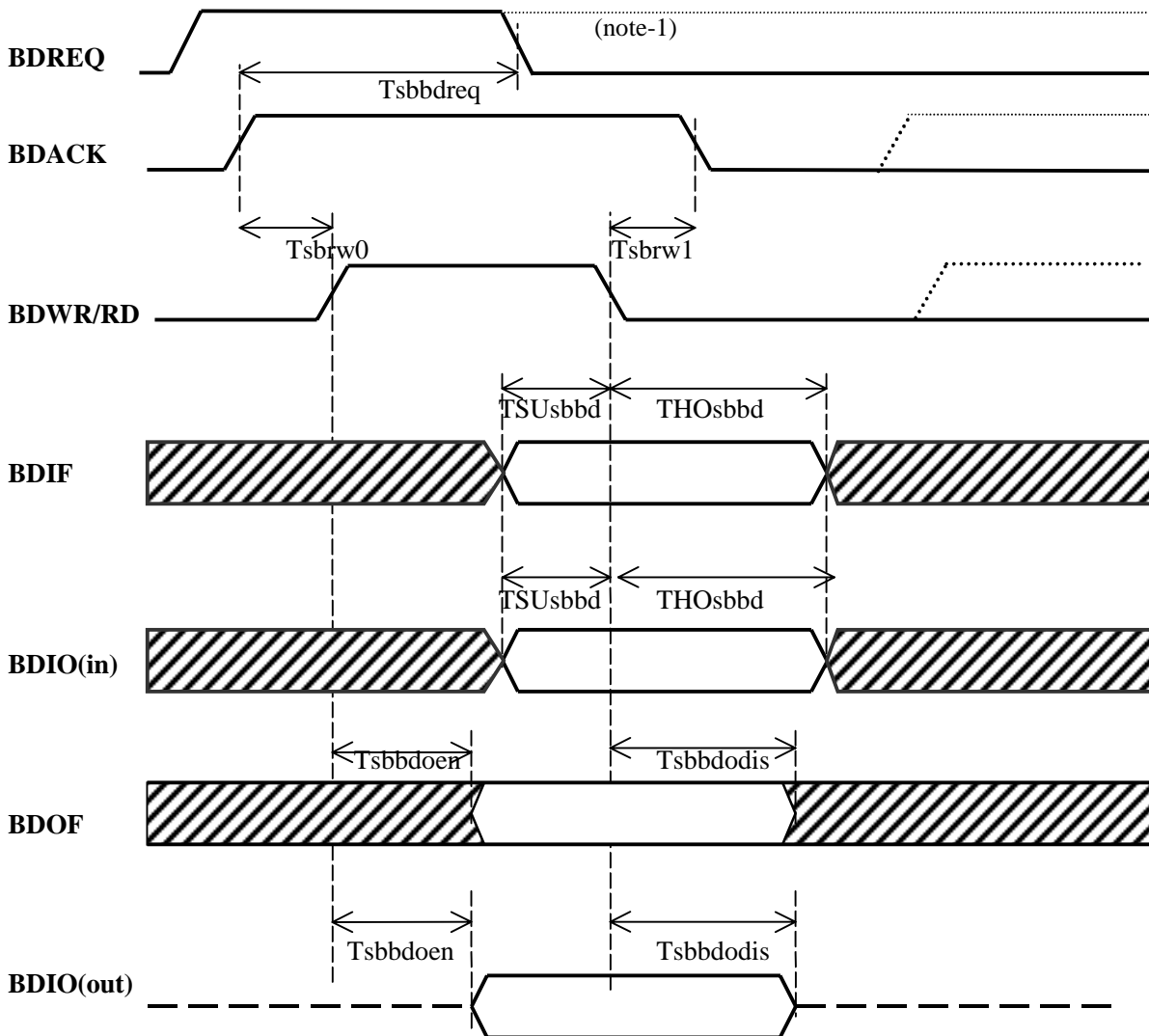


Figure 11-12. SCSI Burst Mode

note-1) BDREQ is active when FIFO has capacity.

note-2) Tsbbdreq means monitoring time of BDREQ transition from BDACK(BDRD/WR) edge.

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Title	Item	min	max	unit
Tui	Unlimit interlock time		TBD	ns
Tenv	Emulate Time		TBD	ns
Tdvs	Data valid setup time	$T_{cyc} * (BDODelay + 1) - 6$		ns
Tdvh	Data valid hold time	$T_{cyc} - 13$		ns
Tcyc	Cycle time	25		ns
Tmli	Interlock time with minimum		TBD	ns
Tli	Unlimited interlock time		TBD	ns
Tziordy	Before driving IORDY	TBD		ns
Tiordyz	pull-up time		TBD	ns

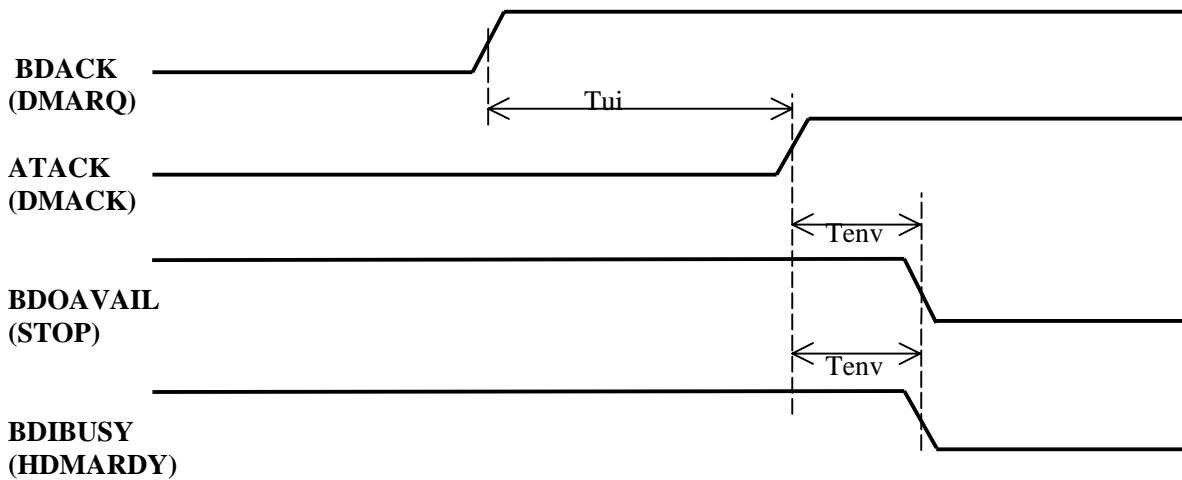


Figure 11-13. ATAPI Initiate (READ)

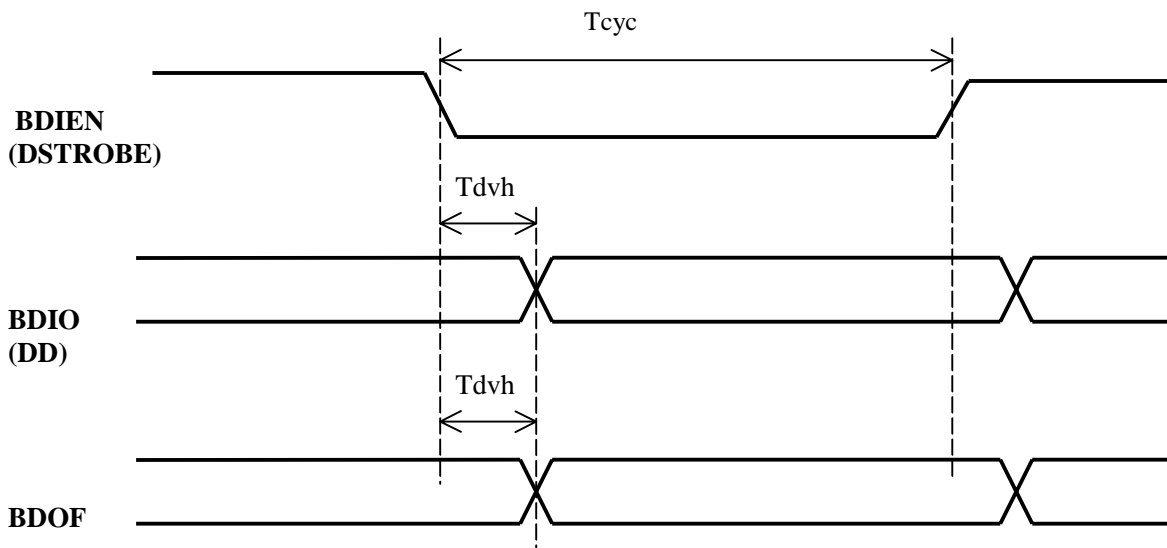


Figure 11-14. ATAPI Read



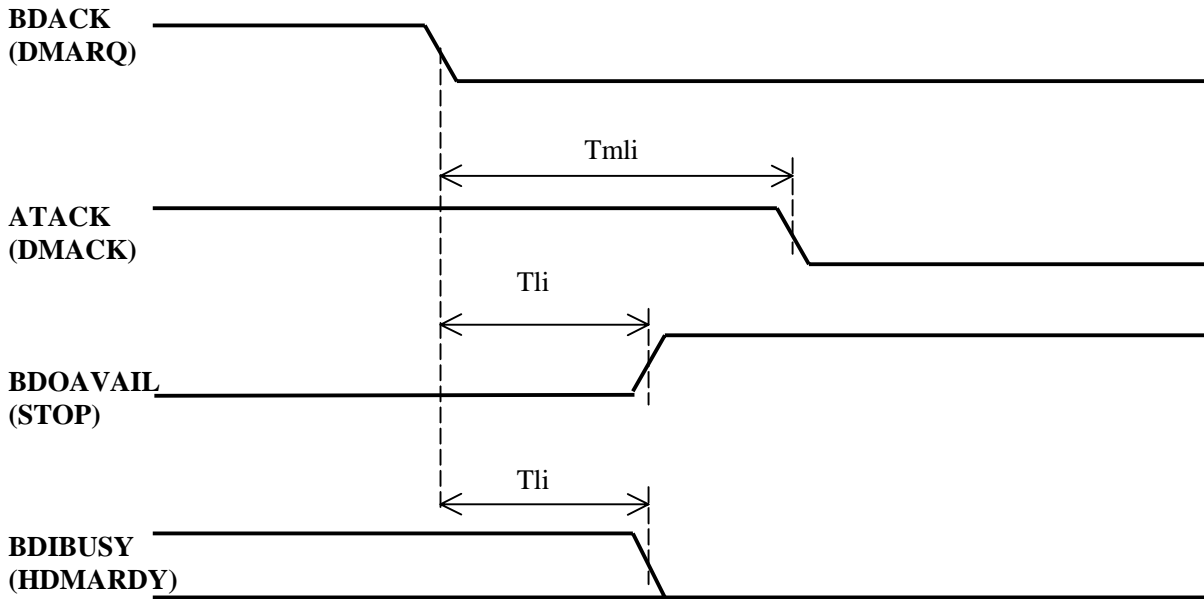


Figure 11-15. ATAPI Terminate (READ)

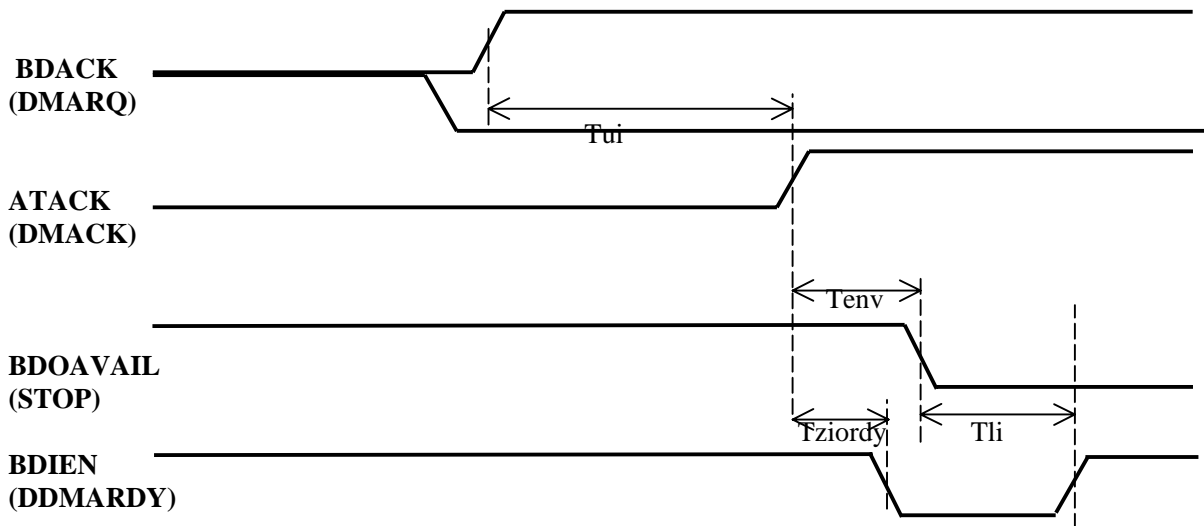


Figure 11-16. ATAPI Initiate (Write)

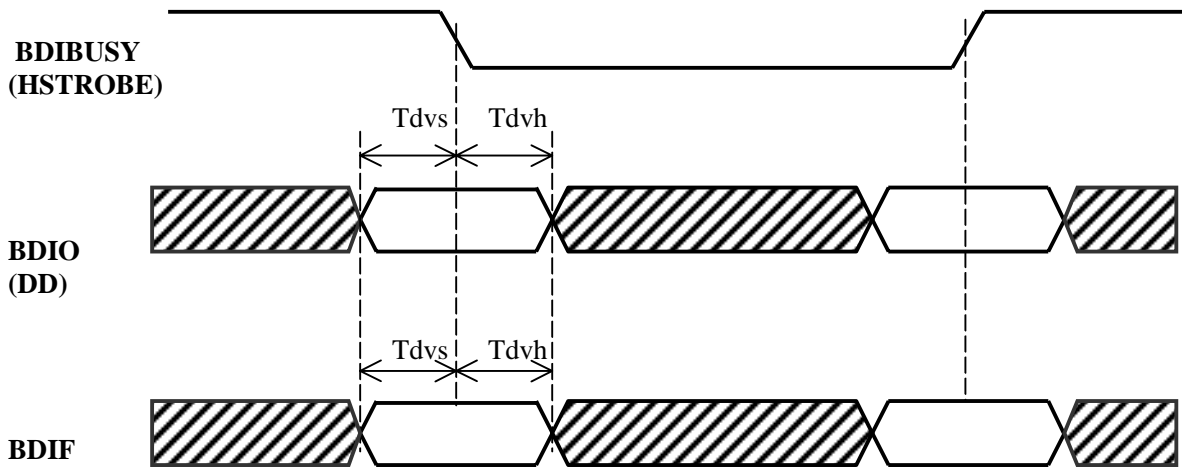


Figure 11-17. ATAPI Write

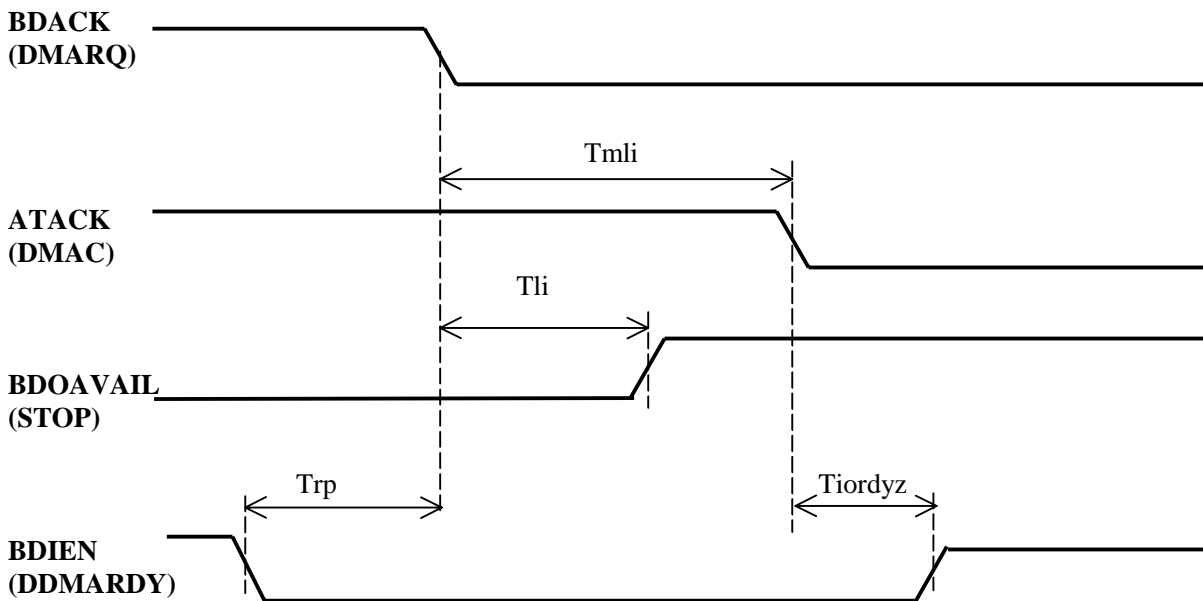
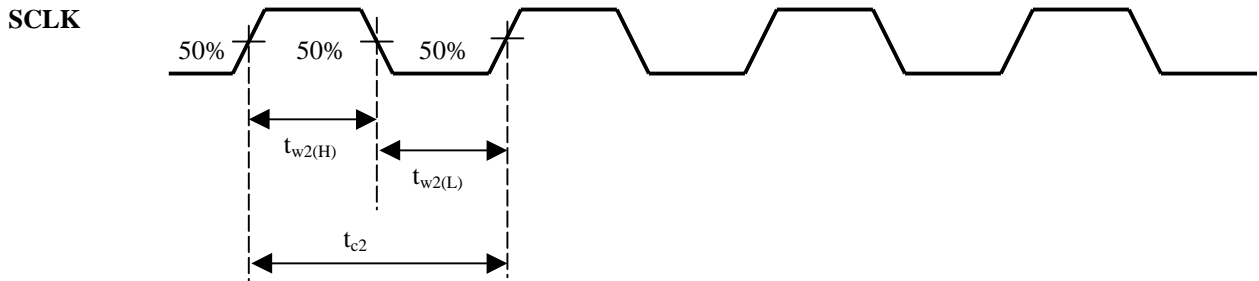
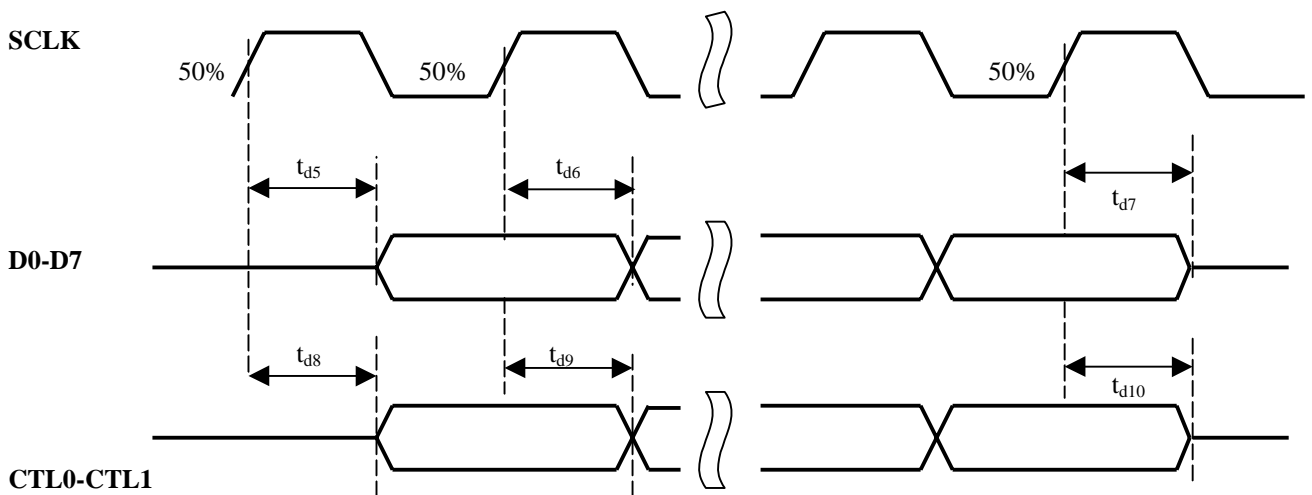


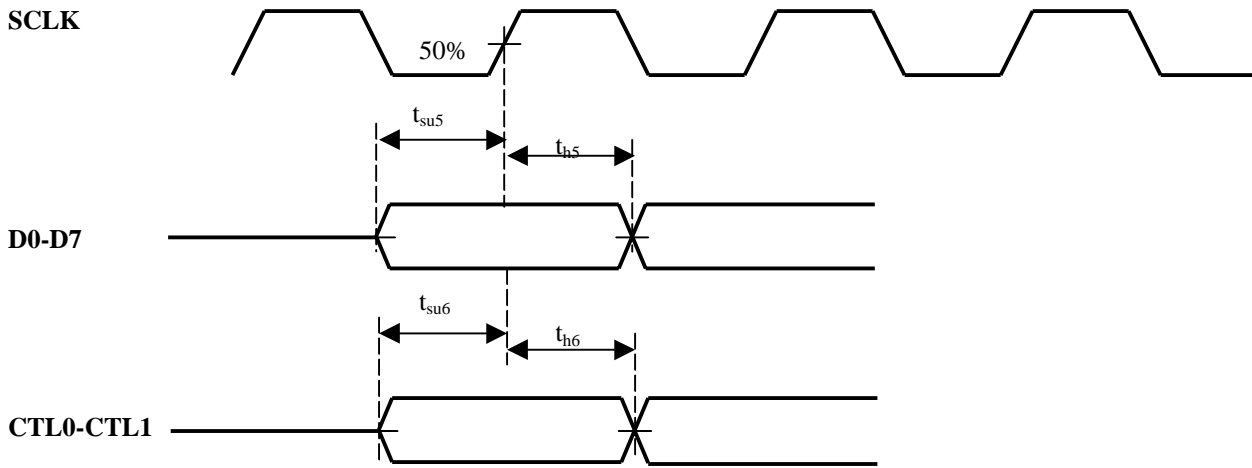
Figure 11-18. ATAPI Terminate (Write)



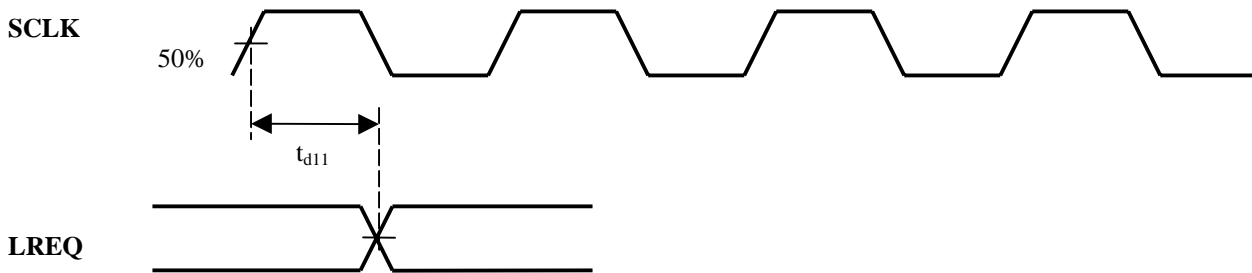
**Figure 11-19. SCLK Waveform**



**Figure 11-20. TSB43LV81-to-Phy-Layer Transfer Waveforms**



**Figure 11-21. Phy Layer-to-TSB43LV81 Transfer Waveforms**



**Figure 11-22. TSB43LV81 link-request-Phy-Layer Waveforms**

**12. PHY internal register configuration**

There are 16 accessible internal registers for PHY block in the TSB43LV81. The configuration of the registers at addresses 0 through 7 (the base registers) is fixed, while the configuration of the registers at addresses 8 through Fh (the paged registers) is dependent upon which one of eight pages, numbered 0 through 7, is currently selected. The selected page is set in base register 7.

The configuration of the base registers is shown in Table 12-1, and corresponding field descriptions given in 12-1. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as “Reserved” or “Rsvd” in the register configuration tables below) is read as 0, but is subject to future usage. All registers in pages 2 through 6 are reserved.

**Table 12-1. Base Register Configuration**

Address	Bit Position							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended ('b111)			Rsvd	Num_Ports ('b0010)			
0011	PHY_Speed ('b010)			Rsvd	Delay ('b0000)			
0100	LCtrl	C	Jitter ('b000)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_select			Rsvd	Port_Select			

**Table 12-2. Base Register Field Descriptions**

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus-reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus-reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power-status. This bit indicates the state of the CPS input pin. The CPS pin is normally tied to serial bus cable power through a 400 kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for guaranteed reliable operation.



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FIELD	SIZE	TYPE	DESCRIPTION
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus-reset. The RHB bit is reset to 0 by hardware reset and is unaffected by bus-reset.
IBR	1	Rd/Wr	Initiate bus-reset. This bit instructs the PHY to initiate a long (166 $\mu$ s) bus-reset at the next opportunity. Any receive or transmit operation in progress when this bit is set will complete before the bus-reset is initiated. The IBR bit is reset to 0 by hardware reset or bus-reset.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value is used to set the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count may be set either by a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is set to 3Fh by hardware reset or after two consecutive bus-resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	Rd	Extended register definition. For the TSB41LV01 this field is 'b111, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. This field indicates the number of ports implemented in the PHY. For the TSB41LV01 this field is 1.
PHY_Speed	3	Rd	PHY speed capability. For the TSB41LV01 PHY this field is 'b010, indicating S400 speed capability.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst case repeater data delay of the PHY, expressed as 144+(delay*20) ns. For the TSB41LV01 this field is 0.
LCtrl	1	Rd/Wr	<p>Link-active status control. This bit is used to control the active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the "L" field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active and the LCtrl bit is set.</p> <p>The LCtrl bit provides a software controllable means to indicate the LLC active status in lieu of using the LPS input.</p> <p>The LCtrl bit is set to 1 by hardware reset and is unaffected by bus-reset.</p> <p>NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information will continue to be presented on the interface, and any requests indicated on the LREQ input will be processed, even if the LCtrl bit is cleared to 0.</p>
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the "c" field (bit 20) of the self-ID packet. This bit is set to the state specified by the C/LKON input pin upon hardware reset and is unaffected by bus-reset.



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FIELD	SIZE	TYPE	DESCRIPTION
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (JITTER+1)*20 ns. For the TSB41LV01 this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node's power consumption and source characteristics, and is replicated in the "pwr" field (bits 21–23) of the self-ID packet. This field is set to the state specified by the PC0–PC2 input pins upon hardware reset and is unaffected by bus-reset. See table 12-5.
RPIE	1	Rd/Wr	Resuming port interrupt enable. This bit, if set to 1, enables the port event interrupt (PEI) bit to be set whenever resume operations begin on any port. This bit also enables the C/LKON output signal to be activated whenever the LLC is inactive and any of the CTOI, CPSI, or STOI interrupt bits are set. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus-reset. This bit, if set to 1, instructs the PHY to initiate a short (1.30 $\mu$ s) arbitrated bus-reset at the next opportunity. This bit is reset to 0 by bus-reset.  NOTE: Legacy IEEE Std 1394-1995 compliant PHYs may not be capable of performing short bus-resets. Therefore, initiation of a short bus-reset in a network that contains such a legacy device will result in a long bus-reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times-out during tree-ID start, and may indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.  If the CTOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY will activate the C/LKON output to notify the LLC to service the interrupt.  NOTE: If the network is configured in a loop, only those nodes that are part of the loop will generate a configuration time-out interrupt. All other nodes will instead time-out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit.  If the CPSI and RPIE bits are both set and the LLC is or becomes inactive, the PHY will activate the C/LKON output to notify the LLC to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus-reset to occur). This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.  If the STOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY will activate the C/LKON output to notify the LLC to service the interrupt.



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FIELD	SIZE	TYPE	DESCRIPTION
PEI	1	Rd/Wr	<p>Port event interrupt. This bit is set to 1 upon a change in the bias (unless disabled), connected, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.</p> <p>If the PEI bit is set (regardless of the state of the RPEI bit) and the LLC is or becomes inactive, the PHY will activate the C/LKON output to notify the LLC to service the interrupt.</p>
EAA	1	Rd/Wr	<p>Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in P1394a (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus-reset.</p> <p>NOTE: The EAA bit should be set only if the attached LLC is P1394a compliant. If the LLC is not P1394a compliant, use of the arbitration acceleration enhancements may interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.</p>
EMC	1	Rd/Wr	<p>Enable multi-speed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in P1394a. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.</p> <p>NOTE: The use of multi-speed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multi-speed concatenation requires that the attached LLC be P1394a compliant.</p>
Page_Select	3	Rd/Wr	<p>Page-select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by hardware reset and is unaffected by bus-reset.</p>
Port_Select	4	Rd/Wr	<p>Port-select. This field selects the port when accessing per-port status or control (e.g., when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus-reset.</p>

The Port Status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page\_Select field and the desired port number to the Port\_Select field in base register 7. The configuration of the Port Status page registers is shown in Table 12-4, and corresponding field descriptions given in Table 12-4. If the selected port is unimplemented, all registers in the Port Status page are read as 0.

**Table 12-3. Page 0 (Port Status) Register Configuration**



Address	Bit Position							
	0	1	2	3	4	5	6	7
1000	AStat		Bstat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

**Table 12-4. Page 0 (Port Status) Register Field Descriptions**

FIELD	SIZE	TYPE	DESCRIPTION										
AStat	2	Rd	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: <table style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;"><u>Code</u></td> <td style="text-align: center;"><u>Line State</u></td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">Z</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">invalid</td> </tr> </table>	<u>Code</u>	<u>Line State</u>	11	Z	01	1	10	0	00	invalid
<u>Code</u>	<u>Line State</u>												
11	Z												
01	1												
10	0												
00	invalid												
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the ASTAT field.										
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus-reset until tree-ID has completed.										
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus-reset.  NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but the port is not necessarily active.										
Bias	1	Rd	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 $\mu$ s for the Bias bit to be set to 1.										



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FIELD	SIZE	TYPE	DESCRIPTION										
Dis	1	Rd/Wr	Port disabled control. If 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus-reset.										
Peer_Speed	3	Rd	<p>Port peer speed. This field indicates the highest speed capability of the peer PHY connected to the selected port, encoded as follows:</p> <table border="0"> <thead> <tr> <th><u>Code</u></th> <th><u>Peer Speed</u></th> </tr> </thead> <tbody> <tr> <td>000</td> <td>S100</td> </tr> <tr> <td>001</td> <td>S200</td> </tr> <tr> <td>010</td> <td>S400</td> </tr> <tr> <td>011–111</td> <td>invalid</td> </tr> </tbody> </table> <p>The Peer_Speed field is invalid after a bus-reset until self-ID has completed.</p> <p>NOTE: Peer speed codes higher than 'b010 (S400) are defined in P1394a. However, the TSB41LV01 is only capable of detecting peer speeds up to S400.</p>	<u>Code</u>	<u>Peer Speed</u>	000	S100	001	S200	010	S400	011–111	invalid
<u>Code</u>	<u>Peer Speed</u>												
000	S100												
001	S200												
010	S400												
011–111	invalid												
PIE	1	Rd/Wr	Port event interrupt enable. When set to 1, a port event on the selected port will set the port event interrupt (PEI) bit and notify the link. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.										
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus-reset.										



The Vendor Identification page is used to identify the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page\_Select field in base register 7. The configuration of the Vendor Identification page is shown in Table 12-5, and corresponding field descriptions given in Table 12-6.

**Table 12-5. Page 1 (Vendor ID) Register Configuration**

Address	Bit Position							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

**Table 12-6. Page 1 (Vendor ID) Register Field Descriptions**

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB41LV01 this field is 01h, indicating compliance with the P1394a specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB41LV01 this field is 08_00_28h (Texas Instruments) (the MSB is at register address 'b1010).
Product_ID	24	Rd	Product identifier. For the TSB41LV01 this field is 41_xx_xxxh (the MSB is at register address 'b1101).

The Vendor-Dependent page provides access to the special control features of the TSB41LV01, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page\_Select field in base register 7. The configuration of the Vendor-Dependent page is shown in Table 12-7, and corresponding field descriptions given in Table 12-8.

**Table 12-7. Page 7 (Vendor-Dependent) Register Configuration**



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Address	Bit Position							
	0	1	2	3	4	5	6	7
1000	NPA	Reserved					Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

**Table 12-8. Page 7 (Vendor-Dependent) Register Field Descriptions**

FIELD	SIZE	TYPE	DESCRIPTION										
NPA	1	Rd/Wr	Null-packet actions flag. This bit instructs the PHY to not clear fair and priority requests when a null packet is received with arbitration acceleration enabled. If 1, then fair and priority requests are cleared only when a packet of more than 8 bits is received; ACK packets (exactly 8 data bits), null packets (no data bits), and mal-formed packets (less than 8 data bits) will not clear fair and priority requests. If 0, then fair and priority requests are cleared when any non-ACK packet is received, including null-packets or mal-formed packets of less than 8 bits. This bit is cleared to 0 by hardware reset and is unaffected by bus-reset.										
Link_Speed	2	Rd/Wr	<p>Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows:</p> <table border="0" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;"><u>Code</u></td> <td style="text-align: center;"><u>Speed</u></td> </tr> <tr> <td style="text-align: center;">00</td> <td style="text-align: center;">S100</td> </tr> <tr> <td style="text-align: center;">01</td> <td style="text-align: center;">S200</td> </tr> <tr> <td style="text-align: center;">10</td> <td style="text-align: center;">S400</td> </tr> <tr> <td style="text-align: center;">11</td> <td style="text-align: center;">illegal</td> </tr> </table> <p>This field is replicated in the "sp" field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the TSB41LV01 PHY identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to 'b10 (S400) by hardware reset and is unaffected by bus-reset.</p>	<u>Code</u>	<u>Speed</u>	00	S100	01	S200	10	S400	11	illegal
<u>Code</u>	<u>Speed</u>												
00	S100												
01	S200												
10	S400												
11	illegal												



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**13. APPENDIX A - PIN ASSIGNMENTS for TSB43LV81**

NOTE: PIN ASSIGNMENT IS PRELIMINARY AND IS SUBJECT TO CHANGE

Pin No	Signal Name	I/O	Pin No	Signal Name	I/O	Pin No	Signal Name	I/O	Pin No	Signal Name	I/O
1	AUX[0]	I/O	37	NCLKOUT	O	73	BDIO12	I/O	109	ALE	I
2	AUX[1]	I/O	38	ATAACK	O	74	BDIO13	I/O	110	XCS	I
3	DVSS		39	DVSS		75	DVDD5		111	XRESETL	I
4	AUX[2]	I/O*	40	BDIF0	I/O	76	BDIO14	I/O	112	DVDD5	
5	DVSS		41	BDIF1	I/O	77	BDIO15	I/O	113	DVSS	
6	AUX[3]	I/O*	42	BDIF2	I/O	78	DVSS		114	AGND	
7	DVDD		43	DVSS		79	XINT	I/O	115	AGND	
8	AUX[4]	I/O*	44	BDOF0	O	80	DVSS		116	AVDD	
9	AUX[5]	I/O*	45	BDOF1	O	81	DA[0]	I/O	117	AVDD	
10	DVDD5		46	BDOF2	O	82	DA[1]	I/O	118	TPB-	I/O
11	AUX[6]	I/O*	47	DVDD		83	DA[2]	I/O	119	TPB+	I/O
12	AUX[7]	I/O*	48	DVSS		84	DA[3]	I/O	120	AGND	
13	AUX[8]	I/O*	49	BDIBSY	O	85	DVDD		121	TPA-	I/O
14	DVSS		50	BDIEN	I	86	DVSS		122	TPA+	I/O
15	AUX[9]	I/O*	51	BDOAVAIL	O	87	DA[4]	I/O	123	TPBIAS	I/O
16	DVSS		52	BDOEN	I	88	DA[5]	I/O	124	AGND	
17	AUX[10]	I	53	DVDD5		89	DA[6]	I/O	125	AGND	
18	AUX[11]	O	54	DVSS		90	DA[7]	I/O	126	R0	I/O*
19	DVDD		55	BDIO0	I/O	91	DVSS		127	R1	I/O*
20	CAN	O	56	BDIO1	I/O	92	DA[8]	I/O	128	AVDD	
21	PD	I	57	BDIO2	I/O	93	DA[9]	I/O	129	AVDD	
22	LPS	I	58	BDIO3	I/O	94	DA[10]	I/O	130	DVDD	
23	DVSS		59	DVSS		95	DVSS		131	DVSS	
24	TM	I	60	BDIO4	I/O	96	DA[11]	I/O	132	DVSS	
25	CPS	I	61	BDIO5	I/O	97	DVDD		133	FLT0	I/O*
26	DVSS		62	BDIO6	I/O	98	DA[12]	I/O	134	FLT1	I/O*
27	DVDD5		63	BDIO7	I/O	99	DA[13]	I/O	135	PLLV	
28	MODE[0]	I	64	DVSS		100	DA[14]	I/O	136	PLLG	
29	MODE[1]	I	65	BDACK		101	DA[15]	I/O	137	PLLG	
30	M8M16	I	66	DVDD		102	DVSS		138	DVSS	
31	DVDD		67	DVSS		103	DVDD5		139	XO	I/O*
32	DVSS		68	BDIO8	I/O	104	DVSS		140	XI	I/O*
33	MUXMODE	I	69	BDIO9	I/O	105	WAIT	O	141	DVSS	
34	CLKSEL	I/O	70	BDIO10	I/O	106	XRD	I	142	DVDD5	
35	BDICLK	I/O	71	BDIO11	I/O	107	XWR	I	143	XRESETP	I
36	NCLKOEN	I/O	72	DVSS		108	DVDD		144	DVDD	

Note) Pins marked “\*” are not 5[V] tolalante, other pins are 5[V] tolalante.

