FEATURES

- **Provides 16 arithmetic operations**
- **Provides 16 logic operations**
- **Full look-ahead for high-speed arithmetic operation on long words**
- **Higher speed compared to 9LS/54LS and 9LS/74LS**
- **8mA sink current over full military temperature range**
- **50mV improved V_{OL} compared to 9LS/74LS**
- **440μA source current**
- **100% reliability assurance testing in compliance with MIL-STD-883.**

DESCRIPTION

The 25LS181 is an arithmetic logic unit (ALU)/function generator which has a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182, full carry ahead look-ahead circuits, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 25LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1 which requires an end-around or forced carry to provide A-B.

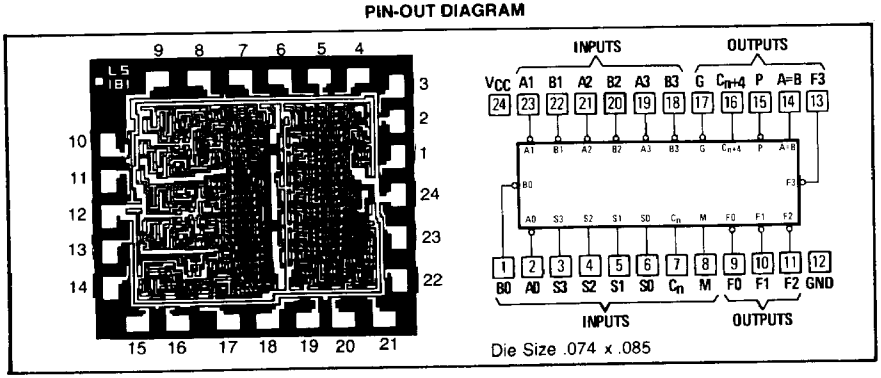
The 25LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs, S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT $\overline{C}_n$	OUTPUT $\overline{C}_{n+4}$	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A = B	A = B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≠ B	A ≠ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

PIN-OUT DIAGRAM



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ALU SIGNAL DESIGNATIONS

The 25LS181 can be used with the signal designations of either Figure 1 or Figure 2

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

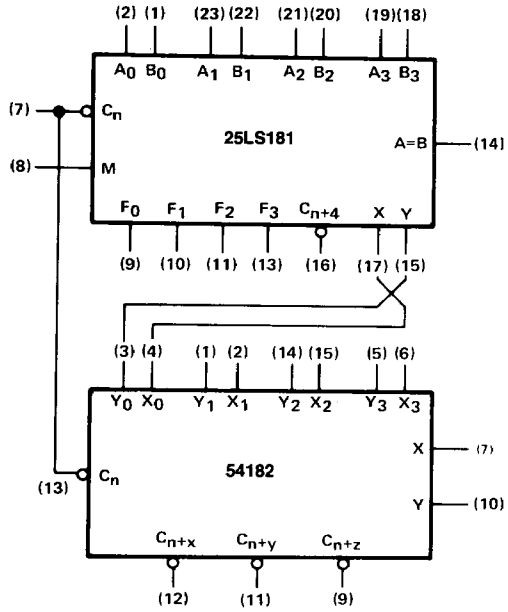


FIGURE 1
(FOR TABLE 1)

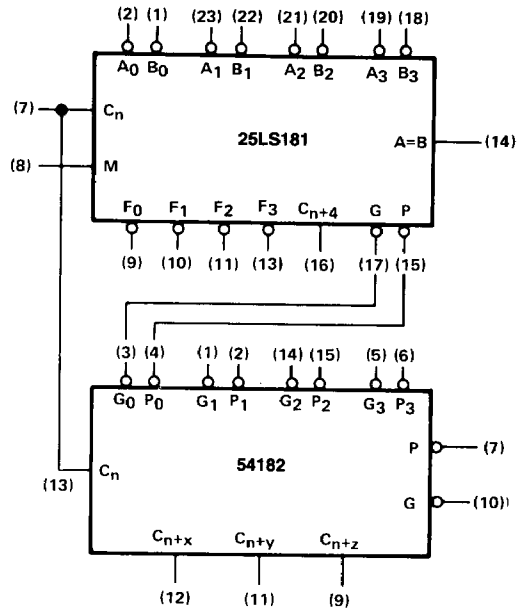


FIGURE 2
(FOR TABLE 2)

TABLE 1

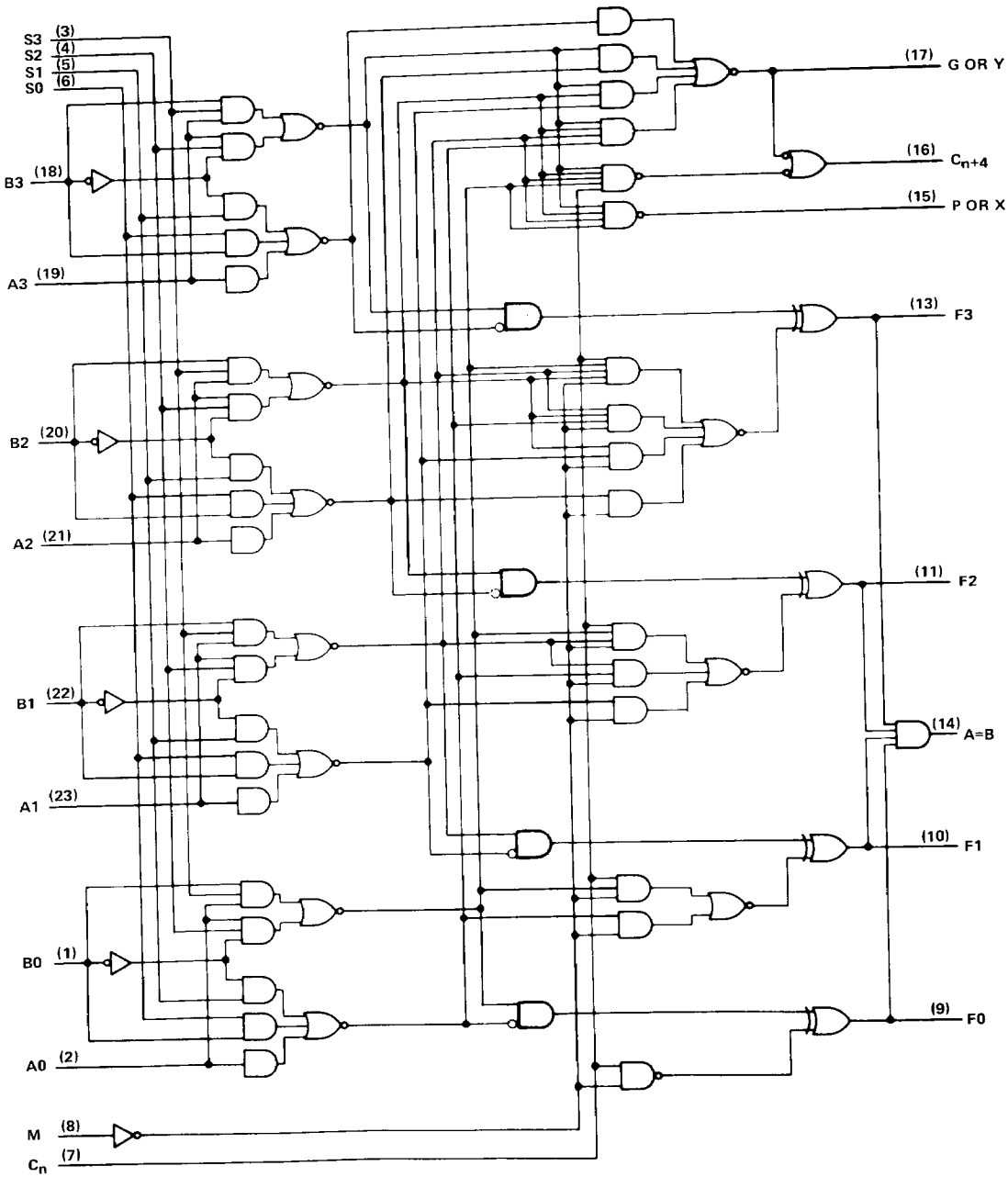
SELECTION S_3 S_2 S_1 S_0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: C_n = H (no carry)	M = L; ARITHMETIC OPERATIONS: C_n = L (no carry)
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE 2

SELECTION S_3 S_2 S_1 S_0	ACTIVE LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: C_n = L (with carry)	M = L; ARITHMETIC OPERATIONS: C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



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Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−440			−440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	Any Output except A = B	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−440μA		2.5	3.4		2.7	3.4		V
I_{OH}	A = B Output only	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, V_I=V_{IH} or V_{IL}				100			100	μA
V_{OL}	All outputs	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max V_I=V_{IH} or V_{IL}	I_{OL}=4mA			0.40			0.40	V
	Output G		I_{OL}=8mA			0.45			0.45	
			I_{OL}=16mA(G)			0.55			0.55	
I_I	Mode input	V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
	Any $\overline{A}$ or $\overline{B}$ input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.5			0.5	
I_{IH}	Mode input	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Any $\overline{A}$ or $\overline{B}$					60			60	
	Any S input					80			80	
	Carry input					100			100	
I_{IL}	Mode input	V_{CC}=MAX, V_I=0.5V				−0.36			−0.36	mA
	Any $\overline{A}$ or $\overline{B}$ input					−1.08			−1.08	
	Any S input					−1.44			−1.44	
	Carry input					−2			−2	
I_{OS}†	Any Output except A=B	V_{CC}=MAX		−15		−85	−15		−85	mA
I_{CC}††		V_{CC}=MAX	Condition A		20	32		20	34	mA
			Condition B		21	35		21	37	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M and A inputs are at 4.5V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter ¶	From (Input)	To (Output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	C_n	C_{n+4}		14	25	ns
t_{PHL}				13	14	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	Any A or B	C_{n+4}		24	33	ns
t_{PHL}				17	31	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	C_{n+4}		24	35	ns
t_{PHL}				29	35	
M = 0V, (SUM or DIFF mode)						
t_{PLH}	C_n	Any F		12	19	ns
t_{PHL}				12	18	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	Any A or B	G		12	25	ns
t_{PHL}				15	23	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	G		20	25	ns
t_{PHL}				17	25	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 4.5V (SUM mode)						
t_{PLH}	Any A or B	P		14	26	ns
t_{PHL}				20	26	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	P		24	30	ns
t_{PHL}				22	26	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	A_i or B_i	F_i		15	28	ns
t_{PHL}				13	19	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	A_i or B_i	F_i		24	30	ns
t_{PHL}				15	19	
M = 4.5V (logic mode)						
t_{PLH}	A_i or B_i	F_i		17	31	ns
t_{PHL}				15	25	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	A = B		33	50	ns
t_{PHL}				29	45	

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All B	All B	Any F or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase