

SN54LS395A, SN74LS395A 4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

OCTOBER 1976 — REVISED MARCH 1988

- Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers
- 'LS395A Offers Three Times the Sink-Current Capability of 'LS395
- Low Power Dissipation . . . 75 mW Typical (Enabled)
- Applications:
 - N-Bit Serial-To-Parallel Converter
 - N-Bit Parallel-To-Serial Converter
 - N-Bit Storage Register

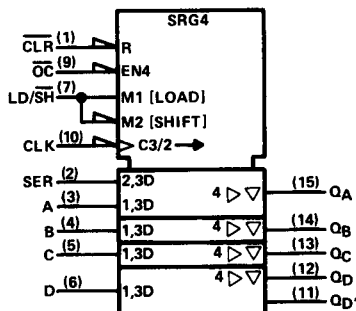
description

These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), load shift (LD/ \overline{SH}), output control (\overline{OC}) and direct overriding clear (CLR) inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D ' is still available for cascading.

logic symbol†



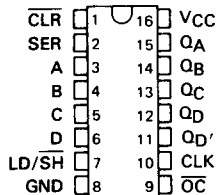
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS395A . . . J OR W PACKAGE

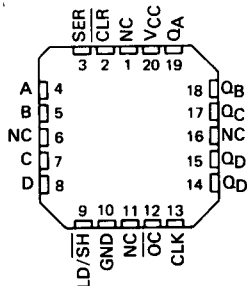
SN74LS395A . . . D OR N PACKAGE

(TOP VIEW)



SN54LS395A . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

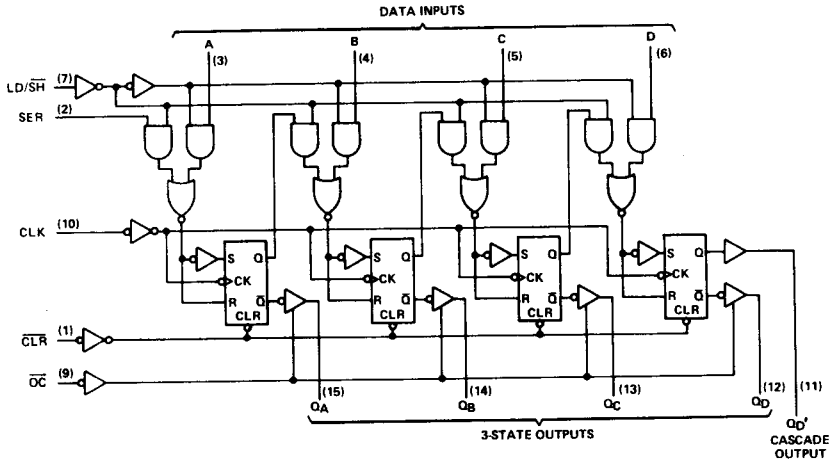
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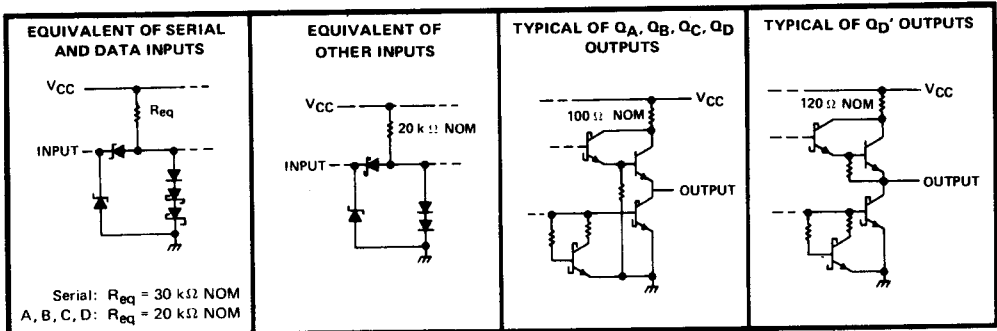
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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



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FUNCTION TABLE

INPUTS					3-STATE OUTPUTS				CASCADE			
CLR	LD/SH	CLK	SER	PARALLEL				Q _A	Q _B	Q _C	Q _D	OUTPUT Q _D '
				A	B	C	D					
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	L	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS395A	-55°C to 125°C
SN74LS395A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS395A			SN74LS395A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	Q _A , Q _B , Q _C , Q _D		-1			-2.6	mA
	Q _D '		-400			-400	μA
Low-level output current, I _{OL}	Q _A , Q _B , Q _C , Q _D		12			24	mA
	Q _D '		4			8	mA
Clock frequency, f _{clock}	0		30	0		30	MHz
Width of clock pulse, t _{w(clock)}	16			16			ns
Setup time, high-level or low-level data, t _{SU}	LD/SH		40	40			ns
	All other inputs		20	20			
Hold time, high-level or low-level data, t _H	10			10			ns
Operating free-air temperature, T _A	-55		125	0		70	°C

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SN54LS395A, SN74LS395A

4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS395A		SN74LS395A		UNIT			
		MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V _{IH} High-level input voltage		2			2	V			
V _{IL} Low-level input voltage				0.7		0.8			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5			
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	Q _A , Q _B , Q _C , Q _D	2.4	3.4	2.4	3.1	V		
		Q _D '	2.5	3.4	2.7	3.4	V		
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max, V _{IH} = 2 V	Q _A , Q _B , Q _C , Q _D	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
			I _{OL} = 24 mA			0.35	0.5		
		Q _D '	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 8 mA				0.35	0.5	
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V	Q _A , Q _B , Q _C , Q _D		20		20	μA		
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V	Q _A , Q _B , Q _C , Q _D		-20		-20	μA		
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA		
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20		20	μA		
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA		
I _{OS} Short-circuit output current§	V _{CC} = MAX	Q _A , Q _B , Q _C , Q _D	-30	-130	-30	-130	mA		
		Q _D '	-20	-100	-20	-100	mA		
I _{CC} Supply current	V _{CC} = MAX, See Note 2	Condition A		22	34	22	34	mA	
		Condition B		21	31	21	31		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

- A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
- B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum clock frequency	See Note 3.	30	45		MHz
t _{PHL} Propagation delay time, high-to-low-level output from clear	Q _A , Q _B , Q _C , Q _D outputs:		22	35	ns
t _{PLH} Propagation delay time, low-to-high-level output	R _L = 667 Ω, C _L = 45 pF		15	30	ns
t _{PHL} Propagation delay time, high-to-low-level output	Q _D ' output:		20	30	ns
t _{pZH} Output enable time to high level	R _L = 2 kΩ, C _L = 15 pF		15	25	ns
t _{pZL} Output enable time to low level			17	25	ns
t _{pHZ} Output disable time from high level	C _L = 5 pF,		11	17	ns
t _{pLZ} Output disable time from low level	See Note 3		12	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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