TECHNICAL MANUAL

LSI53C1035
PCI-X to Ultra320 SCSI
RAID Controller

November 2003

Version 2.0

LSI LOGIC®

DB14-000224-01

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Preface

This book is the primary reference and technical manual for the LSI53C1035 PCI-X to Dual Channel Ultra320 SCSI RAID Controller. It contains a complete functional description for the LSI53C1035 and includes complete physical and electrical specifications for the LSI53C1035.

Audience

This document assumes that the reader has some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSI53C1035 for use in a system
- Engineers who are designing the LSI53C1035 into a system
- Engineers who are testing the LSI53C1035 in a system

Organization

This document has the following chapters:

- Chapter 1, "**Introduction,**" provides an overview of the LSI53C1035 features and capabilities.
- Chapter 2, "**Functional Description,**" provides a detailed functional description of the LSI53C1035 operation. This chapter provides a block diagram description and discusses the possible RAID implementations, the external memory interfaces, and the PCI, PCI-X, and SCSI buses.
- Chapter 3, "**Signal Description,**" provides a detailed signal description of the LSI53C1035.

- Chapter 4, "**PCI Host Register Description,"** provides a bit-level description of the LSI53C1035 register set.
- Chapter 5, "**Specifications,"** provides the electrical, physical, and timing specifications.

Related Publications

LSI Logic Document
Fusion-MPT Device Management User's Guide, Version 2.0,
Document No. DB15-000186-02

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ANSI
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New York, NY 10036
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Global Engineering Documents
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Englewood, CO 80112
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ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

SCSI Electronic Bulletin Board
(719) 533-7950

PCI Special Interest Group
2575 N. E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

Double Data Rate (DDR) SDRAM Specification (JEDEC Standard JESD79C, March 2003)

PCI Local Bus Specification, Revision 2.2

PCI-X Addendum to the *PCI Local Bus Specification, Revision 1.0a*

Proposed *SCSI Parallel Interface-4* (SPI-4) draft standard

PCI Bus Power Management Interface Specification, Revision 1.1

PC2001 System Design Guide

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end with a "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Revision History

Revision	Date	Remarks
Final Version 2.0	11/2003	Final Release. Updated the environmental and operating conditions specifications. Updated the Integrated RAID definitions.
Advance Version 0.1	7/2002	Initial release of document.

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Chapter 1
Introduction

This chapter provides a general overview of the LSI53C1035 PCI-X to Dual Channel Ultra320 SCSI RAID Controller. This chapter contains the following sections:

1.1 General Description

The LSI Logic LSI53C1035 is a high-performance, integrated PCI-X to Ultra320 SCSI RAID on a chip (ROC) controller. The LSI53C1035 integrates two high-performance Ultra320 SCSI RAID channels and a 64-bit, 133 MHz PCI/PCI-X bus master DMA channel. The LSI53C1035 brings Ultra320 SCSI RAID performance to host adapter, workstation, and server designs, making it easy to add a high-performance SCSI bus to any PCI or PCI-X system. The LSI53C1035 can operate as either an Ultra320 SCSI RAID controller or a conventional Ultra320 SCSI controller.

The LSI53C1035 employs three ARM9™ processors to meet the data transfer flexibility requirements of the Ultra320 SCSI and PCI-X specifications. Separate ARM966E-S™ processors manage each SCSI channel, and an ARM946E™ processor manages interactions between the LSI53C1035 and the host processor. The ARM946E processor offers 16 Kbytes of data cache and 16 Kbytes of instruction cache, which provide a significant performance increase to host side interactions. The LSI53C1035 also provides a high speed Dual Data Rate (DDR) SDRAM interface and a hardware assist parity engine to support RAID operations, resulting in unsurpassed performance.

Fusion-MPT™ architecture is a multithreaded I/O algorithm that supports data transfers between the host system and SCSI devices. The Fusion-MPT architecture is a performance based message passing protocol that offloads the host CPU by completely managing all I/Os and minimizes system bus overhead by coalescing interrupts. Fusion-MPT technology provides an efficient architecture that solves the protocol overhead problems of previous intelligent and nonintelligent designs. The Fusion-MPT architecture requires only a thin, easy to develop device driver that is independent of the I/O bus.

The LSI53C1035 supports both the *PCI Local Bus Specification, Revision 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*.[1] The LSI53C1035 supports up to a 64-bit, 133 MHz PCI-X bus, and is backwards compatible with previous versions of the PCI bus.

1. Depending on the operating mode of the device, references to PCI are either inclusive of both PCI and PCI-X, or refer individually to either PCI or PCI-X.

The LSI53C1035 supports both SCSI and RAID modes. In the SCSI mode, the LSI53C1035 functions as the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI controller. In the RAID mode, the LSI53C1035 is a full featured RAID controller that supports RAID levels 0, 1, 5, and 10.

The LSI53C1035 provides a 2-wire serial EEPROM interface, a separate industry standard two-wire serial interface (ISTWI), a Universal Asynchronous Receiver/Transmitter (UART) interface, an external memory interface, an 8-pin General Purpose I/O (GPIO) interface, a 64-bit DDR SDRAM interface, and a test interface. The serial EEPROM stores PCI configuration space information. The ISTWI provides a 400 Kbits/s bus to external peripherals. The UART interface provides a modem connection that facilitates debugging of a LSI53C1035 host bus adapter (HBA). The external memory interface supports nonvolatile synchronous RAM (NVSRAM), Flash ROM, and General Purpose (GP) memory. The NVSRAM supports the Integrated RAID™ feature, which includes Integrated Mirroring™ (IM) technology and Integrated Striping™ (IS) technology. The Flash ROM stores the LSI53C1035 BIOS and firmware.

The DDR SDRAM significantly improves the performance of the LSI53C1035. The LSI53C1035 uses the high speed DDR SDRAM interface to queue, organize, and track SCSI RAID accesses. The host processor can continue to issue RAID writes over the Fusion-MPT interface, even when the SCSI RAID channel is busy. The LSI53C1035 queues the RAID write data in the DDR SDRAM until the SCSI channel is free, and then performs the write. The host need not wait for the SCSI channel. Also, the LSI53C1035 uses the DDR SDRAM to organize read data from the RAID devices before providing the data to the host, which reduces the number of interrupts that the LSI53C1035 issues to the host processor.

Figure 1.1 shows a typical LSI53C1035 board application connected to external ROM memory.

Figure 1.1 Typical LSI53C1035 Host Bus Adapter

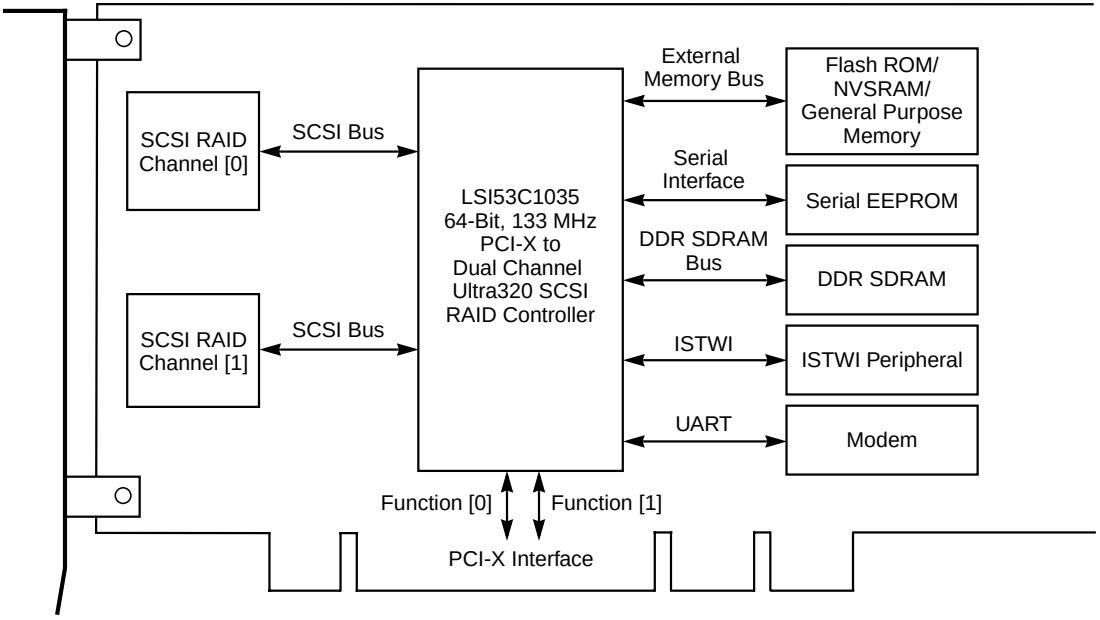
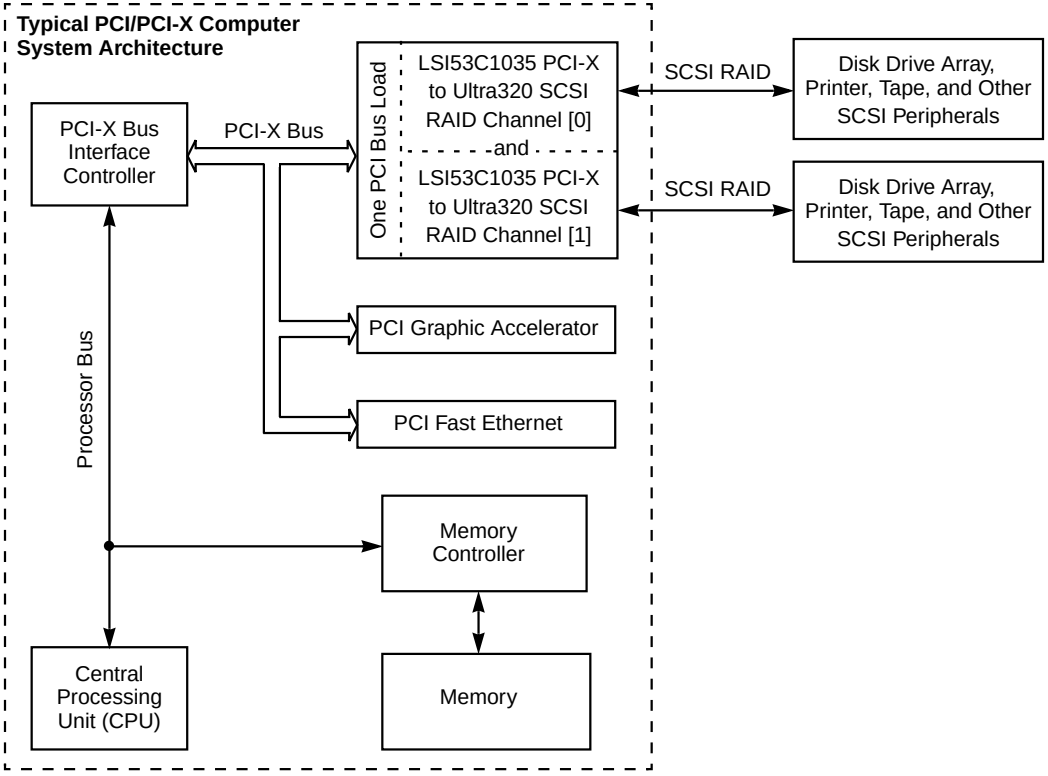


Figure 1.2 illustrates a typical LSI53C1035 system application.

Figure 1.2 Typical LSI53C1035 System Application



1.2 Benefits of the Fusion-MPT Architecture

The Fusion-MPT architecture provides an open architecture that is ideal for SCSI, Fibre Channel, and other emerging interfaces. The I/O interface is interchangeable at the system and application level; embedded software uses the same device interface for SCSI and Fibre Channel implementations just as application software uses the same storage management interfaces for SCSI and Fibre Channel implementations. LSI Logic provides Fusion-MPT device drivers that are binary-compatible between Fibre Channel and Ultra320 SCSI interfaces.

The Fusion-MPT architecture improves overall system performance by requiring only a thin device driver, which offloads the intensive work of managing SCSI I/Os from the system processor to the LSI53C1035. Developed from the proven SDMS™ solution, the Fusion-MPT architecture delivers unmatched performance of up to 100,000 Ultra320 SCSI I/Os per second with minimal system overhead or device maintenance. The use of thin, easy to develop, common OS device drivers accelerates time to market by reducing device driver development and certification times.

The Fusion-MPT architecture provides an interrupt coalescing feature. Interrupt coalescing allows an I/O controller to send multiple reply messages in a single interrupt to the host processor. Sending multiple reply messages per interrupt reduces context switching of the host processor and maximizes the host processor efficiency, which results in a significant improvement of system performance. To use the interrupt coalescing feature, the host processor must be able to accept and manage multiple replies per interrupt.

The Fusion-MPT architecture also provides built-in device driver stability because the device driver need not change for each revision of the LSI53C1035 silicon or firmware. This architecture is a reliable, constant interface between the host device driver and the LSI53C1035. Changes within the LSI53C1035 are transparent to the host device driver, operating system, and user. The Fusion-MPT architecture also saves the user significant development and maintenance effort because it is not necessary to alter or redevelop the device driver when a revision of the LSI53C1035 device or firmware occurs.

1.3 Benefits of RAID

RAID systems increase system performance by striping data across multiple disks. Striping data reduces disk access time because separate disks simultaneously read or write data. RAID systems provide fault tolerance by backing up data with either data mirroring or a parity block. The LSI53C1035 supports RAID 0, 1, 5, and 10. For systems that require fault tolerance, the LSI53C1035 supports RAID configurations that enable either data mirroring or parity-assisted data backup. Either method allows the user to recover lost data in the event of a disk failure. The LSI53C1035 allows users to select the data backup method that best suits their needs. A hardware RAID assist exclusive-OR (XOR) engine speeds parity generation and checking and reduces system access times. Section 2.3, “RAID Systems Functional Description,” on page 2-12 provides detailed information on LSI53C1035 RAID configurations.

The LSI53C1035 provides a high speed DDR SDRAM interface that further boosts system performance by providing a 64-bit, dedicated memory bus to support RAID activities. The DDR SDRAM enables the LSI53C1035 to receive or send RAID data even when the SCSI channel, PCI bus, storage device, or host device is busy.

The LSI53C1035 is an easy and reliable upgrade path from Ultra320 SCSI to Ultra320 SCSI RAID. Simply download and install firmware, change a RAID configuration pin pull-up option, and add memory for the DDR SDRAM interface to complete the upgrade. Refer to the RAIDMODE/ pin description in Section 3.2, “System Signals,” on page 3-5 for details.

1.4 Benefits of the Integrated RAID Solution

The Integrated RAID solution includes:

- Integrated Mirroring (IM) technology, which provides the features of RAID 1 and RAID 1E
- Integrated Striping (IS) technology, which provides the features of RAID 0

The LSI53C1035 supports the Integrated RAID solution when the chip operates in the conventional SCSI mode (LSI53C1030-compatible mode). The LSI Logic CIM interface software continuously monitors the IM volumes and IS volumes, and reports status and error conditions. The IM and IS solutions are supported by different versions of the Fusion-MPT firmware. Therefore, a system with a Fusion-MPT based controller can use either IM technology or IS technology, but cannot use IM technology and IS technology concurrently.

The IM feature provides simultaneous mirroring on configurations of two to six disks to assure fault tolerant, high availability data. If a disk fails, the hot swap capability allows the system to be easily restored by simply swapping disks. The system then automatically remirrors the swapped disk. Additionally, the hot spare feature keeps one disk ready to automatically replace a failed disk in the volume, making the system even more fault-tolerant.

The IM feature uses the same device drivers as the standard Fusion-MPT based controllers, providing seamless and transparent fault tolerance. The IM feature operates independently from the operating system, to conserve system resources. The BIOS-based configuration utility makes it easy to configure a mirrored volume. The LSI Logic Fusion-MPT firmware writes to the boot drive and the mirrored drive. The runtime mirroring of the boot drive is transparent to the BIOS, drivers, and operating system.

The Integrated Striping (IS) feature targets applications that require the faster performance and increased storage capacity of striping. A single IS logical drive may be configured as the boot disk or as a data disk.

The IS feature uses host adapter firmware that supports the Fusion-MPT interface. IS provides improved performance and increased capacity compared to individual SCSI disks without burdening the host CPU. The

firmware splits host I/Os over multiple disks and presents the disks as a single logical drive. Striping is transparent to the BIOS, drivers, and operating system.

The Fusion-MPT BIOS Configuration Utility (CU) configures the IS volume, which can use from two to six disks. The BIOS and drivers support SCSI Domain Validation to the physical member disks associated with a striped logical drive.

1.5 Benefits of PCI-X

PCI-X doubles the maximum clock frequency of the conventional PCI bus. The *PCI-X Addendum* to the *PCI Local Bus Specification, Revision 1.0a*, defines enhancements to the proven *PCI Local Bus Specification, Revision 2.2.* PCI-X provides more efficient data transfers by enabling registered inputs and outputs, improves buffer management by including transaction information with each data transfer, and reduces bus overhead by restricting the use of wait states and disconnects. PCI-X also reduces host processor overhead by providing a wide range of error recovery implementations.

The LSI53C1035 supports up to a 133 MHz, 64-bit PCI-X bus and is backwards-compatible with previous versions of the PCI/PCI-X specification. When operating in conventional SCSI mode, the LSI53C1035 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1035 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] allow independent control of the two PCI functions. When operating in RAID mode, the LSI53C1035 is a single function PCI/PCI-X controller.

According to the PCI-X addendum, the LSI53C1035 includes transaction information with all PCI-X transactions to enable more efficient buffer management schemes. Each PCI-X transaction contains a transaction sequence identifier (Tag), the identity of the initiator, and the number of bytes in the sequence. The LSI53C1035 clocks PCI-X data directly into and out of registers, which creates a more efficient data path. The LSI53C1035 increases bus efficiency because it does not insert wait states after the initial data phase when acting as a PCI-X target and never inserts wait states when acting as a PCI-X initiator.

1.6 Benefits of Ultra320 SCSI

The LSI53C1035 provides two Ultra320 SCSI RAID channels. Ultra320 SCSI is an extension of the SPI-4 draft specification that allows faster synchronous SCSI data transfer rates of up to 320 Mbytes/s. Ultra320 SCSI performs 160 megatransfers/s, resulting in approximately double the synchronous data transfer rates of Ultra160 SCSI. The LSI53C1035 performs 16-bit, Ultra320 SCSI synchronous data transfers as fast as 320 Mbytes/s on each SCSI channel.

Each Ultra320 SCSI channel supports double transition (DT) clocking, packetized protocol, paced transfers, quick arbitrate and select (QAS), skew compensation, intersymbol interference (ISI) compensation, cyclic redundancy check (CRC), and SureLINK™ domain validation technology. These features not only ensure the Ultra320 SCSI data transfer rates, but also provide end-to-end Ultra320 SCSI I/O data protection.

DT clocking enables the LSI53C1035 to achieve data transfer rates of up to 320 Mbytes/s on each SCSI channel, for a total bandwidth of 640 Mbytes/s on both SCSI channels. Packetized protocol increases data transfer capabilities with SCSI information units. QAS minimizes SCSI bus latency by allowing the bus to directly enter the arbitration/selection bus phase after a SCSI disconnect and skip the bus free phase. Skew compensation permits the LSI53C1035 to adjust for cable and bus skew on a per-device basis. Paced transfers enable high speed data transfers during DT data phases by using the REQ/ACK transition as a free-running data clock. Precompensation enables the LSI53C1035 to adjust the signal drive strength to compensate for the charge present on the cable. CRC improves the SCSI data transmission integrity through enhanced detection of communication errors.

Due to the increased data and clock speeds, Ultra320 SCSI introduces skew compensation and ISI compensation. These new features simplify system design by resolving timing issues at the chip level. Skew compensation adjusts for timing differences between data and clock signals. ISI compensation enhances the first pulse after a change in state to ensure data integrity.

1.7 Benefits of SureLINK Domain Validation

SureLINK domain validation detects the SCSI bus configuration and adjusts the SCSI transfer rate to optimize bus interoperability and SCSI data transfer rates.

SureLINK domain validation software ensures robust SCSI interconnect management and low risk Ultra320 SCSI implementations by extending the domain validation guidelines documented in the SPI-4 specifications. Domain validation verifies that the system is capable of transferring data at Ultra320 SCSI speeds, allowing the LSI53C1035 to renegotiate to a lower data transfer speed and bus width if necessary. SureLINK domain validation provides the software control for the domain validation manageability enhancements in the LSI53C1035. SureLINK domain validation software provides domain validation management at boot time as well as during system operation.

SureLINK domain validation ensures robust system operation by providing three levels of integrity checking on a per-device basis: Basic (Level 1) with inquiry command; Enhanced (Level 2) with read/write buffer; and Margined (Level 3) with margining of drive strength and slew rates. Section 2.5.1.8, “SureLINK Domain Validation,” on page 2-31 provides details.

1.8 Benefits of LVDlink™ Technology

The LSI53C1035 supports Low Voltage Differential (LVD) SCSI through LVDlink technology. This signaling technology increases the reliability of SCSI data transfers over longer distances than those that the SE (Single-Ended) SCSI supports. The low current output of LVD enables integration of the I/O transceivers directly onto the chip. To allow the use of the LSI53C1035 in both legacy and Ultra320 SCSI applications, the LSI53C1035 features universal LVDlink transceivers that support LVD SCSI and SE SCSI.

1.9 Benefits of TolerANT® Technology

The LSI53C1035 features TolerANT technology, which provides active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven HIGH rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments where data could be subject to corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps ensure correct data clocking. TolerANT input signal filtering is a built-in feature of the LSI53C1035 and all LSI Logic Fast SCSI, Ultra SCSI, Ultra2 SCSI, Ultra160 SCSI, and Ultra320 SCSI devices.

TolerANT technology increases noise immunity, balances duty cycles, and improves SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, which protects other devices on the bus from data corruption. When used with LVDlink transceivers, TolerANT technology provides excellent signal quality and data reliability in real world cabling environments. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.10 Summary of LSI53C1035 Features

This section provides a summary of the LSI53C1035 features. It contains information on SCSI RAID Features, Ultra320 SCSI Features, PCI Performance, Integration, Flexibility, Reliability, and Testability.

1.10.1 SCSI RAID Features

The LSI53C1035 offers these RAID features:

- Offers a high level of system integration with the patented RAID on a Chip (ROC) architecture
- Provides a cost-effective RAID solution
- Supports RAID levels 0, 1, 5, and 10
- Provides an Exclusive-OR Hardware RAID Parity Assist Engine to speed parity backup and recovery calculations
- Supports a high-speed DDR SDRAM with Error Correcting Code (ECC)
- Supports the Integrated RAID solution when operating in the LSI53C1030 mode, which includes:
  - Integrated Mirroring (IM) technology, which provides the features of RAID 1 and RAID 1E
  - Integrated Striping (IS) technology, which provides the features of RAID 0

1.10.2 Ultra320 SCSI Features

The LSI53C1035 offers these Ultra320 SCSI features:

- Supports Ultra320 SCSI
  - 320 Mbyte/s data transfer rate on each SCSI channel
  - Paced transfers using a free running clock
  - Mandatory packetized protocol
  - Quick arbitrate and select (QAS)
  - Skew compensation with bus training

  - Transmitter precompensation to overcome the ISI effects for SCSI data signals
  - Retained training information (RTI)
- Offers a performance optimized architecture
- Dedicated ARM966E-S™ processors manage each SCSI channel, providing high performance with low latency
- Two independent Ultra320 SCSI channels
- Designed for optimal packetized performance
- Uses proven integrated LVDlink transceivers for direct attach to either LVD or SE SCSI buses with precision-controlled slew rates
- Expander communication protocol (ECP)
- Uses the Fusion-MPT (Message Passing Technology) drivers to provide full support for the Windows, Linux, Solaris, SCO OpenServer, UnixWare, OpenUnix 8, and NetWare operating systems

1.10.3 PCI Performance

The LSI53C1035 supports these PCI features:

- A 133 MHz, 64-bit PCI/PCI-X interface that:
  - Operates at up to 133 MHz PCI-X
  - Operates at 33 MHz or 66 MHz PCI
  - Supports 32-bit or 64-bit data
  - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
  - Provides a theoretical 1066 Mbyte/s zero wait state transfer rate
  - Complies with the *PCI Local Bus Specification, Revision 2.2*
  - Complies with the *PCI-X Addendum* to the *PCI Local Bus Specification, Revision 1.0a*
  - Complies with *PCI Bus Power Management Interface Specification, Revision 1.1*
  - Complies with *PC2001 System Design Guide*
- Offers unmatched performance through the Fusion-MPT architecture

- Provides high throughput and low CPU utilization to offload the host processor
- Uses a dedicated ARM946E processor with additional instruction and data cache to manage host side interactions
- Presents a single electrical load to the PCI Bus
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands
- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, and Memory Write Block commands
- Supports up to eight PCI-X outstanding split transactions
- Supports Message Signaled Interrupts (MSI)

1.10.4 Integration

These features make the LSI53C1035 easy to integrate:

- Single chip integrates full PCI RAID capability
- Backwards-compatible with previous revisions of the PCI and SCSI specifications
- Full 32-bit or 64-bit PCI/PCI-X DMA bus master
- Reduces time to market with the Fusion-MPT architecture
  - Single, binary driver for SCSI and Fibre Channel devices
  - Thin, easy to develop drivers
  - Reduced integration and certification effort
- Integrated LVDlink transceivers

1.10.5 Flexibility

These features increase the flexibility of the LSI53C1035:

- Universal LVD transceivers are backward compatible with SE devices
- Flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Supports MSI or pin-based (INTx/) interrupt signaling
- Capable of responding with multiple SCSI IDs
- External memory interface provides connections to a Flash ROM, NVSRAM, or general purpose memory
- Serial EEPROM enables storage and programming of the PCI Configuration space
- ISTWI provides support for peripheral devices
- Compatible with 3.3 V and 5.0 V PCI signaling
  - Drives and receives 3.3 V PCI signals
  - Receives 5.0 V PCI if the PCI5VBIAS pin connects to 5 V, but does not drive 5.0 V signals on the PCI bus

1.10.6 Reliability

These features enhance the reliability of the LSI53C1035:

- ISI compensation
- 2 kV ESD protection on SCSI signals
- Latch-up protection greater than 150 mA
- Voltage feed-through protection
- LSI Logic Integrated Mirroring (IM) technology provides physical mirroring of the boot volume
- High proportion of power and ground pins
- Power and ground isolation of I/O pads and internal chip logic
- Supports CRC checking and generation in DT phases

- Comprehensive SureLINK domain validation technology:
  - Basic (Level 1) with inquiry command
  - Enhanced (Level 2) with read/write buffer
  - Margined (Level 3) with margining of drive strength and slew rates
- TolerANT technology provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved SCSI transfer rates
  - Input signal filtering on SCSI receivers improves data integrity, even in noisy cabling environments

1.10.7 Testability

These features enhance the testability of the LSI53C1035:

- All the SCSI signals are accessible through programmed I/O
- JTAG boundary scan
- ARM® Multi-ICE® technology for debugging purposes
- A UART interface improves debugging capabilities

Chapter 2
Functional Description

This chapter provides an overview of the LSI53C1035, a discussion of the Fusion-MPT architecture, and a functional description of the LSI53C1035 interfaces. This chapter contains the following sections:

The LSI53C1035 is a high performance, intelligent PCI-X to Dual Channel Ultra320 SCSI RAID Controller. The LSI53C1035 supports Revision 2.2 of the *PCI Local Bus Specification*, Revision 1.0a of the *PCI-X Addendum* to the *PCI Local Bus Specification*, and the proposed *SCSI Parallel Interface-4* (SPI-4) draft standard.

The user can configure the LSI53C1035 to one of two modes. In one mode, the LSI53C1035 is a single function PCI-X to dual channel SCSI RAID controller. This mode is referred to as RAID mode. In the other mode, the LSI53C1035 is a multifunction PCI-X to dual channel Ultra320 SCSI controller. This mode is referred to as non-RAID mode or LSI53C1030-compatible mode. Each mode requires different firmware, which can be obtained from LSI Logic. The Device ID, Class Code, and Header Type are different in each mode.

The LSI53C1035 employs the Fusion-MPT architecture to ensure robust system performance, to support binary compatibility of host software between the LSI Logic SCSI and Fibre Channel products, and to reduce software development time significantly. Refer to the *Fusion-MPT Device Management User's Guide,* for details on the Fusion-MPT architecture operating system support.

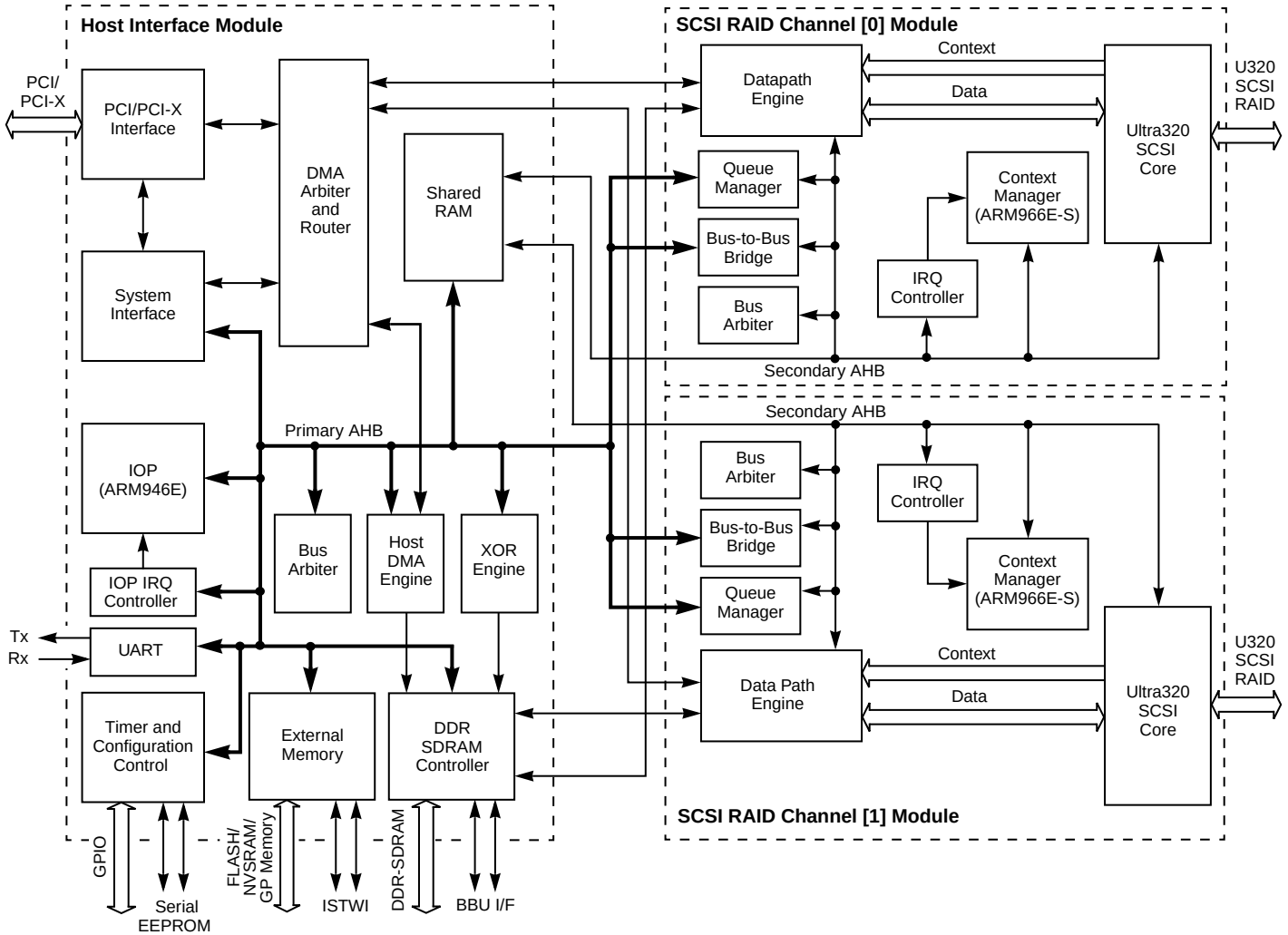
2.1 Block Diagram Description

The LSI53C1035 consists of three main modules: a host interface module and two independent Ultra320 SCSI channel modules. Figure 2.1 illustrates the relationship between these modules. The modules consist of the following components:

- A Host Interface Module that contains:
  - 64-bit, 133 MHz PCI/PCI-X Interface
  - System Interface
  - I/O Processor (IOP)
  - DMA Arbiter and Router
  - Shared RAM
  - Timer and Configuration Control
    - ◊ Serial EEPROM Interface Controller
    - ◊ GPIO Interface
    - ◊ Chip Timer
  - UART
  - IOP Interrupt Request Controller (IRQ)
  - External Memory Controller
    - ◊ Flash ROM/NVSRAM/General Purpose (GP) Memory
    - ◊ ISTWI
  - Host DMA Engine
  - XOR Engine
  - DDR SDRAM Controller

- Two independent Ultra320 SCSI Channel Modules that contain:
  - Queue Manager
  - Ultra320 SCSI Core
  - Datapath Engine
  - Context Manager
  - IRQ Controller

Figure 2.1 LSI53C1035 Block Diagram



2.1.1 Host Interface Module Description

The host interface module provides an interface between the host driver and the two SCSI channels. The host interface module controls system DMA transfers and the host side of the Fusion-MPT architecture. The host interface module controls RAID access to each SCSI channel.

The host interface module also supports the DDR SDRAM, NVSRAM, Flash ROM, GP Memory, Serial EEPROM, UART, and General Purpose I/O (GPIO) interfaces. This subsection explains the host interface submodules in detail.

2.1.1.1 PCI/PCI-X Interface

The LSI53C1035 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. The interface is compatible with all previous implementations of the PCI specification. For details on the PCI interface, refer to Section 2.4, “PCI Functional Description,” on page 2-16.

2.1.1.2 System Interface

The system interface efficiently passes messages between the LSI53C1035 and other I/O agents using a high-performance, packetized, mailbox architecture. The system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance.

All host accesses to the LSI53C1035 and its supported subsystems pass through the system interface and use the primary bus. The host system initiates data transactions on the primary bus with the system interface registers. PCI Memory Space [0] and the PCI I/O Base Address registers identify the location of the system interface register set. Chapter 4, “PCI Host Register Description”, provides a bit-level description of the system interface register set.

2.1.1.3 I/O Processor (IOP)

The LSI53C1035 IOP is an ARM946E RISC processor. The ARM946E processor has a 16 Kbyte data cache and a 16 Kbyte instruction cache that provide an extra performance boost to host side interactions. The IOP controls the system interface and uses the Fusion-MPT architecture to manage the host side of non-DMA accesses to the Ultra320 SCSI bus. The context manager uses the Fusion-MPT architecture to control the

SCSI side of data transfers. The IOP, Context Manager, XOR Engine, and DDR SDRAM controller completely manage all SCSI RAID I/Os without host intervention. Refer to Section 2.2, "Fusion-MPT Overview," for details on the Fusion-MPT architecture.

2.1.1.4 DMA Arbiter and Router

The descriptor based DMA Arbiter and Router subsystem manages the transfer of memory blocks between local memory and the host system. The DMA channel includes PCI bus master interface logic, the internal bus interface logic, and a 256-byte system DMA FIFO.

2.1.1.5 Shared RAM

The shared RAM is a 128 Kbyte memory that is contained in the host interface module but shared between the host interface module and the SCSI channel modules. Both the Primary and Secondary Advanced High-Performance Buses (AHBs) can access the shared RAM. The shared RAM holds a portion of the IOP and context manager firmware, as well as the request message queue and reply message queue. All non-DMA data transfers that use the request and reply message queues pass through the shared RAM.

2.1.1.6 Timer, Serial EEPROM, and GPIO

A 32-bit free-running timer allows firmware time-stamping of events for tracking and managing SCSI I/Os. The LSI53C1035 provides a maskable timer interrupt that continuously increments at 1-microsecond intervals.

A 2-wire serial EEPROM interface connects to nonvolatile storage of both the hardware configuration and the firmware configuration. A checksum byte confirms the download of the parameters held in the serial EEPROM. The serial EEPROM enables programming of the Subsystem ID(s), Subsystem Vendor ID(s), Device ID(s), Revision ID(s), Class Code(s), and the sizes of the PCI Memory Spaces [0] and [1]. This feature enables the firmware or the serial EEPROM reader to initialize these PCI Configuration registers prior to PCI configuration.

The LSI53C1035 provides eight GPIO signals (GPIO[7:0]). These signals are under the control of the LSI53C1035 and default to the input mode upon PCI reset.

The LSI53C1035 provides three LED signals: A_LED/, B_LED/, and HB_LED/. Either firmware or hardware can control A_LED/ and B_LED/. The LSI53C1035 firmware controls HB_LED/ (heartbeat LED), which indicates that the IOP is operational.

2.1.1.7 UART

An industry standard UART supports debugging of the LSI53C1035. The UART performs serial-to-parallel conversion of data characters received from a peripheral device such as a modem, and performs parallel-to-serial conversion on data characters received from the host processor. The UART is compatible with a standard 16550 UART, except for the following items:

- Does not support 5-bit and 6-bit characters.
- Does not provide support for 1.5 stop bits.
- Provides a synchronous interface to allow access to internal LSI53C1035 registers and FIFOs.
- Speedsense logic determines the speed of the connected modem.

2.1.1.8 IOP IRQ Controller

The IOP IRQ controller provides interrupt source mapping from IOP interrupt sources to the IOP ARM FIQ\ and IRQ\ input pins. The IOP IRQ controller supports 24–32 interrupt sources. The IOP IRQ controller provides independent master interrupt enables for each of the interrupt sources.

2.1.1.9 External Memory Controller

The external memory controller block provides an 8-bit external memory interface, an industry standard 2-wire serial interface (ISTWI), and an external reset output. Section 2.6, “External Memory Interface,” on page 2-33 provides a detailed discussion of the external memory interfaces. Section 3.5, “Memory Interface,” on page 3-16 provides signal descriptions for the external memory controller.

8-Bit External Memory Interface – This block provides a direct 8-bit interface between the internal system bus and the external memory. Control signals, an address bus, and a data bus compose this memory interface. This interface supports a Flash ROM, an NVSRAM, and a GP memory.

ISTWI – The LSI53C1035 contains an ISTWI bus that communicates with peripherals, such as EEPROM memories. The ISTWI block operates as either a master or a slave, and sustains data rates of up to 400 Kbits/s. The ITSWI block accomplishes byte-wise bidirectional data transfers by using either an interrupt or a polling handshake at the completion of each byte. The style and operation of this interface closely follows the de facto standard for a two-wire serial interface chip. The ISTWI block controls all bus timing and performs bus-specific sequences.

External Reset Pin – The LSI53C1035 provides an external reset pin that supports the RAID subsystem reset functionality. The external reset pin follows the PCI_RST/ input and can optionally mask an incoming PCI_RST/. Software can also assert or deassert this pin.

2.1.1.10 Host DMA Engine

The host DMA engine moves data between system memory and the local DDR SDRAM controller. The host DMA channel provides higher degrees of concurrency within the I/O flow, which improves the overall system performance.

2.1.1.11 XOR Engine

The XOR engine calculates parity in chip hardware to implement RAID level 5. The XOR engine operates from a control structure format and consists of the controller, control structure memory, and intermediate data path memory. A command set provides the programming structures to autonomously perform exclusive-OR parity generation and checking on multiple blocks of data. The external memory holds the data blocks, which the DDR SDRAM controller then can access. The IOP programs the control structure.

When programmed, the XOR engine automatically fetches blocks of data from the DDR memory, performs an XOR parity generation or check, and writes the generated parity data blocks back into the DDR SDRAM controller. To support multithreaded data systems, the XOR engine supports queueing of multiple operations.

2.1.1.12 DDR SDRAM Controller

The DDR SDRAM controller supports a dedicated high-performance memory interface for DDR SDRAM memories. This interface provides a 64-bit external data bus with 8-bit ECC handling, a 13-bit address bus, memory bank address signals, and write data mask signals. The DDR SDRAM controller supports up to 256 Mbytes of DDR SDRAM. DDR_CS0/ selects the external DDR SDRAM bank, which may contain up to four internal DDR SDRAM banks. BA_ADDR[1:0] select the internal bank within the external bank.

A fixed priority, timed, or round robin arbiter controls access to the AHB bus segments. The ECC capabilities include 72 ECC algorithms, single bit error correction, and multiple bit error detection. Firmware initializes the DDR SDRAM.

The DDR SDRAM provides a local, high-speed memory that streamlines RAID functionality. The LSI53C1035 uses the DDR SDRAM to queue and track accesses to RAID memory. The DDR SDRAM also holds RAID data blocks on which the XOR engine generates and checks parity.

The BBU interface provides a two-wire connection to a battery backup unit for the DDR SDRAM controller. The LSI53C1035 asserts the BBU_PFC signal to indicate that the DDR SDRAM has been placed in the self-refresh mode due to power failure.

2.1.2 AHB Bus System

The LSI53C1035 employs an internal system of three AHB buses. Each ARM9 processor interfaces with a dedicated segment of the AHB bus. The AHB bus segment dedicated to the IOP is the primary (or system) bus, while the AHB bus segments dedicated to the SCSI channel context managers are secondary (or channel) buses. Each SCSI channel module contains a bus-to-bus bridge and a bus arbiter. The bus-to-bus bridges connect the secondary bus segment to the primary bus segment.

A round robin arbitration scheme controls access to the AHB bus. When no other bus masters control the bus, the LSI53C1035 parks the bus on the primary bus by default. This minimizes latency when the IOP requests read/write operations.

2.1.3 SCSI Channel Module Description

The SCSI channel modules independently control the SCSI channels. There are two identical SCSI channel modules: SCSI Channel [0] and SCSI Channel [1]. Both channels support either the Ultra320 SCSI RAID interface or a conventional Ultra320 SCSI bus. This section describes the components of the SCSI channel modules.

2.1.3.1 Queue Manager

The queue manager facilitates process synchronization between the IOP and the context manager. The queue manager coordinates the outbound I/O management, resource allocation for target mode I/Os, completion reporting of I/Os, and message passing between the IOP and context manager.

2.1.3.2 Ultra320 SCSI Cores

The Ultra320 SCSI cores control the LSI53C1035 Ultra320 SCSI bus interfaces. A separate Ultra320 SCSI core exists for each SCSI bus. The LSI53C1035 supports the LVD and SE bus modes and 3-states the SCSI bus if it detects an HVD signal. The LSI53C1035 implements CRC, Domain Validation, DT clocking, QAS, skew controls, ISI compensation, paced transfers, and packetized transfers. These features ensure compliance with the ANSI SCSI Parallel Interface-4 (SPI-4) draft specification.

2.1.3.3 Data Path Engines

The data path engine manages the SCSI side of DMA transactions between the SCSI bus and the host system. A separate data path engine is present for each SCSI channel.

2.1.3.4 Context Managers

The context manager is a 32-bit, ARM966E-S RISC processor. A separate context manager exists on each SCSI channel. The context manager controls the configuration record processing, outbound queue processing, target mode I/O mapping, disconnect and reselect sequences, send/receive scatter/gather lists, and status reports.

2.1.3.5 Interrupt Request (IRQ) Controller

The IRQ controller provides interrupt source mapping from the context manager interrupt sources to the context manager ARM processor FIQ\ and IRQ\ input pins. The context manager interrupt controller is not a full interrupt controller; it simply maps the interrupt sources to either the FIQ\ or IRQ\ pins, and the associated status registers. The IRQ controller provides independent master interrupt enables for each of the interrupt sources.

2.2 Fusion-MPT Overview

The Fusion-MPT architecture provides two I/O methods for the host system to communicate with the IOP: the system interface doorbell and the message queues.

The system interface doorbell is a simple message passing mechanism that allows the host system and IOP to exchange single 32-bit dword messages. When the host system writes to the doorbell, the LSI53C1035 hardware generates a maskable interrupt to the IOP, which then can read the doorbell value and take the appropriate action. When the IOP writes a value to the doorbell, the LSI53C1035 hardware generates a maskable interrupt to the host system. The host system then can read the doorbell value and take the appropriate action.

There are two 32-bit message queues: the request message queue and the reply message queue. The host uses the request message queue to request an action by the LSI53C1035, and the LSI53C1035 uses the reply message queue to return status information to the host. The request message queue consists of only the request post FIFO. The reply message queue consists of both the reply post FIFO and the reply free FIFO. The shared RAM contains the message queues.

Communication using the message queues occurs through request messages and reply messages. Request message frame descriptors are pointers to the request message frames and are passed through the request post FIFO. The request message frame data structure is up to 128 bytes in length and includes a message header and a payload. The header uniquely identifies the message. The payload contains information that is specific to the request. Reply message frame descriptors have one of two formats and are passed through the reply

post FIFO. When indicating the successful completion of a SCSI I/O, the IOP writes the reply message frame descriptor using the Context Reply format, which is a message context. If a SCSI I/O does not complete successfully, the IOP uses the Address Reply format. In this case, the IOP pops a reply message frame from the reply free FIFO, generates a reply message describing the error, writes the reply message to system memory, and writes the address of the reply message frame to the reply post FIFO. The host then can read the reply message and take the appropriate action.

The doorbell mechanism provides both a high-priority communication path that interrupts the host system device driver and an alternative communication path to the message queues. Because data transport through the system doorbell occurs a single dword at a time, use the LSI53C1035 message queues for normal operation and data transport.

2.3 RAID Systems Functional Description

RAID systems increase system performance by striping data across multiple disks and provide fault tolerance through either data mirroring or parity data. RAID systems can also increase the overall storage capacity of a system through disk spanning.

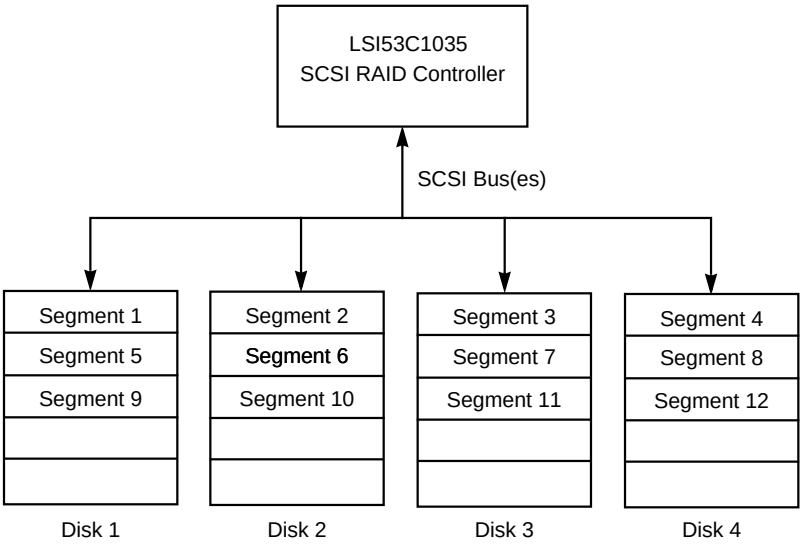
RAID Levels – The LSI53C1035 supports RAID 0, RAID 1, RAID 5, and RAID 10 over each SCSI channel. The following descriptions provide a system-level explanation of the LSI53C1035 implementation of these RAID levels. The LSI53C1035 supports up to 15 physical disks on each SCSI channel, which allows up to 30 physical disks in a single disk array.

LSI53C1035 RAID 0 Description: In a RAID 0 system, the LSI53C1035 stripes data across an array of physical disks. A RAID 0 configuration maximizes the data throughput of the system but does not provide data redundancy. If a disk fails, all the data is lost. Figure 2.2 provides an example of a RAID 0 implementation using a disk array with four disks.

When striping data, the LSI53C1035 RAID controller breaks larger data blocks into smaller data segments and writes each segment to a disk in a repeated, sequential pattern. The stripe width is the number of disks in the disk array. The stripe width in this array is 4. The stripe size is the size, in Kbytes, of the data stripe that the controller writes across the disk array.

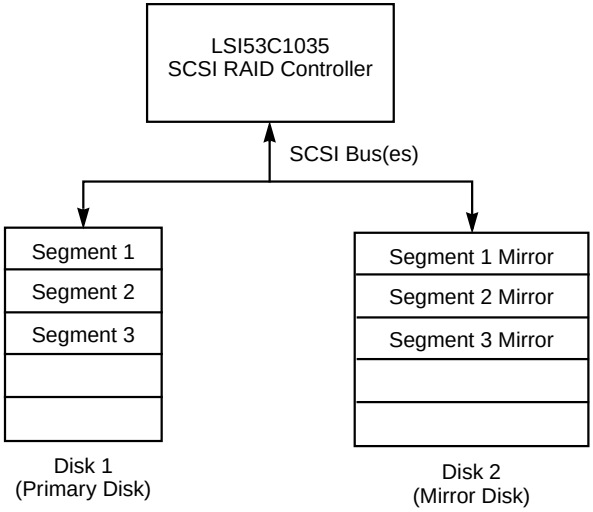
System performance dramatically improves in RAID striping systems because multiple disk heads access the disks simultaneously. A RAID striping system is best suited for systems using large files that do not require data redundancy.

Figure 2.2 RAID 0 Implementation



LSI53C1035 RAID 1 Description: In a RAID 1 configuration, the LSI53C1035 uses disk mirroring to provide bit-for-bit data backup. When the LSI53C1035 writes data to one disk, it simultaneously writes data to a second, mirror disk. The LSI53C1035 writes one set of data to a mirror disk over one SCSI channel and writes the other over the second SCSI channel, or the LSI53C1035 performs a second write to the redundant disk over the same SCSI channel. The backup data is immediately available in the event of a disk failure. Figure 2.3 provides an example of a RAID 1 implementation.

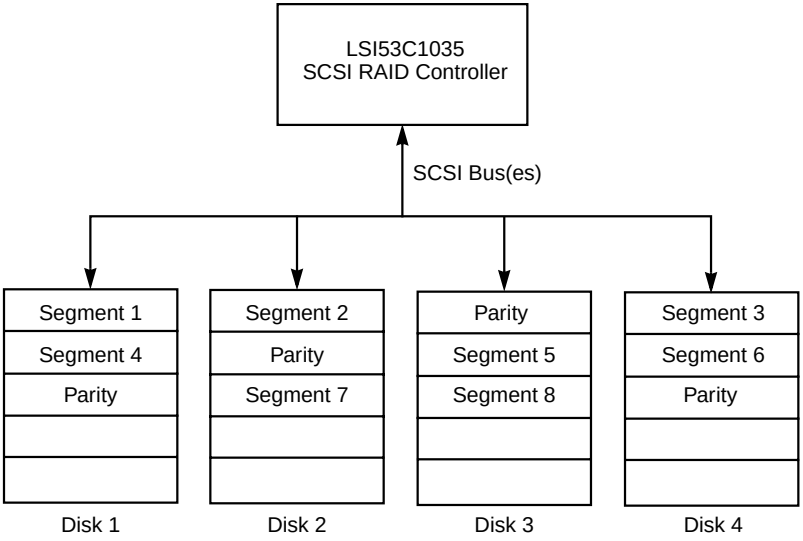
Figure 2.3 RAID 1 Implementation



LSI53C1035 RAID 5 Description: In a RAID 5 configuration, the LSI53C1035 writes a data stripe across multiple disk drives, calculates a parity block for the data stripe, and writes the parity block to the disk array at the end of the data stripe. RAID 5 configurations do not use a dedicated parity disk.

The parity block provides data redundancy without the use of a mirror disk and allows full data recovery in the event of a disk failure. The parity block is based on an XOR of the data blocks written in the data stripe. The LSI53C1035 uses a hardware-based XOR engine and a high-speed DDR SDRAM interface to speed the parity calculation. In the event of a disk failure, the LSI53C1035 uses the parity data to rebuild the data held on the failed disk. RAID 5 configurations also increase performance because the multiple disk heads can access data simultaneously. Figure 2.4 provides an example of a RAID 5 implementation that has a stripe width of 2.

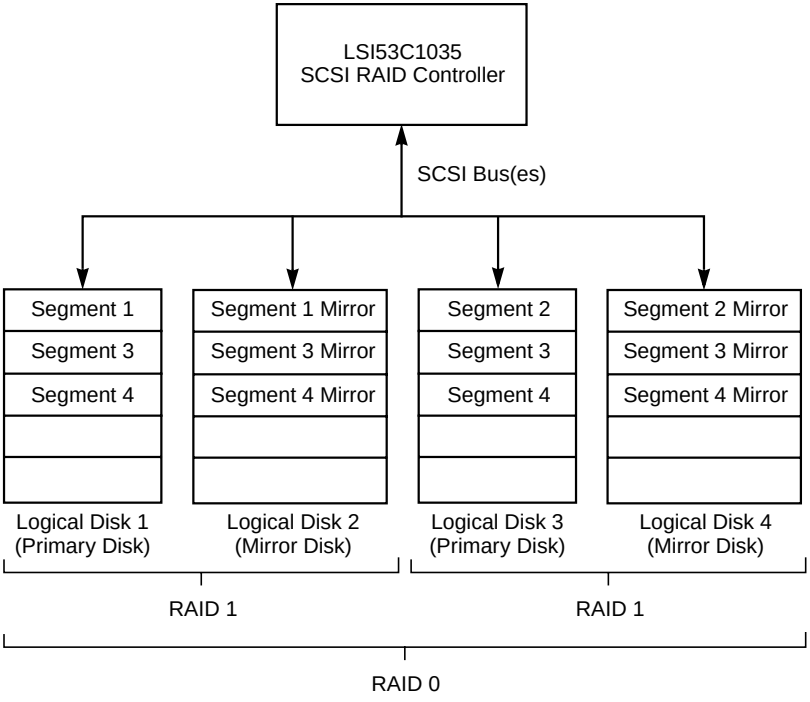
Figure 2.4 RAID 5 Configuration



LSI53C1035 RAID 10 Description: A RAID 10 configuration combines RAID 0 disk mirroring and RAID 1 disk striping to provide both the performance increase of a RAID striping and the data redundancy of RAID mirroring. In a RAID 10 configuration, logical disks are arranged in a RAID 1 disk mirroring configuration. Then, the mirrored logical disk sets are arranged in a disk striping configuration. The LSI53C1035 mirrors data within the mirroring disk sets and stripes data across the mirror disk sets. Figure 2.5 provides an example of a RAID 10 configuration.

In a RAID 10 system, data is not lost when a disk fails; the mirror disk holds a backup copy of every bit. A parity calculation is not necessary, and the backup data is immediately available in the event of a disk failure. The storage capacity of the system is one-half of the physical disk capacity.

Figure 2.5 RAID 10 Configuration



2.4 PCI Functional Description

The host PCI interface complies with the *PCI Local Bus Specification Revision 2.2* and the *PCI-X Addendum* to the *PCI Local Bus Specification, Revision 1.0a*. The LSI53C1035 supports up to a 133 MHz, 64-bit PCI-X bus. The LSI53C1035 provides support for 64-bit addressing with Dual Address Cycles (DAC).

The LSI53C1035 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1035 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] enable independent control of the two PCI functions.

2.4.1 PCI Addressing

The three physical address spaces the PCI specification defines are:

- PCI Configuration Space
- PCI I/O Space
- PCI Memory Space

The following subsections describe the PCI address spaces.

2.4.1.1 PCI Configuration Space

The LSI53C1035 defines an independent set of PCI Configuration Space registers for each PCI function. Each configuration space is a contiguous 256-x-8-bit set of addresses. The system BIOS initializes the configuration registers using PCI configuration cycles. The LSI53C1035 decodes C_BE[3:0]/ to determine whether a PCI cycle intends to access the configuration register space. The IDSEL signal behaves as a chip select signal that enables access to the configuration register space only. The LSI53C1035 ignores configuration read/write cycles when IDSEL is not asserted.

Because the LSI53C1035 is a multifunction PCI device, bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1035 does not respond to any other encodings of AD[10:8]. Bits AD[7:2] select one of the 64 dword registers in the device's PCI Configuration Space. Bits AD[1:0] determine whether the configuration command is a Type 0 Configuration Command (AD[1:0] = 0b00) or a Type 1 Configuration Command (AD[1:0] = 0b01). Because the LSI53C1035 is not a PCI Bridge device, all PCI Configuration Commands designated for the LSI53C1035 must be Type 0. C_BE[3:0]/ address the individual bytes within each dword and determine the type of access to perform.

2.4.1.2 PCI I/O Space

The PCI specification defines I/O Space as a contiguous, 32-bit I/O address that all system resources share, including the LSI53C1035. The I/O Base Address register determines the 256-byte PCI I/O area that the PCI device occupies.

2.4.1.3 PCI Memory Space

The LSI53C1035 contains two PCI memory spaces: PCI Memory Space [0] and PCI Memory Space [1]. PCI Memory Space [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. The LSI53C1035 requires 64 Kbytes of memory space.

The PCI specification defines memory space as a contiguous, 64-bit memory address that all system resources share. The Memory [0] Low and Memory [0] High registers determine which 64 Kbyte memory area PCI Memory Space [0] occupies. The Memory [1] Low and Memory [1] High registers determine which 64 Kbyte memory area PCI Memory Space [1] occupies.

2.4.2 PCI Bus Commands and Functions

Bus commands indicate to the target the type of transaction the master is requesting. The master encodes the bus commands on the C_BE[3:0]/ lines during the address phase. The PCI bus command encodings appear in Table 2.1.

Table 2.1 PCI/PCI-X Bus Commands and Encodings[1]

C_BE[3:0]/	PCI Command	PCI-X Command	Supports as Master	Supports as Slave
0b0000	Interrupt Acknowledge	Interrupt Acknowledge	No	No
0b0001	Special Cycle	Special Cycle	No	No
0b0010	I/O Read	I/O Read	Yes	Yes
0b0011	I/O Write	I/O Write	Yes	Yes
0b0100	Reserved	Reserved	N/A	N/A
0b0101	Reserved	Reserved	N/A	N/A
0b0110	Memory Read	Memory Read Dword	Yes	Yes
0b0111	Memory Write	Memory Write	Yes	Yes
0b1000	Reserved	Alias to Memory Read Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1001	Reserved	Alias to Memory Write Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1010	Configuration Read	Configuration Read	No	Yes
0b1011	Configuration Write	Configuration Write	No	Yes
0b1100	Memory Read Multiple	Split Completion	Yes	Yes[2]
0b1101	Dual Address Cycle	Dual Address Cycle	Yes	Yes
0b1110	Memory Read Line	Memory Read Block	Yes	Yes[2]
0b1111	Memory Write and Invalidate	Memory Write Block	Yes	Yes[3]

1. The LSI53C1035 ignores reserved commands as a slave and never generates them as a master.
2. When acting as a slave in the PCI mode, the LSI53C1035 supports this command as the PCI Memory Read command.
3. When acting as a slave in the PCI mode, the LSI53C1035 supports this command as the PCI Memory Write command.

The following subsections describe how the LSI53C1035 implements these commands.

2.4.2.1 Interrupt Acknowledge Command

The LSI53C1035 ignores this command as a slave and never generates it as a master.

2.4.2.2 Special Cycle Command

The LSI53C1035 ignores this command as a slave and never generates it as a master.

2.4.2.3 I/O Read Command

The I/O Read command reads data from an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1035 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1035 supports this command when operating in either the PCI bus mode or the PCI-X bus mode.

2.4.2.4 I/O Write Command

The I/O Write command writes data to an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1035 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1035 supports this command when operating in either the PCI bus mode or the PCI-X bus mode.

2.4.2.5 Memory Read Command

The LSI53C1035 uses the Memory Read command to read data from an agent mapped in the memory address space. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1035 supports this command when operating in the PCI bus mode.

2.4.2.6 Memory Read Dword Command

The Memory Read Dword command reads up to a single dword of data from an agent mapped in the memory address space. This command only can be initiated as a 32-bit transaction. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1035 supports this command when operating in the PCI-X bus mode.

2.4.2.7 Memory Write Command

The Memory Write command writes data to an agent mapped in the memory address space. The target assumes responsibility for data coherency when it returns “ready.” The LSI53C1035 supports this command when operating in either the PCI bus mode or the PCI-X bus mode.

2.4.2.8 Alias to Memory Read Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1035 never generates this command as a master. When a slave, the LSI53C1035 supports this command using the Memory Read Block command.

2.4.2.9 Alias to Memory Write Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1035 never generates this command as a master. When a slave, the LSI53C1035 supports this command using the Memory Write Block command.

2.4.2.10 Configuration Read Command

The Configuration Read command reads the configuration space of a device. The LSI53C1035 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1035 by asserting its IDSEL signal when AD[1:0] equals 0b00. During the address phase of a configuration cycle, AD[7:2] address one of the 64 dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each dword register and determine the type of access to perform. Bits AD[10:8] address either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1035 treats AD[63:11] as logical don’t cares.

2.4.2.11 Configuration Write Command

The Configuration Write command writes the configuration space of a device. The LSI53C1035 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1035 by asserting its IDSEL signal when bits AD[1:0] equals

0b00. During the address phase of a configuration cycle, AD[7:2] address one of the 64 dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each dword register and determine the type of access to perform. Bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1035 treats AD[63:11] as logical don't cares.

2.4.2.12 Memory Read Multiple Command

The Memory Read Multiple command is identical to the Memory Read command, except it additionally indicates that the master intends to fetch multiple cache lines before disconnecting. The LSI53C1035 supports PCI Memory Read Multiple functionality when operating in the PCI mode and determines when to issue a Memory Read Multiple command instead of a Memory Read command.

Burst Size Selection – The Read Multiple command reads multiple cache lines of data during a single bus ownership. The number of cache lines the LSI53C1035 reads is a multiple of the cache line size, which Revision 2.2 of the PCI specification provides. The LSI53C1035 selects the largest multiple of the cache line size based on the amount of data to transfer.

2.4.2.13 Split Completion Command

Split transactions in PCI-X replace the delayed transactions in conventional PCI. The LSI53C1035 supports up to eight outstanding split transactions when operating in the PCI-X mode. A split transaction consists of at least two separate bus transactions: a split request, which the requester initiates, and one or more split completion commands, which the completer initiates. Revision 1.0a of the PCI-X addendum permits split transaction completion for the Memory Read Block, Alias to Memory Read Block, Memory Read Dword, Interrupt Acknowledge, I/O Read, I/O Write, Configuration Read, and Configuration Write commands. When operating in the PCI-X mode, the LSI53C1035 supports the Split Completion command for all of these commands except the Interrupt Acknowledge command, which the LSI53C1035 neither responds to nor generates.

2.4.2.14 Dual Address Cycles (DAC) Command

The LSI53C1035 performs Dual Address Cycles (DAC), according to the PCI Local Bus Specification, Revision 2.2. The LSI53C1035 supports this command when operating in either the PCI bus mode or the PCI-X bus mode.

2.4.2.15 Memory Read Line Command

This command is identical to the Memory Read command except it additionally indicates that the master intends to fetch a complete cache line. The LSI53C1035 supports this command when operating in the PCI mode.

2.4.2.16 Memory Read Block Command

The LSI53C1035 uses this command to read from memory. The LSI53C1035 supports this command when operating in the PCI-X mode.

2.4.2.17 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except it additionally guarantees a minimum transfer of one complete cache line. The master uses this command when it intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register. The LSI53C1035 determines when to issue a Write and Invalidate command instead of a Memory Write command and supports this command when operating in the PCI bus mode.

Alignment – The LSI53C1035 uses the calculated line size value to determine whether the current address aligns to the cache line size. If the address does not align, the LSI53C1035 bursts data using a noncache command. If the starting address aligns, the LSI53C1035 issues a Memory Write and Invalidate command using the cache line size as the burst size.

Multiple Cache Line Transfers – The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The LSI53C1035 issues a burst transfer as soon as it reaches a cache line boundary. The PCI Local Bus specification states that the transfer size must be a multiple of the cache line size. The LSI53C1035

selects the largest multiple of the cache line size based on the transfer size. When the DMA buffer contains less data than the value Cache Line Size register specifies, the LSI53C1035 issues a Memory Write command on the next cache boundary to complete the data transfer.

2.4.2.18 Memory Write Block Command

The LSI53C1035 uses this command to burst data to memory. The LSI53C1035 supports this command when operating in the PCI-X bus mode.

2.4.3 PCI Bus Arbitration

The LSI53C1035 contains independent bus mastering functions for each of the SCSI functions and for the system interface. The system interface bus mastering function manages DMA operations as well as the request and reply message frames. The SCSI channel bus mastering functions manage data transfers across the SCSI channels.

The LSI53C1035 uses a single REQ/-GNT/ signal pair to arbitrate for access to the PCI bus. To ensure fair access to the PCI bus, the internal arbiter uses a round robin arbitration scheme to decide which of the three internal bus mastering functions can arbitrate for access to the PCI bus.

2.4.4 PCI Cache Mode

The LSI53C1035 supports an 8-bit Cache Line Size register. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. The LSI53C1035 determines when to issue a PCI cache command (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) or a PCI noncache command (Memory Read or Memory Write command).

2.4.5 PCI Interrupts

The LSI53C1035 signals an interrupt to the host processor either using PCI interrupt pins or using Message Signaled Interrupts (MSI). The Interrupt Pin register configures the routing of each PCI function's interrupt signals to either the INTA/ or INTB/ pin.

If using MSI, the LSI53C1035 does not signal interrupts on the interrupt pins. Each PCI function of the LSI53C1035 implements its own MSI register set. The LSI53C1035 supports one requested message and disables MSI after the chip powers-up or resets.

Note: Enabling MSI to mask PCI interrupts is a violation of the PCI specification.

The Host Interrupt Mask register also prevents the assertion of a PCI interrupt to the host processor by selectively masking reply interrupts and system doorbell interrupts. This register masks both pin-based and MSI-based interrupts.

2.4.6 Power Management

The LSI53C1035 complies with the *PCI Bus Power Management Interface Specification, Revision 1.1,* and the *PC2001 System Design Guide*. The LSI53C01035 supports the D0, D1, D2, $D3_{hot}$, and $D3_{cold}$ power states. D0 is the maximum power state, and D3 is the minimum power state. Power State D3 is further categorized as $D3_{hot}$ or $D3_{cold}$. Powering a function off places it in the $D3_{cold}$ power state.

Bits [1:0] of the Power Management Control/Status register independently control the power state of each PCI device on the LSI53C1035. Table 2.2 provides the power state bit settings.

Table 2.2 Power States

Power Management Control/Status Register, Bits [1:0]	Power State	Function
0b00	D0	Maximum Power
0b01	D1	Snooze Mode
0b10	D2	Coma Mode
0b11	D3	Minimum Power

The following sections describe the PCI Function Power States D0, D1, D2, and D3. When the device transitions from one power level to a lower one, the attributes that occur in the higher power state level carry into the lower power state level. For example, Power State D2 includes the attributes for Power State D1, as well as the attributes defined for

Power State D2. The following sections describe the PCI Function power states in conjunction with each SCSI function. Power state actions are separate for each SCSI function.

2.4.6.1 Power State D0

Power State D0 is the maximum power state and is the power-up default state for each function. The LSI53C1035 is fully functional in this state.

2.4.6.2 Power State D1

According to the *PCI Bus Power Management Interface Specification,* Power State D1 must have a power level equal to or lower than Power State D0. A function in Power State D1 places the SCSI core in the snooze mode. In the snooze mode, a SCSI reset does not generate an IRQ/ signal.

2.4.6.3 Power State D2

According to the *PCI Bus Power Management Interface Specification,* Power State D2 must have a power level equal to or lower than Power State D1. A function in this state places the SCSI core in the coma mode. Placing the PCI Function in Power State D2 disables the SCSI and DMA interrupts, and suppresses the following PCI Configuration Space Command register enable bits:

- I/O Space Enable
- Memory Space Enable
- Bus Mastering Enable
- SERR/ Enable
- Enable Parity Error Response

Therefore, the function's memory and I/O spaces cannot be accessed, and the PCI function cannot be a PCI bus master.

If the PCI function is changed from Power State D2 to Power State D1 or Power State D0, the PCI function restores the previous values of the PCI Command register and asserts any interrupts that were pending before the function entered Power State D2.

2.4.6.4 Power State D3

According to the *PCI Bus Power Management Interface Specification,* Power State D3 must have a power level equal to or lower than Power State D2. Power State D3 is the minimum power state and includes the $D3_{hot}$ and $D3_{cold}$ settings. $D3_{hot}$ allows the device to transition to D0 using software. $D3_{cold}$ removes power from the LSI53C1035. $D3_{cold}$ can transition to D0 by applying VCC and resetting the device.

Placing a function in Power State D3 puts the LSI53C1035 core in the coma mode, clears the function's PCI Command register, and continuously asserts the function's soft reset. Asserting soft reset clears all pending interrupts and 3-states the SCSI bus.

2.5 Ultra320 SCSI Functional Description

The LSI53C1035 provides two independent Ultra320 SCSI or SCSI RAID channels on a single chip. Each channel can be independently configured as either an Ultra320 SCSI RAID controller or as a traditional Ultra320 SCSI controller. Each channel on the LSI53C1035 supports wide SCSI synchronous transfer rates of up to 320 Mbytes/s across an SE or LVD SCSI bus. The integrated LVDlink transceivers support both LVD and SE signals and do not require external transceivers. The LSI53C1035 controller supports all previous versions of the SCSI specifications.

2.5.1 Ultra320 SCSI Features

This section describes how the LSI53C1035 implements the features in the SPI-4 draft specification.

2.5.1.1 Parallel Protocol Request (PPR)

A SCSI extended message negotiates the PPR parameters. The PPR parameters include the (1) transfer period, (2) maximum REQ/ACK offset, (3) quick arbitration and selection (QAS), (4) margin control settings, (5) transfer width, (6) IU_Request, (7) write flow, (8) read streaming, (9) RTI, (10) precompensation enable, (11) information unit transfers, and the (12) DT data phases between an initiator and a target.

2.5.1.2 Double Transition (DT) Clocking

Ultra160 SCSI and Ultra320 SCSI implement DT clocking to provide speeds up to 80 megatransfers/s for Ultra160 SCSI, and up to 160 megatransfers/s for Ultra320 SCSI. When implementing DT clocking, a SCSI device samples data on both the asserting and deasserting edge of REQ/ACK. DT clocking is only valid using an LVD SCSI bus.

2.5.1.3 Intersymbol Interference (ISI) Compensation

ISI Compensation uses paced transfers and precompensation to enable high data transfer rates. Ultra320 SCSI data transfers require ISI Compensation.

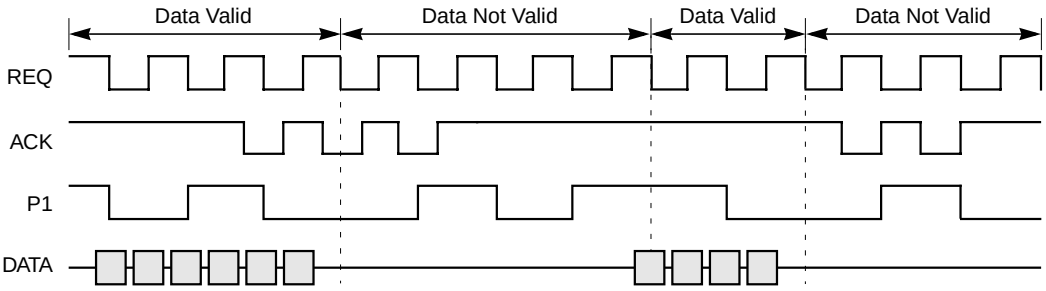
Paced Transfers – The initiator and target must establish a paced transfer agreement that specifies the REQ/ACK offset and the transfer period before using this feature. Devices can only perform paced transfers during Ultra320 SCSI DT data phases. In paced transfers, the device sourcing the data drives the REQ/ACK signal as a free-running clock. The transition of the REQ/ACK signal, either the assertion or the negation, clocks data across the bus. For successful completion of a paced transfer, the number of ACK transitions must equal the number of REQ transitions, and both the REQ and ACK lines must be negated.

The P1 line indicates valid data in 4-byte quantities by using its phase. The transmitting device indicates the start of a valid data state by holding the state of the P1 line for the first two data transfer periods. Beginning on the third data transfer period, the transmitting device continues the valid data state by toggling the state of the P1 line every two data transfer periods for as long as the data is valid. The transmitting device must toggle the P1 line coincident with the REQ/ACK assertion. The method provides a minimum data valid period of two transfer periods.

To pause the data transfer, the transmitting device reverses the phase of P1 by withholding the next transition of P1 at the start of the first two invalid data transfer periods. Beginning with the third invalid data transfer period, the transmitting device toggles the P1 line every two invalid data transfer periods until it sends valid data. The transmitting device returns to the valid data state by reversing the phase of the P1 line. The invalid data state must experience at least one P1 transition before returning to the valid data state. This method provides a minimum data invalid period of four transfer periods.

Figure 2.6 provides a waveform diagram of paced data transfers and illustrates the use of the P1 line.

Figure 2.6 Paced Transfer Example

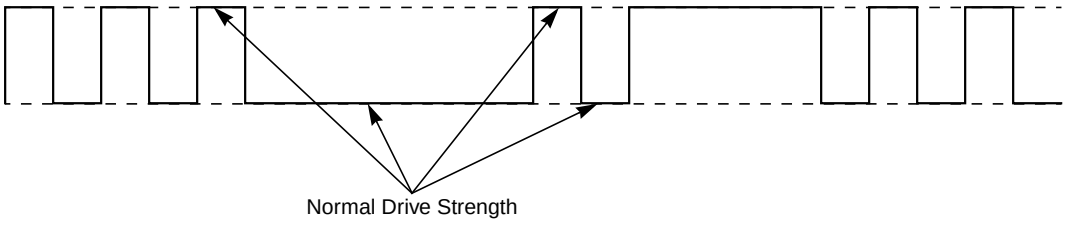


The LSI53C1035 uses the PPR negotiation that the SPI-4 draft standard describes to establish a paced transfer agreement for each initiator-target pair.

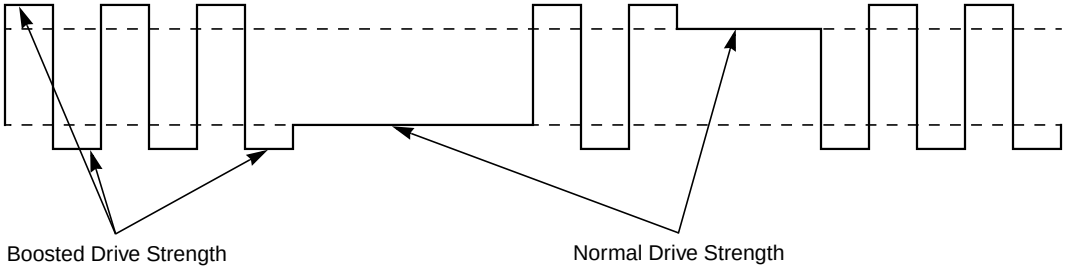
Precompensation – When transmitting in the Ultra320 SCSI mode, the LSI53C1035 uses precompensation to adjust the strength of the REQ, ACK, parity, and data signals. When a signal transitions to HIGH or LOW, the LSI53C1035 boosts the signal drive strength for the first data transfer period, and then lowers the signal drive strength on the second data transfer period if the signal remains in the same state. The LSI53C1035 maintains the lower signal drive strength until the signal again transitions HIGH or LOW. Figure 2.7 illustrates the driver's performance with precompensation enabled and disabled.

Figure 2.7 Precompensation Example

a. Drivers with Precompensation Disabled



b. Drivers with Precompensation Enabled



2.5.1.4 Packetized Transfers

Packetized transfers are also referred to as information unit transfers. They reduce overhead on the SCSI bus by merging several of the SCSI bus phases. Packetized transfers can only occur in DT Data phases. The initiator and target must establish either a DT synchronous transfer agreement or a paced transfer agreement before performing packetized transfers.

The number of bytes an information unit transfers is always a multiple of four. If the number of bytes to transfer in the information unit is not a multiple of four, the LSI53C1035 transmits pad bytes to bring the byte count to a multiple of four.

2.5.1.5 Quick Arbitration and Selection (QAS)

When using packetized transfers, QAS allows devices to arbitrate for the bus immediately after the message phase. QAS reduces the bus overhead and maximizes bus bandwidth by skipping the bus-free phase that normally follows a SCSI connection.

To perform QAS, the target sends a QAS request message to the initiator during the message phase of the bus. QAS-capable devices snoop the SCSI bus for the QAS request message. If a QAS request message is seen, devices can move immediately to the arbitration phase without going to the bus-free phase. The LSI53C1035 employs a fairness algorithm to ensure that all devices have equal bus access.

2.5.1.6 Skew Compensation

The LSI53C1035 provides a method to account for and control system skew between the clock and data signals. Skew compensation is only available when the device operates in the Ultra320 SCSI mode. The initiator-target pair uses the training sequences in the SPI-4 draft standard to determine the skew compensation. Depending on the state of the RTI bit in the PPR negotiation, the LSI53C1035 either can execute this training pattern during each connection, or can execute the training pattern, store the adjustment parameters, and recall them on subsequent connections with the given device. The target determines when to execute the training pattern.

2.5.1.7 Cyclic Redundancy Check (CRC)

Ultra320 SCSI and Ultra160 SCSI devices employ CRC as an error detection code during the DT Data phases. These devices transfer four CRC bytes during the DT Data phases to ensure reliable data transfers.

2.5.1.8 SureLINK Domain Validation

SureLINK domain validation establishes the integrity of a SCSI bus connection between an initiator and a target. Under the SureLINK domain validation procedure, a host queries a device to determine its ability to communicate at the negotiated data transfer rate.

SureLINK domain validation provides three levels of integrity checking: Basic (Level 1) with inquiry command, Enhanced (Level 2) with read/write buffer, and Margined (Level 3) with drive strength margining and slew rate control. The basic check consists of an inquiry command to detect gross problems. The enhanced check sends a known data pattern using the read and write buffer commands to detect additional problems. The margined check verifies that the physical parameters have a reasonable operating margin. Use SureLINK domain validation only during the diagnostic system checks and not during normal system

operation. If transmission errors occur during any of these checks, the system can reduce the transmission rate on a per-target basis to ensure robust system operation.

2.5.2 SCSI Bus Interface

This section describes the SCSI bus modes that the LSI53C1035 supports and the SCSI bus termination methods necessary to operate a high speed SCSI bus.

2.5.2.1 SCSI Bus Modes

The LSI53C1035 supports SE and LVD transfers. To increase device connectivity and SCSI cable length, the LSI53C1035 features LVDlink technology, which is the LSI Logic implementation of LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI and a long-term migration path for faster SCSI transfer rates.

The A_DIFFSENS or B_DIFFSENS signals detect the different input voltages for HVD, LVD, and SE. The LSI53C1035 drivers are tolerant of HVD signal strengths, but do not support the HVD bus mode. The LSI53C1035 SCSI device 3-states its SCSI drivers when it detects an HVD signal level.

2.5.2.2 SCSI Termination

The terminator networks pull signals to an inactive voltage level and match the impedance seen at the end of the cable to the characteristic impedance of the cable. Install terminators at the extreme ends of the SCSI chain, and only at the ends; all SCSI buses must have exactly two terminators.

Note: If using the LSI53C1035 in a design with an 8-bit SCSI bus, designers must terminate all 16 data lines.

2.6 External Memory Interface

The LSI53C1035 external memory controller block provides an 8-bit external memory interface and an ISTWI. The external memory interface supports a Flash ROM, an NVSRAM, and GP memory. Individual select signals on the external memory interface control which memory device is being accessed over the external memory bus. The following subsections describe the implementation of a Flash ROM interface, NVSRAM interface, GP memory interface, and an ISTWI.

Note: Provide 4.7 kΩ pull-ups on the external memory chip selects and write strobes (XM_CS0, XM_CS1, XM_CS2, XM_WS0, and XM_WS1).

2.6.1 Flash ROM Interface

The Flash ROM interface stores the SCSI BIOS and firmware image. A suitable driver must exist to initialize the LSI53C1035.

XM_ADDR[7:0] forms the 8-bit external memory address bus and XM_DATA[7:0] forms the 8-bit external memory data bus. XM_ALE[1] and XM_ALE[0] provide address latches. XM_RS0 and XM_WS0 provide the read and write strobes for accesses to the Flash ROM. XM_CS0 selects the Flash ROM. The Flash ROM interface latches addresses to support up to 4 Mbytes of address space. The interface supports byte, word, and dword accesses. The LSI53C1035 dword aligns dword reads, word aligns word reads, and byte aligns byte reads. The remaining bits from word and byte reads are meaningless.

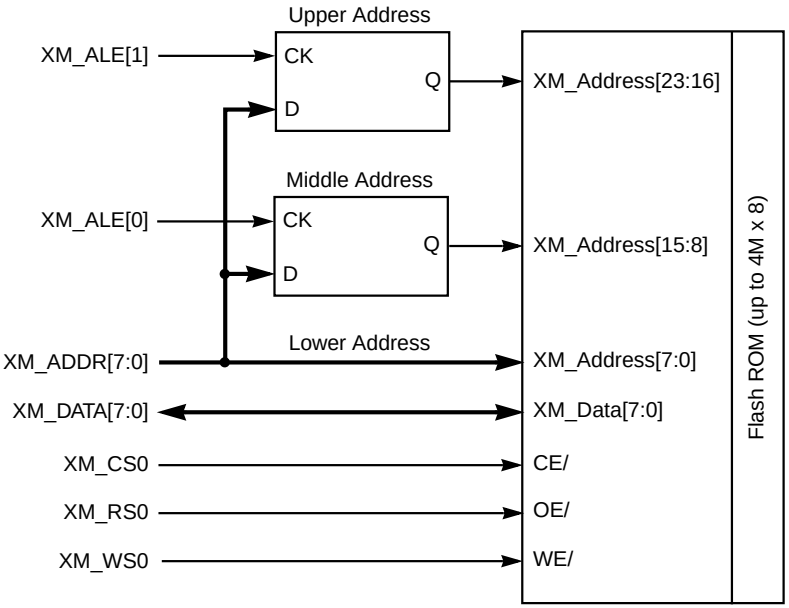
The XM_DATA[2:1] Power-On sense pin configurations define the size of the Flash ROM address space. Table 2.3 provides the pin encoding. By default, internal logic pulls these pins down to indicate that no Flash ROM is present.

Table 2.3 Flash ROM Size Programming

XM_DATA[2:1] Options	Flash ROM Size
0b00	No Flash ROM present (Default)
0b01	Up to 1024 Kbytes
0b10	2048 Kbytes
0b11	4096 Kbytes

The LSI53C1035 defines only the middle (XM_Address[15:8]) and lower (XM_Address[7:0]) address ranges if the Flash ROM addressable space is 64 Kbytes or less. The LSI53C1035 defines the upper (XM_Address[23:16]), middle (XM_Address[15:8]), and lower (XM_Address[7:0]) address ranges if the Flash ROM addressable space is 128 Kbytes or more. Figure 2.8 provides an example of a Flash ROM configuration.

Figure 2.8 Flash ROM Block Diagram



The LSI53C1035 implements a Flash ROM signature recognition mechanism to determine whether the Flash ROM contains a valid image. The Flash ROM can be present and not contain a valid image either before its initial programming or during board testing. The first access to the Flash ROM is a 16-byte burst read beginning at Flash ROM address 0x000000. The LSI53C1035 compares the values read to the Flash signature values that Table 2.4 provides. If the Flash signature values match, the LSI53C1035 performs the instruction located at Flash ROM address 0x000000. If the Flash signature values do not match, the LSI53C1035 records an error and ignores the Flash ROM instruction. The Flash ROM signature does not include the first three bytes of Flash ROM memory as these bytes contain a branch offset instruction.

Table 2.4 Flash Signature Values

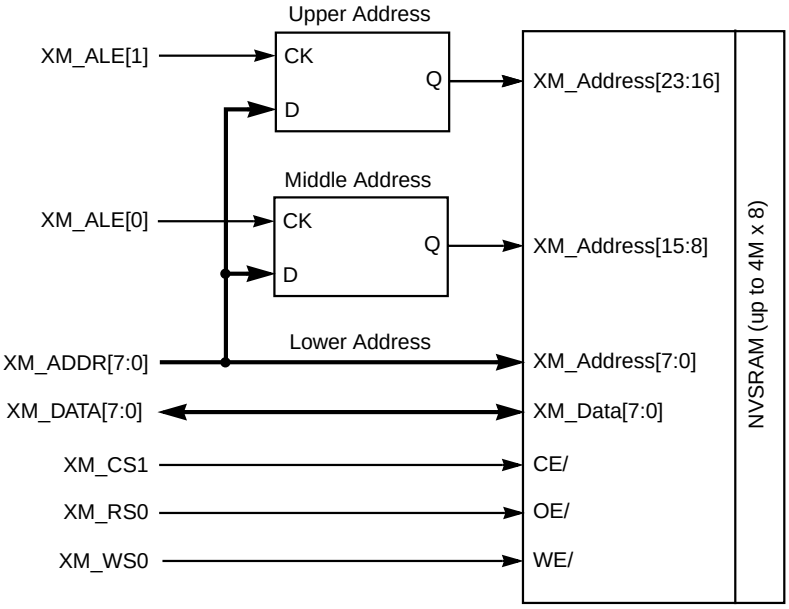
Flash Address	Flash Signature Values			
Bytes [3:0]	0xEA	XX	XX	XX
Bytes [7:4]	0x5A	0xEA	0xA5	0x5A
Bytes [11:8]	0xA5	0x5A	0xEA	0xA5
Bytes [15:12]	0x5A	0xA5	0x5A	0xEA

2.6.2 NVSRAM Interface

When the LSI53C1035 is configured as a SCSI RAID controller, the NVSRAM provides storage for metadata and configuration data. When the LSI53C1035 is configured in the non-RAID mode, the NVSRAM interface supports a battery-backed SRAM that implements write journaling for the Integrated Mirroring (IM) feature. The IM feature provides physical mirroring of up to six drives, and is only available when the LSI53C1035 operates in non-RAID mode. The Fusion-MPT firmware writes to both the boot drive and the mirrored drive. The mirroring of the boot drive is transparent to the BIOS, drivers, and operating system.

XM_ADDR[7:0] forms the 8-bit NVSRAM address bus and XM_DATA[7:0] forms the 8-bit NVSRAM data bus. XM_ALE[1] and XM_ALE[0] provide address latches. XM_CS1 selects the NVSRAM. XM_RS0 and XM_WS0 provide the read and write strobes for accesses to the NVSRAM. The NVSRAM latches the 8-bit address to form up to a 24-bit NVSRAM address. Figure 2.9 provides a block diagram illustrating the NVSRAM connection.

Figure 2.9 NVSRAM Block Diagram

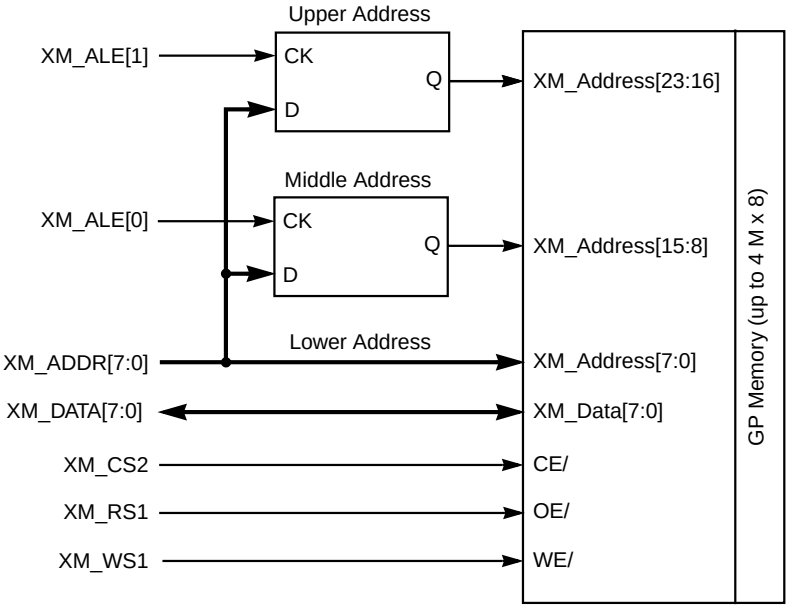


2.6.3 General Purpose (GP) Memory Interface

The GP memory interface supports general devices such as a UART or an 8-bit battery backup. XM_ADDR[7:0] forms the GP memory address bus and XM_DATA[7:0] forms the GP memory data bus. XM_ALE1 and XM_ALE0 provide address latches. XM_CS2 selects the general purpose memory. XM_RS1 and XM_WS1 provide the read and write strobes for accesses to the GP memory.

The GP memory behaves in a similar fashion to the NVSRAM. The GP memory controller latches the 8-bit address bus to address up to 4M x 8 bits. The interface supports byte, word, and dword accesses. The LSI53C1035 dword aligns dword reads, word aligns word reads, and byte aligns byte reads. Figure 2.10 provides an example of a GP memory configuration.

Figure 2.10 GP Memory Block Diagram



2.6.4 ISTWI

The ISTWI interfaces with low bandwidth peripherals that do not require a high performance bus. The ISTWI operates as either a master or a slave at data rates of up to 400 Kbits/s. To accomplish byte-wise, bidirectional data transfers over this bus, the ISTWI controller block shifts data, and uses either an interrupt or polling handshake to signal the completion of each byte. The ISTWI controller manages all ISTWI timing and performs bus-specific sequences. The operation of this bus follows the de facto standard for ISTWI.

When the LSI53C1035 ISTWI controller operates as a bus master, it initiates data transfers and generates the clock signal for the data transfer. The ISTWI supports multimaster capabilities, which permits multiple masters on the same 2-wire bus. The ISTWI controller follows the arbitration protocol for multimaster ISTWI buses. If the controller wins arbitration, the data transfer proceeds normally. If the controller loses arbitration, the ISTWI reports that it lost the arbitration, and controlling software is responsible for restarting the transfer.

When the LSI53C1035 ISTWI controller is operating as a slave, a bus master on the ISTWI bus can address the LSI53C1035 ISTWI controller. The LSI53C1035 ISTWI controller responds to a specific programmed address as well as to a general call address. The ISTWI also supports a monitor mode, in which it snoops all data on the bus without acknowledgment on the bus.

2.7 DDR SDRAM Controller

The LSI53C1035 dedicates a 5-port arbitrated interface module to provide high-performance access to DDR SDRAM memory. Operation of the LSI53C1035 in RAID mode requires DDR SDRAM, but operation of the LSI53C1035 in the conventional SCSI mode does not require DDR SDRAM.

2.7.1 DDR SDRAM Features

The DDR SDRAM interface supports:

- a 64-bit external data bus with 8-bit ECC
- up to 256 Mbytes of DDR SDRAM
- five AHB agents
- linear burst transfers from 1 to 64 bytes
- self-refresh capability
- 120 MHz frequency with a maximum burst rate of 1,920 Mbytes/s (240 MHz x 64 bits)
- separate address and data buses
- unbuffered DDR SDRAM with ECC (72-bit bus)
- Open Bank Management
- 13-bit RAS and 10-bit CAS support (four internal banks)
- single external bank configuration (one chip select per DIMM bank)

LSI Logic recommends using a minimum of 64 Mbytes of DDR SDRAM. For DDR operation, pull TMS HIGH through a 4.7 kΩ resistor.

2.7.2 Battery Backup

To minimize the effects of power failure, LSI Logic recommends implementing a battery backup unit (BBU) for the DDR SDRAM. LSI Logic offers a proprietary BBU for purchase.

The LSI53C1035 battery backup interface consists of two signals: PFS/ and BBU_PFC. PFS/, or Power Fail Signal, is an input to the controller that asserts when a power failure occurs. BBU_PFC, or Battery Backup Power Fail Complete, is an output from the controller that informs external logic when the DDR controller places the DDR memory in self-refresh mode.

2.8 Serial EEPROM Interface

The nonvolatile external serial EEPROM stores configuration fields for the LSI53C1035. The serial EEPROM contains fields for the Subsystem ID(s), Subsystem Vendor ID(s), Device ID(s), Revision ID(s), Class Code(s), and the sizes of the PCI Memory Spaces [0] and [1]. The LSI53C1035 must establish each of these parameters prior to reading system BIOS and loading the PCI Configuration Space registers. Allowing the internal pull-down to pull the XM_CS[7] power-on sense pin LOW enables the download of PCI configuration data from the serial EEPROM. For details on the setting of the power-on options, refer to Section 3.9, “Power-On Sense Pins Description.”

The SerialCLK and SerialDATA signals form the 2-wire serial interface that provides the connection to the serial EEPROM. Board designs must provide at least a 2 Kbyte, 400 kHz serial EEPROM through this interface. During initialization, the firmware checks if a serial EEPROM exists. Firmware uses the checksum byte to determine whether the configuration held in the serial EEPROM is valid. If the checksum fails, the firmware checks for a valid NVData signature. If a valid NVData signature is found, the firmware individually checksums each Fusion-MPT configuration page to find the invalid page or pages. Table 2.5 provides the structure of the configuration record in the serial EEPROM.

Table 2.5 Serial EEPROM Auto-Download Information

Byte 3	Byte 2	Byte 1	Byte 0	Offset
PCI Function [0] Subsystem Vendor ID [15:0]		PCI Function [0] Subsystem ID [15:0]		0x00
PCI Function [1] Subsystem ID [15:0]		Reserved	PCI Memory [0] and PCI Memory [1] Size	0x04
Reserved	Checksum	PCI Function [1] Subsystem Vendor ID [15:0]		0x08
PCI Function [0] Device ID [15:0]		PCI Function [0] Vendor ID [15:0]		0x0C
PCI Function [1] Device ID [15:0]		PCI Function [1] Vendor ID [15:0]		0x10
Reserved	PCI Function [0] Class Code [23:0]			0x14
Reserved	PCI Function [1] Class Code [23:0]			0x18
Reserved		PCI Function [1] Revision ID [7:0]	PCI Function [0] Revision ID [7:0]	0x1C
PCI Function [0] Offset[31:0] in bytes from option ROM Address				0x20
PCI Function [1] Offset[31:0] in bytes from option ROM Address				0x24

2.9 Test Interface

This section describes the LSI Logic requirements for the test interface. To use the test interface, route all Multi-ICE test signals to a header on the board.

The Multi-ICE test interface header is a 20-pin header for Multi-ICE debugging through the ICE JTAG port. This header is essential for debugging both the firmware and the design functionality, and must be included in board designs. The connector is a 20-pin header that mates with the IDC sockets mounted on a ribbon cable. Table 2.6 provides the pinout of the 20-pin header.

Table 2.6 20-Pin Multi-ICE Header Pinout

Pin Number	Signal	Pin Number	Signal
1	VDD (3.3 V)	2	VDD (3.3 V)
3	TRST_ICE[1]	4	VSS
5	TDI_ICE[1]	6	VSS
7	TMS_ICE[1]	8	VSS
9	TCK_ICE[1]	10	VSS
11	RTCK_ICE	12	VSS
13	TDO_ICE	14	VSS
15	TRST/[1]	16	VSS
17	NC	18	VSS
19	NC	20	VSS

1. Connect a 4.7 kΩ resistor from this signal to 3.3 V.

Chapter 3
Signal Description

This chapter describes the input and output signals of the LSI53C1035. The chapter consists of the following sections:

A slash (/) at the end of a signal indicates that the signal is active LOW. When the slash is absent, the signal is active HIGH. *NC* designates a No Connect signal.

3.1 Signal Organization

The LSI53C1035 has the following major interfaces:

- System Signals
- PCI Bus Signals
- SCSI Bus Signals
- DDR SDRAM Memory Signals
- Memory Bus Signals
- Test Signals
- General Purpose I/O (GPIO) and LED Signals

There are five signal types:

I	Input, a standard input-only signal
O	Output, a standard output driver (typically a Totem Pole output)
I/O	Input and/or output (bidirectional)
P	Power
G	Ground

Figure 3.1 contains the functional signal groupings of the LSI53C1035. Figure 5.12 on page 5-29 provides a diagram of the LSI53C1035 788-Ball Grid Array (BGA). Table 5.23 and Table 5.24 on page 5-23 and page 5-26, respectively, provide pinout listings for the LSI53C1035.

Figure 3.1 LSI53C1035 Signal Block Diagram

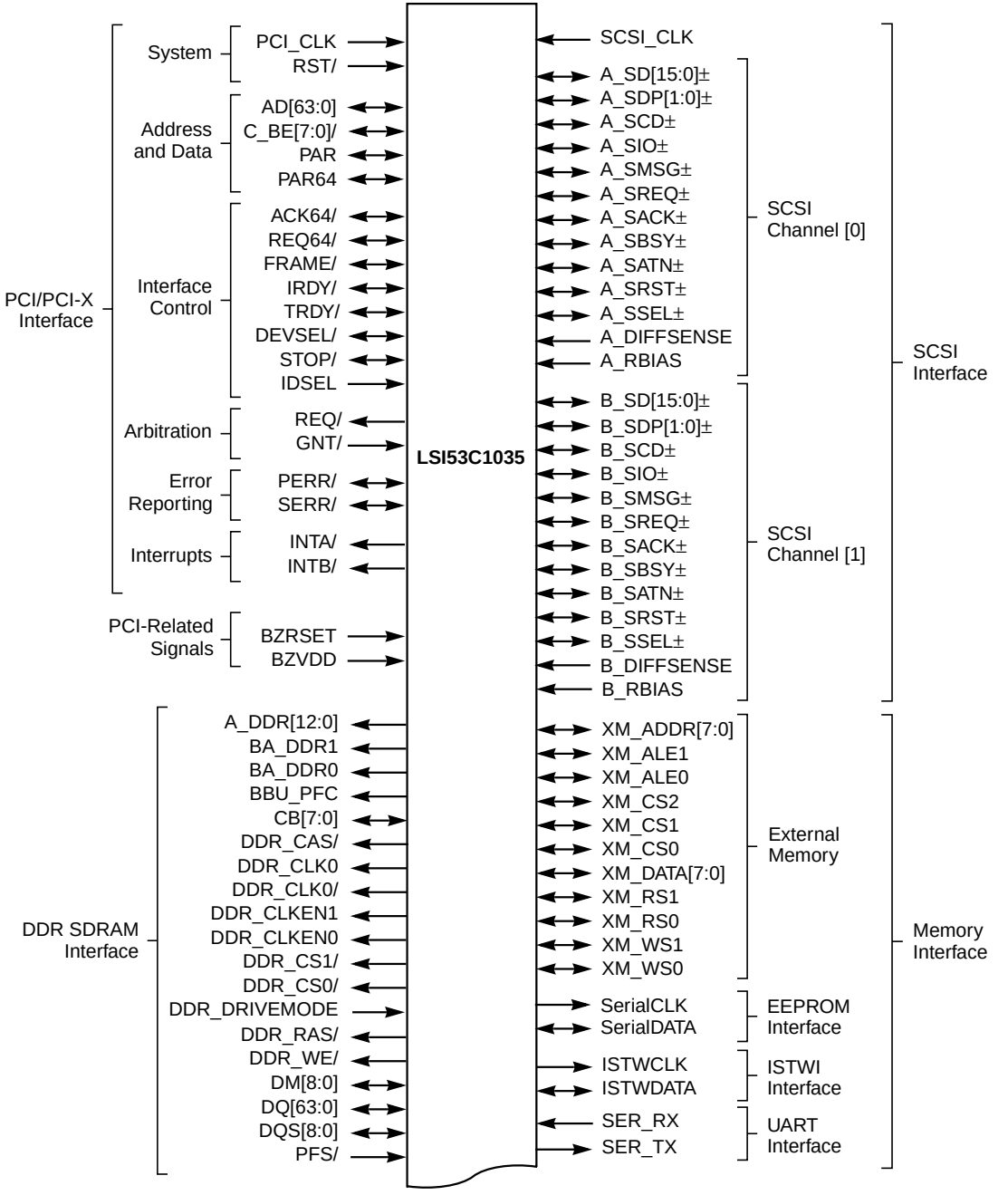
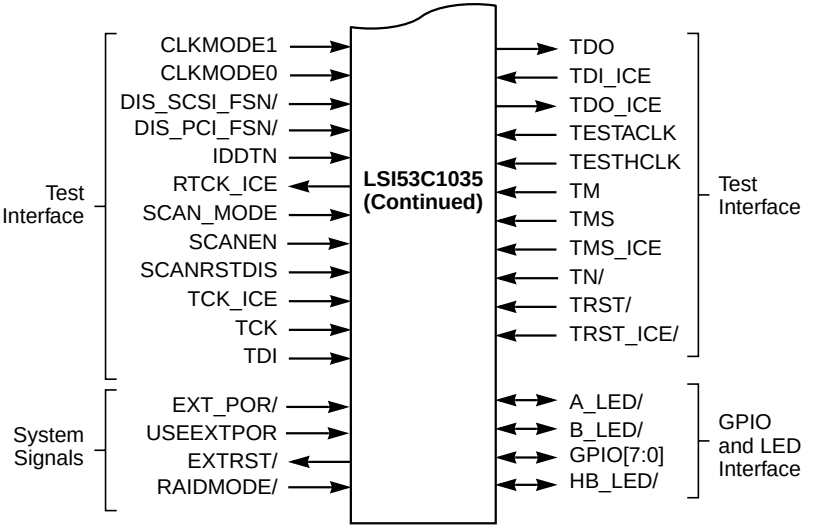


Figure 3.1 LSI53C1035 Signal Block Diagram (Cont.)



3.2 System Signals

Table 3.1 describes the System signals.

Table 3.1 System Signals

Signal Name	BGA Position	Type	Strength	Description
EXTRST/	AF3	O	8 mA	This signal provides an external reset pin.
EXT_POR/	AH5	I	N/A	This signal provides an external Power-On reset pin.
RAIDMODE/	C30	I	N/A	Asserting this signal configures the LSI53C1035 as a single function PCI-X to Ultra320 SCSI RAID controller. Firmware then can configure the LSI53C1035 as a PCI-X to dual channel Ultra320 SCSI RAID controller. By default, the LSI53C1035 internally pulls this signal HIGH. Deasserting this signal places the LSI53C1035 in the LSI53C1030 compatibility mode.
USEEXTPOR	AK1	I	N/A	This signal enables the use of an external POR. If this signal is pulled HIGH, the LSI53C1035 uses the POR signal provided externally on EXT_POR/.

3.3 PCI Bus Interface Signals

This section describes the PCI interface. The PCI interface consists of the System, Address and Data, Interface Control, Arbitration, Error Reporting, and Interrupt signal groups. Another signal group describes signals that are related to the PCI bus, but not defined within the PCI specifications.

3.3.1 PCI System Signals

Table 3.2 describes the PCI System signals.

Table 3.2 PCI System Signals

Signal Name	BGA Position	Type	Strength	Description
PCI_CLK	AP8	I	N/A	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
RST/	AK11	I	N/A	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.2 PCI Address and Data Signals

Table 3.3 describes the PCI Address and Data signals.

Table 3.3 PCI Address and Data Signals

Signal Name	BGA Position	Type	Strength	Description
AD[63:0]	AM22, AK24, AP23, AJ24, AN23, AK25, AN24, AJ25, AP25, AL26, AM25, AK26, AP26, AL27, AN26, AK27, AP27, AJ27, AN27, AL28, AP29, AK28, AN29, AJ28, AM29, AL29, AP30, AK29, AN30, AJ29, AM30, AL30, AM10 AK12, AN10, AL12, AP10, AL13, AN11, AL14, AN12, AK15, AP12, AL15, AM13, AK16, AN13, AL16, AL19, AM17, AK19, AP17, AJ19, AP18, AL20, AN18, AM18, AJ20, AP20, AL21, AN20, AJ21, AP21, AL22	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
C_BE[7:0]/	AK23, AM21, AJ23, AP22, AP11, AP13, AP16, AK20	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
PAR	AK18	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
PAR64	AL24	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.3 PCI Interface Control Signals

Table 3.4 describes the PCI Interface Control signals.

Table 3.4 PCI Interface Control Signals

Signal Name	BGA Position	Type	Strength	Description
ACK64/	AN21	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
REQ64/	AL23	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
FRAME/	AJ17	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
IRDY/	AM14	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
TRDY/	AK17	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
DEVSEL/	AN14	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
STOP/	AL17	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
IDSEL	AJ15	I	N/A	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.4 PCI Arbitration Signals

Table 3.5 describes the PCI Arbitration signals.

Table 3.5 PCI Arbitration Signals

Signal Name	BGA Position	Type	Strength	Description
REQ/	AP9	O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
GNT/	AL11	I	N/A	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.5 PCI Error Reporting Signals

Table 3.6 describes the PCI Error Reporting signals.

Table 3.6 PCI Error Reporting Signals

Signal Name	BGA Position	Type	Strength	Description
PERR/	AP14	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
SERR/	AN16	I/O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.6 PCI Interrupt Signals

Table 3.7 describes the PCI Interrupt signals.

Table 3.7 PCI Interrupt Signals

Signal Name	BGA Position	Type	Strength	Description
INTA/	AL8	O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.
INTB/	AN9	O	8 mA PCI	Refer to the *PCI Local Bus Specification, Version 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Version 1.0a*, for this signal description.

3.3.7 PCI-Related Signals

Table 3.8 describes the PCI-related signals.

Table 3.8 PCI-Related Signals

Signal Name	BGA Position	Type	Strength	Description
BZRSET	AN6	I	N/A	BZRSET and BZVDD provide biasing for the PCI signals. Connect a 50 Ω resistor between BZRSET and BZVDD.
BZVDD	AP6	I	N/A	

3.4 SCSI Interface Signals

The SCSI Interface signals section describes the signals for the SCSI Channel [0] and SCSI Channel [1] interfaces. Table 3.9 describes the SCSI bus signals that are common to both SCSI Channel [0] and SCSI Channel [1].

In the LVD mode, the negative and positive signals form the differential pair. In the SE mode, the negative signals represent the signal pin and the positive signals are a virtual ground. The LSI53C1035 does not support the HVD mode. If HVD signaling is present, the SCSI Channel 3-states its drivers.

Table 3.9 SCSI Bus Interface Signals

Signal Name	BGA Position	Type	Strength	Description
SCSI_CLK	F1	I	N/A	This signal provides the 80 MHz clock for the LSI53C1035 SCSI buses.

3.4.1 SCSI Channel [0] Signals

Table 3.10 describes the SCSI Channel [0] Interface signals.

Table 3.10 SCSI Channel [0] Interface Signals

Signal Name	BGA Position	Type	Strength	Description
A_SD[15:0]+	AA4, Y2, AA2, AB1, J3, J1, H5, K2, T2, U1, U5, U3, V4, V2, W4, W1	I/O	SE: 48 mA LVD: 12 mA	**SCSI Channel [0] Data** signals.
A_SD[15:0]-	AB4, AA1, AA3, AB2, J2, K3, G4, K1, T1, U2, U4, V1, V5, V3, W5, W2			
A_SDP[1:0]+	Y4, R2			**SCSI Channel [0] Data Parity** signals.
A_SDP[1:0]-	Y5, R1			
A_VDDBIAS	R4	O	N/A	**A_VDDBIAS** provides power for the A_RBIAS circuit.
A_RBIAS	P1	I	N/A	Connect a 9.76 kΩ or 10.0 kΩ resistor between the A_VDDBIAS and the **A_RBIAS** signals to generate the LVD signaling pad bias current.
A_DIFFSENS	H1	I	N/A	The **SCSI Channel [0] Differential Sense** pin detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus. SE Mode: Driving this pin below 0.5 V (LOW) indicates an SE bus mode and places SCSI Channel [0] transceivers in the SE bus mode. LVD Mode: Driving this pin between 0.7 V and 1.9 V (intermediate) indicates an LVD bus mode and places SCSI Channel [0] transceivers in the LVD bus mode. HVD Mode: Driving this pin above 2.0 V (HIGH) indicates an HVD bus mode and causes SCSI Channel [0] to 3-state its SCSI drivers.

Table 3.11 describes the SCSI Channel [0] Control signals.

Table 3.11 SCSI Channel [0] Control Signals

Signal Name	BGA Position	Type	Strength	Description
A_SCD±	K5, J4	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [0] **Command/Data**.
A_SIO±	J5, H4			SCSI Channel [0] **Input/Output**.
A_SMSG±	M5, L4			SCSI Channel [0] **Message**.
A_SREQ±	L2, L1			SCSI Channel [0] **Request**.
A_SACK±	M4, N4			SCSI Channel [0] **Acknowledge**.
A_SBSY±	P3, P2			SCSI Channel [0] **Busy.**
A_SATN±	P4, R5			SCSI Channel [0] **Attention**.
A_SRST±	N2, N1			SCSI Channel [0] **Bus Reset.**
A_SSEL±	M2, M1			SCSI Channel [0] **Select.**

3.4.2 SCSI Channel [1] Signals

Table 3.12 describes the SCSI Channel [1] Interface signals.

Table 3.12 SCSI Channel [1] Interface Signals

Signal Name	BGA Position	Type	Strength	Description
B_SD[15:0]+	B10, D6, B9, E5, A22, D23, B21, B20, B15, D10, C14, B13, D9, A12, D8, A11	I/O	SE: 48 mA LVD: 12 mA	**SCSI Channel [1] Data** signals.
B_SD[15:0]-	C10, E7, C9, F6, C21, D22, A21, A20, A14, D11, A13, C13, E10, B12, E9, B11			
B_SDP[1:0]+	D7, D14			**SCSI Channel [1] Data Parity** signals.
B_SDP[1:0]-	E8, D13			
B_VDDBIAS	E15	O	N/A	**B_VDDBIAS** provides power for the B_RBIAS circuit.
B_RBIAS	A15	I	N/A	Connect a 9.76 kΩ or 10.0 kΩ resistor between the B_VDDBIAS and the **B_RBIAS** pins to generate the LVD signaling pad bias current.
B_DIFFSENS	A7	I	N/A	The **SCSI Channel [1] Differential Sense** signal detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus. SE Mode: Driving this signal below 0.5 V (LOW) indicates an SE bus mode and places SCSI Channel [1] transceivers in the SE mode. LVD Mode: Driving this signal between 0.7 V and 1.9 V (intermediate) indicates an LVD bus mode and places SCSI Channel [1] transceivers in the LVD mode. HVD Mode: Driving this signal above 2.0 V (HIGH) indicates an HVD bus mode and causes SCSI Channel [1] to 3-state its SCSI drivers.

Table 3.13 describes the SCSI Channel [1] Control signals.

Table 3.13 SCSI Channel [1] Control Signals

Signal Name	BGA Position	Type	Strength	Description
B_SCD±	D19, E18	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [1] **Command/Data**.
B_SIO±	D20, E19			SCSI Channel [1] **Input/Output**.
B_SMSG±	D18, D17			SCSI Channel [1] **Message**.
B_SREQ±	B19, A19			SCSI Channel [1] **Request**.
B_SACK±	B17, A17			SCSI Channel [1] **Acknowledge**.
B_SBSY±	E16, D15			SCSI Channel [1] **Busy**.
B_SATN±	A16, B16			SCSI Channel [1] **Attention**.
B_SRST±	A18, C17			SCSI Channel [1] **Bus Reset**.
B_SSEL±	C18, B18			SCSI Channel [1] **Select.**

3.5 Memory Interface

Table 3.14 describes the DDR SDRAM Interface and Control signals.

Table 3.14 DDR SDRAM Interface Signals

Signal Name	BGA Position	Type	Strength	Description
A_DDR[12:0]	K32, J31, U31, K33, M34, N32, M31, N33, N31, T34, T31, U32, U30	O	8 mA	The **DDR Address** signals form the DDR SDRAM address bus.
BA_DDR[1:0]	Y33, Y30	O	8 mA	BA_DDR[1:0] select one of the four internal DDR SDRAM banks on an external DDR SDRAM Dual Inline Memory Module (DIMM).
BBU_PFC	A24	O	8 mA	The LSI53C1035 asserts the **Power Fail Complete** signal when the DDR controller places the DDR memory into the self-refresh mode.
CB[7:0]	Y31, W33, W30, W34, V32, V33, V31, V34	I/O	9 mA or 16.8 mA	These signals form the 8-bit **ECC Data Bus** for the DDR SDRAM.
DDR_CAS/	AC30	O	8 mA	This signal provides the **DDR Column Address Strobe**.
DDR_CLK0, DDR_CLK0/	U34, U33	O	9 mA or 16.8 mA	These signals form the **DDR Differential Clock Output**.
DDR_CLKEN1	K30	O	8 mA	Leave this signal unconnected.
DDR_CLKEN0	J34	O	8 mA	The LSI53C1035 asserts **DDR Clock Enable 0** to activate the internal clock signals and I/O buffers for DDR SDRAM memory bank 0.
DDR_CS1/	AD30	O	8 mA	Leave this signal unconnected.
DDR_CS0/	AD34	O	8 mA	Active LOW **DDR Chip Select 0** is the chip select signal to the external DDR SDRAM memory bank 0.
DDR_ DRIVEMODE	AP4	I	N/A	Leave this signal unconnected.
DDR_RAS/	AD31	O	8 mA	This signal provides the **DDR Row Address Strobe**.

Table 3.14 DDR SDRAM Interface Signals (Cont.)

Signal Name	BGA Position	Type	Strength	Description
DDR_WE/	AC33	O	8 mA	This signal provides the **DDR Write Enable**.
DM[8:0]	W31, AK34, AH30, AF31, AB33, R30, L34, H34, F32	I/O	8 mA	The **DDR Data Mask** signals provide the DDR SDRAM write data masks. DM8 is the mask for CB[7:0].
DQ[63:0]	AM34, AL34, AK32, AK33, AJ33, AJ34, AK30, AH33, AJ30, AH34, AK31, AG33, AJ31, AF32, AG30, AF33, AH31, AF34, AE30, AE32, AG31, AE34, AF30, AD33, AC34, AE31, AB32, AC31, AA32, AA31, AA33, AA34, T30, T33, R34, R31, P31, P34, P33, P32 K31, M33, L31, M30, L33, K34, H31, J30, G31, J33, H30, J32, G30, H33, E31, G34, G33, F30, F34, F33, E33, E32, D34, C34	I/O	8 mA	These signals form the **DDR Data Bus**.
DQS[8:0]	V30, AJ32, AG34, AE33, AB31, R33, L30, F31, E34	I/O	8 mA	These signals provide the **DDR Data Strobes**.
PFS/	B24	I	N/A	This signal indicates a **Power Failure**.

Table 3.15 describes the External Memory Interface signals.

Table 3.15 External Memory Signals

Signal Name	BGA Position	Type	Strength	Description
XM_ADDR[7:0]	D28, F23, E27, B25, C25, D29, A26, E28	I/O	4 mA	The **External Memory Address** signals form the external memory address bus to the Flash ROM, NVSRAM, and GP memory.
XM_ALE[1:0]	E25, A25	I/O	4 mA	The **External Memory Address Latch** signals provide an address latch for the Flash ROM, NVSRAM, and GP memory buses. Use **XM_ALE0** and **XM_ALE1** in conjunction with XM_ADDR[7:0] to generate external memory addresses.
XM_CS2	F24	I/O	4 mA	**External Memory Chip Select 2** is the chip select for the GP memory interface.
XM_CS1	B26	I/O	4 mA	**External Memory Chip Select 1** is the chip select for the NVSRAM memory interface.
XM_CS0	B31	I/O	4 mA	**External Memory Chip Select 0** is the chip select for the Flash ROM memory interface.
XM_DATA[7:0]	A27, F25, E29, B27, A30, A28, B28, F26	I/O	8 mA	The **External Memory Data** signals form the external memory data bus to the Flash ROM, NVSRAM, and GP memory.
XM_RS[1:0]	C29, F27	I/O	4 mA	**External Memory Read Strobe 1** provides the read strobe for the GP memory interface. **External Memory Read Strobe 0** provides the read strobe for the Flash ROM and NVSRAM memory interfaces.
XM_WS[1:0]	A29, B29	I/O	4 mA	**External Memory Write Strobe 1** provides the write strobe for the GP memory interface. **External Memory Write Strobe 0** provides the write strobe for the Flash ROM and NVSRAM memory interfaces.

Table 3.16 describes the Serial EEPROM Interface signals.

Table 3.16 Serial EEPROM Interface Signals

Signal Name	BGA Position	Type	Strength	Description
SerialCLK	AK4	O	8 mA	**Serial Clock** is the clock signal for the Serial EEPROM. Pull this signal HIGH through a 4.7 KΩ resistor when an EEPROM is present.
SerialDATA	AD6	I/O	4 mA	**Serial Data** is the data signal for the Serial EEPROM. Pull this signal HIGH through a 4.7 KΩ resistor when an EEPROM is present.

Table 3.17 describes the ISTWI signals.

Table 3.17 ISTWI Signals

Signal Name	BGA Position	Type	Strength	Description
ISTWCLK	A31	O	8 mA	**ISTWI Clock** is the clock signal for the ISTWI bus. The ISWI controller provides the clock signal to the ISTWI bus when the LSI53C1035 is the ISTWI bus master.
ISTWDATA	F28	I/O	4 mA	**ISTWI Data** is the data signal for the ISTWI bus.

Table 3.18 describes the UART Interface signals.

Table 3.18 UART Interface Signals

Signal Name	BGA Position	Type	Strength	Description
SER_RX	AJ5	I	N/A	**SER_RX** is the UART receive pin.
SER_TX	AF2	O	8 mA	**SER_TX** is the UART transmit pin.

3.6 GPIO and LED Signals

Table 3.19 describes the GPIO and LED signals.

Table 3.19 GPIO and LED Signals

Signal Name	BGA Position	Type	Strength	Description
GPIO[7:0]	D3, D2, D1, G6, E3, E2, E1, H6	I/O	12 mA	**GPIO pins**. The LSI53C1035 controls these signals and may configure them as inputs or as outputs. These pins default to input mode after chip initialization.
A_LED/	AE2	I/O	12 mA	**A_LED/** either drives the SCSI Channel [0] activity LED or provides a GPIO pin. A_LED can be controlled by firmware or driven by chip activity.
B_LED/	AJ4	I/O	12 mA	**B_LED/** either drives the SCSI Channel [1] activity LED or provides a GPIO pin. B_LED/ can be controlled by firmware or driven by chip activity.
HB_LED/	AC6	I/O	12 mA	Firmware blinks **Heart Beat LED** at a 1.0 second interval when the IOP is operational.

3.7 Test Interface

Table 3.20 describes the JTAG and Multi-ICE debug signals.

Table 3.20 JTAG Debug Signals

Signal Name	BGA Position	Type	Strength	Description
TRST/	AC5	I	N/A	Active LOW **Test Reset** provides asynchronous initialization of the test access port (TAP) controller.
TCK	AE1	I	N/A	**Chip Test Clock** provides the clock for the JTAG test logic.
TDI	AG5	I	N/A	**Test Data In** is the serial input to the JTAG test logic for serial test instructions.
TDO	AC2	O	8 mA	**Test Data Out** is the serial output from the JTAG test logic.
TMS	AH4	I	N/A	The TAP controller decodes **Test Mode Select** to control JTAG test operations.
RTCK_ICE	AE5	O	8 mA	**Test Clock Acknowledge** provides the JTAG test clock acknowledge signal for the ICE debug logic.
TRST_ICE/	AB3	I	N/A	**ICE Test Reset** provides the JTAG test reset signal for the ICE debug logic. This signal is internally pulled HIGH.
TCK_ICE	AG4	I	N/A	**ICE Test Clock** provides the test clock for the ICE debug logic. This signal is internally pulled HIGH.
TDI_ICE	AA6	I	N/A	**ICE Test Data In** provides the JTAG test data in signal for the ICE debug logic. This signal is internally pulled HIGH.
TDO_ICE	AF4	O	8 mA	**ICE Test Data Out** provides the JTAG test data out signal for the ICE debug logic.
TMS_ICE	AF5	I	N/A	**ICE Test Mode Select** provides the JTAG test mode select signal for the ICE debug logic. This signal is internally pulled HIGH.

Table 3.21 lists the LSI Logic test signals.

Table 3.21 LSI Logic Test Signals

Signal Name	BGA Position	Type	Strength	Description
SCANEN	B6	I	N/A	**SCANEN** is reserved for LSI Logic use.
SCAN_MODE	C6	I	N/A	**SCAN_MODE** is reserved for LSI Logic use.
SCANRSTDIS	F8	I	N/A	**SCANRSTDIS** is reserved for LSI Logic use.
IDDTN	E24	I	N/A	**IDDTN** is reserved for LSI Logic use.
CLKMODE0	D26	I	N/A	**CLKMODE_0** is reserved for LSI Logic use.
CLKMODE1	F22	I	N/A	**CLKMODE_1** is reserved for LSI Logic use.
DIS_PCI_FSN/	AG1	I	N/A	Pulling **DIS_PCI_FSN/** LOW disables the PCI frequency synthesizer (FSN). Pulling this pin HIGH allows the chip to enable the PCI FSN when operating in PCI-X mode, or to disable the PCI FSN when operating in PCI mode. The LSI53C1035 controls the PCI FSN.
DIS_SCSI_FSN/	E4	I	N/A	**DIS_SCSI_FSN/** is reserved for LSI Logic use.
TESTACLK	E26	I	N/A	**TESTACLK** is reserved for LSI Logic use.
TESTHCLK	B23	I	N/A	**TESTHCLK** is reserved for LSI Logic use.
TM	B5	I	N/A	**TM** is reserved for LSI Logic use.
TN/	A5	I	N/A	**TN/** is reserved for LSI Logic use.

3.8 Power and Ground Pins

Table 3.22 describes the Power and Ground signals.

Table 3.22 Power and Ground Signals[1]

Signal Name	BGA Position	Type	Description
PWR_01	G7, G8, G9, G12, G13, G16, G19, G22, G23, G27, H7, J7, M7, N7, T7, W7, AB7, AC7, AF7, AF28, AG7, AG28, AH7, AH8, AH12, AH13, AH16, AH19, AH22, AH23, AH26, AH27, AH28	P	The **Power_01** pins provide the common 3.3 V I/O power.
PWR_01-NC	G28, H28, J28, M28, N28, T28, W28, AB28, AC28	P	These pins are reserved. Do not connect these pins.
PWR_02	K7, L7, P7, R7, U7, V7, Y7, AA7, AD7, AE7	P	The **Power_02** pins provide power to SCSI Channel [0]. These pins connect to an isolated 3.3 V I/O power plane.
PWR_03	AH9, AH10, AH11, AH14, AH15, AH17, AH18, AH20, AH21, AH24, AH25	P	The **Power_03** pins provide power to PCI subsystem. These pins connect to an isolated 3.3 V I/O power plane.
PWR_04	K28, L28, P28, R28, U28, V28, Y28, AA28, AD28, AE28	P	The **Power_04** pins provide power to the DDR SDRAM controller. These pins connect to an isolated 2.5 V I/O power plane.
PWR_05	G10, G11, G14, G15, G17, G18, G20, G21, G24, G25, G26	P	The **Power_05** pins provide power to SCSI Channel [1]. These pins connect to an isolated 3.3 V I/O power plane.
GND_01	A2, A3, A33, B1, B2, B3, B34, C3, C7, C8, C11, C12, C15, C16, C19, C20, C23, C24, C27, C28, C31, D4, D32, E13, E14, E21, E22, G3, G32, H3, H32, L3, L32, M3, M32, N5, N30, P5, P30, R3, R15-R20, R32, T3, T15-T20, T32, U15-U20, V15-V20, W3, W15-W20, W32, Y3, Y15-Y20, Y32, AA5, AA30, AB5, AB30, AC3, AC32, AD3, AD32, AG3, AG32, AH3, AH32, AK13, AK14, AK21, AK22, AL3, AL4, AL31, AL32, AM3, AM4, AM7, AM8, AM11, AM12, AM15, AM16, AM19, AM20, AM23, AM24, AM27, AM28, AM31, AM32, AN1, AN2, AN33, AN34, AP2, AP33	G	The **Ground_01** pins provide common I/O ground.

Table 3.22 Power and Ground Signals[1] (Cont.)

Signal Name	BGA Position	Type	Description
GND_01-NC	B33, C32, D31	G	These pins are reserved. Do not connect these pins.
VDDC	F7, F10, B14, F20, F21, C26, H29, K29, N29, U29, AB29, AF29, AN28, AL25, AP19, AJ14, AK5, AP5, AL2, AD1, Y1, P6, L6, F3	P	**VDDC** provides power for the core logic.
VSSC	C5, A8, F15, F18, D24, D30, G29, J29, M29, T29, AA29, AE29, AP28, AJ22, AJ18, AK8, AM9, AN5, AF1, AD2, W6, T5, N6, F2	G	**VSSC** provides ground for the core logic.
VREF[2:0]	V29, AD29, L29	I	The **VREF** signals provide the 1.25 V voltage reference for the DDR SDRAM controller.
PCIPLLVDDA	AN7	P	**PCIPLLVDDA** provides analog power for the PCI PLL.
PCIPLLVSSA	AP7	G	**PCIPLLVSSA** provides analog ground for the PCI PLL.
SCSIPLLVDDA	G2	P	**SCSIPLLVDDA** provides analog power for the SCSI PLL.
SCSIPLLVSSA	G1	G	**SCSIPLLVSSA** provides analog ground for the SCSI PLL.
PCI5VBIAS	AJ26, AL5, AL7, AL18, AM26, AN15, AN17, AN19, AN22, AN25, AP24	I	Connect the PCI5VBIAS pins to 5 V in a 5 V system or to 3.3 V in a 3.3 V system.
SPARE[1:0]	AJ1, AH1	--	--
NC	A1, A4, A6, A9, A10, A23, A32, A34, B4, B7, B8, B22, B30, B32, C1, C2, C4, C22, C33, D5, D12, D16, D21, D25, D27, D33, E6, E11, E12, E17, E20, E23, E30, F4, F5, F9, F11, F12, F13, F14, F16, F17, F19, F29, G5, H2, J6, K4, K6, L5, M6, N3, N34, P29, R6, R29, T4, T6, U6, V6, W29, Y6, Y29, Y34, AB6, AB34, AC1, AC4, AC29, AD4, AD5, AE3, AE4, AE6, AF6, AG2, AG6, AG29, AH2, AH6, AH29, AJ2, AJ3, AJ6, AJ7, AJ8, AJ9, AJ10, AJ11, AJ12, AJ13, AJ16, AK2, AK3, AK6, AK7, AK9, AK10, AL1, AL6, AL9, AL10, AL33, AM1, AM2, AM5, AM6, AM33, AN3, AN4, AN8, AN31, AN32, AP1, AP3, AP15, AP31, AP32, AP34	--	No Connect.

1. To reduce signal noise that can affect FSN functionality, place a ferrite bead in series with the PCIPLLVDDA, SCSIPLLVDDA, PCIPLLVSSA, and SCSIPLLVSSA pins. LSI Logic recommends a bead with a 120 Ω at 100 MHz rating.

3.9 Power-On Sense Pins Description

For setting global operating conditions, the LSI53C1035 has 18 Power-On-Sense register bits. These bits source their data during PCI reset from the XM_DATA[7:0], XM_ADDR[7:0], and XM_RS[1:0] signals. Many of these signals cause direct hardware manipulation to occur. These signals are 3-stated, read continuously during PCI reset, and latched upon removal of PCI reset. Each signal contains an internal pull-down and senses the presence of an external 4.7 kΩ pull-up option resistor tied to the 3.3 V V_{DD_IO} power rail. To allow for programmable power-on options, provide both pull-up and pull-down options for all of the signals listed in Table 3.23.

Table 3.23 Power-On Sense Configuration Pins

Pin	Ball	Function	Pulled-Down (Default)	Pulled-Up
XM_DATA7	A27	Serial EEPROM Download Enable	Enables the download of the PCI configuration information from the serial EEPROM.	Disables the download of the PCI configuration information from the serial EEPROM.
XM_DATA6	F25	IOP Boot Disable	Enables the IOP at power-up.	Disables the IOP at power-up.
XM_DATA5	E29	Reserved		
XM_DATA4	B27	SCSI Channels	Dual Channel SCSI.	Single Channel SCSI.
XM_DATA3	A30	Test Mux Enable	Disables the Test Mux at power-up.	Enables the Test Mux at power-up.
XM_DATA2	A28	Flash ROM Size	Configures the ROM Size according to Table 3.24.	
XM_DATA1	B28			
XM_DATA0	F26	Reserved		
XM_ADDR7	D28	133 MHz PCI-X	Enables 133 MHz PCI-X.	Disables 133 MHz PCI-X.
XM_ADDR6	F23	64-bit PCI	Configures a 64-bit PCI Bus.	Configures a 32-bit PCI Bus.
XM_ADDR5	E27	66 MHz PCI	Enables 66 MHz PCI.	Disables 66 MHz PCI.
XM_ADDR4	B25	ID Mode Select	Configures the ID Control bits to set only bit [15] of the Subsystem ID register.	Configures the ID Control bits to set bit [15] of the Subsystem ID register and bit [0] of the Device ID register.
XM_ADDR3	C25	ID Control [1]	Has no effect.	Sets the PCI Function [1] bits indicated by the ID Mode pin.
XM_ADDR2	D29	ID Control [0]	Has no effect.	Sets the PCI Function [0] bits indicated by the ID Mode pin.
XM_ADDR1	A26	EEPROM Size	2 Kbytes or less.	4 Kbytes or 8 Kbytes.
XM_ADDR0	E28	Reserved.		
XM_RS1	C29	Reserved.		
XM_RS0	F27	PCI-X Mode	Enables PCI-X.	Disables PCI-X.

- **XM_DATA7, Serial EEPROM Download Enable** – By default, internal logic pulls this pin LOW to enable the download of PCI configuration information from the serial EEPROM. Pulling this pin HIGH disables the download of the PCI configuration information from the serial EEPROM. Disabling the download of PCI configuration information defaults the Subsystem Vendor ID register to 0x1000 and defaults the Subsystem ID register for the respective PCI Function to either 0x1000 if XM_ADDR[3:2] are pulled LOW, or to 0x9000 if XM_ADDR[3:2] are pulled HIGH.
- **XM_DATA6, IOP Boot Disable** – By default, internal logic pulls this pin LOW, which enables the IOP to boot at power-up and enables the LSI53C1035 to download firmware from the Flash ROM. Pulling this pin HIGH disables the IOP boot at power-up and causes the IOP to await a firmware download from the host system.
- **XM_DATA5** – Reserved.
- **XM_DATA4, SCSI Channels** – By default, internal logic pulls this pin LOW to configure the LSI53C1035 as dual channel SCSI device. Pulling this pin HIGH configures the LSI53C1035 a single channel SCSI device.
- **XM_DATA3, Test Mux Enable** – By default, internal logic pulls this pin LOW to disable the text mux. Pulling this pin HIGH enables the test mux.
- **XM_DATA[2:1], Flash ROM Size** – These pins program the size of the Flash ROM memory. Table 3.24 provides the pin encoding. By default, internal logic pulls these pins LOW to indicate that no Flash ROM is present in the system.

Table 3.24 Flash ROM Size Programming

XM_DATA[2:1]	Flash ROM Size
0b00	No Flash ROM present
0b01	Up to 1024 Kbytes
0b10	2048 Kbytes
0b11	4096 Kbytes

- **XM_DATA0** – Reserved.

- **XM_ADDR7, 133 MHz PCI-X** – By default, internal logic pulls this pin LOW to enable 133 MHz PCI-X operation and to set the 133 MHz Capable bit in the PCI-X Status register. Pulling this pin HIGH disables 133 MHz PCI-X operation and clears the 133 MHz Capable bit in the PCI-X Status register.
- **XM_ADDR6, 64-Bit PCI** – By default, internal logic pulls this pin LOW to enable 64-bit PCI operation and to set the 64-bit Enable bit in the PCI-X Status register. Pulling this pin HIGH configures the PCI connection as a 32-bit connection and clears the 64-bit Enable bit in the PCI-X Status register.
- **XM_ADDR5, 66 MHz PCI** – By default, internal logic pulls this pin LOW to enable 66 MHz PCI operation and to set the 66 MHz Capable bit in the PCI Status register. Pulling this pin HIGH disables 66 MHz PCI operation and clears the 66 MHz Capable bit in the PCI Status register.
- **XM_ADDR4, ID Mode Select** – By default, internal logic pulls this pin LOW. In the default mode, the ID Control Power-On Sense pins affect only the Subsystem ID register. Pulling this pin HIGH causes the ID Control pins to affect both the Subsystem ID and the Device ID registers.
- **XM_ADDR3, ID Control [1]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [1] Subsystem ID register or allows this bit to default to 0b0. Pulling this pin HIGH sets bit 15 to 0b1.
- **XM_ADDR2, ID Control [0]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [0] Subsystem ID register or allows this bit to default to 0b0. Pulling this pin HIGH sets bit 15 to 0b1.
- **XM_ADDR1, Serial EEPROM Size** – By default, internal logic pulls this pin LOW to indicate a serial EEPROM size of 2 Kbytes or less. Pulling this pin HIGH indicates a serial EEPROM size of either 4 Kbytes or 8 Kbytes.
- **XM_ADDR0** – Reserved.
- **XM_RS1** – Reserved.
- **XM_RS0, PCI-X Mode** – By default, internal logic pulls this pin LOW to enable the PCI-X mode. Pulling this pin HIGH disables the PCI-X mode. Pull this pin HIGH when the host board does not support the

PCI-X mode. The setting of this pin must coincide with the setting of the PCI_CAP pin on the host board. When the PCI-X mode is disabled, the PCI-X extended capabilities register structure is not visible in PCI Configuration Space.

3.10 Internal Pull-ups and Pull-downs

Table 3.25 describes the internal pull-up and pull-down signals for the LSI53C1035.

Table 3.25 Pull-up and Pull-down Conditions

Signal Name	BGA Position	Pull Type
GPIO[7:0], CLKMODE0, CLKMODE1	D3, D2, D1, G6, E3, E2, E1, H6, D26, F22	Internal Pull-down
A_LED/, B_LED/, HB_LED/	AE2, AJ4, AC6	Internal Pull-up
DIS_SCSI_FSN/, DIS_PCI_FSN/, TESTACLK, TESTHCLK, TN/	E4, AG1, E26, B23, A5	Internal Pull-up
SCAN_MODE, SCANEN, SCANRSTDIS, TM, EXTRST/, USEEXTPOR, EXTPOR/, IDDTN	C6, B6, F8, B5, AF3, AK1, AH5,E24	Internal Pull-down
RAIDMODE/, SPARE[1:0], TMS_ICE, TRST_ICE/, TDI, TMS[1], TRST/, TCK_ICE, TDI_ICE, TCK	C30, AJ1, AH1, AF5, AB3, AG5, AH4, AC5, AG4, AA6, AE1	Internal Pull-up
ISTWCLK, ISTWDATA, SerialDATA, SER_RX	A31, F28, AD6, AJ5	Internal Pull-up
SER_TX	AF2	Internal Pull-down
XM_ADDR[7:0], XM_ALE[1:0], XM_CS[2:0], XM_DATA[7:0], XM_RS[1:0], XM_WS[1:0]	D28, F23, E27, B25, C25, D29, A26, E28, E25, A25, F24, B26, B31, A27, F25, E29, B27, A30, A28, B28, F26, C29, F27, A29, B29	Internal Pull-down
PFS/	B24	Internal Pull-up
A_DDR[12:0], BA_DDR[1:0], DDR_CAS/, DDR_CLKEN[1:0], DDR_CS[1:0], DDR_DRIVEMODE, DDR_RAS/, DDR_WE/	K32, J31, U31, K33, M34, N32, M31, N33, N31, T34, T31, U32, U30, Y33, Y30, AC30, K30, J34, AD30, AD34, AP4, AD31, AC33	Internal Pull-Down

1. Connect a 4.7 kΩ external pull-up resistor to TMS.

Chapter 4
PCI Host Register Description

This chapter describes the PCI host register space. This chapter contains the following sections:

- Section 4.1, “PCI Configuration Space Registers”
- Section 4.2, “PCI I/O Space and Memory Space Registers”

The register map at the beginning of each register description provides the default bit settings for the register. Shading indicates a reserved bit or register. Do not access the reserved address areas.

There are two PCI functions on the LSI53C1035. Each PCI function has its own independent interrupt pin and its own PCI Address space. The PCI System Address space consists of three regions: Configuration Space, Memory Space, and I/O Space. PCI Configuration Space supports the identification, configuration, initialization, and error management functions for the LSI53C1035 PCI devices.

PCI Memory Space [0] and Memory Space [1] form the PCI Memory Space. PCI Memory Space [0] provides normal system accesses to memory, and PCI Memory Space [1] provides diagnostic memory accesses. PCI I/O Space provides normal system access to memory.

4.1 PCI Configuration Space Registers

This section provides bit-level descriptions of the PCI Configuration Space registers. Table 4.1 defines the PCI Configuration Space registers. A separate set of PCI Configuration Space registers exists for each PCI function.

The LSI53C1035 enables, orders, and locates the PCI-extended capability register structures (Power Management, Message Signaled Interrupts, and PCI-X) to optimize device performance. The LSI53C1035 does not hardcode the location and order of the PCI-extended capability structures. The address and location of the PCI-extended capability structures are subject to change. To access a PCI-extended capability structure, follow the pointers held in the Capability Pointer registers and identify the extended capability structure with the Capability ID register for the given structure.

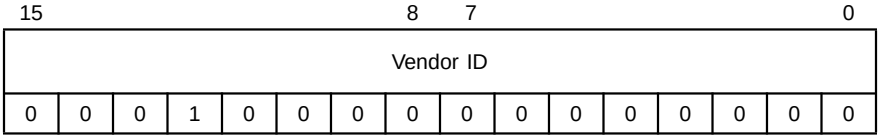
Table 4.1 LSI53C1035 PCI Configuration Space Address Map

31	24	23	16	15	8	7	0	Offset	Page
Device ID				Vendor ID				0x00	4-4
Status				Command				0x04	4-5
Class Code						Revision ID		0x08	4-8
Reserved		Header Type		Latency Timer		Cache Line Size		0x0C	4-9
I/O Base Address								0x10	4-11
Memory [0] Low								0x14	4-11
Memory [0] High								0x18	4-12
Memory [1] Low								0x1C	4-12
Memory [1] High								0x20	4-13
Reserved								0x24	--
								0x28	--
Subsystem ID				Subsystem Vendor ID				0x2C	4-14
Expansion ROM Base Address								0x30	4-16
Reserved						Capabilities Pointer		0x34	4-17
								0x38	--
Maximum Latency		Minimum Grant		Interrupt Pin		Interrupt Line		0x3C	4-18
Reserved								0x40-0x7F	--
Power Management Capabilities				PM Next Pointer		PM Capability ID			4-20
PM Data		PM BSE		Power Management Control/Status					4-22
Reserved									--
Message Control				MSI Next Pointer		MSI Capability ID			4-24
Message Address									4-26
Message Upper Address									4-26
				Message Data					4-27
Reserved									--
PCI-X Command				PCI-X Next Pointer		PCI-X Capability ID			4-28
PCI-X Status									4-30
Reserved									--

Register: 0x00–0x01

Vendor ID

Read Only



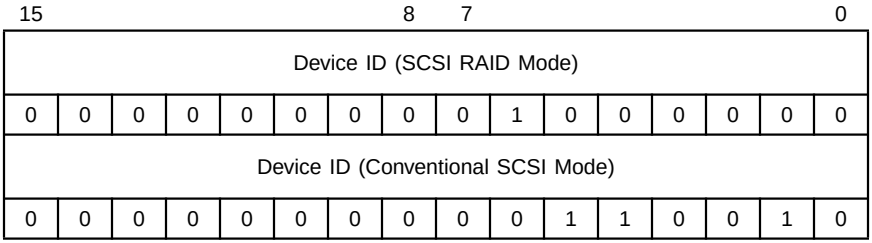
Vendor ID **[15:0]**

This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Register: 0x02–0x03

Device ID

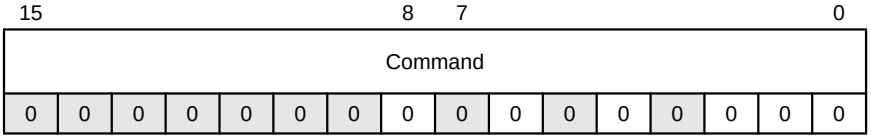
Read Only



Device ID **[15:0]**

This 16-bit register identifies the device. When the LSI53C1035 operates in the SCSI RAID mode, its default Device ID is 0x0040. When the LSI53C1035 operates in the conventional SCSI mode, its default Device ID is 0x0032. Pulling the RAIDMODE/ signal (ball C30) LOW during device reset or power-up configures the LSI53C1035 in the SCSI RAID mode.

Register: 0x04–0x05
Command
Read/Write



The Command register provides coarse control over the PCI function's ability to generate and respond to PCI cycles. Writing a zero to this register logically disconnects the LSI53C1035 PCI function from the PCI bus for all accesses except configuration accesses.

Reserved **[15:9]**
This field is reserved.

SERR/ Enable **8**
Setting this bit enables the LSI53C1035 to activate the SERR/ driver. Clearing this bit disables the SERR/ driver.

Reserved **7**
This bit is reserved.

Enable Parity Error Response **6**
Setting this bit enables the LSI53C1035 PCI function to detect parity errors on the PCI bus and report these errors to the system. Clearing this bit causes the LSI53C1035 PCI function to set the Detected Parity Error bit (bit 15 in the PCI Status register), but not assert the PERR/ signal (ball AP14) when the PCI function detects a parity error. This bit only affects parity checking. The PCI function always generates parity for the PCI bus.

Reserved **5**
This bit is reserved.

Write and Invalidate Enable **4**
Setting this bit enables the PCI function to generate write and invalidate commands on the PCI bus when operating in the conventional PCI mode.

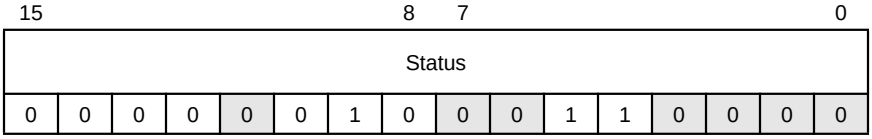
Reserved **3**
This bit is reserved.

Enable Bus Mastering **2**
Setting this bit allows the PCI function to behave as a PCI bus master. Clearing this bit disables the PCI function from generating PCI bus master accesses.

Enable Memory Space **1**
This bit controls the ability of the PCI function to respond to Memory Space accesses. Setting this bit allows the LSI53C1035 to respond to Memory Space accesses at the address range specified by the Memory [0] Low, Memory [0] High, Memory [1] Low, Memory [1] High, and the Expansion ROM Base Address registers. Clearing this bit disables the PCI function's response to PCI Memory Space accesses.

Enable I/O Space **0**
This bit controls the LSI53C1035 PCI function's response to I/O Space accesses. Setting this bit enables the PCI function to respond to I/O Space accesses at the address range the PCI Configuration Space I/O Base Address register specifies. Clearing this bit disables the PCI function's response to I/O Space accesses.

Register: 0x06–0x07
Status
Read/Write



Reads to this register behave normally. To clear a bit location that is currently set, write the bit to one (1). For example, to clear bit 15 when it is set, and not to affect any other bits, write 0x8000 to the register.

Detected Parity Error (from Slave) **15**
This bit is set according to the *PCI Local Bus Specification, Revision 2.2*, and *PCI-X Addendum* to the *PCI Local Bus Specification, Revision 1.0a*.

Signaled System Error **14**
The LSI53C1035 PCI function sets this bit when asserting the SERR/ signal (ball AN16).

Received Master Abort (from Master) **13**
A master device sets this bit when a Master Abort command terminates its transaction (except for Special Cycle).

Received Target Abort (from Master) **12**
A master device sets this bit when a Target Abort command terminates its transaction.

Reserved **11**
This bit is reserved.

DEVSEL/ Timing **[10:9]**
These two read-only bits encode the timing of DEVSEL/ and indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C1035 only supports medium DEVSEL/ timing. The possible timing values are:

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved

Data Parity Error Reported **8**
This bit is set according to the *PCI Local Bus Specification, Revision 2.2*, and the *PCI-X Addendum* to the *PCI Local Bus Specification, Revision 1.0a*. Refer to bit 0 of the PCI-X Command register for details.

Reserved **[7:6]**
This field is reserved.

66 MHz Capable **5**
The XM_ALE[1] Power-On Sense pin controls this bit. Allowing the internal pull-down to pull XM_ALE[1] LOW sets this bit and indicates to the host system that the LSI53C1035 PCI function is capable of operating at 66 MHz. Pulling XM_ALE[1] HIGH clears this bit and indicates to the host system that the LSI53C1035 PCI function is not configured to operate at 66 MHz. Refer to Section 3.9, “Power-On Sense Pins Description,” on page 3-25 for details.

New Capabilities **4**
The LSI53C1035 PCI function sets this read-only bit to indicate a list of PCI-extended capabilities such as PCI Power Management, MSI, and PCI-X support.

Reserved **[3:0]**
This field is reserved.

Register: 0x08
Revision ID
Read/Write

7							0
Revision ID							
X	X	X	X	X	X	X	X

Revision ID **[7:0]**
This register indicates the current revision level of the device.

Register: 0x09–0x0B
Class Code
Read Only

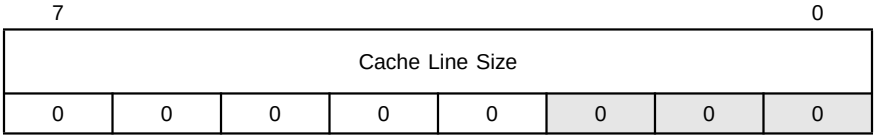
23								16	15							8	7							0
Class Code (RAID Mode)																								
0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
Class Code (Conventional SCSI Mode)																								
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Class Code **[23:0]**
This 24-bit register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface.

When the LSI53C1035 is configured as a SCSI RAID controller, the value of this register is 0x010400 to identify a RAID controller. When the LSI53C1035 is configured as a conventional SCSI controller, the value of this register is 0x010000 to identify a SCSI controller.

Register: 0x0C

Cache Line Size
Read/Write

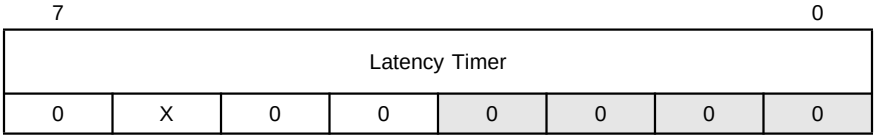


Cache Line Size **[7:3]**
This register specifies the system cache line size in units of 32-bit words. In the conventional PCI mode, the LSI53C1035 PCI function uses this register to determine whether to use the Write and Invalidate command or the Write command for performing write cycles. Programming this register to a number other than a nonzero power of two disables the use of the PCI performance commands to execute data transfers. The PCI function ignores this register when operating in the PCI-X mode.

Reserved **[2:0]**
This field is reserved.

Register: 0x0D

Latency Timer
Read/Write



Latency Timer **[7:4]**
The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. If the LSI53C1035 initializes in the PCI mode, the default value of this register is 0x00. If the LSI53C1035 initializes in the PCI-X mode, the default value of this register is 0x40.

Reserved **[3:0]**
This field is reserved.

Register: 0x0E
Header Type
Read Only

7							0
Header Type (RAID Mode)							
0	0	0	0	0	0	0	0
Header Type (Conventional SCSI Mode)							
1	0	0	0	0	0	0	0

Header Type **[7:0]**
This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also indicates whether the device is a single function or multifunction PCI device.

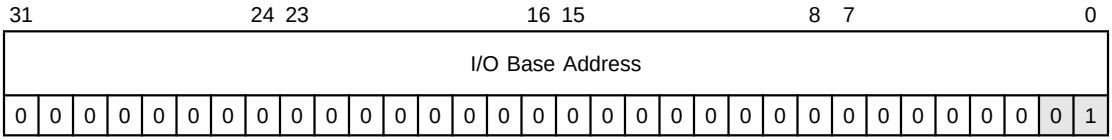
When the LSI53C1035 operates in the SCSI RAID mode, the device is a single function PCI device and bit 7 is cleared. When the LSI53C1035 operates in the conventional SCSI mode, the device is a multifunction PCI device and bit 7 is set.

Register: 0x0F
Reserved

7							0
Reserved							
0	0	0	0	0	0	0	0

Reserved **[7:0]**
This register is reserved.

Register: 0x10–0x13
I/O Base Address
Read/Write

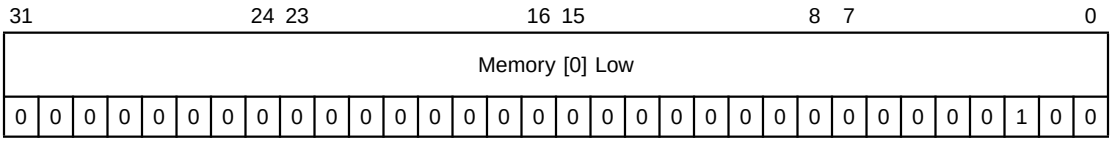


The I/O Base Address register maps the operating register set into I/O Space. The LSI53C1035 requires 256 bytes of I/O Space for this base address register. Hardware sets bit 0 to 0b1. Bit 1 is reserved and returns 0b0 on all reads.

I/O Base Address **[31:2]**
This field contains the I/O Base address.

Reserved **[1:0]**
This field is reserved.

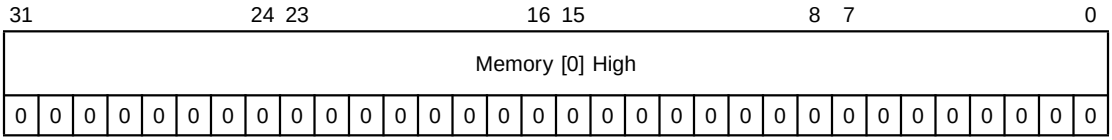
Register: 0x14–0x17
Memory [0] Low
Read/Write



The Memory [0] Low register and the Memory [0] High register map the SCSI operating registers into Memory Space [0]. This register contains the lower 32 bits of the Memory Space [0] base address. Hardware programs bits [9:0] to 0b0000000100, which indicates that the Memory Space [0] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1035 requires 1024 bytes of memory space.

Memory [0] Low **[31:0]**
This field contains the Memory [0] Low address.

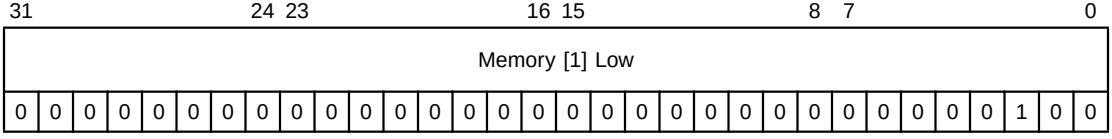
Register: 0x18–0x1B
Memory [0] High
Read/Write



The Memory [0] High register and the Memory [0] Low register map the SCSI operating registers into Memory Space [0]. This register contains the upper 32 bits of the Memory Space [0] base address. The LSI53C1035 requires 1024 bytes of memory space.

Memory [0] High **[31:0]**
This field contains the Memory [0] High address.

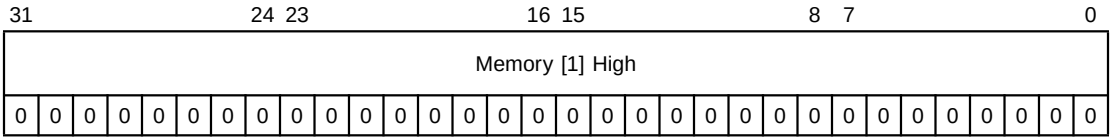
Register: 0x1C–0x1F
Memory [1] Low
Read/Write



The Memory [1] Low register and the Memory [1] High register map the RAM into Memory Space [1]. This register contains the lower 32 bits of the Memory Space [1] base address. Hardware programs bits [12:0] to 0b0000000000100, which indicates that the Memory Space [1] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1035 requires 64 Kbytes of memory for Memory Space [1].

Memory [1] Low **[31:0]**
This field contains the Memory [1] Low address.

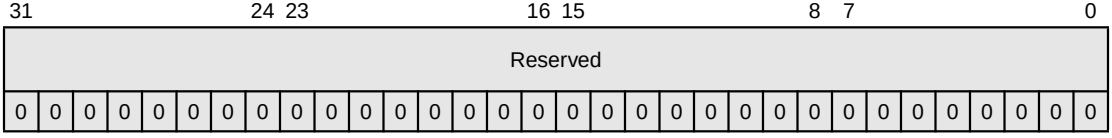
Register: 0x20–0x23
Memory [1] High
Read/Write



The Memory [1] High register and the Memory [1] Low register map the RAM into Memory Space [1]. This register contains the upper 32 bits of the Memory Space [1] base address. The LSI53C1035 requires 64 Kbytes of memory for Memory Space [1].

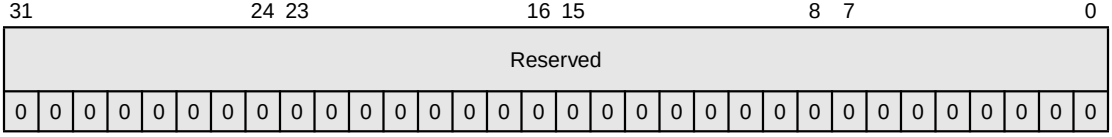
Memory [1] High **[31:0]**
This field contains the Memory [1] High address.

Register: 0x24–0x27
Reserved



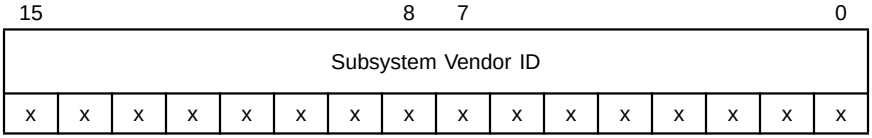
Reserved **[31:0]**
This register is reserved.

Register: 0x28–0x2B
Reserved



Reserved **[31:0]**
This register is reserved.

Register: 0x2C–0x2D
Subsystem Vendor ID
Read Only



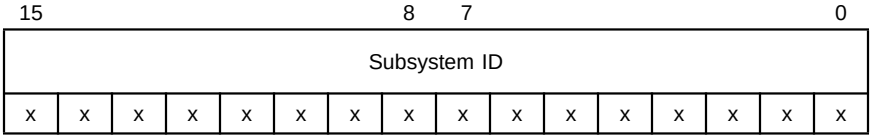
Subsystem Vendor ID **[15:0]**

This 16-bit register uniquely identifies the vendor that manufactures the add-in board or subsystem where the LSI53C1035 resides. This register provides a mechanism for an add-in card vendor to distinguish its cards from another vendor's cards, even if the cards use the same PCI controller (and have the same Vendor ID and Device ID).

The external serial EEPROM can hold a vendor-specific, 16-bit value for this register, which the board designer must obtain from the PCI Special Interest Group (PCI-SIG). By default, an internal pull-down on the XM_CS[7] Power-On Sense pin enables autodownload from the serial EEPROM so that the LSI53C1035 can load this register from the serial EEPROM at power-up. If the download from the EEPROM fails, this register contains 0x0000.

If the board designer disables autodownload from the EEPROM by pulling the XM_CS[7] Power-On Sense pin HIGH, this register returns a value of 0x1000. Refer to Section 3.9, "Power-On Sense Pins Description," on page 3-25, for details.

Register: 0x2E–0x2F
Subsystem ID
Read Only



Subsystem ID **[15:0]**

This 16-bit register uniquely identifies the add-in board or subsystem where this PCI device resides. This register provides a mechanism for an add-in card vendor to distinguish its cards from one another, even if the cards use the same PCI controller (and have the same Vendor ID and Device ID). The board designer can store a vendor-specific, 16-bit value in an external serial EEPROM.

The ID Control Power-On Sense pins (XM_ADDR[3] for PCI Function [1], XM_ADDR[2] for PCI Function [0]) and the Serial EEPROM Download Enable Power-On Sense pin (XM_DATA[7]) control the value of bit [15] of this register. These pins have internal pull-downs. Allowing XM_DATA[7] to remain internally pulled down enables autodownload from the serial EEPROM and permits the LSI53C1035 to load this register from the serial EEPROM at power up. Pulling XM_DATA[7] HIGH disables autodownload from the serial EEPROM. Allowing the ID Control pins to remain internally pulled LOW has no effect on this register. Pulling the ID Control pins HIGH sets bit [15] of this register for the given PCI function. Pulling the ID Control pins HIGH takes precedence over all other settings for bit [15].

Table 4.2 lists the configuration options for the Power-On Sense pins and settings for this register. If autodownload from the serial EEPROM is disabled and the ID Control pins are internally pulled LOW, this register contains 0x1000. If the autodownload from serial EEPROM is disabled and the ID Control pins are pulled HIGH, this register contains 0x8000. If a download from the serial EEPROM fails and the ID Control pins are internally pulled LOW, this register contains 0x0000. If a download from the serial EEPROM fails and the ID Control pins are pulled HIGH, this register contains 0x8000. Refer to Section 3.9, “Power-On Sense Pins Description,” on page 3-25, for details.

Table 4.2 Subsystem ID Register Download Conditions and Values

XM_DATA[7] State	XM_ADDR[3] or XM_ADDR[2] LOW	XM_ADDR[3] or XM_ADDR[2] HIGH
XM_DATA[7] LOW	Subsystem ID = 0xXXXX Bits [15:0] are downloaded.[1] (Default)	Subsystem ID = 0b1XXXXXXXXXXXXXXX Bits [14:0] are downloaded with Bit [15] set.[2]
XM_DATA[7] HIGH	Subsystem ID = 0x1000.	Subsystem ID = 0x8000.

1. The Subsystem ID register returns 0x0000 if the serial EEPROM download fails.
2. The Subsystem ID register returns 0x8000 if the serial EEPROM download fails.

Register: 0x30–0x33
Expansion ROM Base Address
Read/Write

31								24	23							16	15							8	7							0
Expansion ROM Base Address																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This four-byte register contains the base address and size information for the expansion ROM.

Expansion ROM Base Address [31:11]
These bits correspond to the upper 21 bits of the expansion ROM base address. The host system detects the size of the external memory by first writing 0xFFFFFFFF to this register and then reading the register back. The LSI53C1035 responds with zeros in all don't care locations. The least significant one (1) that remains represents the binary version of the external memory size. For example, to indicate an external memory size of 32 Kbytes, this register returns ones in the upper 17 bits when written with 0xFFFFFFFF and read back.

Reserved [10:1]
This field is reserved.

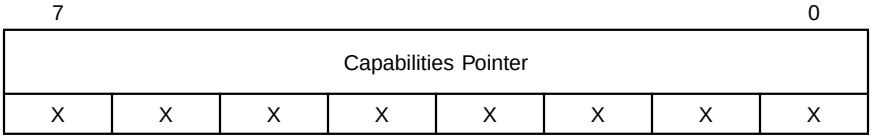
Expansion ROM Enable **0**

This bit controls whether the device accepts accesses to its expansion ROM. Setting this bit enables address decoding. Depending on the system configuration, the device can optionally use an expansion ROM. Note that to access the expansion ROM, the user also must set bit 1 in the PCI Command register.

Register: 0x34

Capabilities Pointer

Read Only

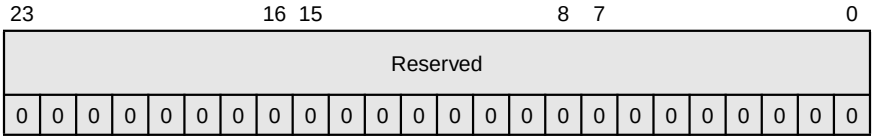


Capabilities Pointer **[7:0]**

This register indicates the location of the first extended capabilities register in PCI Configuration Space. The value of this register varies according to system configuration.

Register: 0x35–0x37

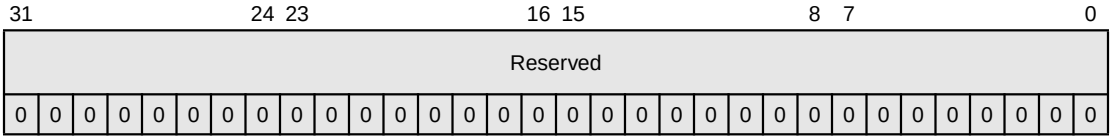
Reserved



Reserved **[23:0]**

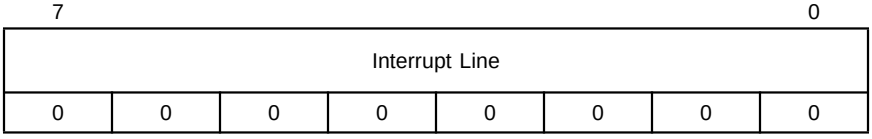
This register is reserved.

Register: 0x38–0x3B
Reserved



Reserved **[31:0]**
This register is reserved.

Register: 0x3C
Interrupt Line
Read/Write



Interrupt Line **[7:0]**
This register communicates interrupt line routing information. Power-On-Self-Test (POST) software writes the routing information into this register as it configures the system. This register indicates the system interrupt controller input to which this PCI function's interrupt pin connects. System architecture determines the values in this register.

Register: 0x3D

Interrupt Pin

Read Only

7							0
Function [0] Interrupt Pin							
0	0	0	0	0	0	0	1
Function [1] Interrupt Pin							
0	0	0	0	0	0	1	0

Interrupt Pin **[7:0]**

The encoding of this read-only register is unique to each function on the LSI53C1035. It indicates which interrupt pin the function uses. The value for Function [0] is 0x01, which indicates that Function [0] presents interrupts on INTA/. The value for Function [1] is 0x02, which indicates that Function [1] presents interrupts on INTB/.

Register: 0x3E

Minimum Grant

Read Only

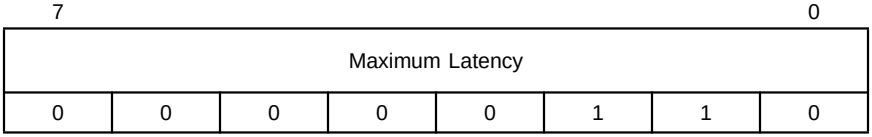
7							0
Minimum Grant							
0	0	0	1	0	0	0	0

Min_Gnt **[7:0]**

This register specifies the desired settings for the latency timer values in units of 0.25 µs. Min_Gnt specifies how long of a burst period the device needs. The LSI53C1035 sets this register to 0x10, indicating a burst period of 4.0 µs.

Register: 0x3F

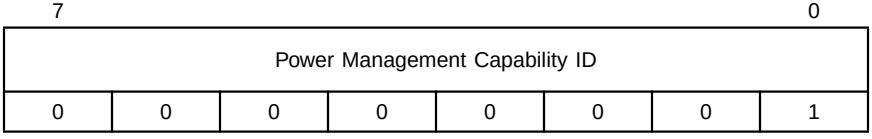
Maximum Latency
Read Only



Max_Lat **[7:0]**
This register specifies the desired settings for the latency timer values in units of 0.25 µs. Max_Lat specifies how often the device needs to gain access to the PCI bus. The LSI53C1035 sets this register to 0x06 because it requires the PCI bus every 1.5 µs to maintain a data transfer rate of 320 Mbytes/s.

Register: 0xXX

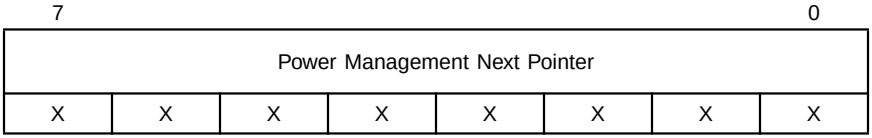
Power Management Capability ID
Read Only



Power Management Capability ID **[7:0]**
This register indicates the type of the current data structure. It is set to 0x01 to indicate the Power Management Data Structure.

Register: 0xXX

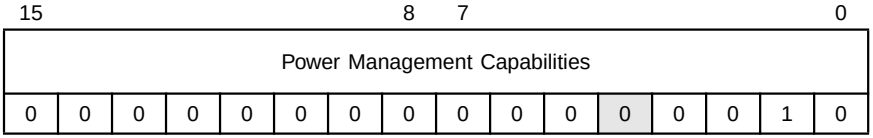
Power Management Next Pointer
Read Only



Power Management Next Pointer **[7:0]**
This register contains the pointer to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX

Power Management Capabilities
Read Only



PME_Support **[15:11]**
This field defines the power management states in which the device asserts the Power Management Event (PME) pin. The LSI53C1035 clears these bits because the LSI53C1035 does not provide a PME signal.

D2_Support **10**
The PCI function sets this bit because the LSI53C1035 supports power management state D2.

D1_Support **9**
The PCI function sets this bit because the LSI53C1035 supports power management state D1.

Aux_Current **[8:6]**
The PCI function clears this field because the LSI53C1035 does not support Aux_Current.

Device-Specific Initialization **5**
The PCI function clears this bit because no special initialization is required before a generic class device driver can use it.

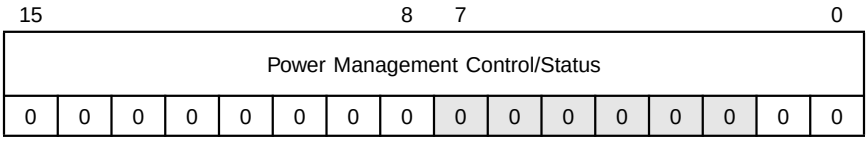
Reserved **4**
This bit is reserved.

PME Clock **3**
The LSI53C1035 clears this bit because the chip does not provide a PME pin.

Version **[2:0]**
The PCI function programs this field to 0b010 to indicate that the LSI53C1035 complies with the *PCI Bus Power Management Interface Specification, Revision 1.1*.

Register: 0xXX

Power Management Control/Status
Read/Write



PME_Status **15**
The PCI function clears this bit because the LSI53C1035 does not support PME signal generation from $D3_{cold}$.

Data_Scale **[14:13]**
The PCI function clears this field because the LSI53C1035 does not support the Power Management Data register.

Data_Select **[12:9]**
The PCI function clears this field because the LSI53C1035 does not support the Power Management Data register.

PME_Enable **8**
The PCI function clears this bit because the LSI53C1035 does not provide a PME signal and disables PME assertion.

Reserved **[7:2]**
This field is reserved.

Power State **[1:0]**
This field determines the current power state of the LSI53C1035. The power states are:

0b00	D0
0b01	D1
0b10	D2
0b11	$D3_{hot}$

Register: 0xXX

Power Management Bridge Support Extensions
Read Only

7							0
Power Management Bridge Support Extensions							
0	0	0	0	0	0	0	0

Power Management Bridge Support Extensions [7:0]
This register indicates PCI Bridge specific functionality. The LSI53C1035 always returns 0x00 in this register.

Register: 0xXX

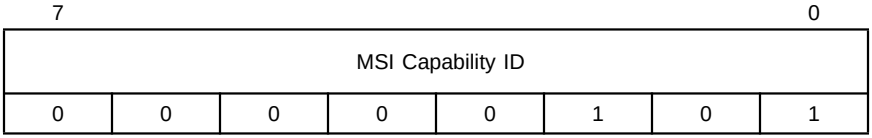
Power Management Data
Read Only

7							0
Power Management Data							
0	0	0	0	0	0	0	0

Power Management Data **[7:0]**
This register provides an optional mechanism for the PCI function to report state-dependent operating data. The LSI53C1035 always returns 0x00 in this register.

Register: 0xXX

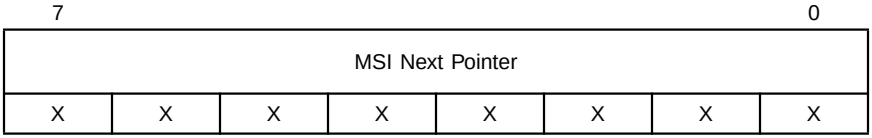
MSI Capability ID
Read Only



MSI Capability ID **[7:0]**
This register indicates the type of the current data structure. This register always returns 0x05, indicating Message Signaled Interrupts (MSI).

Register: 0xXX

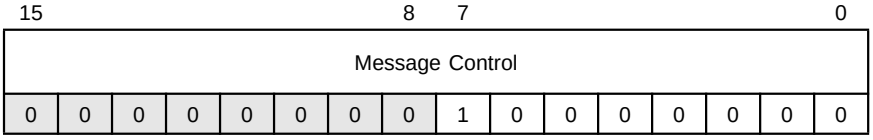
MSI Next Pointer
Read Only



MSI Next Pointer **[7:0]**
This register points to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX

Message Control
Read/Write



Reserved **[15:8]**
This field is reserved.

64-Bit Address Capable **7**

The PCI function sets this read-only bit to indicate support of a 64-bit message address.

Multiple Message Enable **[6:4]**

This read/write field indicates the number of messages that the host allocates to the LSI53C1035. The host system software allocates all or a subset of the requested messages by writing to this field. The number of allocated request messages must align to a power of two. The following table provides the bit encoding of this field.

Bits [6:4] Encoding	Number of Allocated Messages
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	Reserved
0b111	Reserved

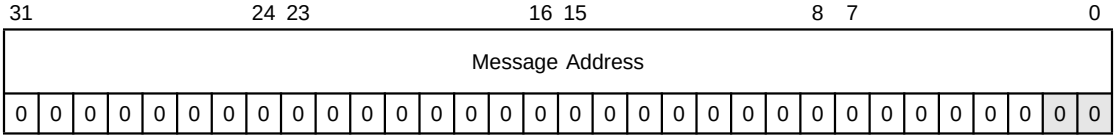
Multiple Message Capable **[3:1]**

This read-only field indicates the number of messages that the LSI53C1035 requests from the host. The host system software reads this field to determine the number of requested messages. The number of requested messages must align to a power of two. The LSI53C1035 sets this field to 0b000 to request one message. All other encodings of this field are reserved.

MSI Enable **0**

System software sets this bit to enable MSI. Setting this bit enables the device to use MSI to interrupt the host and request service. Setting this bit also prohibits the device from using the interrupt pins to request service from the host. Setting this bit to mask interrupts on the interrupt pins is a violation of the PCI specification.

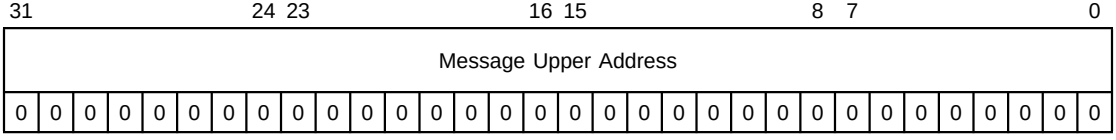
Register: 0xXX
Message Address
Read/Write



Message Address **[31:2]**
This register contains message address bits [31:2] for the MSI memory write transaction. The host system specifies and dword aligns the message address. During the address phase, the LSI53C1035 drives Message Address [1:0] to 0b00.

Reserved **[1:0]**
This field is reserved.

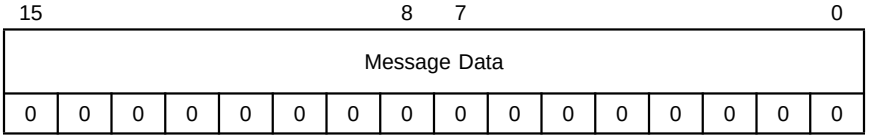
Register: 0xXX
Message Upper Address
Read/Write



Message Upper Address **[31:0]**
The LSI53C1035 supports 64-bit MSI. This register contains the upper 32 bits of the 64-bit message address, which the system specifies. The host system software can program this register to 0x0000 to force the PCI function to generate 32-bit message addresses.

Register: 0xXX

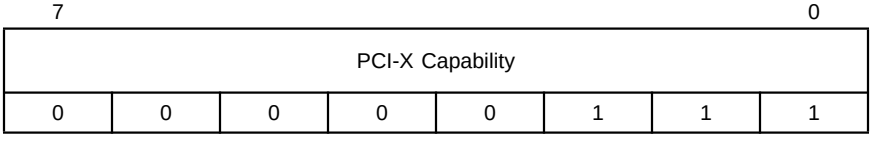
Message Data
Read/Write



Message Data **[15:0]**
System software initializes this register by writing to it. The LSI53C1035 sends an interrupt message by writing a dword to the address held in the Message Address and Message Upper Address registers. This register forms bits [15:0] of the dword message that the PCI function passes to the host. The PCI function drives bits [31:16] of this message to 0x0000.

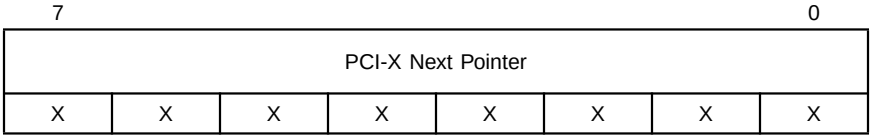
Register: 0xXX

PCI-X Capability ID
Read Only



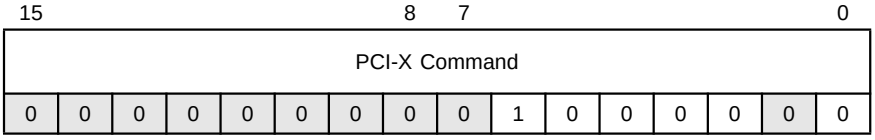
PCI-X Capability ID **[7:0]**
This register indicates the type of the current data structure. This register returns 0x07, indicating the PCI-X Data Structure.

Register: 0xXX
PCI-X Next Pointer
Read Only



PCI-X Next Capabilities Pointer **[7:0]**
This register points to the next item in the device's capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
PCI-X Command
Read/Write



Reserved **[15:7]**
This field is reserved.

Maximum Outstanding Split Transactions **[6:4]**
This field indicates the maximum number of split transactions the LSI53C1035 can have outstanding at one time. The LSI53C1035 uses the most recent value of this register each time it prepares a new sequence. Note that if the LSI53C1035 prepares a sequence before the setting of this field changes, the PCI function initiates the prepared sequence with the previous setting. The following table provides the bit encodings for this field.

Bits [6:4] Encoding	Maximum Outstanding Split Transactions
0b000	1
0b001	2
0b010	3
0b011	4
0b100	8
0b101	Reserved
0b110	Reserved
0b111	Reserved

Maximum Memory Read Byte Count **[3:2]**
This field indicates the maximum byte count the LSI53C1035 uses when initiating a sequence with one of the burst memory read commands. The following table provides the bit encodings for this field.

Bits [3:2] Encoding	Maximum Memory Read Byte Count
0b00	512
0b01	1024
0b10	2048
0b11	Reserved

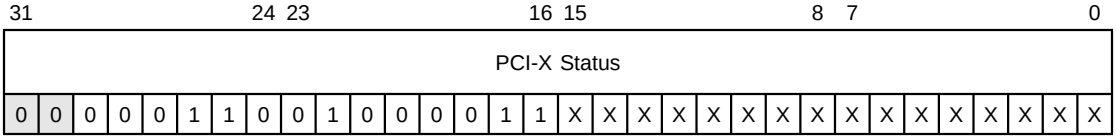
Reserved **1**
This bit is reserved.

Data Parity Error Recovery Enable **0**
The host device driver sets this bit to allow the LSI53C1035 to attempt to recover from data parity errors. If the user clears this bit and the LSI53C1035 is operating in the PCI-X mode, the LSI53C1035 asserts SERR/ whenever the Master Data Parity Error bit in the PCI Status register is set.

Register: 0xXX

PCI-X Status

Read/Write



Reserved **[31:30]**

This field is reserved.

Received Split Completion Error Message **29**

The LSI53C1035 sets this bit upon receipt of a split completion message if the split completion error attribute bit is set. Write a one (1) to this bit to clear it.

Designed Maximum Cumulative Read Size **[28:26]**

This read-only field indicates a number greater than or equal to the maximum cumulative size of all outstanding burst memory read transactions for the LSI53C1035 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1035 reports 0b001 in this field to indicate a designed maximum cumulative read size of 2 Kbytes.

Designed Maximum Outstanding Split Transactions **[25:23]**

This read-only field indicates a number greater than or equal to the maximum number of all outstanding split transactions for the LSI53C1035 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1035 reports 0b100 in this field to indicate that the designed maximum number of outstanding split transactions is eight.

Designed Maximum Memory Read Byte Count **[22:21]**

This read-only field indicates a number greater than or equal to the maximum byte count for the LSI53C1035 device. The PCI function uses this count to initiate a sequence with one of the burst memory read commands. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1035 reports 0b10 in this field to indicate that the designed maximum memory read byte count is 2048.

Device Complexity **20**
The PCI function clears this read-only bit to indicate that the LSI53C1035 is a simple device.

Unexpected Split Completion **19**
The PCI function sets this read-only bit when it receives an unexpected split completion. When set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

Split Completion Discarded **18**
The PCI function sets this read-only bit when it discards a split completion. When set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

133 MHz Capable **17**
The XM_ADDR[7] Power-On Sense pin controls this read-only bit. Allowing the internal pull-down to pull XM_ADDR[7] LOW sets this bit and enables 133 MHz operation of the PCI-X bus. Pulling XM_ADDR[7] HIGH clears this bit and disables 133 MHz operation of the PCI-X bus. Refer to Section 3.9, “Power-On Sense Pins Description,” on page 3-25 for details on the Power-On Sense pins.

64-Bit Device **16**
The XM_ADDR[6] Power-On Sense pin controls this read-only bit. Allowing the internal pull-down to pull XM_ADDR[6] LOW sets this bit and indicates a 64-bit PCI Address/Data bus. Pulling XM_ADDR[6] HIGH clears this bit and indicates a 32-bit PCI Address/Data bus. If using the LSI53C1035 on an add-in card, this bit must indicate the size of the card’s PCI Address/Data bus. Refer to Section 3.9, “Power-On Sense Pins Description,” for details on the Power-On Sense pins.

Bus Number **[15:8]**
This read-only field indicates the number of the LSI53C1035 bus segment. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Device Number **[7:3]**
This read-only field indicates the device number of the LSI53C1035. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Function Number **[2:0]**
This read-only field indicates the number in the Function Number field (AD[10:8]) of a Type 0 PCI configuration transaction. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

4.2 PCI I/O Space and Memory Space Registers

This section describes the host interface registers in the PCI I/O Space and PCI Memory Space. These address spaces contain the Fusion-MPT host interface register set. PCI Memory Space [0] and PCI Memory Space [1] form the PCI Memory Space. PCI Memory [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. For all registers except the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers, access the address offset through either PCI I/O Space or PCI Memory Space [0]. Access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers is only through PCI I/O Space.

When the LSI53C1035 operates as a multifunction PCI device, the entire PCI I/O Space and PCI Memory Space register sets are visible to both PCI functions. When the LSI53C1035 operates as a single function PCI device, only PCI Function [0] register sets are accessible.

Table 4.3 defines the PCI I/O Space address map.

Table 4.3 PCI I/O Space Address Map

31 16 15 0	Offset	Page
System Doorbell	0x0000	4-34
Write Sequence	0x0004	4-35
Host Diagnostic	0x0008	4-36
Test Base Address	0x000C	4-38
Diagnostic Read/Write Data	0x0010	4-39
Diagnostic Read/Write Address	0x0014	4-40
Reserved	0x0018–0x002F	–
Host Interrupt Status	0x0030	4-41
Host Interrupt Mask	0x0034	4-42
Reserved	0x0038–0x003F	–
Request FIFO	0x0040	4-43
Reply FIFO	0x0044	4-43
Reserved	0x0048–0x007F	–

Table 4.4 defines the PCI Memory Space [0] address map.

Table 4.4 PCI Memory [0] Address Map

31 16 15 0	Offset	Page
System Doorbell	0x0000	4-34
Write Sequence	0x0004	4-35
Host Diagnostic	0x0008	4-36
Test Base Address	0x000C	4-38
Reserved	0x0010–0x002F	–
Host Interrupt Status	0x0030	4-41
Host Interrupt Mask	0x0034	4-42
Reserved	0x0038–0x003F	–
Request FIFO	0x0040	4-43
Reply FIFO	0x0044	4-43
Reserved	0x0048–0x007F	–
Shared Memory	0x0080– 0x(Sizeof(Mem0)-1)	–

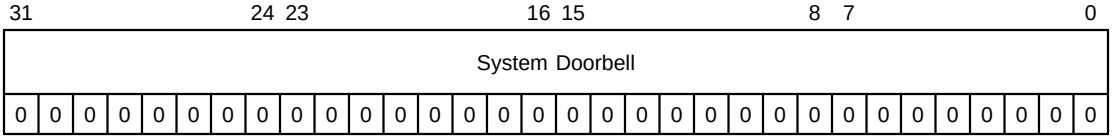
Table 4.5 defines the PCI Memory Space [1] address map.

Table 4.5 PCI Memory [1] Address Map

31 16 15 0	
Diagnostic Memory	0x0000 - 0x(Sizeof(Mem1)-1)

A bit level description of the PCI Memory and PCI I/O Spaces follows.

Register: 0x00
System Doorbell
Read/Write



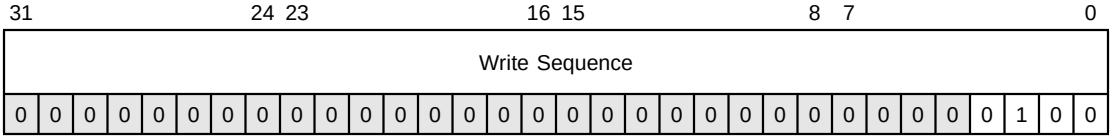
The System Doorbell register is a simple message passing mechanism that allows the system to pass single word messages to the embedded IOP processor and vice versa. There is a unique system doorbell for each PCI function.

When a host system PCI master writes to the Host Registers->Doorbell register, the LSI53C1035 generates a maskable interrupt to the IOP. The value written by the host system is available for the IOP to read in the System Interface Registers->Doorbell register. The IOP clears the interrupt status after reading the value.

Conversely, when the IOP writes to the System Interface Registers->Doorbell register, the LSI53C1035 generates a maskable interrupt to the PCI system. The host system can read the value written by the IOP in the Host Registers->Doorbell register. The host system clears the interrupt status bit and interrupt pin by writing any value to the Host Registers->Interrupt Status register.

Host Doorbell Value **[31:0]**
During a write, this register contains the doorbell value that the host system passes to the IOP. During a read, this register contains the doorbell value that the IOP passes to the host system.

Register: 0x04
Write Sequence
Read/Write

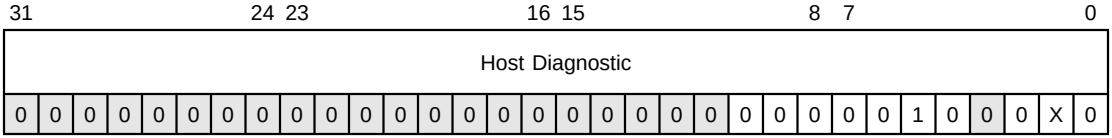


The Write Sequence register provides a protection mechanism against inadvertent writes to the Host Diagnostic register. There is one Write Sequence register that is visible to both PCI functions. The two PCI functions physically share this register.

Reserved **[31:4]**
This field is reserved.

Write Sequence Key **[3:0]**
To enable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic registers, perform five data-specific writes to the Write Sequence Key. Writing an incorrect value to the Write Sequence Key invalidates the key sequence and the host must rewrite the entire sequence. The Write Sequence Key is: 0x0004, 0x000B, 0x0002, 0x0007, and 0x000D. To disable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic registers, write any value except the Write Sequence Key sequence to the Write Sequence register. The Diagnostic Write Enable bit (bit 7 in the Host Diagnostic register), indicates the write access status.

Register: 0x08
Host Diagnostic
Read/Write



The Host Diagnostic register contains diagnostic controls and status information. There is one Host Diagnostic register that is visible to both PCI functions. The two PCI functions physically share this register. However, the Reset History bit operates independently for each PCI function. This register can only be written when bit 7 of this register is set.

Reserved **[31:11]**
This field is reserved.

Clear Bad Flash Signature **10**
Setting this bit resets the Flash signature recognition latch. This bit is self-clearing.

Prevent IOP Boot **9**
The host sets this bit to prevent the IOP from restarting following an adapter reset.

BIST Complete **8**
The LSI53C1035 sets this read-only bit when all internal built-in self-test (BIST) operations complete.

Diagnostic Write Enable **7**
The LSI53C1035 sets this read-only bit when the host writes the correct Write Sequence Key to the Write Sequence register. The LSI53C1035 clears this bit when the host writes a value other than the Write Sequence Key to the Write Sequence register.

Flash Bad Signature **6**
The LSI53C1035 sets this bit if the IOP ARM946E processor encounters a bad Flash signature when booting from Flash ROM. The LSI53C1035 also sets the DisARM bit (bit 1 in this register) to hold the IOP ARM processor in a reset state. The LSI53C1035 maintains this state until the PCI host clears both the Flash Bad Signature and DisARM bits.

Reset History **5**
The LSI53C1035 sets this bit if it experiences a Power On Reset (POR), PCI Reset, or TestReset/. A host driver can clear this bit to help coordinate recovery between multiple driver instances in a multifunction PCI implementation.

Diagnostic Read/Write Enable 4
Setting this bit enables access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers.

Reserved **3**
This bit is reserved.

Reset Adapter **2**
Setting this write-only bit causes a hard reset within the LSI53C1035. The bit self-clears after eight PCI clock periods. After deasserting this bit, the IOP ARM processor executes from its default reset vector.

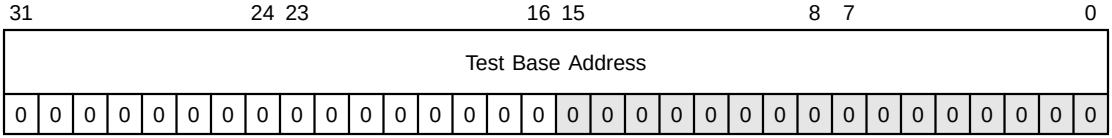
DisARM **1**
Setting this bit holds the IOP ARM processor in a reset state.

Diagnostic Memory Enable **0**
Setting this bit enables diagnostic memory accesses through PCI Memory Space [1]. Clearing this bit disables diagnostic memory accesses to PCI Memory Space [1] and returns 0xFFFF on reads.

Register: 0x0C

Test Base Address

Read/Write

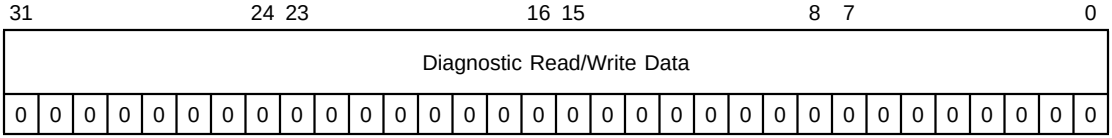


The Test Base Address register specifies the base address for Memory Space [1] accesses. There is one Test Base Address register that is visible to both PCI functions. The two PCI functions physically share this register. Because Diagnostic Memory is visible only to PCI Function [0], PCI Function [1] cannot write to this register.

Test Base Address **[31:16]**
The number of significant bits in this field is determined by the size of the PCI Memory Space [1] in the serial EEPROM.

Reserved **[15:0]**
This field is reserved.

Register: 0x10
Diagnostic Read/Write Data
Read/Write



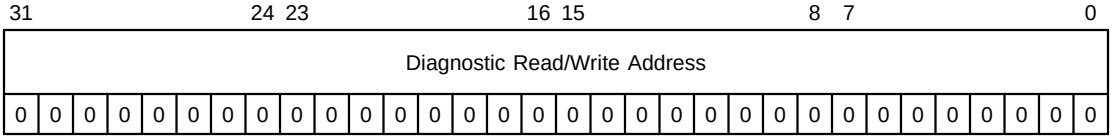
The Diagnostic Read/Write Data register reads or writes dword locations on the LSI53C1035 internal bus. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write Sequence Key to the Write Sequence register and setting bit 4 (the Diagnostic Read/Write Enable bit) of the Host Diagnostic register. A write of any value other than the correct Write Sequence Key to the Write Sequence register disables write access to this register. There is one Diagnostic Read/Write Data register that is visible to both PCI functions. The two PCI functions physically share this register.

Diagnostic Read/Write Data **[31:0]**
Using this register, the LSI53C1035 reads/writes data at the address that the Diagnostic Read/Write Address register specifies.

Register: 0x14

Diagnostic Read/Write Address

Read/Write



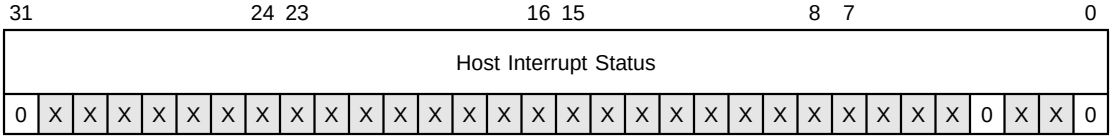
The Diagnostic Read/Write Address register specifies a dword location on the internal bus. The address increments by a dword whenever the host system accesses the Diagnostic Read/Write Address register. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write Sequence Key to the Write Sequence register and setting bit 4 (the Diagnostic Read/Write Enable bit) of the Host Diagnostic register. A write of any value other than the correct Write Sequence Key to the Write Sequence register disables write access to this register. There is one Diagnostic Read/Write Address register that is visible to both PCI functions. The two PCI functions physically share this register.

Diagnostic Read/Write Address **[31:0]**
The Diagnostic Read/Write Data register writes data to or reads data from the address that this register holds.

Register: 0x30

Host Interrupt Status

Read/Write



The Host Interrupt Status register provides read-only interrupt status information to the PCI Host. A write to this register of any value clears the associated System Doorbell interrupt. There is a unique Host Interrupt Status register for each PCI function.

IOP Doorbell Status **31**

The LSI53C1035 sets this bit when the IOP receives a message from the system doorbell but has yet to process it. The IOP processes the System Doorbell message by clearing the corresponding system request interrupt.

Reserved **[30:4]**

This field is reserved.

Reply Interrupt **3**

The LSI53C1035 sets this bit when the Reply Post FIFO is not empty. The LSI53C1035 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

Reserved **[2:1]**

This field is reserved.

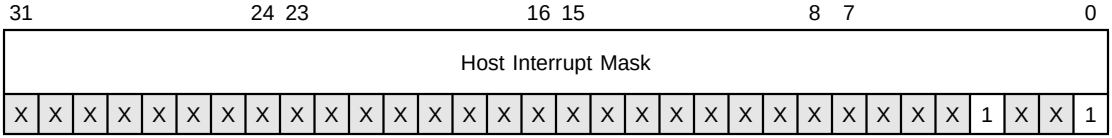
System Doorbell Interrupt **0**

The LSI53C1035 sets this bit when the IOP writes a value to the System Doorbell. The host can clear this bit by writing any value to this register. The LSI53C1035 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

Register: 0x34

Host Interrupt Mask

Read/Write



The Host Interrupt Mask register masks and/or routes the interrupt conditions that the Host Interrupt Mask register reports. There is a unique Host Interrupt Mask register for each PCI function.

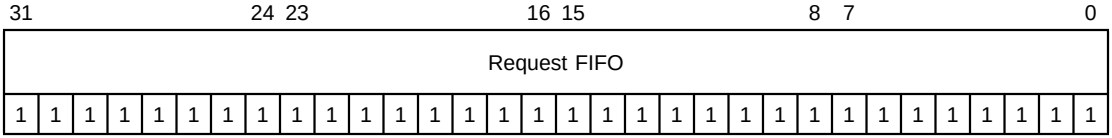
Reserved **[31:4]**
This field is reserved.

Reply Interrupt Mask **3**
Setting this bit masks reply interrupts and prevents the assertion of a PCI interrupt for all reply interrupt conditions.

Reserved **[2:1]**
This field is reserved.

Doorbell Interrupt Mask **0**
Setting this bit masks System Doorbell interrupts and prevents the assertion of a PCI interrupt for all System Doorbell interrupt conditions.

Register: 0x40
Request FIFO
Write Only



The Request FIFO accepts Request Post MFAs from the host system on writes. There is one Request FIFO register that is visible to both PCI functions. The two PCI functions physically share this register.

Request FIFO **[31:0]**
For writes, this register contains the Request Post MFA.

Register: 0x44
Reply FIFO
Read/Write

The Reply FIFO provides Reply Post MFAs to the host system on reads and accepts Reply Free MFAs from the host system on writes. There is a unique Reply FIFO register for each PCI function.

Reply FIFO **[31:0]**
For reads, this register contains the Reply Message Frame descriptor. For writes, the register contains the Reply Free MFA.

Chapter 5
Specifications

This chapter specifies the LSI53C1035 electrical and mechanical characteristics. This chapter contains the following sections:

- Section 5.1, “DC Characteristics”
- Section 5.2, “TolerANT Technology Electrical Characteristics”
- Section 5.3, “AC Characteristics”
- Section 5.4, “External Memory Timing Diagrams”
- Section 5.5, “Package Drawings”

Refer to the *PCI Local Bus Specification*, the *PCI-X Addendum* to the *PCI Local Bus Specification*, and the *SCSI Parallel Interface-4 Specification* for PCI, PCI-X, and SCSI timings and timing diagrams. The LSI53C1035 timings conform to the timings these specifications provide.

5.1 DC Characteristics

This section describes the LSI53C1035 DC characteristics. The information presented in this section is for RAID mode operation. Tables 5.1 through 5.14 give current and voltage specifications. Figures 5.1 and 5.2 are LVD transceiver schematics.

Table 5.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage Temperature	–40	125	°C	–
$V_{DD\text{-}Core}$	Core Supply Voltage	–0.3	2.2	V	–
$V_{DD\text{-}IO}$	I/O Supply Voltage	–0.3	3.9	V	–
$V_{DD\text{-}DDR}$	DDR Supply Voltage	–0.3	3.10	V	–
V_{IN}	Input Voltage	–0.5	V_{DD} + 0.5	V	–
I_{LP}[2]	Latch-up Current	±150	–	mA	–2 V < V_{PIN} < 8 V
T[2]	Lead Temperature	–	125	°C	–
ESD[2]	Electrostatic Discharge	–	2000	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above can damage the device. These are stress ratings only; functional operation of the device at or beyond these values is not implied.
2. SCSI pins only.

Table 5.2 Operating Conditions[1]

Symbol	Parameter	Min	Nominal	Max	Unit	Test Conditions
$V_{DD\text{-}Core}$	Core and Analog Supply Voltage	1.71	1.80	1.89	V	–
$V_{DD\text{-}IO}$	I/O Supply Voltage	3.14	3.3	3.47	V	–
$V_{DD\text{-}DDR}$	DDR Supply Voltage	2.25	2.5	2.75	V	–
$I_{DD\text{-}Core}$	Core and Analog Supply Current (dynamic)[2]	–	1600	–	mA	–
$I_{DD\text{-}I/O}$	I/O Supply Current (dynamic)	–	550	–	mA	–
$I_{DD\text{-}DDR}$	DDR Supply Current (dynamic)	–	900	–	mA	–
T_j	Junction Temperature	–	–	115	°C	0 LFPM[3]
T_A	Operating Free Air	–	–	55	°C	
θ_{JA}	Thermal Resistance (junction to ambient air)	–	–	15.2	°C/W	

1. Conditions that exceed the operating limits can cause the device to function incorrectly.
2. Core and analog supply only.
3. LFPM = linear feet per minute.

The core voltage must come up before I/O voltage. The following equation must hold at all times: VDD_I/O ≤ (VDD_CORE + 2 V).

Table 5.3 LVD Driver SCSI Signals[1] – SACK±, SATN±, SBSY±, SCD±, SD[15:0]±, SDP[1:0]±, SIO±, SMSG±, SREQ±, SRST±, SSEL±

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_O+	Source (+) current	–6.5	–13.5	mA	Asserted state
$I_O–$	Sink (–) current	6.5	13.5	mA	Asserted state
I_O+	Source (+) current	2.5	9.5	mA	Negated state
$I_O–$	Sink (–) current	–2.5	–9.5	mA	Negated state
I_{OZ}	3-state leakage	–	20	µA	–

1. V_{CM} = 0.7–1.8 V (Common Mode, nominal ~1.2 V), Rbias = 10.0 kΩ.

Figure 5.1 LVD Driver

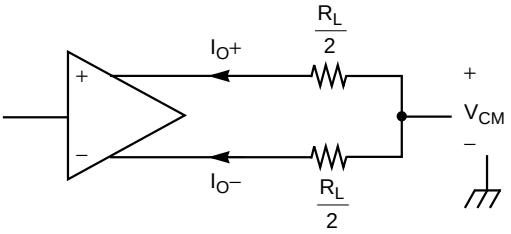


Table 5.4 LVD Receiver SCSI Signals[1] – SACK±, SATN±, SBSY±, SCD±, SD[15:0]±, SDP[1:0]±, SIO±, SMSG±, SREQ±, SRST±, SSEL±

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_I	LVD receiver voltage asserting	|30|	–	mV	Differential voltage
V_I	LVD receiver voltage negating	–	|30|	mV	Differential voltage

1. V_{CM} = 0.7–1.8 V (Common Mode Voltage, nominal ~1.2 V).

Figure 5.2 LVD Receiver

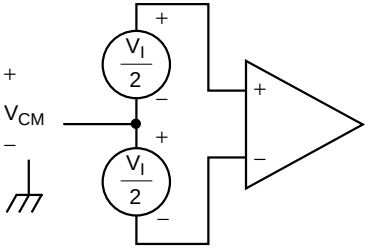


Table 5.5 A_DIFFSENS and B_DIFFSENS SCSI Signals

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	HVD sense voltage	2.4	3.6	V	Refer to note[1]
V_S	LVD sense voltage	0.7	1.9	V	Refer to note[1]
V_{IL}	SE sense voltage	VSS – 0.35	0.5	V	Refer to note[1]
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 3.6 V

1. V_{IH}, V_s, and V_{IL} are specified in the SPI-4 draft specification.

Table 5.6 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	Guaranteed by design
C_{IO}	Input capacitance of I/O pads	–	15	pF	Guaranteed by design
C_{PCI}	Input capacitance of PCI pads	–	8	pF	Guaranteed by design
C_{LVD}	Input capacitance of LVD pads	–	8	pF	6.5 pF pad, 1.5 pF package

Table 5.7 8 mA PCI Bidirectional Signals – ACK64/, AD[63:0], C_BE[7:0]/, DEVSEL/, FRAME/, IRDY/, PAR, PAR64, PERR/, REQ64/, SERR/, STOP/, TRDY/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 VDD	PCI5VBIAS[1]	V	–
V_{IL}	Input low voltage	–0.5	0.3 VDD	V	–
V_{OH}	Output high voltage	0.9 VDD	VDD	V	–500 µA
V_{OL}	Output low voltage	VSS	0.1 VDD	V	1500 µA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
$I_{PULL-DOWN}$	Pull-down current[2]	25	–	µA	–

1. The maximum PCI input voltage depends on the operating mode of the PCI bus, which PCI5VBIAS determines. The maximum input voltage in a 5 V PCI system is 5 V. The maximum input voltage in a 3.3 V PCI system is VDD. Refer to the signal description in Section 3.8, “Power and Ground Pins,” on page 3-23 for details on PCI5VBIAS.
2. Pull-down text does not apply to AD[31:0] and C_BE[3:0]/.

Table 5.8 8 mA Output Signals – A_DDR[12:0], BA_DDR[1:0], DDR_CAS/, DDR_CLKEN[1:0], DDR_CS[1:0]/, DDR_RAS/, DDR_WE/, EXTRST/, SER_TX

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	3.6	V	–
V_{IL}	Input low voltage	–0.3	0.8	V	–
V_{OH}	Output high voltage	2.4	VDD	V	–8 mA
V_{OL}	Output low voltage	VSS	0.4	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
$I_{PULL-UP}$	Pull-up current	25	–	µA	–

Table 5.9 9 mA Bidirectional and Output Signals – CB[7:0], DDRCLK0, DDRCLK0/, DM[8:0], DQ[63:0], DQS[8:0]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH-}	Input high voltage	VREF + 0.15	3.05	V	–
V_{IL}	Input low voltage	–0.5	VREF –0.15	V	–
V_{OH-9}	Output high voltage	–	VDD	V	–9 mA
V_{OL-9}	Output low voltage	VSS	–	V	9 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}	Pull current	25	–	µA	–
VREF	Reference Voltage	1.15	1.35	V	–

Table 5.10 4 mA Bidirectional Signals – ISTWDATA, SerialDATA, XM_ADDR[7:0], XM_ALE[1:0], XM_CS[2:0], XM_DATA[7:0], XM_RS[1:0], XM_WS[1:0]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	3.6	V	–
V_{IL}	Input low voltage	–0.3	0.8	V	–
V_{OH}	Output high voltage	2.4	VDD	V	–4 mA
V_{OL}	Output low voltage	VSS	0.4	V	4 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}	Pull current	25	–	µA	–

Table 5.11 8 mA PCI Output Signals[1] – INTA/, INTB/, REQ/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	VDD	V	–8 mA
V_{OL}	Output low voltage	VSS	0.4 VDD	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 3.6 V
I_{PULL}	Pull current	25	–	µA	–

1. Do not place pulls on REQ/. The pull information given does not apply to these signals.

Table 5.12 4 mA Output Signals – ISTWCLK, BBU_PFC, TDO_ICE, RTCK_ICE, SerialCLK, TDO

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	VDD	V	–4 mA
V_{OL}	Output low voltage	VSS	0.4 VDD	V	4 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 3.6 V
I_{PULL}	Pull current	25	–	µA	–

Table 5.13 Input Signals[1] – BZRSET, BZVDD, CLKMODE0, CLKMODE1, DIS_PCI_FSN/, DIS_SCSI_FSN/, DDR_DRIVEMODE, EXT_POR/, GNT/, IDDTN, IDSEL, PCI_CLK, PFS/, RAIDMODE/, RST/, SCANEN, SCAN_MODE, SCANRSTDIS, SCSI_CLK, SER_RX, TCK, TCK_ICE, TESTACLK, TESTHCLK, TDI, TDI_ICE, TM, TMS, TMS_ICE, TN/, TRST/, TRST_ICE/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	VDD + 0.5	V	–
V_{IL}	Input low voltage	–0.3	0.8	V	–
I_{IN}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, VDD + 0.5 V
I_{PULL}	Pull current	25	–	µA	–

1. Do not place external pulls on PCI_CLK, GNT/, IDSEL, RST/, and SCSI_CLK. The pull information given does not apply to these signals.

Table 5.14 12 mA Bidirectional Signals – A_LED/, B_LED/, HB_LED/, GPIO[7:0], SPARE[1:0], USEEXTPOR

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	VDD	V	–12 mA
V_{OL}	Output low voltage	VSS	0.4 VDD	V	12 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 3.6 V
I_{PULL}	Pull current	25	–	µA	–

5.2 TolerANT Technology Electrical Characteristics

The LSI53C1035 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be pulled up passively by terminators.

Table 5.15 provides electrical characteristics for SE SCSI signals. Figure 5.3 and Figure 5.4 provide the reference information for testing SCSI signals.

Table 5.15 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}[2]	Output high voltage	2.5	3.7	V	I_{OH} = 0 mA
V_{OL}	Output low voltage	0.0	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	1.9	5.50	V	Signal FALSE State
V_{IL}	Input low voltage	–0.5	1.0	V	Referenced to V_{SS} Signal TRUE State
V_{IK}	Input clamp voltage	–	–0.75	V	V_{pp} = Min; I_1 = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.00	–	V	–
V_{TL}	Threshold, LOW to HIGH	–	1.90	V	–
V_{TH}–V_{TL}	Hysteresis	375	–	mV	–
$I_{ih.hp}$	Hot Plug High Level Current Peak	–	1.5	mA	Transient duration of 10% of peak equals 20 µs. This applies during physical insertion only.
I_{OH2}	Output high current	0	7	mA	V_{OH} = 2.2 V
I_{OL}	Output low current	48	–	mA	V_{OL} = 0.5 V
I_{OSH2}	Short-circuit output high current	48	–	mA	Short to V_{DD}[3]
I_{OSL}	Short-circuit output low current	22	–	mA	Short to V_{SS}

Table 5.15 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{LH}	Input high leakage	–	20	µA	$-0.5<V_{DD}<5.25$ V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	20	µA	$-0.5<V_{DD}<5.25$ V_{PIN} = 0.5 V
R_I	Input resistance	20	–	MΩ	Receivers Disabled
C_P	Capacitance per pin	–	8	pF	PQFP
dVH/dt	Slew rate LOW to HIGH	110	540	mV/ns	Figure 5.3
dVL/dt	Slew rate HIGH to LOW	110	540	mV/ns	Figure 5.3
ESD_{HBM}	Electrostatic discharge (HBM)	2	–	kV	MIL-STD-883C; Method 3015-7; 100 pF at 1.5 kΩ
ESD_{CDM}	Electrostatic discharge (CDM)	0.5	–	kV	ESD DS5.3.1-1996
–	Latch-up	100	–	mA	–
–	Filter delay	20	30	ns	Figure 5.4
–	Ultra filter delay	10	15	ns	Figure 5.4
–	Ultra2 filter delay	5	8	ns	Figure 5.4
–	Extended filter delay	40	60	ns	Figure 5.4

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, and SACK/. SCSI SE mode only (minus pins).
3. Single pin only; irreversible damage can occur if sustained for longer than 1 second.

Figure 5.3 Rise and Fall Time Test Condition

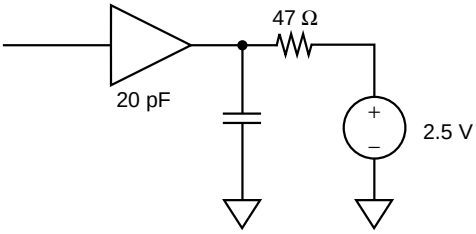
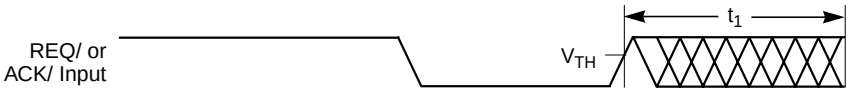


Figure 5.4 SCSI Input Filtering



Note: t_1 is the input filtering period.

5.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 5.1, “DC Characteristics,” on page 5-1). Chip timing is based on simulation at worst case voltage, temperature, and processing. Timing has been developed with a load capacitance of 50 pF. Table 5.16 and Figure 5.5 provide external clock timing data.

Table 5.16 External Clock Timing

Symbol	Parameter	133 MHz PCI-X		66 MHz PCI-X		66 MHz PCI		33 MHz PCI		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_1	PCI Bus clock period[1]	7.5	20	15	20	15	30	30	250	ns
	SCSI clock period	12.5	12.5	12.5	12.5	12.5	12.5	12.5	12.5	ns
t_2	PCI CLK LOW time[2]	3	–	6	–	6	–	11	–	ns
	SCLK LOW time	5	7.5	5	7.5	5	7.5	5	7.5	ns
t_3	PCI CLK HIGH time	3	–	6	–	6	–	11	–	ns
	SCLK HIGH time	5	7.5	5	7.5	5	7.5	5	7.5	ns
t_4	PCI CLK slew rate	1.5	4	1.5	4	1.5	4	1	4	V/ns

1. For frequencies above 33 MHz, the clock frequency cannot be changed beyond the spread spectrum limits except while RST/ is asserted.
2. Duty cycle not to exceed 60/40.

Figure 5.5 External Clock Timing

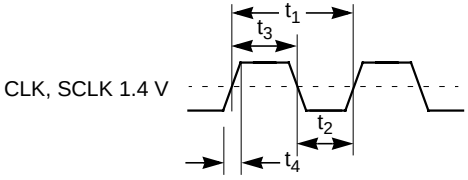


Table 5.17 and Figure 5.6 provide reset input timing data.

Table 5.17 Reset Input Timing

Symbol	Parameter	Min	Max	Unit
t_1	Reset pulse width	10	–	ns
t_2	Reset deasserted setup to CLK HIGH	0	–	ns
t_3	XM_ADDR, XM_DATA, and XM_RS setup time to CLK HIGH[1]	20	–	ns
t_4	XM_ADDR, XM_DATA, and XM_RS hold time from CLK HIGH	20	–	ns

1. For configuring the external memory Power-on Sense pins only.

Figure 5.6 Reset Input Timing

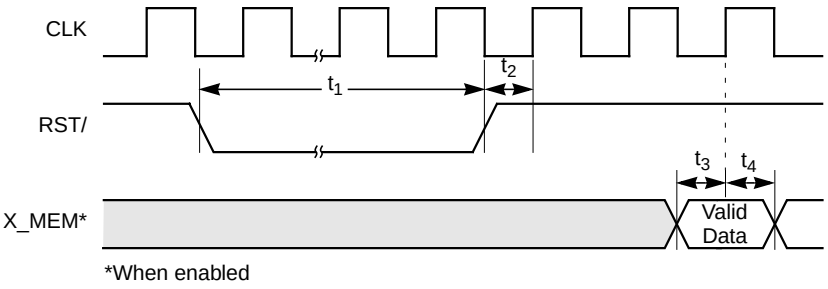
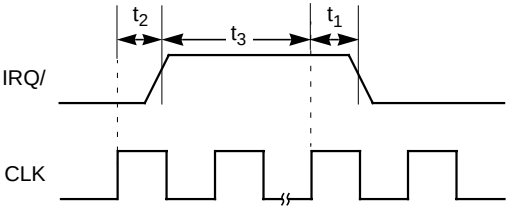


Table 5.18 and Figure 5.7 provide Interrupt Output timing data.

Table 5.18 Interrupt Output Timing

Symbol	Parameter	Min	Max	Unit
t_1	CLK HIGH to IRQ/ LOW	2	11	ns
t_2	CLK HIGH to IRQ/ HIGH	2	11	ns
t_3	IRQ/ deassertion time	3	–	CLK

Figure 5.7 Interrupt Output Timing



5.4 External Memory Timing Diagrams

This section provides external memory timing diagrams and data for NVSRAM and Flash ROM interfaces. Refer to the *Double Data Rate (DDR) SDRAM Specification* (JEDEC Standard JESD79C, March 2003) for details on the DDR SDRAM interface.

5.4.1 NVSRAM Timing

Table 5.19 and Figure 5.8 provide the timing information for NVSRAM external memory bus read accesses.

Table 5.19 NVSRAM Read Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_1	Address setup to XM_ALE HIGH	25	–	ns
t_2	Address hold from XM_ALE HIGH	25	–	ns
t_3	XM_ALE pulse width	25	–	ns
t_4	Address valid to data clocked in	135	–	ns
t_5	XM_CS1 LOW to data clocked in	85	–	ns
t_6	XM_RS0 LOW to data clocked in	75	–	ns
t_7	Data setup to XM_RS0 HIGH	10	–	ns
t_8	Data setup to XM_CS1 HIGH	10	–	ns
t_9	Data hold from XM_CS1 HIGH	0	–	ns

Figure 5.8 NVSRAM Read Cycle Timing

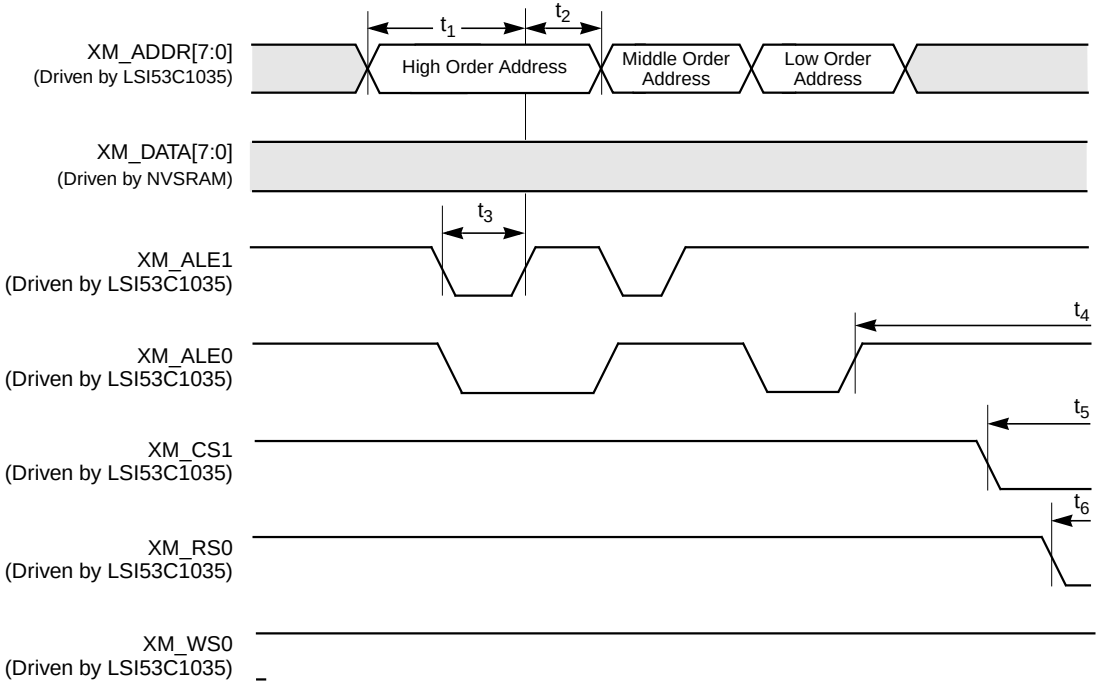


Figure 5.8 NVSRAM Read Cycle Timing (Cont.)

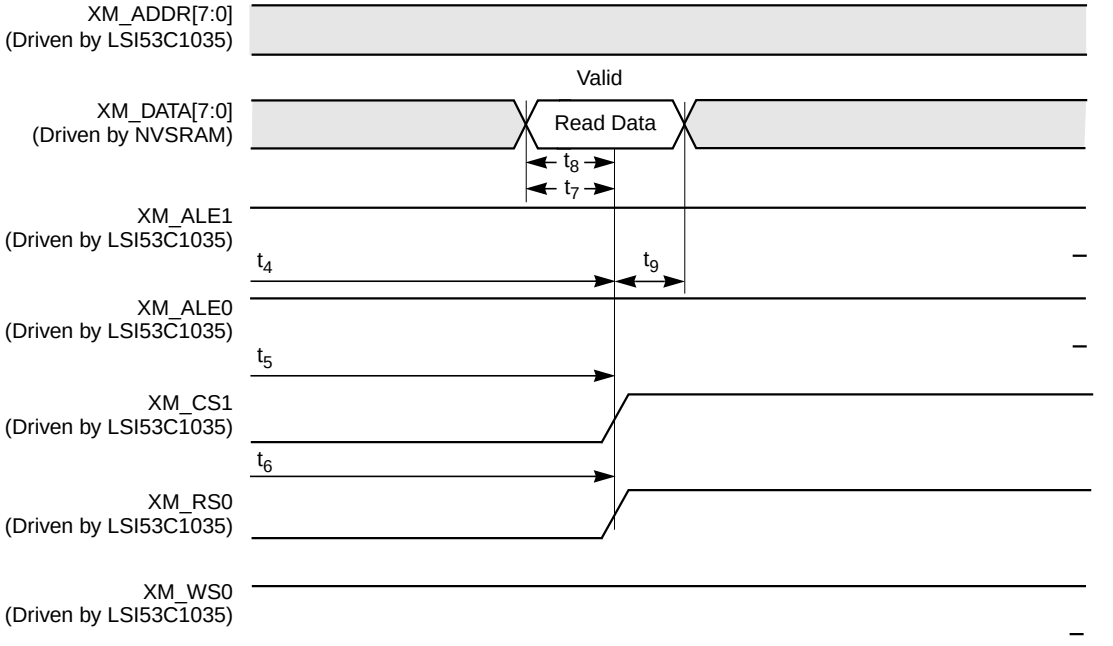


Table 5.20 and Figure 5.9 provide the timing information for NVSRAM write accesses.

Table 5.20 NVSRAM Write Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to XM_ALE1 HIGH	25	–	ns
t_{12}	Address hold from XM_ALE1 HIGH	25	–	ns
t_{13}	XM_ALE1 pulse width	25	–	ns
t_{20}	Data setup to XM_WS0 LOW	40	–	ns
t_{21}	Data hold from XM_WS0 HIGH	30	–	ns
t_{22}	XM_WS0 pulse width	20	–	ns
t_{23}	Address setup to XM_WS0 LOW	75	–	ns
t_{24}	XM_CS1 LOW to XM_WS0 HIGH	60	–	ns
t_{25}	XM_CS1 LOW to XM_WS0 LOW	25	–	ns
t_{26}	XM_WS0 HIGH to XM_CS1 HIGH	25	–	ns
t_{27}	XM_CS1 pulse width	100	–	ns

Figure 5.9 NVSRAM Write Cycle Timing

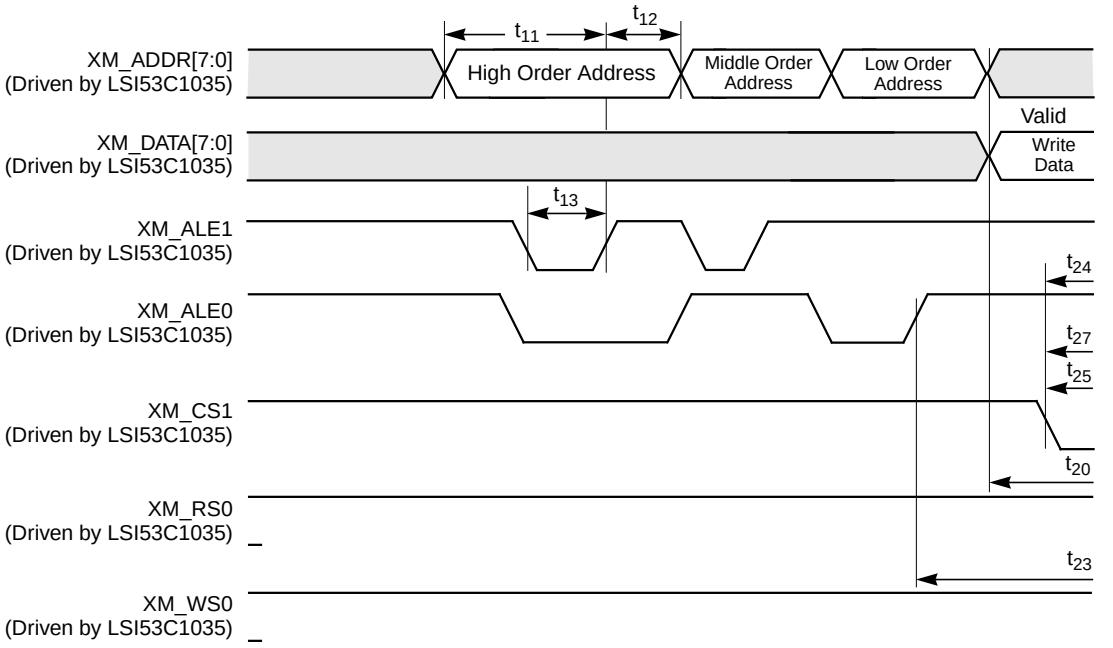
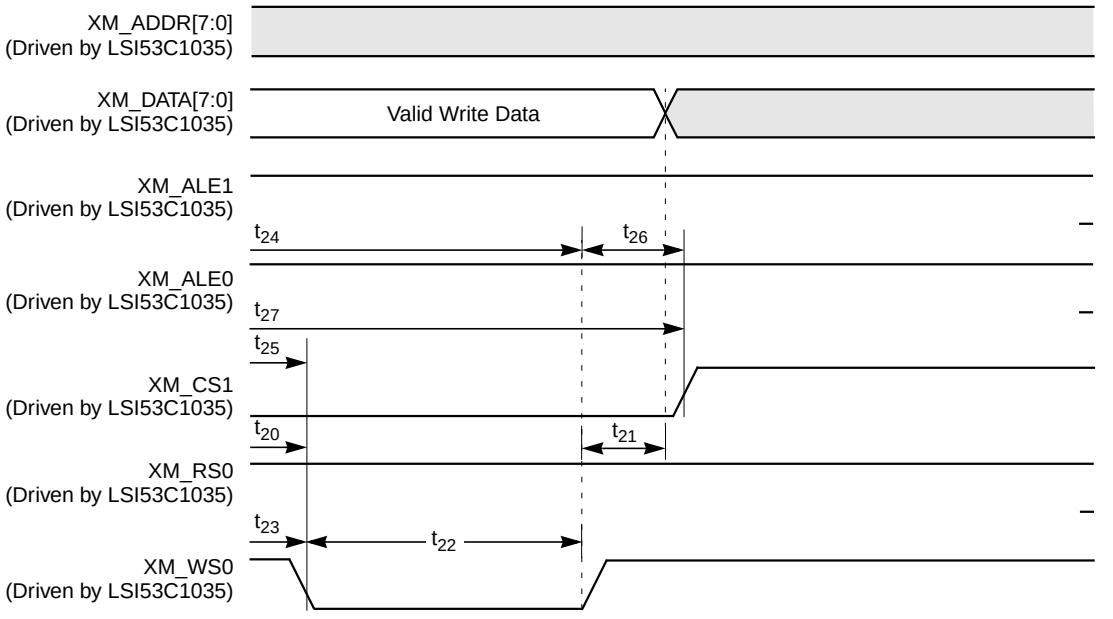


Figure 5.9 NVSRAM Write Cycle Timing (Cont.)



5.4.2 Flash ROM Timing

Table 5.21 and Figure 5.10 provide the timing information for Flash ROM read accesses.

Table 5.21 Flash ROM Read Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_1	Address setup to XM_ALE HIGH	25	–	ns
t_2	Address hold from XM_ALE HIGH	25	–	ns
t_3	XM_ALE pulse width	25	–	ns
t_4	Address valid to data clocked in	135	–	ns
t_5	XM_CS0 LOW to data clocked in	85	–	ns
t_6	XM_RS0 LOW to data clocked in	75	–	ns
t_7	Data setup to XM_RS0 HIGH	10	–	ns
t_8	Data setup to XM_CS0 HIGH	10	–	ns
t_9	Data hold from XM_CS0 HIGH	0	–	ns

Figure 5.10 Flash ROM Read Cycle Timing

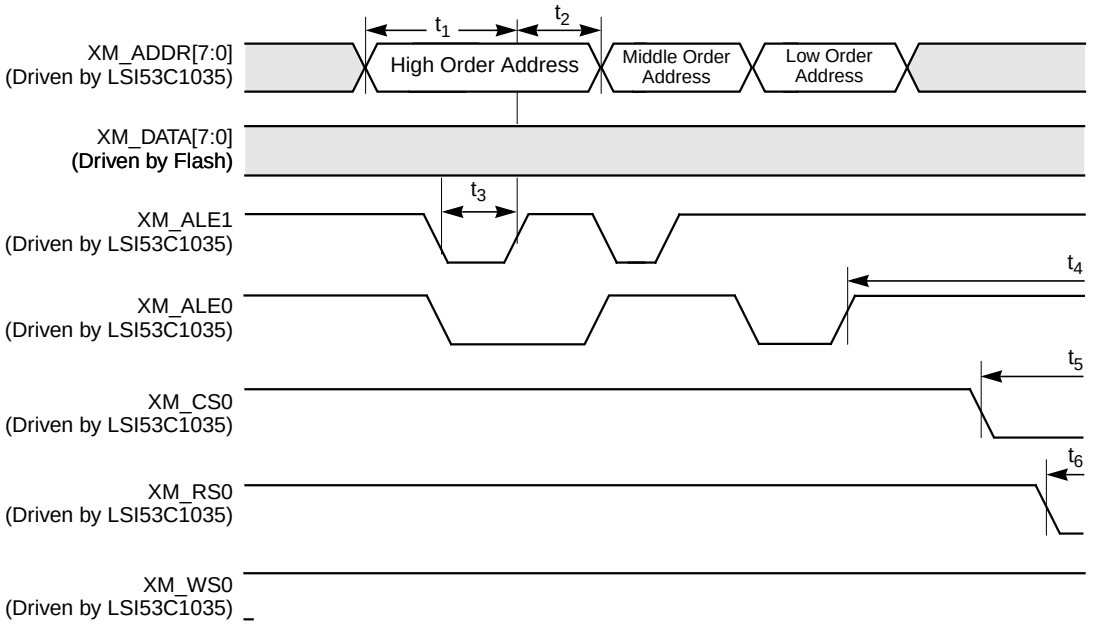


Figure 5.10 Flash ROM Read Cycle Timing (Cont.)

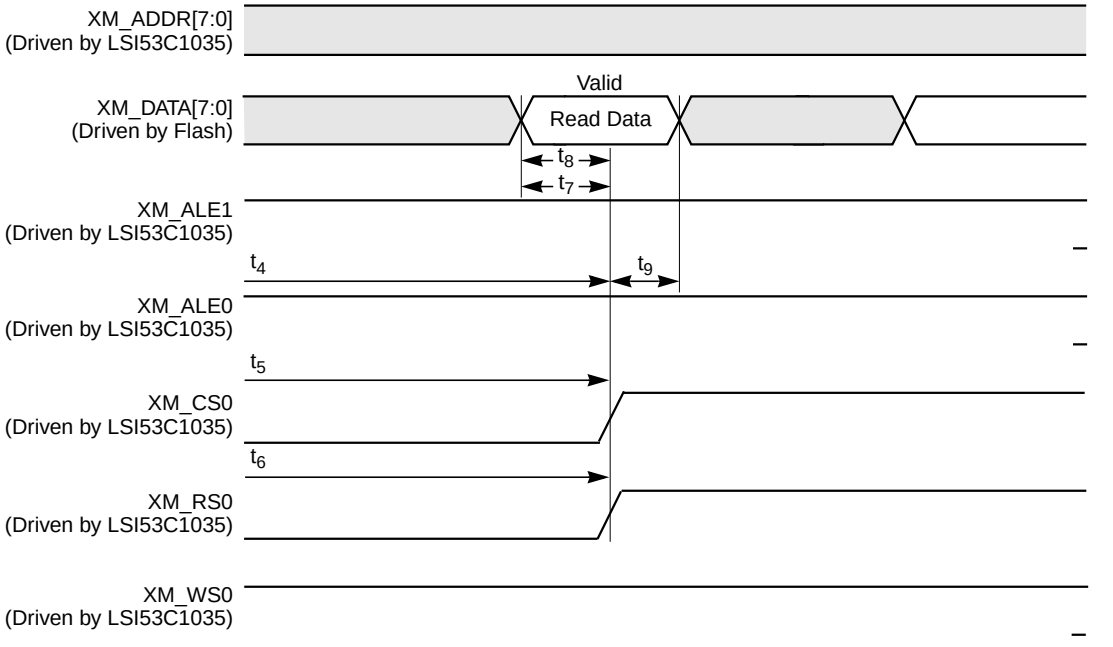


Table 5.22 and Figure 5.11 provide the timing information for Flash ROM write accesses.

Table 5.22 Flash ROM Write Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to XM_ALE HIGH	25	–	ns
t_{12}	Address hold from XM_ALE HIGH	25	–	ns
t_{13}	XM_ALE pulse width	25	–	ns
t_{20}	Data setup to XM_WS0 LOW	40	–	ns
t_{21}	Data hold from XM_WS0 HIGH	30	–	ns
t_{22}	XM_WS0 pulse width	20	–	ns
t_{23}	Address setup to XM_WS0 LOW	75	–	ns
t_{24}	XM_CS0 LOW to XM_WS0 HIGH	60	–	ns
t_{25}	XM_CS0 LOW to XM_WS0 LOW	25	–	ns
t_{26}	XM_WS0 HIGH to XM_CS0 HIGH	25	–	ns
t_{27}	XM_CS0 pulse width	100	–	ns

Figure 5.11 Flash ROM Write Cycle Timing

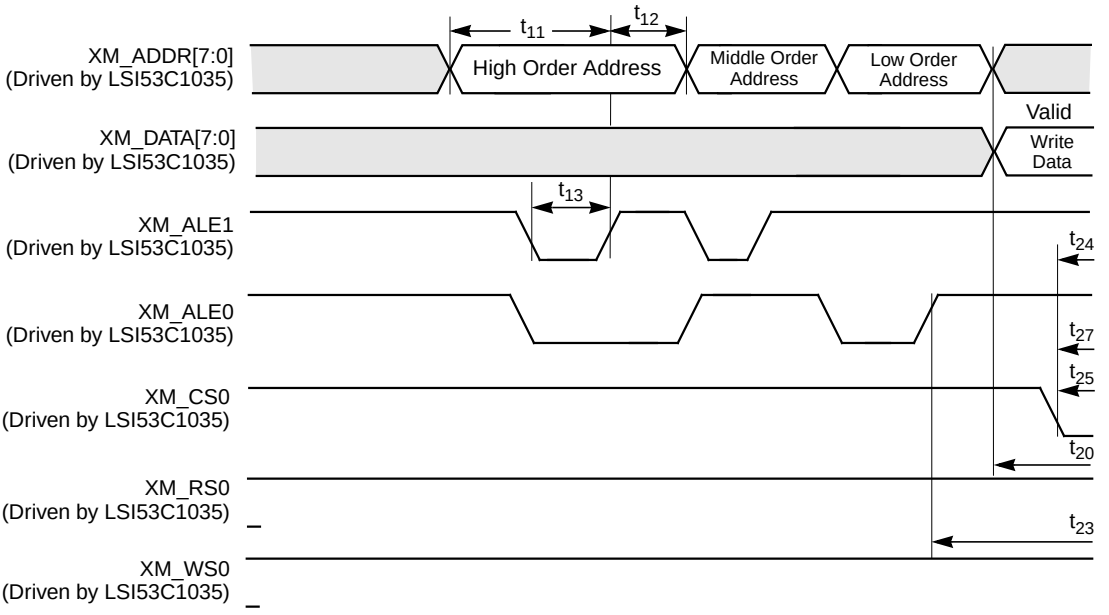
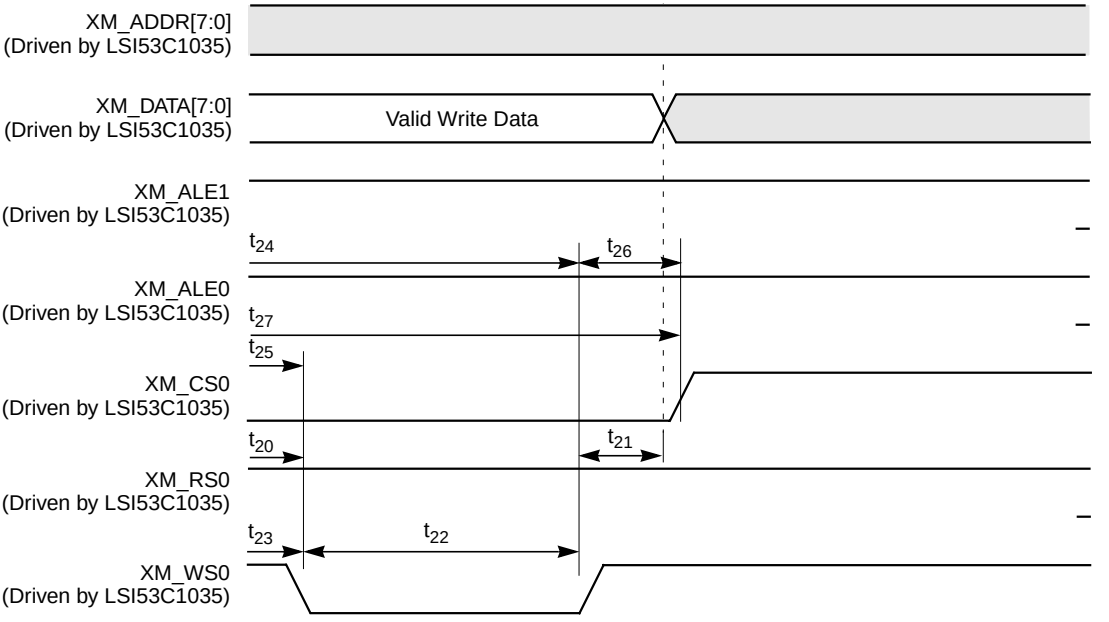


Figure 5.11 Flash ROM Write Cycle Timing (Cont.)



5.5 Package Drawings

Table 5.23 provides the signal list for the LSI53C1035 organized by signal name. Table 5.24 provides the signal list for the LSI53C1035 organized by BGA position.

Figure 5.12 is a mechanical drawing of the LSI53C1035 788 EPBGA.

Table 5.23 Alphanumeric List by Signal Name

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
A_DDR0	U30	AD41	AN29	A_SD10–	K3	B_SD7–	A14	DDR_CLKEN0	J34
A_DDR1	U32	AD42	AK28	A_SD11+	J3	B_SD8+	B20	DDR_CLKEN1	K30
A_DDR2	T31	AD43	AP29	A_SD11–	J2	B_SD8–	A20	DDR_CS0/	AD34
A_DDR3	T34	AD44	AL28	A_SD12+	AB1	B_SD9+	B21	DDR_CS1/	AD30
A_DDR4	N31	AD45	AN27	A_SD12–	AB2	B_SD9–	A21	DDR_DRIVEMODE	AP4
A_DDR5	N33	AD46	AJ27	A_SD13+	AA2	B_SD10+	D23	DDR_RAS/	AD31
A_DDR6	M31	AD47	AP27	A_SD13–	AA3	B_SD10–	D22	DDR_WE/	AC33
A_DDR7	N32	AD48	AK27	A_SD14+	Y2	B_SD11+	A22	DEVSEL/	AN14
A_DDR8	M34	AD49	AN26	A_SD14–	AA1	B_SD11–	C21	DIS_PCI_FSN/	AG1
A_DDR9	K33	AD50	AL27	A_SD15+	AA4	B_SD12+	E5	DIS_SCSI_FSN/	E4
A_DDR10	U31	AD51	AP26	A_SD15–	AB4	B_SD12–	F6	DM0	F32
A_DDR11	J31	AD52	AK26	A_SDP0+	R2	B_SD13+	B9	DM1	H34
A_DDR12	K32	AD53	AM25	A_SDP0–	R1	B_SD13–	C9	DM2	L34
ACK64/	AN21	AD54	AL26	A_SDP1+	Y4	B_SD14+	D6	DM3	R30
AD0	AL22	AD55	AP25	A_SDP1–	Y5	B_SD14–	E7	DM4	AB33
AD1	AP21	AD56	AJ25	A_SIO+	J5	B_SD15+	B10	DM5	AF31
AD2	AJ21	AD57	AN24	A_SIO–	H4	B_SD15–	C10	DM6	AH30
AD3	AN20	AD58	AK25	A_SMSG+	M5	B_SDP0+	D14	DM7	AK34
AD4	AL21	AD59	AN23	A_SMSG–	L4	B_SDP0–	D13	DM8	W31
AD5	AP20	AD60	AJ24	A_SREQ+	L2	B_SDP1+	D7	DQ0	C34
AD6	AJ20	AD61	AP23	A_SREQ–	L1	B_SDP1–	E8	DQ1	D34
AD7	AM18	AD62	AK24	A_SRST+	N2	B_SIO+	D20	DQ2	E32
AD8	AN18	AD63	AM22	A_SRST–	N1	B_SIO–	E19	DQ3	E33
AD9	AL20	A_DIFFSENSE	H1	A_SSEL+	M2	B_SMSG	+ D18	DQ4	F33
AD10	AP18	A_LED/	AE2	A_SSEL–	M1	B_SMSG–	D17	DQ5	F34
AD11	AJ19	A_RBIAS	P1	A_VDDBIAS	R4	B_SREQ+	B19	DQ6	F30
AD12	AP17	A_SACK+	M4	BA_DDR0	Y30	B_SREQ–	A19	DQ7	G33
AD13	AK19	A_SACK–	N4	BA_DDR1	Y33	B_SRST+	A18	DQ8	G34
AD14	AM17	A_SATN+	P4	BBU_PFC	A24	B_SRST–	C17	DQ9	E31
AD15	AL19	A_SATN–	R5	B_DIFFSENSE	A7	B_SSEL+	C18	DQ10	H33
AD16	AL16	A_SBSY+	P3	B_LED/	AJ4	B_SSEL–	B18	DQ11	G30
AD17	AN13	A_SBSY–	P2	B_RBIAS	A15	B_VDDBIAS	E15	DQ12	J32
AD18	AK16	A_SCD+	K5	B_SACK+	B17	BZRSET	AN6	DQ13	H30
AD19	AM13	A_SCD–	J4	B_SACK–	A17	BZVDD	AP6	DQ14	J33
AD20	AL15	A_SD0+	W1	B_SATN+	A16	C_BE0/	AK20	DQ15	G31
AD21	AP12	A_SD0–	W2	B_SATN–	B16	C_BE1/	AP16	DQ16	J30
AD22	AK15	A_SD1+	W4	B_SBSY+	E16	C_BE2/	AP13	DQ17	H31
AD23	AN12	A_SD1–	W5	B_SBSY–	D15	C_BE3/	AP11	DQ18	K34
AD24	AL14	A_SD2+	V2	B_SCD+	D19	C_BE4/	AP22	DQ19	L33
AD25	AN11	A_SD2–	V3	B_SCD–	E18	C_BE5/	AJ23	DQ20	M30
AD26	AL13	A_SD3+	V4	B_SD0+	A11	C_BE6/	AM21	DQ21	L31
AD27	AP10	A_SD3–	V5	B_SD0–	B11	C_BE7/	AK23	DQ22	M33
AD28	AL12	A_SD4+	U3	B_SD1+	D8	CB0	V34	DQ23	K31
AD29	AN10	A_SD4–	V1	B_SD1–	E9	CB1	V31	DQ24	P32
AD30	AK12	A_SD5+	U5	B_SD2+	A12	CB2	V33	DQ25	P33
AD31	AM10	A_SD5–	U4	B_SD2–	B12	CB3	V32	DQ26	P34
AD32	AL30	A_SD6+	U1	B_SD3+	D9	CB4	W34	DQ27	P31
AD33	AM30	A_SD6–	U2	B_SD3–	E10	CB5	W30	DQ28	R31
AD34	AJ29	A_SD7+	T2	B_SD4+	B13	CB6	W33	DQ29	R34
AD35	AN30	A_SD7–	T1	B_SD4–	C13	CB7	Y31	DQ30	T33
AD36	AK29	A_SD8+	K2	B_SD5+	C14	CLKMODE0	D26	DQ31	T30
AD37	AP30	A_SD8–	K1	B_SD5–	A13	CLKMODE1	F22	DQ32	AA34
AD38	AL29	A_SD9+	H5	B_SD6+	D10	DDR_CAS/	AC30	DQ33	AA33
AD39	AM29	A_SD9–	G4	B_SD6–	D11	DDR_CLK0	U34	DQ34	AA31
AD40	AJ28	A_SD10+	J1	B_SD7+	B15	DDR_CLK0/	U33		

Table 5.23 Alphanumeric List by Signal Name (Cont.)

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
DQ35	AA32	GND_01	C19	GND_01	W16	GND_01	AP33	NC	F5
DQ36	AC31	GND_01	C20	GND_01	W17	GND_01-NC	B33	NC	F9
DQ37	AB32	GND_01	C23	GND_01	W18	GND_01-NC	C32	NC	F11
DQ38	AE31	GND_01	C24	GND_01	W19	GND_01-NC	D31	NC	F12
DQ39	AC34	GND_01	C27	GND_01	W20	GNT/	AL11	NC	F13
DQ40	AD33	GND_01	C28	GND_01	W32	GPIO0	H6	NC	F14
DQ41	AF30	GND_01	C31	GND_01	Y3	GPIO1	E1	NC	F16
DQ42	AE34	GND_01	D4	GND_01	Y15	GPIO2	E2	NC	F17
DQ43	AG31	GND_01	D32	GND_01	Y16	GPIO3	E3	NC	F19
DQ44	AE32	GND_01	E13	GND_01	Y17	GPIO4	G6	NC	F29
DQ45	AE30	GND_01	E14	GND_01	Y18	GPIO5	D1	NC	G5
DQ46	AF34	GND_01	E21	GND_01	Y19	GPIO6	D2	NC	H2
DQ47	AH31	GND_01	E22	GND_01	Y20	GPIO7	D3	NC	J6
DQ48	AF33	GND_01	G3	GND_01	Y32	HB_LED/	AC6	NC	K4
DQ49	AG30	GND_01	G32	GND_01	AA5	IDDTN	E24	NC	K6
DQ50	AF32	GND_01	H3	GND_01	AA30	IDSEL	AJ15	NC	L5
DQ51	AJ31	GND_01	H32	GND_01	AB5	INTA/	AL8	NC	M6
DQ52	AG33	GND_01	L3	GND_01	AB30	INTB/	AN9	NC	N3
DQ53	AK31	GND_01	L32	GND_01	AC3	IRDY/	AM14	NC	N34
DQ54	AH34	GND_01	M3	GND_01	AC32	ISTWCLK	A31	NC	P29
DQ55	AJ30	GND_01	M32	GND_01	AD3	ISTWDATA	F28	NC	R6
DQ56	AH33	GND_01	N5	GND_01	AD32	NC	A1	NC	R29
DQ57	AK30	GND_01	N30	GND_01	AG3	NC	A4	NC	T4
DQ58	AJ34	GND_01	P5	GND_01	AG32	NC	A6	NC	T6
DQ59	AJ33	GND_01	P30	GND_01	AH3	NC	A9	NC	U6
DQ60	AK33	GND_01	R3	GND_01	AH32	NC	A10	NC	V6
DQ61	AK32	GND_01	R15	GND_01	AK13	NC	A23	NC	W29
DQ62	AL34	GND_01	R16	GND_01	AK14	NC	A32	NC	Y6
DQ63	AM34	GND_01	R17	GND_01	AK21	NC	A34	NC	Y29
DQS0	E34	GND_01	R18	GND_01	AK22	NC	B4	NC	Y34
DQS1	F31	GND_01	R19	GND_01	AL3	NC	B7	NC	AB6
DQS2	L30	GND_01	R20	GND_01	AL4	NC	B8	NC	AB34
DQS3	R33	GND_01	R32	GND_01	AL31	NC	B22	NC	AC1
DQS4	AB31	GND_01	T3	GND_01	AL32	NC	B30	NC	AC4
DQS5	AE33	GND_01	T15	GND_01	AM3	NC	B32	NC	AC29
DQS6	AG34	GND_01	T16	GND_01	AM4	NC	C1	NC	AD4
DQS7	AJ32	GND_01	T17	GND_01	AM7	NC	C2	NC	AD5
DQS8	V30	GND_01	T18	GND_01	AM8	NC	C4	NC	AE3
EXT_POR/	AH5	GND_01	T19	GND_01	AM11	NC	C22	NC	AE4
EXTRST/	AF3	GND_01	T20	GND_01	AM12	NC	C33	NC	AE6
FRAME/	AJ17	GND_01	T32	GND_01	AM15	NC	D5	NC	AF6
GND_01	A2	GND_01	U15	GND_01	AM16	NC	D12	NC	AG2
GND_01	A3	GND_01	U16	GND_01	AM19	NC	D16	NC	AG6
GND_01	A33	GND_01	U17	GND_01	AM20	NC	D21	NC	AG29
GND_01	B1	GND_01	U18	GND_01	AM23	NC	D25	NC	AH2
GND_01	B2	GND_01	U19	GND_01	AM24	NC	D27	NC	AH6
GND_01	B3	GND_01	U20	GND_01	AM27	NC	D33	NC	AH29
GND_01	B34	GND_01	V15	GND_01	AM28	NC	E6	NC	AJ2
GND_01	C3	GND_01	V16	GND_01	AM31	NC	E11	NC	AJ3
GND_01	C7	GND_01	V17	GND_01	AM32	NC	E12	NC	AJ6
GND_01	C8	GND_01	V18	GND_01	AN1	NC	E17	NC	AJ7
GND_01	C11	GND_01	V19	GND_01	AN2	NC	E20	NC	AJ8
GND_01	C12	GND_01	V20	GND_01	AN33	NC	E23	NC	AJ9
GND_01	C15	GND_01	W3	GND_01	AN34	NC	E30	NC	AJ10
GND_01	C16	GND_01	W15	GND_01	AP2	NC	F4	NC	AJ11

Table 5.23 Alphanumeric List by Signal Name (Cont.)

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
NC	AJ12	PWR_01	G22	PWR_03	AH25	TRST_ICE/	AB3	XM_ADDR2	D29
NC	AJ13	PWR_01	G23	PWR_04	K28	USEEXTPOR	AK1	XM_ADDR3	C25
NC	AJ16	PWR_01	G27	PWR_04	L28	VDDC0	F3	XM_ADDR4	B25
NC	AK2	PWR_01	H7	PWR_04	P28	VDDC1	L6	XM_ADDR5	E27
NC	AK3	PWR_01	J7	PWR_04	R28	VDDC2	P6	XM_ADDR6	F23
NC	AK6	PWR_01	M7	PWR_04	U28	VDDC3	Y1	XM_ADDR7	D28
NC	AK7	PWR_01	N7	PWR_04	V28	VDDC4	AD1	XM_ALE0	A25
NC	AK9	PWR_01	T7	PWR_04	Y28	VDDC5	AL2	XM_ALE1	E25
NC	AK10	PWR_01	W7	PWR_04	AA28	VDDC6	AP5	XM_CS0	B31
NC	AL1	PWR_01	AB7	PWR_04	AD28	VDDC7	AK5	XM_CS1	B26
NC	AL6	PWR_01	AC7	PWR_04	AE28	VDDC8	AJ14	XM_CS2	F24
NC	AL9	PWR_01	AF7	PWR_05	G10	VDDC9	AP19	XM_DATA0	F26
NC	AL10	PWR_01	AF28	PWR_05	G11	VDDC10	AL25	XM_DATA1	B28
NC	AL33	PWR_01	AG7	PWR_05	G14	VDDC11	AN28	XM_DATA2	A28
NC	AM1	PWR_01	AG28	PWR_05	G15	VDDC12	AF29	XM_DATA3	A30
NC	AM2	PWR_01	AH7	PWR_05	G17	VDDC13	AB29	XM_DATA4	B27
NC	AM5	PWR_01	AH8	PWR_05	G18	VDDC14	U29	XM_DATA5	E29
NC	AM6	PWR_01	AH12	PWR_05	G20	VDDC15	N29	XM_DATA6	F25
NC	AM33	PWR_01	AH13	PWR_05	G21	VDDC16	K29	XM_DATA7	A27
NC	AN3	PWR_01	AH16	PWR_05	G24	VDDC17	H29	XM_RS0	F27
NC	AN4	PWR_01	AH19	PWR_05	G25	VDDC18	C26	XM_RS1	C29
NC	AN8	PWR_01	AH22	PWR_05	G26	VDDC19	F21	XM_WS0	B29
NC	AN31	PWR_01	AH23	RAIDMODE/	C30	VDDC20	F20	XM_WS1	A29
NC	AN32	PWR_01	AH26	REQ/	AP9	VDDC21	B14		
NC	AP1	PWR_01	AH27	REQ64/	AL23	VDDC22	F10		
NC	AP3	PWR_01	AH28	RST/	AK11	VDDC23	F7		
NC	AP15	PWR_01-NC	G28	RTCK_ICE	AE5	VREF0	L29		
NC	AP31	PWR_01-NC	H28	SCAN_MODE	C6	VREF1	AD29		
NC	AP32	PWR_01-NC	J28	SCANEN	B6	VREF2	V29		
NC	AP34	PWR_01-NC	M28	SCANRSTDIS	F8	VSSC0	F2		
PAR	AK18	PWR_01-NC	N28	SCSIPLLVDDA	G2	VSSC1	N6		
PAR6	4AL24	PWR_01-NC	T28	SCSIPLLVSSA	G1	VSSC2	T5		
PCI5VBIAS	AL5	PWR_01-NC	W28	SCSI_CLK	F1	VSSC3	W6		
PCI5VBIAS	AL7	PWR_01-NC	AB28	SerialCLK	AK4	VSSC4	AD2		
PCI5VBIAS	AN15	PWR_01-NC	AC28	SerialDATA	AD6	VSSC5	AF1		
PCI5VBIAS	AN17	PWR_02	K7	SERR/	AN16	VSSC6	AN5		
PCI5VBIAS	AN19	PWR_02	L7	SER_RX	AJ5	VSSC7	AM9		
PCI5VBIAS	AL18	PWR_02	P7	SER_TX	AF2	VSSC8	AK8		
PCI5VBIAS	AN22	PWR_02	R7	SPARE0	AH1	VSSC9	AJ18		
PCI5VBIAS	AP24	PWR_02	U7	SPARE1	AJ1	VSSC10	AJ22		
PCI5VBIAS	AN25	PWR_02	V7	STOP/	AL17	VSSC11	AP28		
PCI5VBIAS	AM26	PWR_02	Y7	TCK	AE1	VSSC12	AE29		
PCI5VBIAS	AJ26	PWR_02	AA7	TCK_ICE	AG4	VSSC13	AA29		
PCIPLLVDDA	AN7	PWR_02	AD7	TDI	AG5	VSSC14	T29		
PCIPLLVSSA	AP7	PWR_02	AE7	TDI_ICE	AA6	VSSC15	M29		
PCI_CLK	AP8	PWR_03	AH9	TDO	AC2	VSSC16	J29		
PERR/	AP14	PWR_03	AH10	TDO_ICE	AF4	VSSC17	G29		
PFS/	B24	PWR_03	AH11	TESTACLK	E26	VSSC18	D30		
PWR_01	G7	PWR_03	AH14	TESTHCLK	B23	VSSC19	D24		
PWR_01	G8	PWR_03	AH15	TM	B5	VSSC20	F18		
PWR_01	G9	PWR_03	AH17	TMS	AH4	VSSC21	F15		
PWR_01	G12	PWR_03	AH18	TMS_ICE	AF5	VSSC22	A8		
PWR_01	G13	PWR_03	AH20	TN/	A5	VSSC23	C5		
PWR_01	G16	PWR_03	AH21	TRDY/	AK17	XM_ADDR0	E28		
PWR_01	G19	PWR_03	AH24	TRST/	AC5	XM_ADDR1	A26		

Table 5.24 Alphanumeric List by BGA Position

BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name
A1	NC	B22	NC	D9	B_SD3+	E30	NC	G17	PWR_05
A2	GND_01	B23	TESTHCLK	D10	B_SD6+	E31	DQ9	G18	PWR_05
A3	GND_01	B24	PFS/	D11	B_SD6–	E32	DQ2	G19	PWR_01
A4	NC	B25	XM_ADDR4	D12	NC	E33	DQ3	G20	PWR_05
A5	TN/	B26	XM_CS1	D13	B_SDP0–	E34	DQS0	G21	PWR_05
A6	NC	B27	XM_DATA4	D14	B_SDP0+	F1	SCSI_CLK	G22	PWR_01
A7	B_DIFFSENSE	B28	XM_DATA1	D15	B_SBSY–	F2	VSSC0	G23	PWR_01
A8	VSSC22	B29	XM_WS0	D16	NC	F3	VDDC0	G24	PWR_05
A9	NC	B30	NC	D17	B_SMSG–	F4	NC	G25	PWR_05
A10	NC	B31	XM_CS0	D18	B_SMSG+	F5	NC	G26	PWR_05
A11	B_SD0+	B32	NC	D19	B_SCD+	F6	B_SD12–	G27	PWR_01
A12	B_SD2+	B33	GND_01-NC	D20	B_SIO+	F7	VDDC23	G28	PWR_01-NC
A13	B_SD5–	B34	GND_01	D21	NC	F8	SCANRSTDIS	G29	VSSC17
A14	B_SD7–	C1	NC	D22	B_SD10–	F9	NC	G30	DQ11
A15	B_RBIAS	C2	NC	D23	B_SD10+	F10	VDDC22	G31	DQ15
A16	B_SATN+	C3	GND_01	D24	VSSC19	F11	NC	G32	GND_01
A17	B_SACK–	C4	NC	D25	NC	F12	NC	G33	DQ7
A18	B_SRST+	C5	VSSC23	D26	CLKMODE0	F13	NC	G34	DQ8
A19	B_SREQ–	C6	SCAN_MODE	D27	NC	F14	NC	H1	A_DIFFSENSE
A20	B_SD8–	C7	GND_01	D28	XM_ADDR7	F15	VSSC21	H2	NC
A21	B_SD9–	C8	GND_01	D29	XM_ADDR2	F16	NC	H3	GND_01
A22	B_SD11+	C9	B_SD13–	D30	VSSC18	F17	NC	H4	A_SIO–
A23	NC	C10	B_SD15–	D31	GND_01-NC	F18	VSSC20	H5	A_SD9+
A24	BBU_PFC	C11	GND_01	D32	GND_01	F19	NC	H6	GPIO0
A25	XM_ALE0	C12	GND_01	D33	NC	F20	VDDC20	H7	PWR_01
A26	XM_ADDR1	C13	B_SD4–	D34	DQ1	F21	VDDC19	H28	PWR_01-NC
A27	XM_DATA7	C14	B_SD5+	E1	GPIO1	F22	CLKMODE1	H29	VDDC17
A28	XM_DATA2	C15	GND_01	E2	GPIO2	F23	XM_ADDR6	H30	DQ13
A29	XM_WS1	C16	GND_01	E3	GPIO3	F24	XM_CS2	H31	DQ17
A30	XM_DATA3	C17	B_SRST–	E4	DISSCSIFSN/	F25	XM_DATA6	H32	GND_01
A31	ISTWCLK	C18	B_SSEL+	E5	B_SD12+	F26	XM_DATA0	H33	DQ10
A32	NC	C19	GND_01	E6	NC	F27	XM_RS0	H34	DM1
A33	GND_01	C20	GND_01	E7	B_SD14–	F28	ISTWDATA	J1	A_SD10+
A34	NC	C21	B_SD11–	E8	B_SDP1–	F29	NC	J2	A_SD11–
B1	GND_01	C22	NC	E9	B_SD1–	F30	DQ6	J3	A_SD11+
B2	GND_01	C23	GND_01	E10	B_SD3–	F31	DQS1	J4	A_SCD–
B3	GND_01	C24	GND_01	E11	NC	F32	DM0	J5	A_SIO+
B4	NC	C25	XM_ADDR3	E12	NC	F33	DQ4	J6	NC
B5	TM	C26	VDDC18	E13	GND_01	F34	DQ5	J7	PWR_01
B6	SCANEN	C27	GND_01	E14	GND_01	G1	SCSIPLLVSSA	J28	PWR_01-NC
B7	NC	C28	GND_01	E15	B_VDDBIAS	G2	SCSIPLLVDDA	J29	VSSC16
B8	NC	C29	XM_RS1	E16	B_SBSY+	G3	GND_01	J30	DQ16
B9	B_SD13+	C30	RAIDMODE/	E17	NC	G4	A_SD9–	J31	A_DDR11
B10	B_SD15+	C31	GND_01	E18	B_SCD–	G5	NC	J32	DQ12
B11	B_SD0–	C32	GND_01-NC	E19	B_SIO–	G6	GPIO4	J33	DQ14
B12	B_SD2–	C33	NC	E20	NC	G7	PWR_01	J34	DDR_CLKEN0
B13	B_SD4+	C34	DQ0	E21	GND_01	G8	PWR_01	K1	A_SD8–
B14	VDDC21	D1	GPIO5	E22	GND_01	G9	PWR_01	K2	A_SD8+
B15	B_SD7+	D2	GPIO6	E23	NC	G10	PWR_05	K3	A_SD10–
B16	B_SATN–	D3	GPIO7	E24	IDDTN	G11	PWR_05	K4	NC
B17	B_SACK+	D4	GND_01	E25	XM_ALE1	G12	PWR_01	K5	A_SCD+
B18	B_SSEL–	D5	NC	E26	TESTACLK	G13	PWR_01	K6	NC
B19	B_SREQ+	D6	B_SD14+	E27	XM_ADDR5	G14	PWR_05	K7	PWR_02
B20	B_SD8+	D7	B_SDP1+	E28	XM_ADDR0	G15	PWR_05	K28	PWR_04
B21	B_SD9+	D8	B_SD1+	E29	XM_DATA5	G16	PWR_01		

Table 5.24 Alphanumeric List by BGA Position (Cont.)

BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name
K29	VDDC16	P28	PWR_04	U16	GND_01	Y4	A_SDP1+	AC31	DQ36
K30	DDR_CLKEN1	P29	NC	U17	GND_01	Y5	A_SDP1–	AC32	GND_01
K31	DQ23	P30	GND_01	U18	GND_01	Y6	NC	AC33	DDR_WE/
K32	A_DDR12	P31	DQ27	U19	GND_01	Y7	PWR_02	AC34	DQ39
K33	A_DDR9	P32	DQ24	U20	GND_01	Y15	GND_01	AD1	VDDC4
K34	DQ18	P33	DQ25	U28	PWR_04	Y16	GND_01	AD2	VSSC4
L1	A_SREQ–	P34	DQ26	U29	VDDC14	Y17	GND_01	AD3	GND_01
L2	A_SREQ+	R1	A_SDP0–	U30	A_DDR0	Y18	GND_01	AD4	NC
L3	GND_01	R2	A_SDP0+	U31	A_DDR10	Y19	GND_01	AD5	NC
L4	A_SMSG–	R3	GND_01	U32	A_DDR1	Y20	GND_01	AD6	SerialDATA
L5	NC	R4	A_VDDBIAS	U33	DDR_CLK0/	Y28	PWR_04	AD7	PWR_02
L6	VDDC1	R5	A_SATN–	U34	DDR_CLK0	Y29	NC	AD28	PWR_04
L7	PWR_02	R6	NC	V1	A_SD4–	Y30	BA_DDR0	AD29	VREF1
L28	PWR_04	R7	PWR_02	V2	A_SD2+	Y31	CB7	AD30	DDR_CS1/
L29	VREF0	R15	GND_01	V3	A_SD2–	Y32	GND_01	AD31	DDR_RAS/
L30	DQS2	R16	GND_01	V4	A_SD3+	Y33	BA_DDR1	AD32	GND_01
L31	DQ21	R17	GND_01	V5	A_SD3–	Y34	NC	AD33	DQ40
L32	GND_01	R18	GND_01	V6	NC	AA1	A_SD14–	AD34	DDR_CS0/
L33	DQ19	R19	GND_01	V7	PWR_02	AA2	A_SD13+	AE1	TCK
L34	DM2	R20	GND_01	V15	GND_01	AA3	A_SD13–	AE2	A_LED/
M1	A_SSEL–	R28	PWR_04	V16	GND_01	AA4	A_SD15+	AE3	NC
M2	A_SSEL+	R29	NC	V17	GND_01	AA5	GND_01	AE4	NC
M3	GND_01	R30	DM3	V18	GND_01	AA6	TDI_ICE	AE5	RTCK_ICE
M4	A_SACK+	R31	DQ28	V19	GND_01	AA7	PWR_02	AE6	NC
M5	A_SMSG+	R32	GND_01	V20	GND_01	AA28	PWR_04	AE7	PWR_02
M6	NC	R33	DQS3	V28	PWR_04	AA29	VSSC13	AE28	PWR_04
M7	PWR_01	R34	DQ29	V29	VREF2	AA30	GND_01	AE29	VSSC12
M28	PWR_01-NC	T1	A_SD7–	V30	DQS8	AA31	DQ34	AE30	DQ45
M29	VSSC15	T2	A_SD7+	V31	CB1	AA32	DQ35	AE31	DQ38
M30	DQ20	T3	GND_01	V32	CB3	AA33	DQ33	AE32	DQ44
M31	A_DDR6	T4	NC	V33	CB2	AA34	DQ32	AE33	DQS5
M32	GND_01	T5	VSSC2	V34	CB0	AB1	A_SD12+	AE34	DQ42
M33	DQ22	T6	NC	W1	A_SD0+	AB2	A_SD12–	AF1	VSSC5
M34	A_DDR8	T7	PWR_01	W2	A_SD0–	AB3	TRST_ICE/	AF2	SER_TX
N1	A_SRST–	T15	GND_01	W3	GND_01	AB4	A_SD15–	AF3	EXTRST/
N2	A_SRST+	T16	GND_01	W4	A_SD1+	AB5	GND_01	AF4	TDO_ICE
N3	NC	T17	GND_01	W5	A_SD1–	AB6	NC	AF5	TMS_ICE
N4	A_SACK–	T18	GND_01	W6	VSSC3	AB7	PWR_01	AF6	NC
N5	GND_01	T19	GND_01	W7	PWR_01	AB28	PWR_01-NC	AF7	PWR_01
N6	VSSC1	T20	GND_01	W15	GND_01	AB29	VDDC13	AF28	PWR_01
N7	PWR_01	T28	PWR_01-NC	W16	GND_01	AB30	GND_01	AF29	VDDC12
N28	PWR_01-NC	T29	VSSC14	W17	GND_01	AB31	DQS4	AF30	DQ41
N29	VDDC15	T30	DQ31	W18	GND_01	AB32	DQ37	AF31	DM5
N30	GND_01	T31	A_DDR2	W19	GND_01	AB33	DM4	AF32	DQ50
N31	A_DDR4	T32	GND_01	W20	GND_01	AB34	NC	AF33	DQ48
N32	A_DDR7	T33	DQ30	W28	PWR_01-NC	AC1	NC	AF34	DQ46
N33	A_DDR5	T34	A_DDR3	W29	NC	AC2	TDO	AG1	DISPCIFSN/
N34	NC	U1	A_SD6+	W30	CB5	AC3	GND_01	AG2	NC
P1	A_RBIAS	U2	A_SD6–	W31	DM8	AC4	NC	AG3	GND_01
P2	A_SBSY–	U3	A_SD4+	W32	GND_01	AC5	TRST/	AG4	TCK_ICE
P3	A_SBSY+	U4	A_SD5–	W33	CB6	AC6	HB_LED/	AG5	TDI
P4	A_SATN+	U5	A_SD5+	W34	CB4	AC7	PWR_01	AG6	NC
P5	GND_01	U6	NC	Y1	VDDC3	AC28	PWR_01-NC	AG7	PWR_01
P6	VDDC2	U7	PWR_02	Y2	A_SD14+	AC29	NC	AG28	PWR_01
P7	PWR_02	U15	GND_01	Y3	GND_01	AC30	DDR_CAS/	AG29	NC

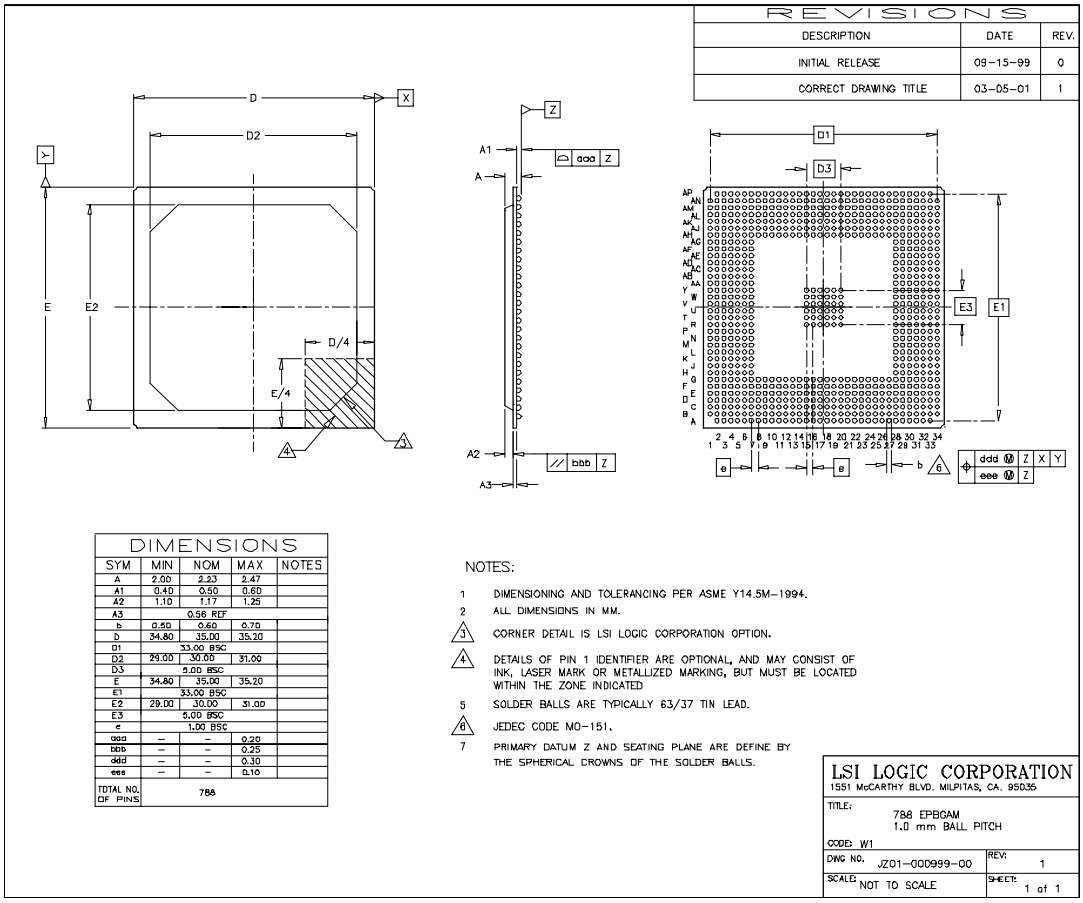
1. NC – Not Connected

Table 5.24 Alphanumeric List by BGA Position (Cont.)

BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name
AG30	DQ49	AJ17	FRAME/	AL4	GND_01	AM25	AD53	AP11	C_BE3/
AG31	DQ43	AJ18	VSSC9	AL5	PCI5VBIAS	AM26	PCI5VBIAS	AP12	AD21
AG32	GND_01	AJ19	AD11	AL6	NC	AM27	GND_01	AP13	C_BE2/
AG33	DQ52	AJ20	AD6	AL7	PCI5VBIAS	AM28	GND_01	AP14	PERR/
AG34	DQS6	AJ21	AD2	AL8	INTA/	AM29	AD39	AP15	NC
AH1	SPARE0	AJ22	VSSC10	AL9	NC	AM30	AD33	AP16	C_BE1/
AH2	NC	AJ23	C_BE5/	AL10	NC	AM31	GND_01	AP17	AD12
AH3	GND_01	AJ24	AD60	AL11	GNT/	AM32	GND_01	AP18	AD10
AH4	TMS	AJ25	AD56	AL12	AD28	AM33	NC	AP19	VDDC9
AH5	EXTPOR/	AJ26	PCI5VBIAS	AL13	AD26	AM34	DQ63	AP20	AD5
AH6	NC	AJ27	AD46	AL14	AD24	AN1	GND_01	AP21	AD1
AH7	PWR_01	AJ28	AD40	AL15	AD20	AN2	GND_01	AP22	C_BE4/
AH8	PWR_01	AJ29	AD34	AL16	AD16	AN3	NC	AP23	AD61
AH9	PWR_03	AJ30	DQ55	AL17	STOP/	AN4	NC	AP24	PCI5VBIAS
AH10	PWR_03	AJ31	DQ51	AL18	PCI5VBIAS	AN5	VSSC6	AP25	AD55
AH11	PWR_03	AJ32	DQS7	AL19	AD15	AN6	BZRSET	AP26	AD51
AH12	PWR_01	AJ33	DQ59	AL20	AD9	AN7	PCIPLLVDDA	AP27	AD47
AH13	PWR_01	AJ34	DQ58	AL21	AD4	AN8	NC	AP28	VSSC11
AH14	PWR_03	AK1	USEEXTPOR	AL22	AD0	AN9	INTB/	AP29	AD43
AH15	PWR_03	AK2	NC	AL23	REQ64/	AN10	AD29	AP30	AD37
AH16	PWR_01	AK3	NC	AL24	PAR64	AN11	AD25	AP31	NC
AH17	PWR_03	AK4	SerialCLK	AL25	VDDC10	AN12	AD23	AP32	NC
AH18	PWR_03	AK5	VDDC7	AL26	AD54	AN13	AD17	AP33	GND_01
AH19	PWR_01	AK6	NC	AL27	AD50	AN14	DEVSEL/	AP34	NC
AH20	PWR_03	AK7	NC	AL28	AD44	AN15	PCI5VBIAS		
AH21	PWR_03	AK8	VSSC8	AL29	AD38	AN16	SERR/		
AH22	PWR_01	AK9	NC	AL30	AD32	AN17	PCI5VBIAS		
AH23	PWR_01	AK10	NC	AL31	GND_01	AN18	AD8		
AH24	PWR_03	AK11	RST/	AL32	GND_01	AN19	PCI5VBIAS		
AH25	PWR_03	AK12	AD30	AL33	NC	AN20	AD3		
AH26	PWR_01	AK13	GND_01	AL34	DQ62	AN21	ACK64/		
AH27	PWR_01	AK14	GND_01	AM1	NC	AN22	PCI5VBIAS		
AH28	PWR_01	AK15	AD22	AM2	NC	AN23	AD59		
AH29	NC	AK16	AD18	AM3	GND_01	AN24	AD57		
AH30	DM6	AK17	TRDY/	AM4	GND_01	AN25	PCI5VBIAS		
AH31	DQ47	AK18	PAR	AM5	NC	AN26	AD49		
AH32	GND_01	AK19	AD13	AM6	NC	AN27	AD45		
AH33	DQ56	AK20	C_BE0/	AM7	GND_01	AN28	VDDC11		
AH34	DQ54	AK21	GND_01	AM8	GND_01	AN29	AD41		
AJ1	SPARE1	AK22	GND_01	AM9	VSSC7	AN30	AD35		
AJ2	NC	AK23	C_BE7/	AM10	AD31	AN31	NC		
AJ3	NC	AK24	AD62	AM11	GND_01	AN32	NC		
AJ4	B_LED/	AK25	AD58	AM12	GND_01	AN33	GND_01		
AJ5	SER_RX	AK26	AD52	AM13	AD19	AN34	GND_01		
AJ6	NC	AK27	AD48	AM14	IRDY/	AP1	NC		
AJ7	NC	AK28	AD42	AM15	GND_01	AP2	GND_01		
AJ8	NC	AK29	AD36	AM16	GND_01	AP3	NC		
AJ9	NC	AK30	DQ57	AM17	AD14	AP4	DDR_DRIVEMODE		
AJ10	NC	AK31	DQ53	AM18	AD7				
AJ11	NC	AK32	DQ61	AM19	GND_01	AP5	VDDC6		
AJ12	NC	AK33	DQ60	AM20	GND_01	AP6	BZVDD		
AJ13	NC	AK34	DM7	AM21	C_BE6/	AP7	PCIPLLVSSA		
AJ14	VDDC8	AL1	NC	AM22	AD63	AP8	PCI_CLK		
AJ15	IDSEL	AL2	VDDC5	AM23	GND_01	AP9	REQ/		
AJ16	NC	AL3	GND_01	AM24	GND_01	AP10	AD27		

2. NC – Not Connected

Figure 5.12 LSI53C1035 788-EPBGA Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code W1.**

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