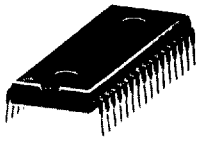
OSD IC WITH SYNC SEPARATOR

KS5513C is a monolithic IC that has On-Screen-Display function and internal sync separator.

32-SDIP-400



FUNCTION

- On-Screen-Display(OSD)
- Sync separator

FEATURES

- Maximum number of displayable characters: 240 (24 characters ×10 rows)
- Construction of character: 12 × 18 dots
- 28 kind of character available
- Maximum size of character: 4×4 times of normal
- Display: 62 ways in horizontal and 64 ways in vertical controlled by μ-com.
- Blinking: Adjustable blinking time and able to control each character
- Selectable blanking way
- Automatically select the internal sync or external sync
- Sync detector & separator
- Internal AFC circuit
- Internal test loging

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5513C	32-SDIP-400	−20°C~+70°C

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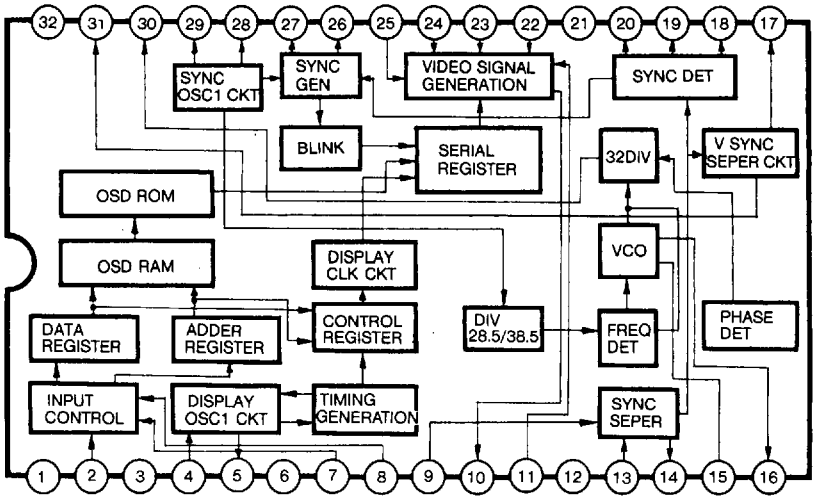
BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	I/O	FUNCTION
1	DGND		Digital GND
2	CLK	I	Clock input
3	AC	I	Auto Clear, Reset whole circuit when "L"
4	OSC1	I	Standard oscillation frequency is 7MHz. Horizontal starting position
5	OSC2	O	is adjustable by means of clock of this oscillation pins.
6	N/P	I	"H" for NTSC and "L" for PAL
7	CS	I	"L" for serial data input
8	SIN	I	Serial data input
9	CVIN1	I	Composite video signal input for detecting and separating of sync.
10	CVIOUT	O	Composite video signal output($2V_{p\text{-}p}$)
11	CVIN2	I	Composite video signal input
12	AGND		Analog GND
13	LFT	I	Separating sync from composite signal
14	CSY OUT	O	Separated H, V sync out
15	AFCIN	I	Composite sync input
16	AFCFIL	O	Filter for automatic frequency control
17	SYNCINT	O	Separate Vsync from composite sync
18	MMTC	O	Decide the time constant of MONOMULTI
19	MMINT	O	Integrating MONOMULTI OUTPUT
20	SYD	O	"H" if sync signal exist, unless "L"
21	AVCC		Analog VCC
22	RSIN	I	Level controlled pin 26 RS output
23	LEBK	I	Blanking level input
24	LECHA	I	Character level input
25	CBIN	I	Level converted input pin from CB output pin
26	RS	O	Color subcarrier output for backscreen of characters
27	CB	O	Color burst signal output
28	OSCOUT	O	Oscillation circuit for backscreen, 14.43MHz for NTSC
29	OSCIN	I	17.73MHz for PAL
30	HOR	O	Separated Hsync output from composite sync
31	VERT	O	Separated Vsync output from composite sync
32	DVCC		Digital VCC

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power VTG	V_{DD}	−0.3~6	V
Input VTG	V_I	$V_{SS}-0.3 \simeq V_I$ $V_I \simeq V_{DD}+0.3$	V
Output VTG	V_O	$V_{SS} \simeq V_O \simeq V_{DD}$	V
Power Dissipation	P_d	300	mW
Operating Temperature	T_{opr}	−20~+70	°C
Storage Temperature	T_{stg}	−40~+12.5	°C

ELECTRICAL CHARACTERISTICS (V_{DD}=5V, Ta=25°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Operating VTG	V_{DD}		4.75	5.00	5.25	V
Operating Current	I_{DD}		15	20	25	mA
AFC Freerun Freq	F_{FR}		15.5	15.7	15.9	KHz
AFC Pulse Width	T_{WD}		3.7	4.0	4.3	usec
AFC Delay Time	T_D		2.0	3.0	4.0	usec
AFC Locking Range I	F_{ALH}		+600	–	–	KHz
AFC Locking Range II	F_{ALL}		−900	–	–	KHz
AFC Capture Range H	F_{ACH}		+400	–	–	KHz
AFC Capture Range L	F_{ACL}		−700	–	–	KHz
AFC Output H	V_{HAH}		3.9	4.1	4.3	V
AFC Output L	V_{HAL}		0	0.1	0.18	V
Sync Sep. Level	V_{SE}		0.1	0.2	0.3	V
Sync Sep. Delay Time	T_{SD}		0	0.6	1.5	usec
Sync Sep. Output H	V_{OH}		3.9	4.1	4.3	V
Sync Sep. Output L	V_{OL}		0	0.1	0.18	V
V Sync Threshold H	V_{TH}		2.35	2.5	2.65	V
V Sync Threshold L	V_{TL}		1.4	1.55	1.7	V
V Sync Output H	V_{DH}		3.9	4.1	4.3	V
V Sync Output L	V_{DL}		0	0.1	0.18	V
V Sync Delay Time	T_{VD}		5	10	15	usec
V Sync Pulse Width	T_{VW}		212	272	332	usec
Sync Det. Lock VTG	V_{IH}		2.5	2.7	2.85	V
Sync Det. Lock VTG	V_{II}		1.3	1.45	1.6	V
Sync Det. Capture VTG	V_{CH}		2.15	2.3	2.45	V
Sync Det. Capture VTG	V_{CL}		1.5	1.7	1.85	V

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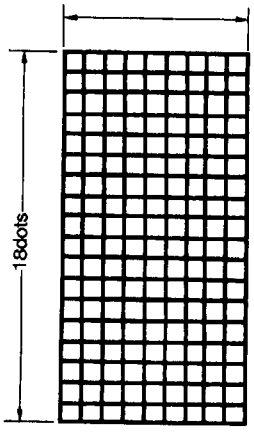
ELECTRICAL CHARACTERISTICS (V_{DD}=5V, Ta=25°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Operating VTG	V_{DD}		4.75	5.00	5.25	V
Operating Current	I_{DD}		20	27	35	mA
AFC Freerun Frequency	F_{fr}		15.5	15.7	15.9	KHz
AFC Pulse Width	t_{wd}		3.7	4.0	4.3	usec
AFC Delay Time	t_d		2.0	3.0	4.0	usec
AFC Locking Range H	F_{alh}		+600	–	–	Hz
AFC Locking Range L	F_{all}		−900	–	–	Hz
AFC Capture Range H	F_{ach}		+400	–	–	Hz
AFC Capture Range L	F_{acl}		−700	–	–	KHz
AFC Output H	V_{hah}		3.9	4.1	4.3	V
AFC Output L	V_{hal}		0	0.1	0.18	V
Sync Sep. Level	V_{se}		0.1	0.2	0.3	V
Sync Sep. Delay Time	t_{sd}		0	0.6	1.5	usec
Sync Sep. Output H	V_{oh}		3.9	4.1	4.3	V
Sync Sep. Output L	V_{ol}		0	0.1	0.18	V
V Sync Threshold H	V_{th}		2.35	2.5	2.65	V
V Sync Threshold L	V_{tl}		1.4	1.55	1.7	V
V Sync Output H	V_{DH}		3.9	4.1	4.3	V
V Sync Output L	V_{dl}		0	0.1	0.18	V
V Sync Delay Time	t_{vd}		5	10	15	usec
V Sync Pulse Width	t_{vw}		212	272	332	usec
Sync Det. Lock VTG H	V_{lh}		2.5	2.7	2.85	V
Sync Det. Lock VTG L	V_{ll}		1.3	1.45	1.6	V
Sync Det. Capture VTG H	V_{ch}		2.15	2.3	2.45	V
Sync Det. Capture VTG L	V_{cl}		1.5	1.7	1.85	V

CHARACTER STRUCTURE

One character consists of 12×18 Dots, however, character blocks can be combined to make larger, more detailed characters.



- **When the character is in the first line, there is no outline above.**
- **When the character is in the 18th line, there is no outline below.**

SCREEN STRUCTURE

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239

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MEMORY STRUCTURE

- The memory address consists of 16 bits
- The address 0~239 are for the display data memory
- The address 240~243 are for the display control register

DATA MEMORY

BIT / ADDRESS	DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H	X	X	X	X	T3	T2	T1	T0	BL	M6	M5	M4	M3	M2	M1	M0
01H	X	X	X	X	T3	T2	T1	T0	BL	M6	M5	M4	M3	M2	M1	M0
02H	X	X	X	X	T3	T2	T1	T0	BL	M6	M5	M4	M3	M2	M1	M0
									BL -IN -K							
EFH	X	X	X	X	T3	T2	T1	T0	BL	M6	M5	M4	M3	M2	M1	M0

CONTROL REGISTER

BIT / ADDRESS	DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	비 고
F0H	X	X	X	X	X	INT/ NON	HRS 21	HRS 20	HRS 11	HRS 10	H5	H4	H3	H2	H1	H0	Instruction Register 1
F1H	X	X	X	X	X	BLI NK2	VRS 21	VRS 20	VRS 11	VRS 10	V5	V4	V3	V2	V1	V0	Instruction Register 2
F2H	X	X	X	X	X	DR3	DR2	DR1	RAM ERS	TE- ST	X	LVL 1	LVL 0	P2	P1	P0	Instruction Register 3
F3H	X	X	X	X	X	BB	BG	BR	DSP ON	BLA NK1	BLA- NK0	BLA- NK1	BLI- NK0	EX/ IN	Y	AB- LND	Instruction Register 4

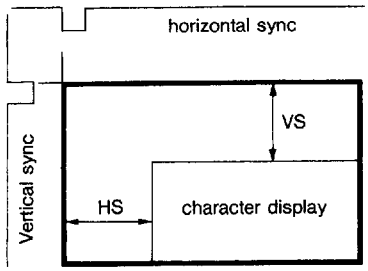
(1) Address 240

<table>
<tr><th rowspan="2">Data
0~B</th><th rowspan="2">Bit
Name</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>Value</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0
(LSB)</td><td>0</td><td rowspan="11">The horizontal display start position is HS
$HS=T_c\{\times[4\times\sum_{n=0}^{5}(HP(n)\times 2^2)]+N\}$
T_c=oscillation period
<table><tr><th>HSZ11
HSZ21</th><th>HSZ10
HSZ20</th><th>N</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="11">The horizontal display start position is defined with 6 bits, HP-5~HP0. HS horizontal display start position is reset by a one shot pulse in front of the HOR' signal. The available are is HPS~HP 0=(000010)~(111111) HP5~HP0=(000001) ~(000000) can't be used</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5
(MSB)</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">HSZ10</td><td>0</td><td rowspan="3"><table><tr><th>HSZ10
HSZ11</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1TC/DOT</td><td>2TC/DOT</td></tr><tr><td>1</td><td>3TC/DOT</td><td>4TC/DOT</td></tr></table><table><tr><th>HSZ11</th><th>HSZ10</th><th>N</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="3">The first ROW horizontal character size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">HSZ11</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">HSZ20</td><td>0</td><td rowspan="3"><table><tr><th>HSZ20
HSZ21</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1TC/DOT</td><td>2TC/DOT</td></tr><tr><td>1</td><td>3TC/DOT</td><td>4TC/DOT</td></tr></table><table><tr><th>HSZ21</th><th>HSZ20</th><th>N</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="3">Horizontal character size for ROWs two to ten</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">HSZ21</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">INT/NON</td><td>0</td><td>Interlace (262.5H/field)</td><td rowspan="2">Display change to interlace or non-interlace. Effective internally</td></tr>
<tr><td>1</td><td>Non-interlace (263H/field)</td></tr>
<tr><td>B</td><td>P</td><td>–</td><td>Parity</td><td>There is no register for this.</td></tr>
</table>

Reset state is set to all "0"

5

(2) Address 241

<table>
<tr><th>Data
0~B</th><th>Bit
Name</th><th colspan="2">Contents
Value</th><th>Function</th><th>Notes</th></tr>
<tr><td>0</td><td>VP0</td><td>0
1</td><td colspan="2" rowspan="9">The starting position of vertical direction display VS
VS=H*(4(2*VP5+2*VP4+2*VP3+2*VP2
+2*VP1+2*VP0+2)
H:horizontal sync pulse period
 
</td><td rowspan="9">Vertical
start
position</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>5</td><td>VP5</td><td>0
1</td></tr>
<tr><td>6</td><td>VSZ10</td><td>0
1</td><td colspan="2" rowspan="2"><table><tr><th>VSZ10
VSZ11</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/DOT</td><td>2H/DOT</td></tr><tr><td>1</td><td>3H/DOT</td><td>4H/DOT</td></tr></table></td><td rowspan="2">Vertical
direction
character size
of 1st row</td></tr>
<tr><td>7</td><td>VSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>VSZ20</td><td>0
1</td><td colspan="2" rowspan="2"><table><tr><th>HSZ20
HSZ21</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/DOT</td><td>2H/DOT</td></tr><tr><td>1</td><td>3H/DOT</td><td>4H/DOT</td></tr></table></td><td rowspan="2">Vertical
direction
character size
of 2nd~10th
row</td></tr>
<tr><td>9</td><td>VSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>BLINK2</td><td>0
1</td><td colspan="2">Vsync/64 by period 1sec
Vsync/32 by period 0.5sec</td><td>Blink period
control</td></tr>
<tr><td>B</td><td>P</td><td>–</td><td colspan="2">Parity</td><td></td></tr>
</table>

(3) Address 242

<table>
<tr><th>Data
0~B</th><th>Bit
Name</th><th colspan="2">Contents
Value / Function</th><th>Notes</th></tr>
<tr><td>0</td><td>PHASE0</td><td>0
1</td><td rowspan="4"><table><tr><th>phase2</th><th>phase1</th><th>phase0</th><th>NTSC</th><th>PAL</th></tr><tr><td>0</td><td>0</td><td>0</td><td>90°</td><td>± 90°</td></tr><tr><td>0</td><td>0</td><td>1</td><td>180°</td><td>+0°</td></tr><tr><td>0</td><td>1</td><td>0</td><td>270°</td><td>∓ 90°</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0°</td><td>± 180°</td></tr><tr><td>1</td><td>0</td><td>0</td><td>45°</td><td>± 135°</td></tr><tr><td>1</td><td>0</td><td>1</td><td>135°</td><td>± 45°</td></tr><tr><td>1</td><td>1</td><td>0</td><td>225°</td><td>∓ 45°</td></tr><tr><td>1</td><td>1</td><td>1</td><td>315°</td><td>∓ 135°</td></tr></table></td><td rowspan="4">Backscreen
control bit</td></tr>
<tr><td>1</td><td>PHASE0</td><td>0
1</td></tr>
<tr><td>2</td><td>PHASE0</td><td>0
1</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>3</td><td>LEVEL0</td><td>0
1</td><td rowspan="2"><table><tr><th>level1 \ level0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>No internal bias</td><td>internal bias(1)</td></tr><tr><td>1</td><td>internal bias(2)</td><td>internal bias(3)</td></tr></table></td><td rowspan="2">Color level
control</td></tr>
<tr><td>4</td><td>LEVEL1</td><td>0
1</td></tr>
<tr><td>5</td><td>TC455/
454</td><td>0
1</td><td>1H=454T_C T_C=2fosc
1H=455T_C</td><td></td></tr>
<tr><td>6</td><td>TESTCK</td><td>0
1</td><td>Active mode
Test mode</td><td>Test
register</td></tr>
<tr><td>7</td><td>RAM
ERS</td><td>0
1</td><td>RAM is not erasable
RAM erase</td><td></td></tr>
<tr><td>8</td><td>DSP1</td><td>0
1</td><td>Fixed blanking of 1st row directed by BLK0, BLK1
Adjustable blanking of 1st row</td><td></td></tr>
<tr><td>9</td><td>DSP2</td><td>0
1</td><td>Fixed blanking of 2nd~9th row directed by BLK0, BLK1
Adjustable blanking of 2nd~9th row</td><td></td></tr>
<tr><td>10</td><td>DSP3</td><td>0
1</td><td>Fixed blanking of 10th row directed by BLK0, BLK1
Adjustable blanking of 10th row</td><td></td></tr>
<tr><td>B</td><td>P</td><td>——</td><td>Parity</td><td></td></tr>
</table>

5

(4) Address 243

<table>
<tr><th rowspan="2">Data
0~B</th><th rowspan="2">register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>0</td><td>Painting the blanking area</td><td rowspan="2">Docided by
blk0, blk1, BR, BG
BB</td></tr>
<tr><td>1</td><td>Painting TV whole screen area</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">YM</td><td>0</td><td>The same color of character and backscreen</td><td rowspan="2">Dacided by BCOL

BLK0, BLK1</td></tr>
<tr><td>1</td><td>Backacreen luminance is adjustable</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>0</td><td>External sync is used</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Internal sync is used</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="3">blinking mode control
<table><tr><th>blink0
blink1</th><th>0</th><th>1</th></tr><tr><td>0</td><td>blinking off</td><td>duty 25%</td></tr><tr><td>1</td><td>duty 50%</td><td>duty 75%</td></tr></table></td><td rowspan="3">Blinking
duty is
adjustable</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="3">blanking mode control
<table><tr><th>blink0
blink1</th><th>0</th><th>1</th></tr><tr><td>0</td><td>blinking off</td><td>character blanking</td></tr><tr><td>1</td><td>outline size</td><td>whole blanking</td></tr></table></td><td rowspan="3">Blinking
area is
adjustable</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">DSP
ON</td><td>0</td><td>Display off</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display on</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">BR</td><td>0</td><td>Backacreen color R ON</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Backacreen color R OFF</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">BG</td><td>0</td><td>Backacreen color G ON</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Backacreen color G OFF</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">BB</td><td>0</td><td>Backacreen color B ON</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Backacreen color B OFF</td></tr>
<tr><td>B</td><td>P</td><td></td><td>Parity</td><td></td></tr>
</table>

10. BLANKING METHOD

BCOL	BLANKING SIZE		BLANKING METHOD	DSP 3	DSP 2	DSP 1	DISPLAY METHOD	
	BLK1	BLK0						
0	0	0	BLANKING OFF	0	0	0	Blanking OFF	REST is O
				0	0	1	1st row C	
				0	1	0	2nd~9th row C	
				1	0	0	10th row C	
	0	1	CHARACTER BLANKING	0	0	0	Blanking OFF	REST is C
				0	0	1	1st row O	
				0	1	0	2nd~9th row O	
				1	0	0	10th row O	
	1	0	OUTLINE BLANKING	0	0	0		REST is O
				0	0	1	1st row R	
				0	1	0	2nd~9th row R	
				1	0	0	10th row R	
	1	1	WHOLE BLANKING	0	0	0		REST is R
				0	0	1	1st row C	
				0	1	0	2nd~9th row C	
				1	0	0	10th row C	
1	X	X		X	X	X	Whole area blanking except while part of character.	

C: Character blanking

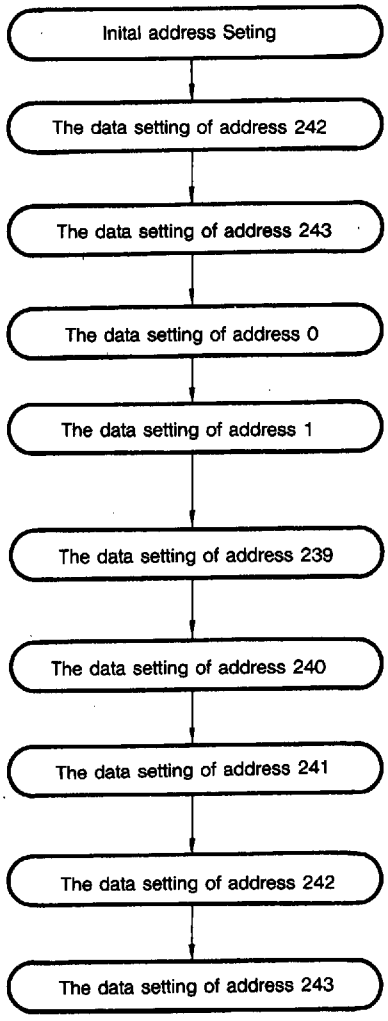
O: Outline blanking

R: Whole blanking

5

SERIAL DATA INPUT METHOD

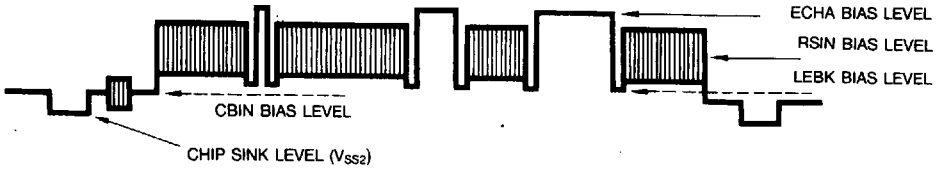
THE DATA, Inputed From Micom, is inputted as 16 BIT SERIAL METHOD 16BIT IS 1 WORD, The method of serial data input is following



COMPOSITE VIDEO SIGNAL

External Bias (no internal bias)

When the composite video signal is created with extemal bias, it is possible to have any size signal, depending on the bias power level external to the IC.

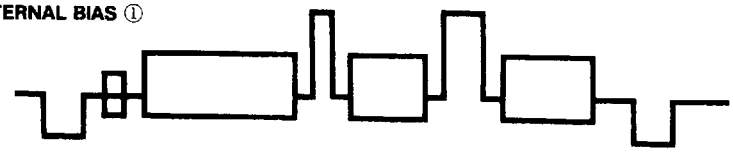


INTERNAL BIAS

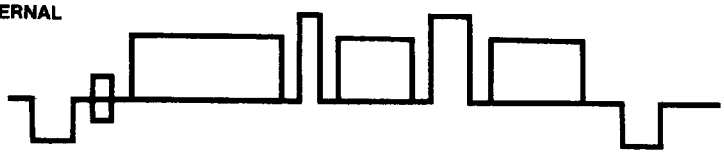
MODE / PIN	INTERNAL BIAS (1)	INTERNAL BIAS (1)	INTERNAL BIAS (1)	UNIT
BKLEV PIN OUTPUT LEVEL	0.6	0.6	0.6	V
CHRLEV PIN OUTPUT LEVEL	2.32	2.32	2.32	V
BURIN PIN OUTPUT LEVEL	0.6	0.6	0.6	V
BSCIN PIN OUTPUT LEVEL	0.8	1.15	1.54	V

5

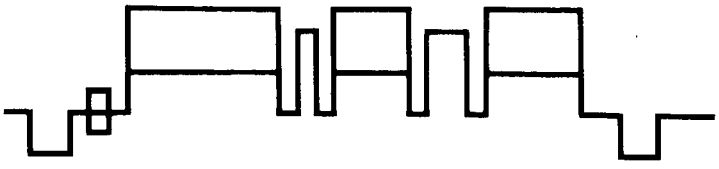
INTERNAL BIAS ①



INTERNAL



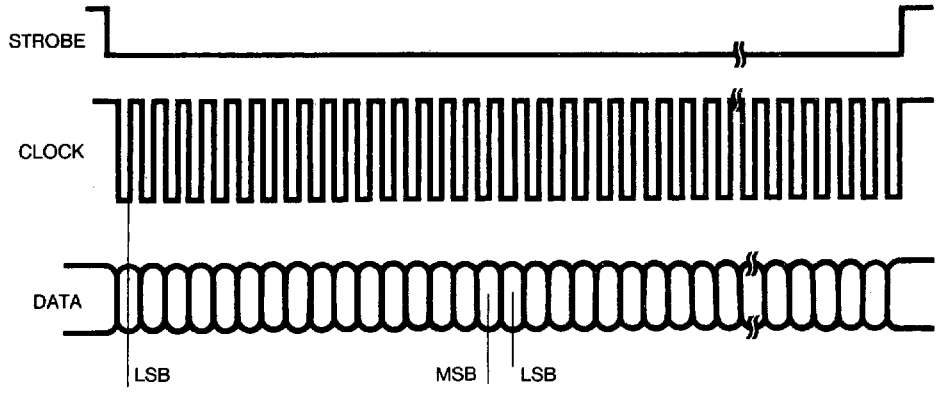
INTERNAL BIAS ②



TIMING AT DATA INPUT

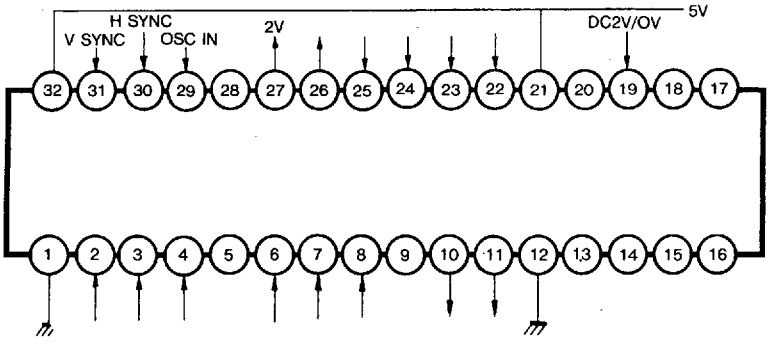
Serial Input

(1) The address is comprised of 16 bits the effective address being the lower 8 bits are 4 "0"s followed by a parity bit and 3 more "0"s.
(2) The data are comprised of 16 bits, the lower 11 bits being data preceeded by a parity bit, the upper 4 bits all being "0".
(3) After CS signal trailing edge, 16 bits of SCK are the address, after that, data being input increments the address every 16 bits.
(4) LSB is first & Clock timing is rising edge
(5) The active data OF ADDRESS is 8 bits FROM LSB
(6) The active data of CONTROL registers is 11 bits from LSB
(7) The active data of RAM is 8 bits from LSB

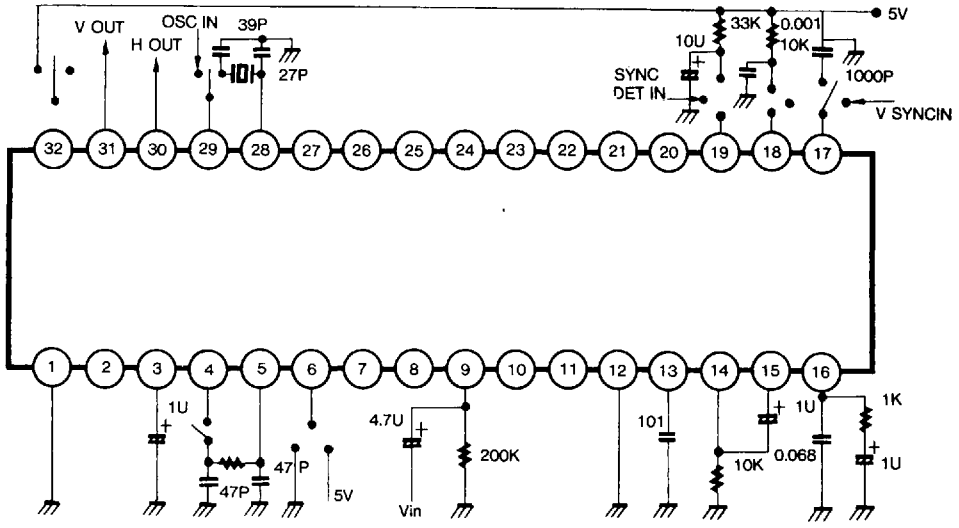


TEST CIRCUIT

1) OSD BLOCK



2)SYNC BLOCK



TYPICAL APPLICATION CIRCUIT