Z89195/ Z89196 (ROMLESS)

VOICE PROCESSING CONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z89195	32	256	63	4.5V to 5.5V
Z89196	–	256	47	4.5V to 5.5V

Note: *General-Purpose

- Watch-Dog Timer and Power-On Reset
- Improved Low Power Stop Mode
- Two Comparators
- RAM and ROM Protect
- Phase Locked Loop to generate up to 20.48 MHz DSP clock rate (10.24 MHz for Z8), with direct clock bypass option.
- On-Board Oscillator for 32.768 kHz Real-Time Clock
- Flexible Audio RAM Controller
- UART/Self-Clocking Transceiver Interface
- 16-Bit Digital Signal Processor (DSP) at 20 MIPs
- 16K-Word DSP Program ROM
- Two 256-Word DSP RAM Banks
- 8-Bit A/D Converter with up to 16 kHz Sample Rate
- Single Channel Codec Interface
- 10-Bit PWM D/A Converter
- Six Vectored, Prioritized Z8 Interrupts
- Three Vectored, Prioritized DSP Interrupts
- Two DSP Timers to Support Different A/D and D/A Sampling Rates
- Developer's Toolbox for Bellcore 202 and CCITT V.23 compliant CID Applications
- Developer's Toolbox for T.A.M. Applications

GENERAL DESCRIPTION

The Z89195/196 is a fully integrated, dual processor controller designed for voice processing applications. The I/O control processor is a Z8® MCU with 32 KB of program memory, two 8-bit counter/timers, and up to 63 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512x16 bits of RAM, single cycle instructions, and 16K words of program ROM. The chip also contains a half-flash 8-bit A/D converter with up to a 16 kHz sample rate and a 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D can be extended by resampling the data at a lower rate in software. In addition, a single-channel Codec Interface, a UART/Self-Clocking Transceiver, as well as a flexible Audio RAM Controller are incorporated. The Z8 and DSP processors are coupled by mailbox registers and an interrupt system. DSP or Z8 programs can be directed by events in each other's domain.

The Z89196 is the ROMless version of the Z89195. However, the on-chip DSP is not ROMless.

Note: All signals with an overline, "‾" are active Low. For example, B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z8 Core Processor

The on-chip Z8 is Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripheral and I/O circuits. The Z8 offers a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features which makes it ideally suited for high-volume processing, peripheral controllers and consumer applications.

For applications demanding powerful I/O capabilities, the Z89195 provides 63 pins dedicated to input and output. These I/O lines are grouped into eight ports. Each port is configurable under software control to provide timing, status signals and parallel I/O with or without handshake.

Four basic memory resources for the Z8 are available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Z8 core processor is supported by an efficient register file that allows any of 256 on-board data and control registers to be either the source and/or the destination of almost any instruction. This unique architecture eliminates traditional microprocessor accumulator bottlenecks and permits rapid content switching.

The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of mailbox registers, WDT mode register, DSP Control register, Stop-Mode Recovery register, Port Configuration register, and the control and data registers for Ports 4, 5, 6 and 7. Some of these registers are shared with the DSP.

The Z8 can access external audio RAMs in various configurations via the ARAM Controller.

A UART/Self-Clocking transceiver is provided to communicate with an external processor or peripheral device.

To unburden the software from supporting real-time problems such as counting/timing and data communication, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes.

Watch-Dog Timer and Stop-Mode Recovery features are software driven by setting specific bits in control registers.

STOP and HALT instructions support reduced power operation. The low-power STOP Mode allows parameter information to be stored in the register file if power fails. An external capacitor or battery will retain device memory and power the 32 kHz timer.

DSP Coprocessor

The DSP coprocessor is a second generation, 16-bit two's complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains two on-chip data RAM blocks of 256 words, a 16K word program ROM, 24-bit ALU, 16x16 multiplier, 24-bit Accumulator, shifter, six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of four pointers which can be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single-cycle scalar multiply.

Four external DSP registers are mapped into the expanded register file of the Z8. Communication between the Z8 and the DSP occurs through those common registers which form the mailbox registers.

The analog output is generated by a 10-bit resolution Pulse Width Modulator. The PWM output is a digital signal with CMOS output levels. The output signal has a resolution of 1 in 1024 with a sampling rate of 16 kHz (PLL clock = 20.48 MHz). The sampling rate can be changed under software control and can be set at 10 and 16 kHz.

An 8-bit resolution half-flash A/D converter is provided. The conversion is conducted with a sampling frequency of 16 kHz in order to provide oversampling. The input signal is 4V peak to peak.

Two additional timers (Timer2 and Timer3) have been added to support different sampling rates for the A/D and D/A converters. These timers are free-running counters that divide the crystal frequency to the appropriate sampling of frequency. Two DSP controlled output pins: DSP0, DSP1 are provided for application.

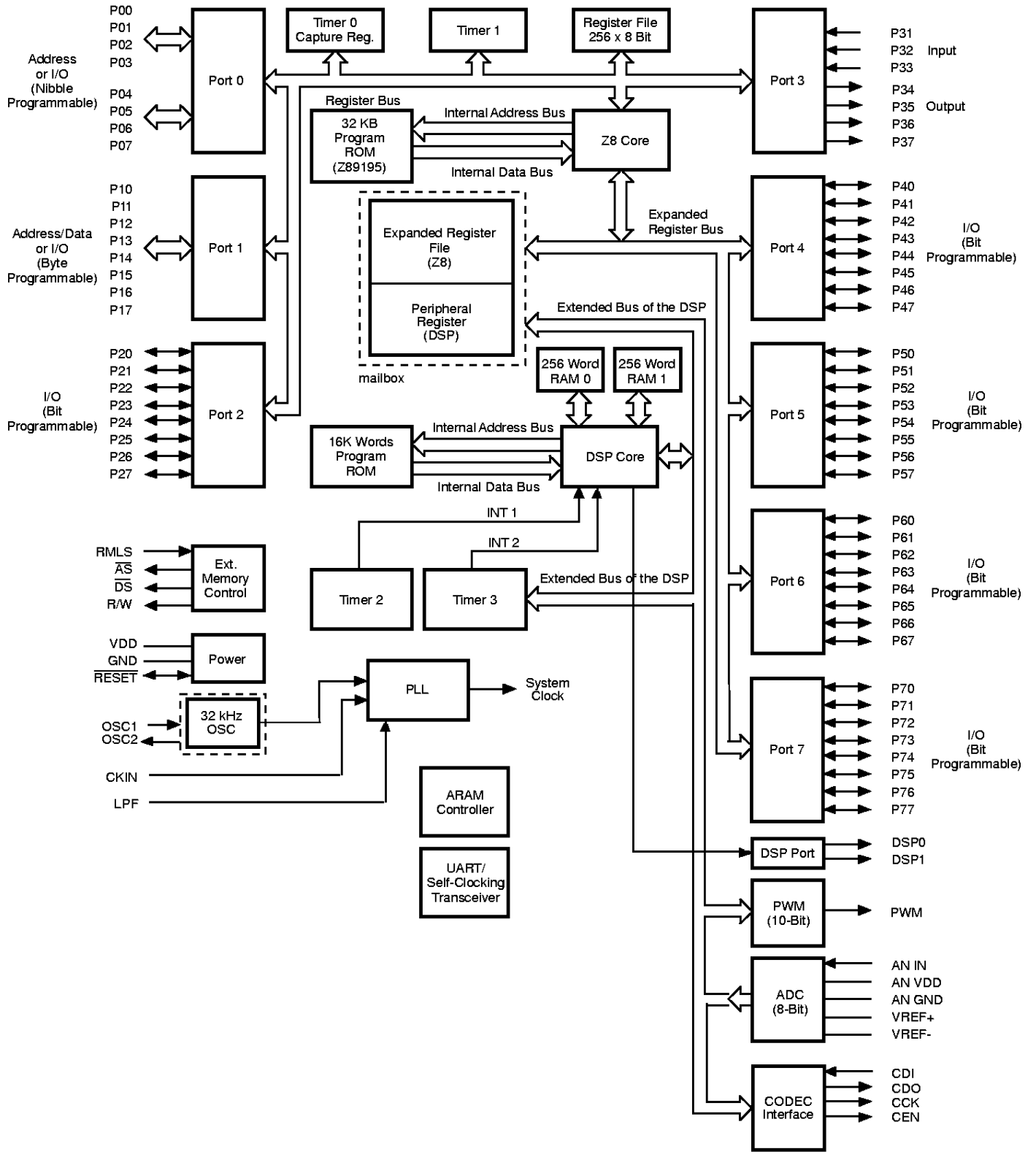

Figure 1. Z89195/196 Functional Block Diagram

PIN DESCRIPTION

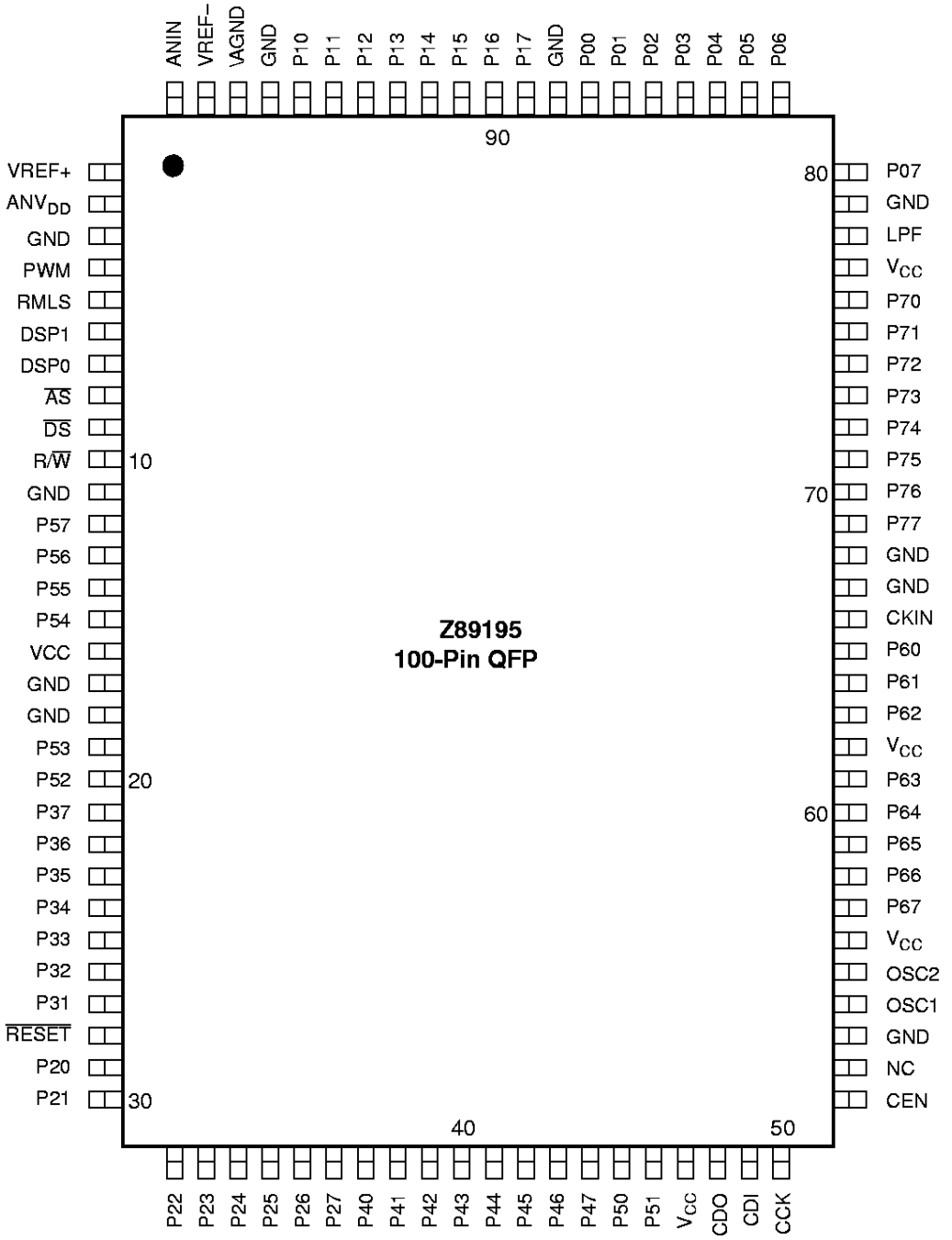

Figure 2. Z89195 100-Pin QFP Pin Configuration

Table 1. Z89195 100-Pin QFP Pin Identification

Pin Number	I/O Port Symbol	Direction	Function
3, 11, 17, 18, 53, 67, 68, 79, 88, 97	GND		Digital Ground
16, 47, 56, 62,77	V_{CC}		Digital V_{CC} = +5V
1	VREF+	Input/Output	Analog Voltage Ref+
2	ANV_{DD}		Analog V_{DD}
4	PWM	Output	PWM Output
5	RMLS	Input	ROMLESS Control Input
6, 7	DSP1–0	Output	DSP User Output 1, 0
8	$\overline{AS}$	Output	Address Strobe
9	$\overline{DS}$	Output	Data Strobe
10	R/$\overline{W}$	Output	Read/Write
12–15	P57–P54	Input/Output	Port 5 Bit 7–4
19, 20	P53–P52	Input/Output	Port 5 Bit 3–2
21–24	P37–P34	Output	Port 3 Bit 7–4
25–27	P33–P31	Input	Port 3 Bit 3–1
28	$\overline{RESET}$	Input/Output	Reset
29–36	P20–P27	Input/Output	Port 2, Bit 0–7
37–44	P40–P47	Input/Output	Port 4, Bit 0–7
45, 46	P50–P51	Input/Output	Port 5, Bit 0–1
48	CDO	Output	Codec Interface Output
49	CDI	Input	Codec Interface Input
50	CCK	Output	Codec clock
51	CEN	Output	Codec enable
52	NC	Input	No connection
54	OSC1	Input	Crystal Input (32.768 kHz)
55	OSC2	Output	Crystal Output (32.768 kHz)
57–61	P67–P63	Input/Output	Port 6, Bit 7–3
63–65	P62–P60	Input/Output	Port 6, Bit 2–0
66	CKIN	Input	Input Clock
69–76	P77–P70	Input/Output	Port 7, Bit 7–0
78	LPF	Input	PLL Low Pass Filter
80–87	P07–P00	Input/Output	Port 0, Bit 7–0
89–96	P17–P10	Input/Output	Port 1, Bit 7–0
98	ANGND		Analog GND
99	VREF–	Input	Analog Voltage Ref–
100	ANIN	Input	Analog Input

PIN DESCRIPTION (Continued)

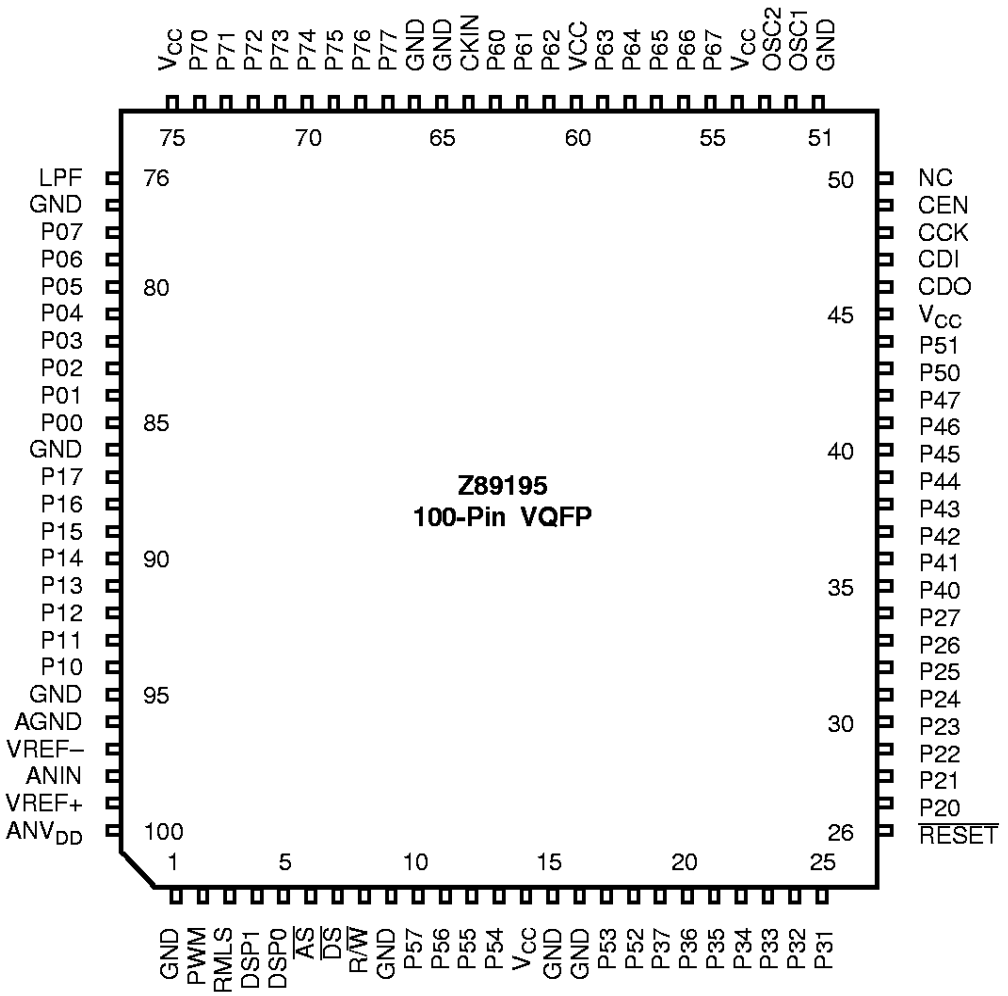

Figure 3. Z89195 100-Pin VQFP Pin Configuration

Table 2. Z89195 100-Pin VQFP Pin Identification

Pin Number	I/O Port Symbol	Direction	Symbol
1, 9, 15, 16, 51, 65, 66, 77, 86, 95	GND		Digital Ground
14, 45, 54, 60, 75	V_{CC}		Digital V_{CC} = +5V
99	VREF+	Input/Output	Analog Voltage Ref+
100	ANV_{DD}		Analog V_{DD}
2	PWM	Output	PWM Output
3	RMLS	Input	ROMLESS Control Input
4, 5	DSP1–0	Output	DSP User Output 1, 0
6	$\overline{AS}$	Output	Address Strobe
7	$\overline{DS}$	Output	Data Strobe
8	R/$\overline{W}$	Output	Read/Write
10–13	P57–P54	Input/Output	Port 5 Bit 7–4
17, 18	P53–P52	Input/Output	Port 5 Bit 3–2
19–22	P37–P34	Output	Port 3 Bit 7–4
23–25	P33–P31	Input	Port 3 Bit 3–1
26	$\overline{RESET}$	Input/Output	Reset
27–34	P20–P27	Input/Output	Port 2, Bit 0–7
35–42	P40–P47	Input/Output	Port 4, Bit 0–7
43, 44	P50–P51	Input/Output	Port 5, Bit 0–1
46	CDO	Output	Codec Interface Output
47	CDI	Input	Codec Interface Input
48	CCK	Output	Codec Clock
49	CEN	Output	Codec Enable
52	OSC1	Input	Crystal Input (32.768 kHz)
53	OSC2	Output	Crystal Output (32.768 kHz)
55–59	P67–P63	Input/Output	Port 6, Bit 7–3
61–63	P62–P60	Input/Output	Port 6, Bit 2–0
64	CKIN	Input	Input Clock
67–74	P77–P70	Input/Output	Port 7, Bit 7–0
76	LPF	Input	PLL Low Pass Filter
78–85	P07–P00	Input/Output	Port 0, Bit 7–0
87–94	P17–P10	Input/Output	Port 1, Bit 7–0
96	ANGND		Analog GND
97	VREF–	Input	Analog Voltage Ref–
98	ANIN	Input	Analog Input

PIN DESCRIPTION (Continued)

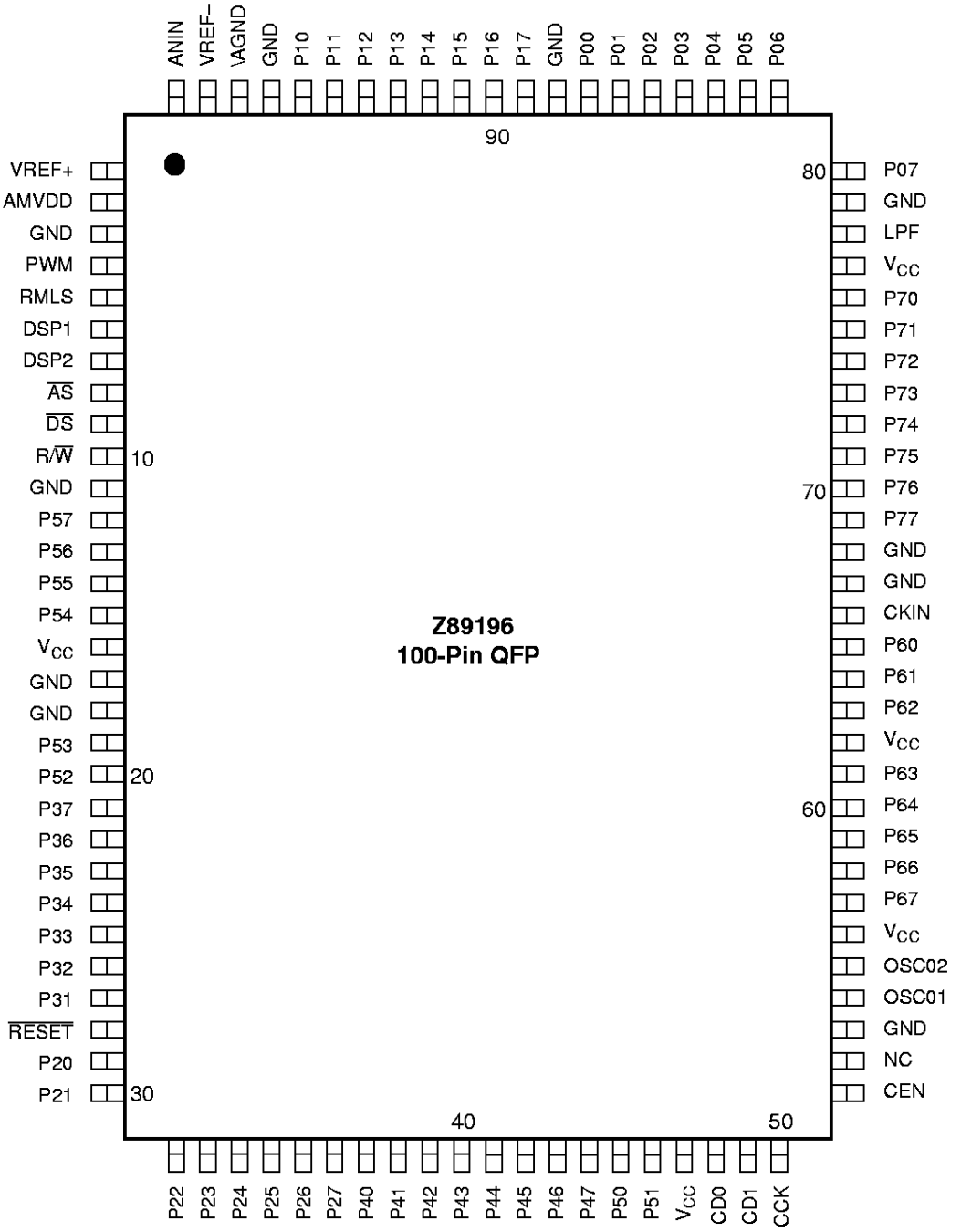

Figure 4. Z89196 100-Pin QFP Pin Configuration

Table 3. Z89196 100-Pin QFP Pin Identification

Pin Number	I/O Port Symbol	Direction	Function
3, 11, 17, 18, 53, 67, 68, 79, 88, 97	GND		Digital Ground
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1	VREF+	Input/Output	Analog Voltage Ref+
2	ANV_{DD}		Analog V_{DD}
4	PWM	Output	PWM Output
6, 7	DSP1–0	Output	DSP User Output 1, 0
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78	LPF	Input	PLL Low Pass Filter
80–87	P07–P00	Input/Output	Port 0, Bit 7–0
89–96	P17–P10	Input/Output	Port 1, Bit 7–0
98	ANGND		Analog GND
99	VREF–	Input	Analog Voltage Ref–
100	ANIN	Input	Analog Input

PIN DESCRIPTION (Continued)

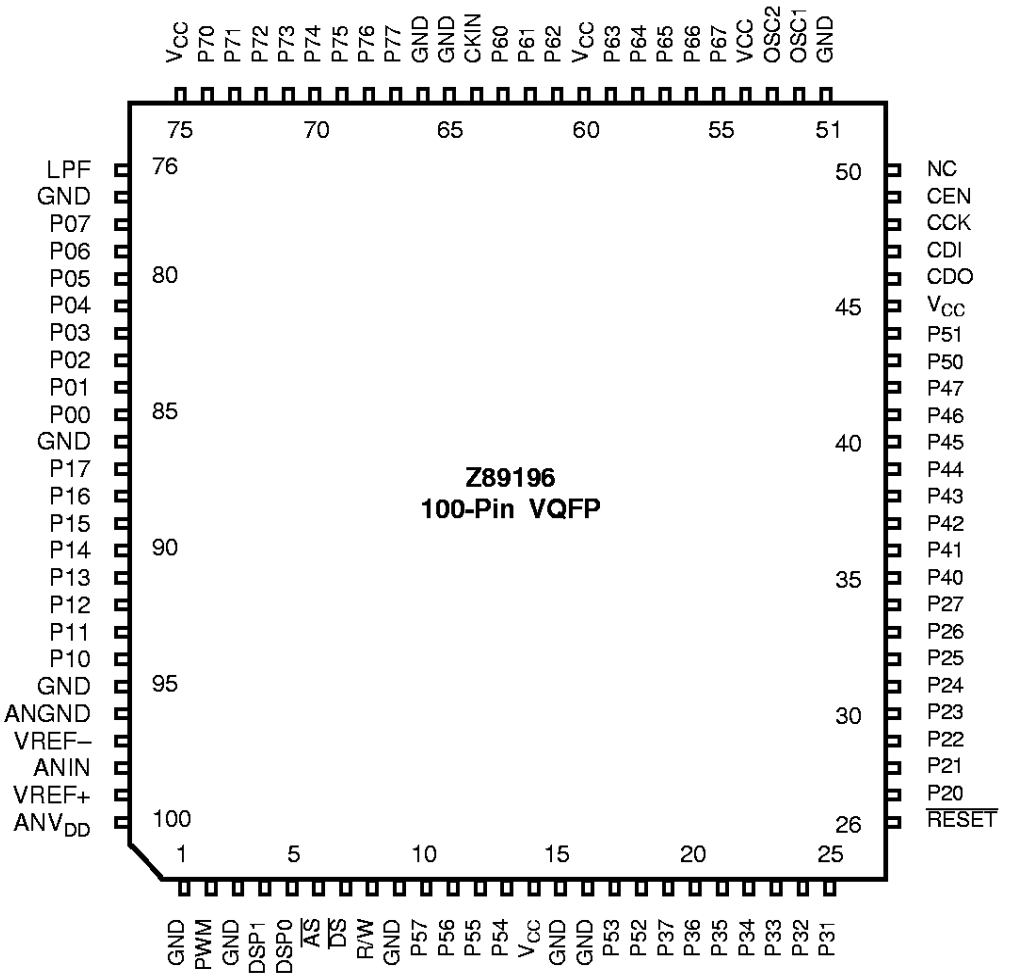

Figure 5. Z89196 100-Pin VQFP Pin Configuration

Table 4. Z89196 100-Pin VQFP Pin Identification

Pin Number	I/O Port Symbol	Direction	Function
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3, 14, 45, 54, 60, 75	V_{CC}		Digital V_{CC} = +5V
99	VREF+	Input/Output	Analog Voltage Ref+
100	ANV_{DD}		Analog V_{DD}
2	PWM	Output	PWM Output
4, 5	DSP1–0	Output	DSP User Output 1, 0
6	$\overline{AS}$	Output	Address Strobe
7	$\overline{DS}$	Output	Data Strobe
8	R/$\overline{W}$	Output	Read/Write
10–13	P57–P54	Input/Output	Port 5 Bit 7–4
17, 18	P53–P52	Input/Output	Port 5 Bit 3–2
19–22	P37–P34	Output	Port 3 Bit 7–4
23–25	P33–P31	Input	Port 3 Bit 3–1
26	$\overline{RESET}$	Input/Output	Reset
27–34	P20–P27	Input/Output	Port 2, Bit 0–7
35–42	P40–P47	Input/Output	Port 4, Bit 0–7
43, 44	P50–P51	Input/Output	Port 5, Bit 0–1
46	CDO	Output	Codec Interface Output
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49	CEN	Output	Codec Enable
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55–59	P67–P63	Input/Output	Port 6, Bit 7–3
61–63	P62–P60	Input/Output	Port 6, Bit 2–0
64	CKIN	Input	Input Clock
67–74	P77–P70	Input/Output	Port 7, Bit 7–0
76	LPF	Input	PLL Low Pass Filter
78–84	P07–P00	Input/Output	Port 0, Bit 7–0
86–94	P17–P10	Input/Output	Port 1, Bit 7–0
96	ANGND		Analog GND
97	VREF–	Input	Analog Voltage Ref–
98	ANIN	Input	Analog Input

ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
*Voltage on all pins with respect to GND.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

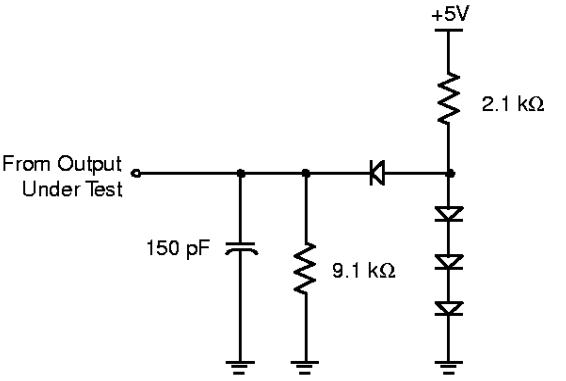


Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note 1	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	5.0V		65	40	mA	
I_{CC1}	HALT Mode Current	5.0V		20	6	mA	
I_{CC2}	STOP Mode Current	5.0V		20	6	uA	
V_{MAX}	Max Input Voltage	5.0V		7			
V_{CH}	Clock Input High Voltage	5.0V	0.9 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	5.0V	GND –0.3	0.1 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V	
V_{IL}	Input Low Voltage	5.0V	GND –0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	5.0V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA
V_{OL1}	Output Low Voltage	5.0V		0.4	0.1	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	5.0V		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{RH}	Reset Input High Voltage	5.0V	.8 V_{CC}	V_{CC}	2.1	V	
V_{RI}	Reset Input Low Voltage	5.0V	GND –0.3		0.2 V_{CC}	1.7	
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		25	10	mV	
I_{IL}	Input Leakage	5.0V	–10	10	10	µA	
I_{OL}	Output Leakage	5.0V	–10	10	10	µA	
I_{IR}	Reset Input Current	5.0V		–55	–30	µA	

Note:
1. 5.0V ±0.5V

DC ELECTRICAL CHARACTERISTICS (Continued)

Z89195 A/D Converter

			T_A = 0° C to +70°C						
Sym	**Parameter**	**V_{DD}**	**Min**	**Max**	**Units**	**Conditions**			
I_{IL}	Input Leakage Analog Input	5.5V		1.00	uA	ANV_{DD}	=	5.50	V
						V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						V_{REFL}	=	0.00	V
I_{IH}	Input Leakage Analog Input	5.5V		2.00	µA	ANV_{DD}	=	5.50	V
						V_{IN}	=	5.50	V
						V_{REFH}	=	5.50	V
						V_{REFL}	=	0.00	V
I_{VREFH}	Input Current	5.5V		1.00	mA	V_{IN}	=	5.50	V
						V_{REFL}	=	0.00	V
						ANV_{DD}	=	5.50	V
I_{VREFL}	Input Current	5.5V		2	µA	V_{IN}	=	5.50	V
						V_{REFL}	=	5.50	V
						ANV_{DD}	=	5.50	V
I_{VEFL}	Input Current	5.5V		–2.00	mA	V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						ANV_{DD}	=	0.00	V
I_{VREFL}	Input Current	5.5V		2	µA	V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						ANV_{DD}	=	5.50	V

21 Other Non-Regular I/O

			T_A = 0° C to +70°C			
Sym	**Parameter**	**V_{DD}**	**Min**	**Max**	**Units**	**Conditions**
I_{IRH}	Input Current ROMless Pin	5.5V		6.00	µA	V_{IN} = 5.50 V
I_{IR1}	Input Current ROMless Pin	5.5V		6.00	µA	V_{IN} = 0.00 V
I_{IR}	Input Current ROMless Pin During Reset Active	5.5V		1.00	mA	V_{IN} = 5.50 V
I_{IHX2}	Input Current XTAL2 pin in STOP Mode	5.5V		1.00	µA	V_{IN} = 0.00 V
I_{ILX2}	Input Current XTAL2 Pin in STOP Mode	5.5V		1.00	µA	V_{IN} = 5.50 V
I_{IHX1}	Input current XTAL1 Pin	5.5V		30	µA	V_{IN} = 0.00 V
I_{ILX1}	Input Current XTAL1 Pin	5.5V		30	µA	V_{IN} = 5.50 V
V_{OLXR}	Output Low Voltage XTAL2 Reset Inactive	5.5V		1.20	V	I_{OL} = 4.00 mA
V_{OLX}	Output Low Voltage XTAL2 Reset Inactive	5.5V		0.60	V	I_{OL} =1.00 mA
V_{OHXR}	Output High Voltage XTAL2 Reset Inactive	5.5V	4.00		V	I_{OH} = 4.00 mA
I_{VOHX}	Output High Voltage XTAL2 Reset Inactive	5.5V	4.00		V	I_{OH} =1.00 mA
I_{IH}	Input Current P31, P32, P33	5.5V		1.00	µA	V_{IN} = 5.50 V
I_{IL}	Input Current P31, P32, P33	5.5V		1.00	µA	V_{IN} = 0.00 V

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

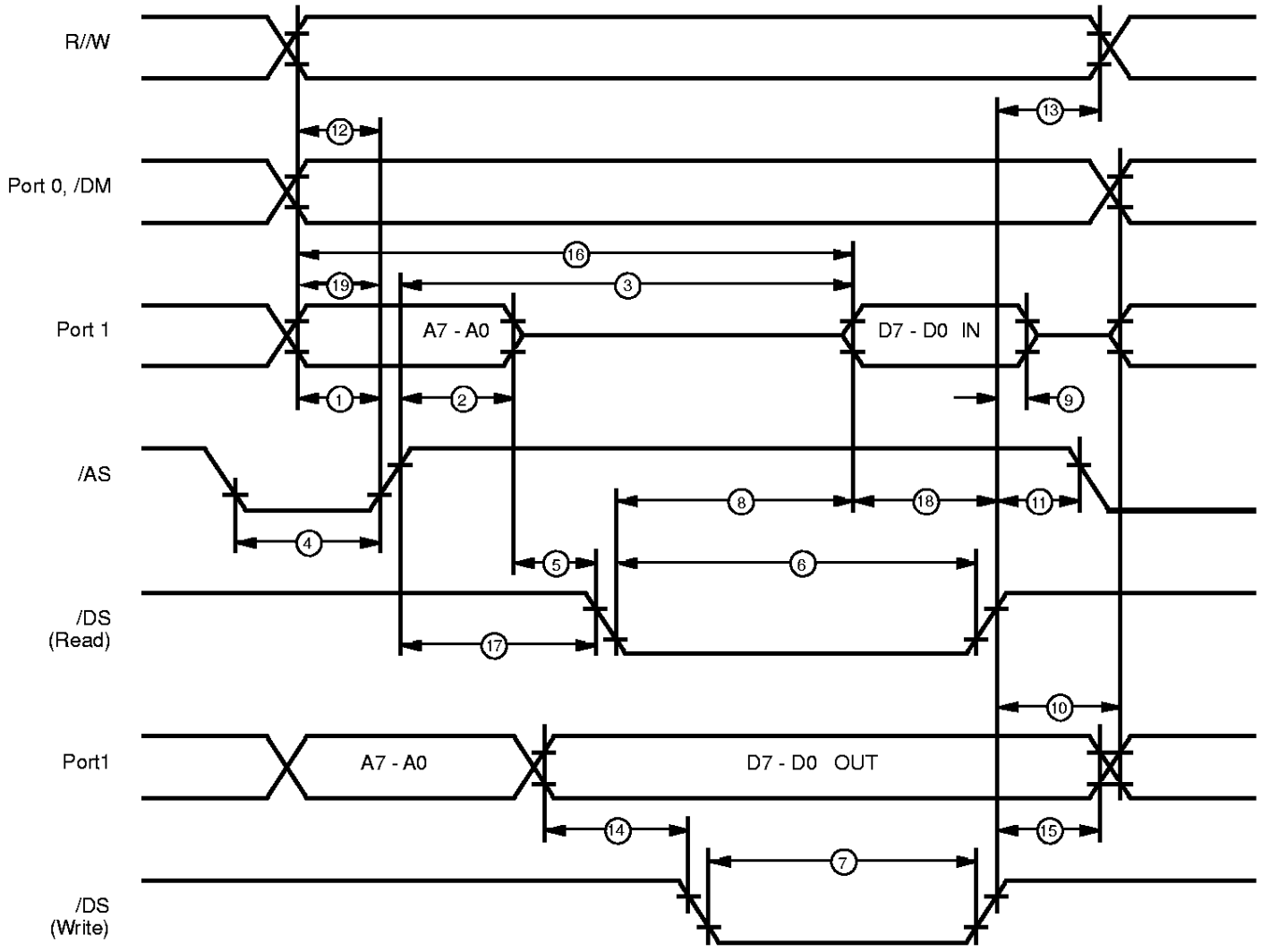


Figure 7. External I/O or Memory Read/Write Timing

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{CC} Note 4	T_A= 0°C to +70°C Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	5.0V	15		ns	2,3
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	5.0V	25		ns	2,3
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	5.0V		100	ns	1,2,3
4	TwAS	$\overline{AS}$ Low Width	5.0V	25		ns	2,3
5	TdAZ(DS)	Address Float to $\overline{DS}$ Fall	5.0V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	5.0V	75		ns	1,2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	5.0V	75		ns	1,2,3
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	5.0V	50	45	ns	1,2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	5.0V	0		ns	2,3
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	5.0V	20		ns	2,3
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	5.0V	20		ns	2,3
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	5.0V	15		ns	2,3
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	5.0V	25		ns	2,3
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	5.0V	20		ns	2,3
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	5.0V	15		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		90	ns	1,2,3
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	5.0V	24		ns	2,3
18	TdDI(DS)	Data Input Setup to $\overline{DS}$ Rise	5.0V	25		ns	1,2,3
19	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	5.0V	10		ns	2,3

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.
4. 5.0 V ±0.5 V.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS (Continued)

Additional Timing Diagram

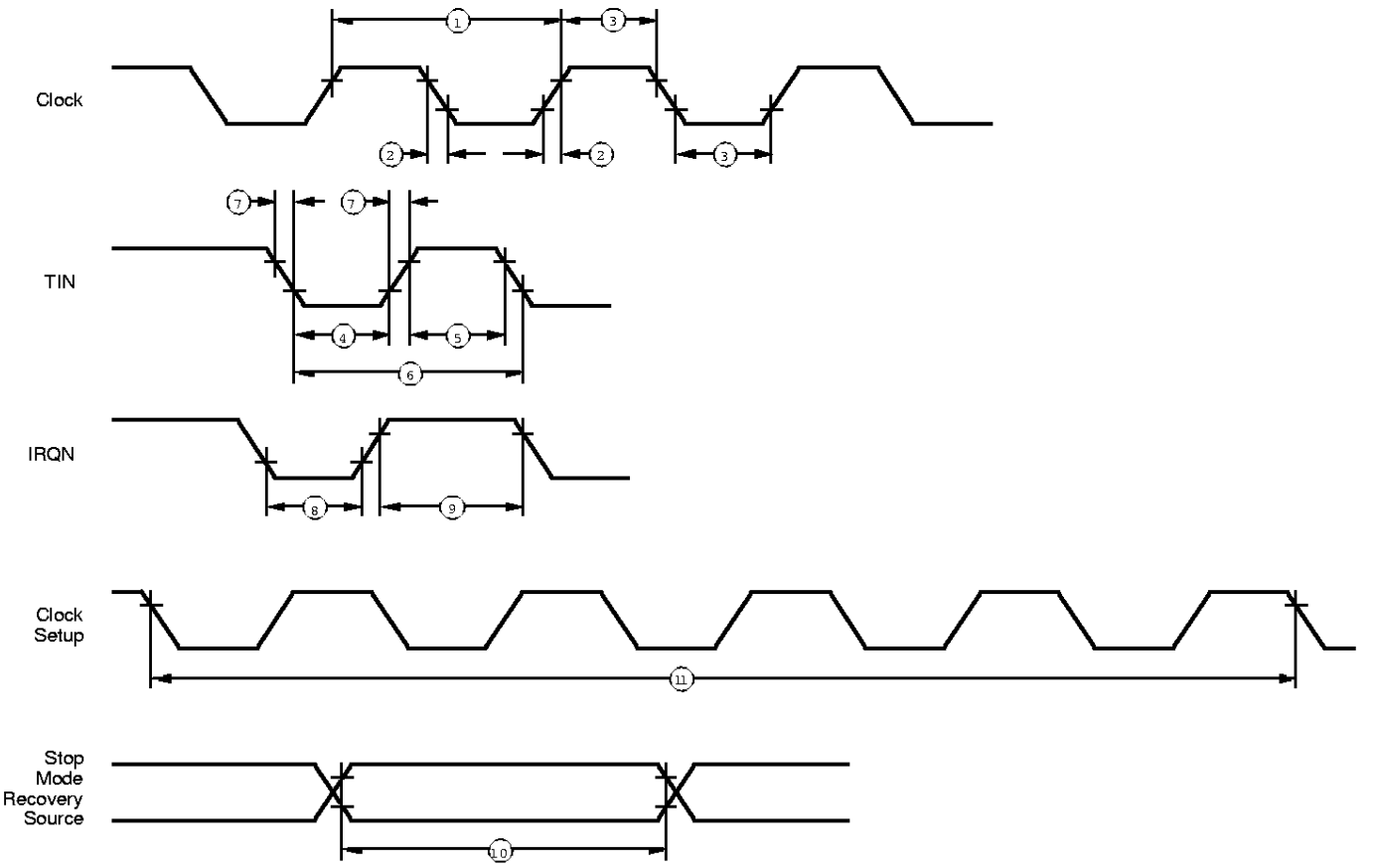


Figure 8. Additional Timing

Additional Timing Table

No	Sym	Parameter	V_{CC} Note 5	T_A= 0°C to +70°C Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	48.8		ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		6	ns	1
3	TwC	Input Clock Width	5.0V	17		ns	1
4	TwTinL	Timer Input Low Width	5.0V	70		ns	
5	TwTinH	Timer Input High Width	5.0V	3TpC			1
6	TpTin	Timer Input Period	5.0V	8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100	ns	1
8a	TwIL	Int. Request Low Time	5.0V	70		ns	1,2
8b	TwIL	Int. Request Low Time	5.0V	3TpC			1
9	TwIH	Int. Request Input High Time	5.0V	3TpC			1
10	Twsm	Stop-Mode Recovery Width Spec	5.0V	12		ns	1
11	Tost	Oscillator Start-up Time	5.0V	5TpC			3
12	Twdt	Watch-Dog Timer	5.0V	5		ms	D1 = 0, D0 = 1 [4]
			5.0V	15		ms	D1 = 0, D0 = 1 [4]
			5.0V	25		ms	D1 = 0, D0 = 1 [4]
			5.0V	100		ms	D1 = 0, D0 = 1 [4]

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31–P33).
3. SMR-D5 = 0
4. Reg. WDT
5. 5.0 V ±0.5 V

AC CHARACTERISTICS (Continued)

Handshake Timing Diagrams

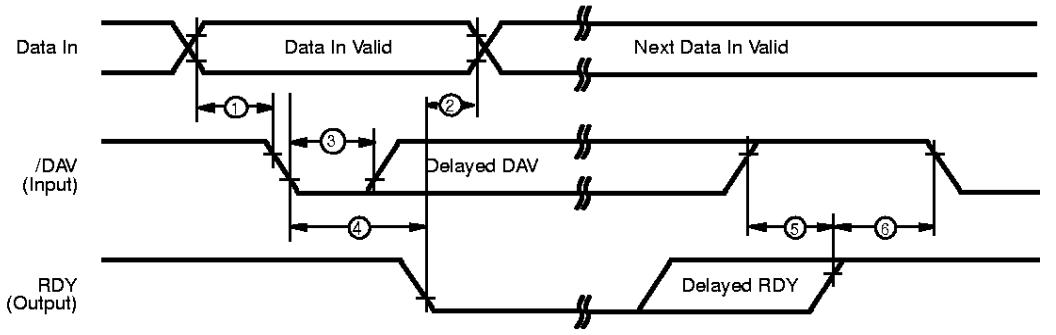


Figure 9. Input Handshake Timing

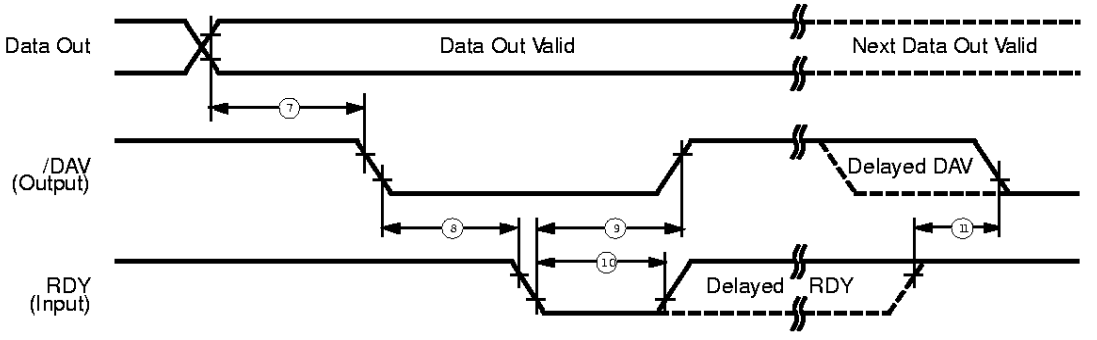


Figure 10. Output Handshake Timing

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note	T_A= 0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0V	0		ns	IN
2	ThDI(RDY)	RDY to Data Hold Time	5.0V	0		ns	IN
3	TwDAV	Data Available Width	5.0V	40		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		70	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		40	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0V	TpC		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		70	ns	OUT
10	TwRDY	RDY Width	5.0V	40		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V		40	ns	OUT

Note: 5.0V ±0.5V

PIN FUNCTIONS

$\overline{\text{RESET}}$ (input, active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) reset, Stop-Mode Recovery, or external reset. During POR and WDT Reset, the internally generated reset signal is driving the reset pin Low for the POR time. Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. A $\overline{\text{RESET}}$ will reset both the Z8 and the DSP.

For the Z8: After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the $\overline{\text{RESET}}$ is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000CH (hexadecimal), 5–10 TpC cycles after $\overline{\text{RESET}}$ is released. The Z8 does not reset WDT, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

For the DSP: After POR, the DSP is in RUN Mode. The Z8 controls the DSP commands to HALT, RUN or RESET. When the DSP is in HALT Mode, it cannot be woke up with WDT or SMR.

RMLS ROMless (input, active High). This pin, when connected to V_{DD}, disables the internal Z8 ROM. (Note that, when pulled Low to GND, the device functions normally as the ROM version.) The DSP cannot be configured as ROMless. This pin is only available on the Z89195.

R/$\overline{\text{W}}$ Read/Write (output, write Low). The R/$\overline{\text{W}}$ signal defines the signal flow when the Z8 is reading or writing to an external program or data memory. The Z8 is reading when this pin is High and writing when this pin is Low.

$\overline{\text{AS}}$ Address Strobe (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{\text{AS}}$. Under program control, $\overline{\text{AS}}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

$\overline{\text{DS}}$ Data Strobe (output, active Low). Data Strobe is activated once for each external memory transfer. For read operations, data must be available prior to the trailing edge of $\overline{\text{DS}}$. For write operations, the falling edge of $\overline{\text{DS}}$ indicates that output data is valid.

LPF (input). PLL low pass filter.

CKIN (input). Direct clock input for PLL bypass option.

DSP0 (output). DSP0 is a general-purpose output pin connected to bit 6 of the Analog Control Register (DSP EXT6). This bit has no special significance and can be used to output data by writing to bit 6 of the ACR.

DSP1 (output). DSP1 is a general-purpose output pin connected to bit 7 of the Analog Control Register (DSP EXT6). This bit has no special significance and can be used to output data by writing to bit 7 of the ACR.

PWM Pulse Width Modulator (Output). The PWM is a 10-bit resolution D/A converter. This output is a digital signal with CMOS output levels.

AN_{IN} (input). Analog input for the A/D converter.

ANV_{DD}. Analog power supply for the A/D converter.

ANGND. Analog ground for the A/D converter.

VREF+ (input). Reference voltage (High) for the A/D converter.

VREF– (input). Reference voltage (Low) for the A/D converter.

V_{DD}. Digital power supply for the Z89195.

GND. Digital ground for the Z89195.

OSC1 Oscillator 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network to the on-chip oscillator input.

OSC2 Oscillator 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network to the on-chip oscillator output.

CDI (input). Codec Interface data input.

CDO (output). Codec Interface data output.

CCK (output). Codec Interface shift clock.

CEN (output). Codec Interface channel enable.

PIN FUNCTIONS (Continued)

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{DAV0}$ and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 can be set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ (Figure 11).

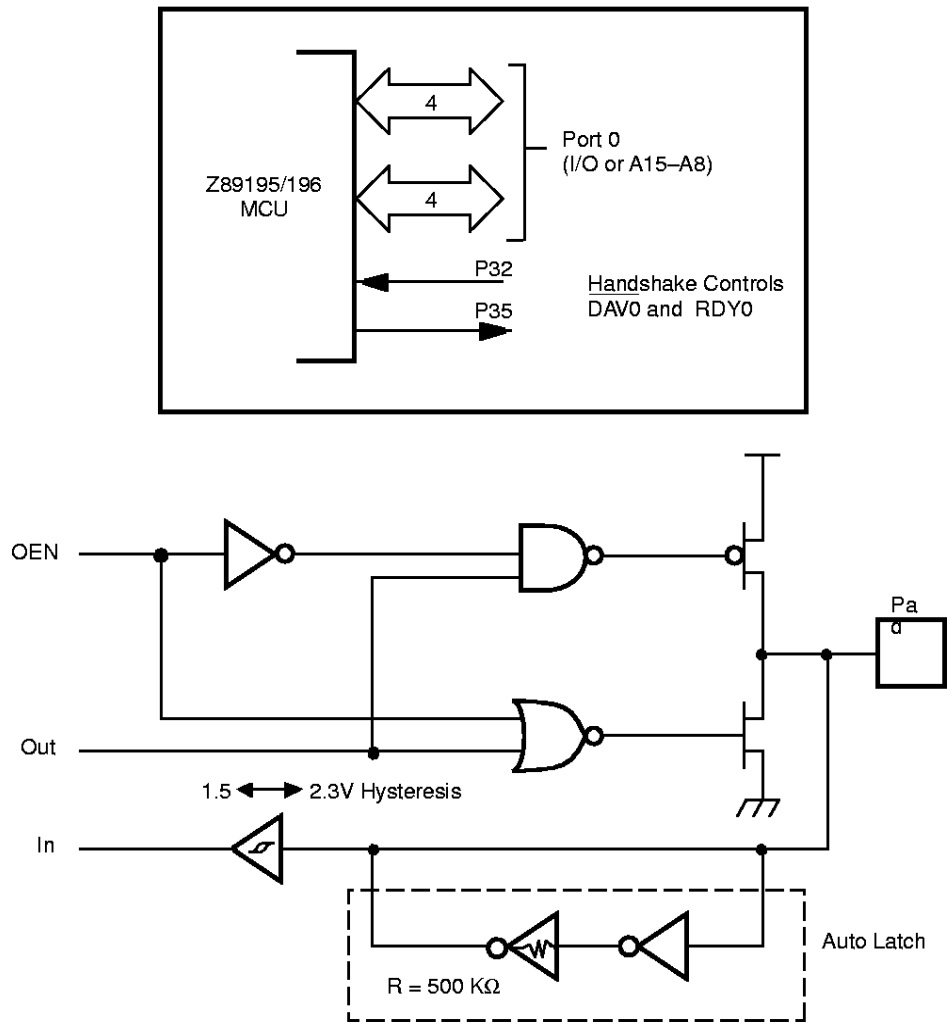


Figure 11. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port (Figure 12). It has multiplexed Address (A7–A0) and Data (D7–D0) ports. These eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull.

Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{DAV1}$ (Ready and Data Available). Memory locations greater than 32768 (Z89195) (in ROM mode) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z89195/196 to share common resources in multiprocessor and DMA applications.

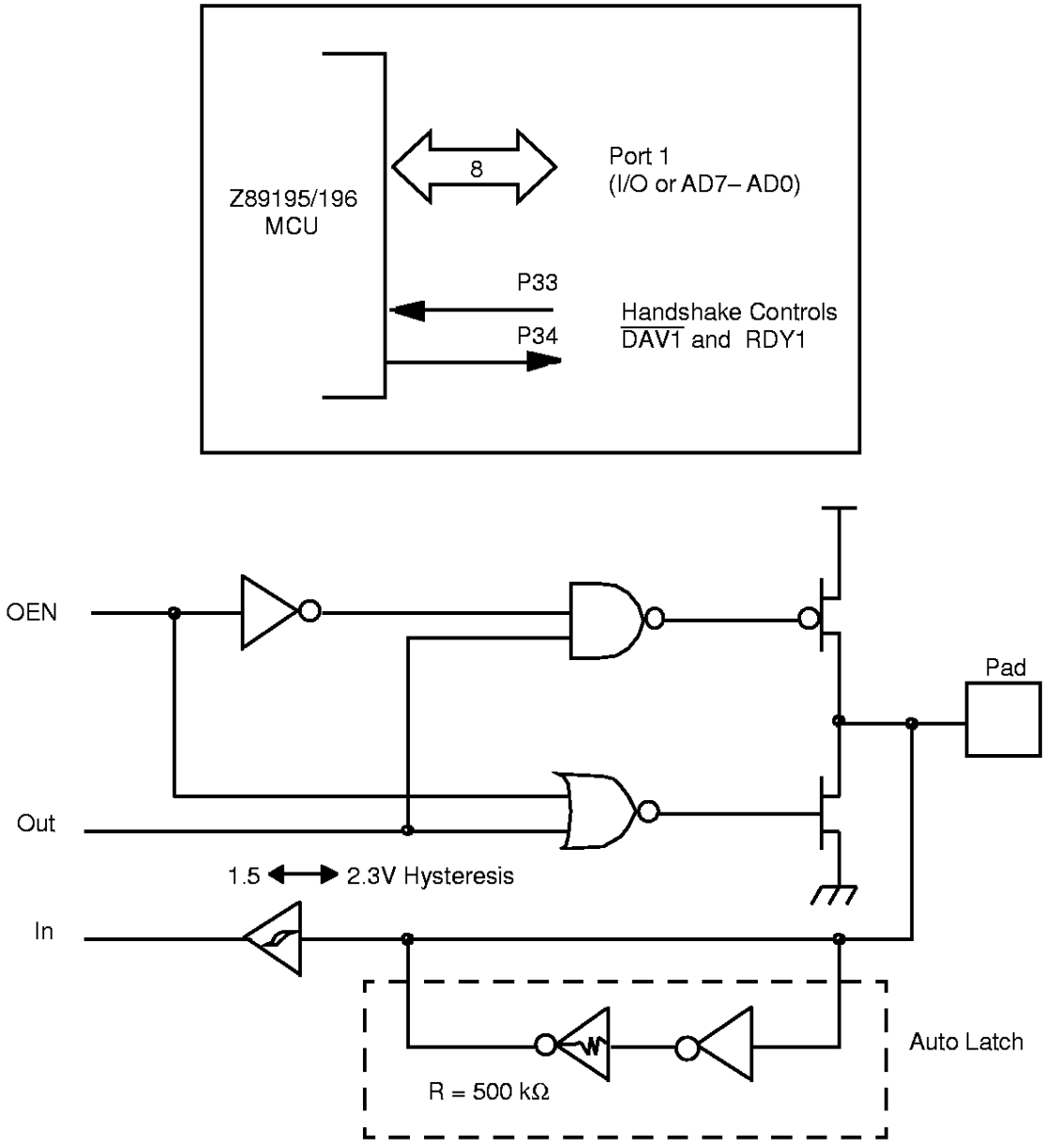


Figure 12. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control independently as inputs or outputs. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake controls lines $\overline{DAV2}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 13).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

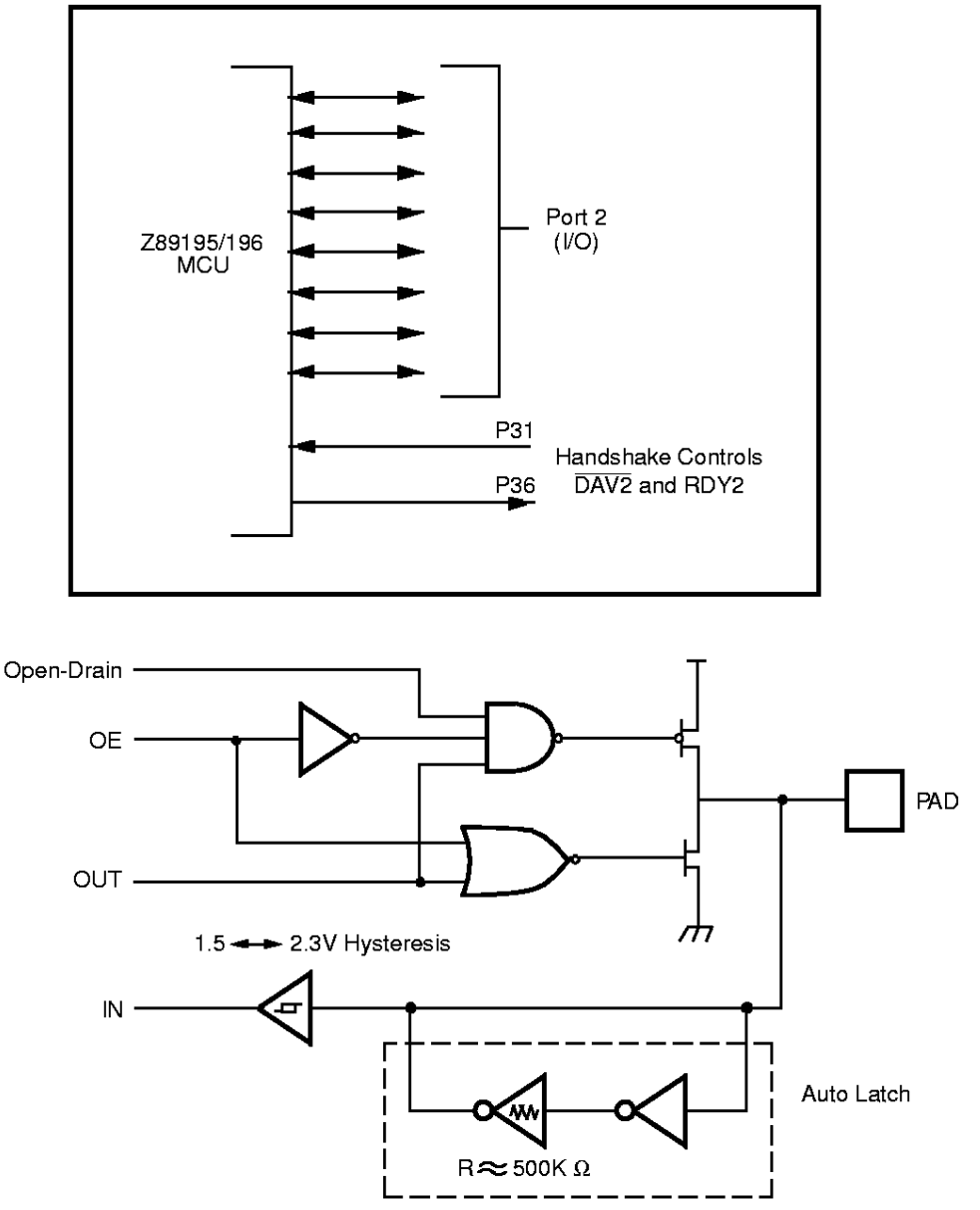


Figure 13. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37–P31). Port 3 is a 7-bit, CMOS-compatible port with three fixed inputs (P33–P31) and four fixed outputs (P37–P34). It is configured under software control for input/output, counter/timers, interrupt, and port handshakes. Pins P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming bit 1 of the Port 3 Mode Register. Port 3, pin 3 is a falling edge interrupt input. P31 and P32 are programmable as rising, falling or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to counter/timers is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ3–IRQ1); timer input and output signals (T_{IN} and T_{OUT}) (Figure 14).

Comparator Inputs. Port 3, pins P31 and P32 all have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source.

Table 5. Port 3 Pin Assignments

Pin	I/O	T0,1	AN IN	Int.	P0 HS	P1 HS	P2 HS	EXT
P31	IN	TIN	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT					R/D		DM
P35	OUT				R/D			
P36	OUT	TOUT					R/D	
P37	OUT							

Notes:
HS = Handshake Signals
D = DAV
R = RDY
TIN is for Timer1 only
TOUT can be from either Timer0 or 1

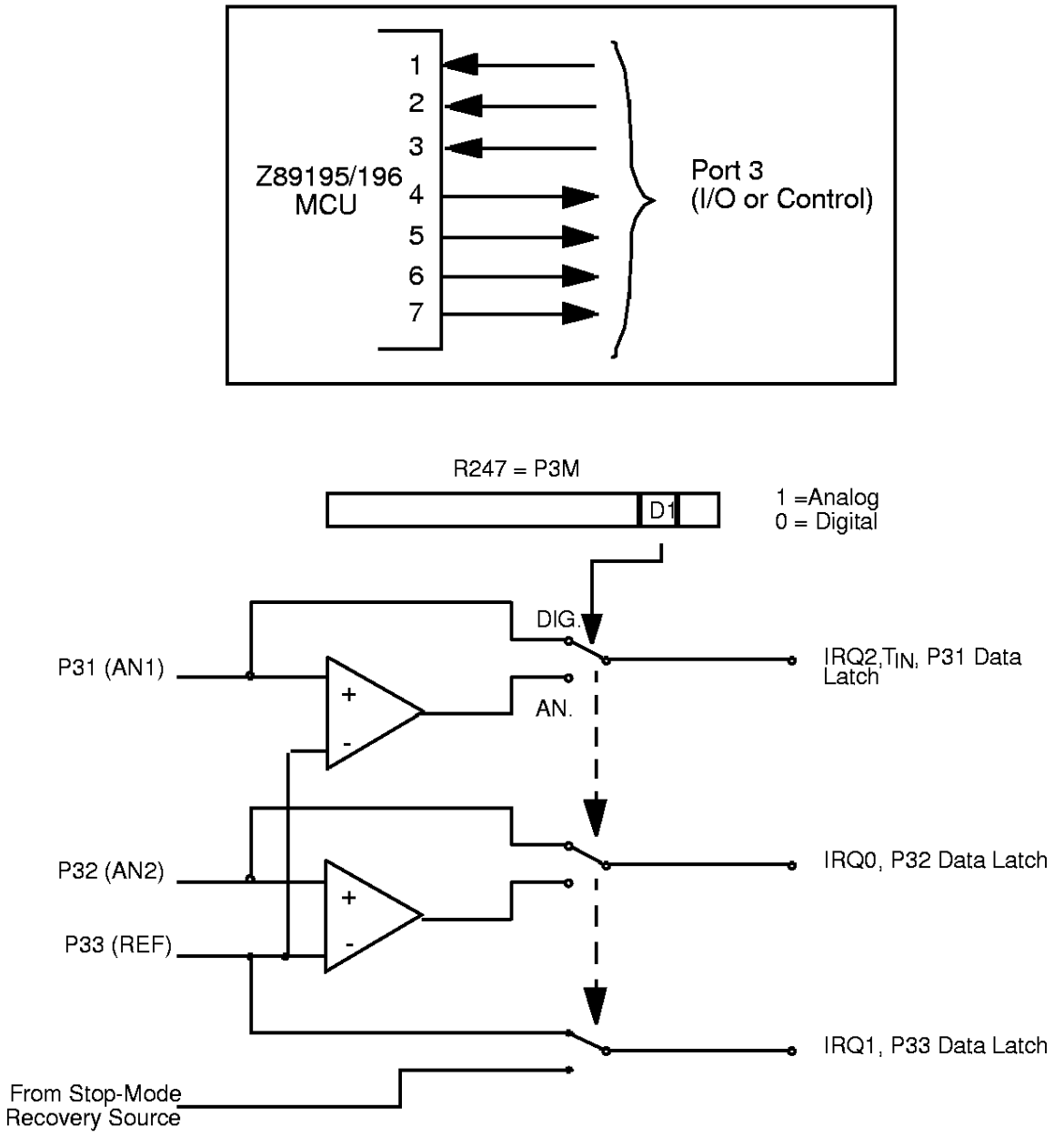


Figure 14. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port 4 (P47–P40). Port 4 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 15). These eight I/O lines are configured under software control independently as inputs or outputs. Port 4 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 4 is a bit programmable general-purpose I/O port. The control registers for Port 4 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 4 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

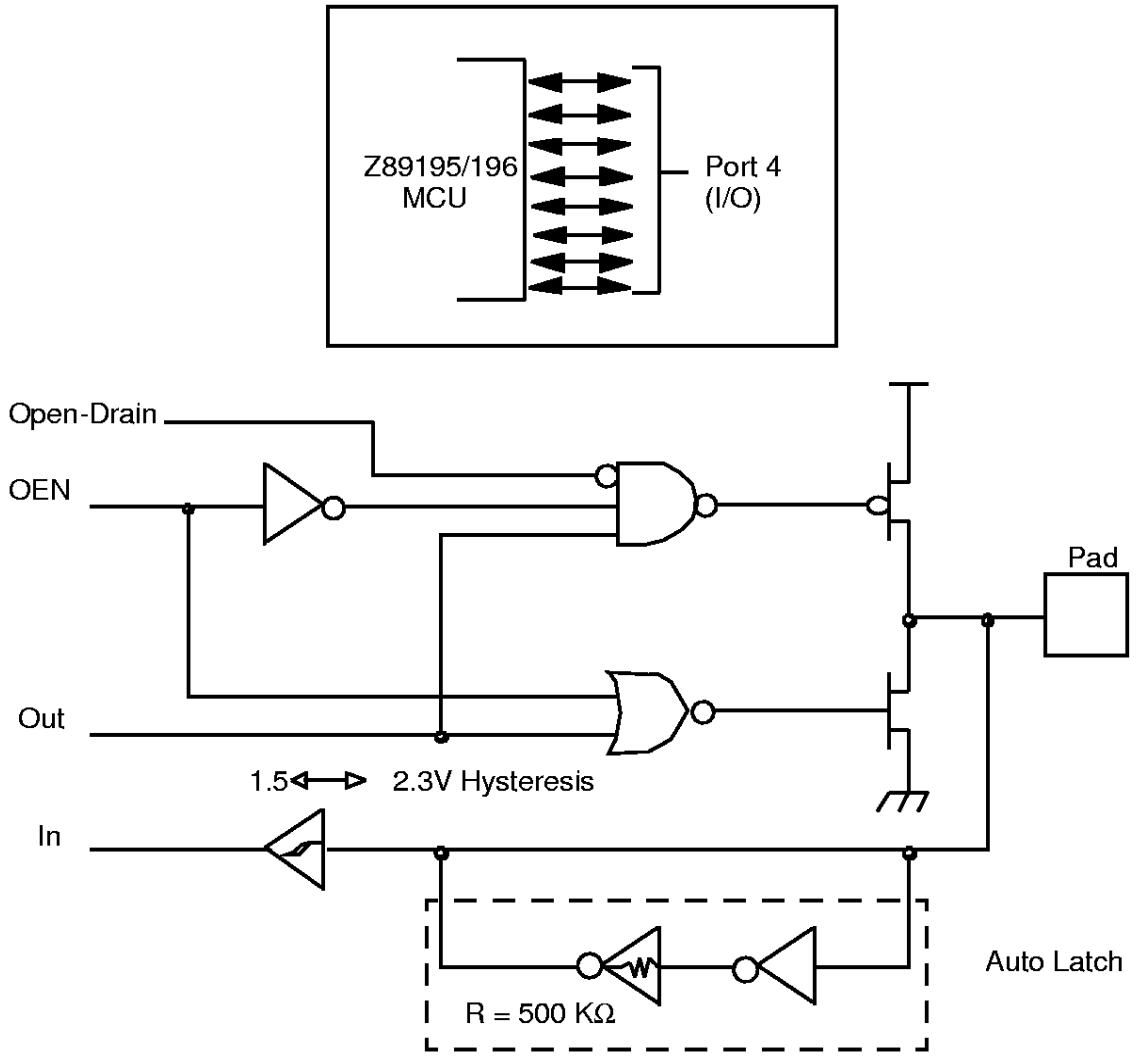


Figure 15. Port 4 Configuration

Port 5 (P57–P50). When the Z89195's ARAM Controller function is enabled, a portion of Port 5 (P57–P52) is used as external ARAM control signals. Refer to the section on ARAM Controller for details. Otherwise, Port 5 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 16). These I/O lines are configured under software control independently as inputs or outputs. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 5 is a bit programmable general-purpose I/O port. The control registers for Port 5 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 5 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

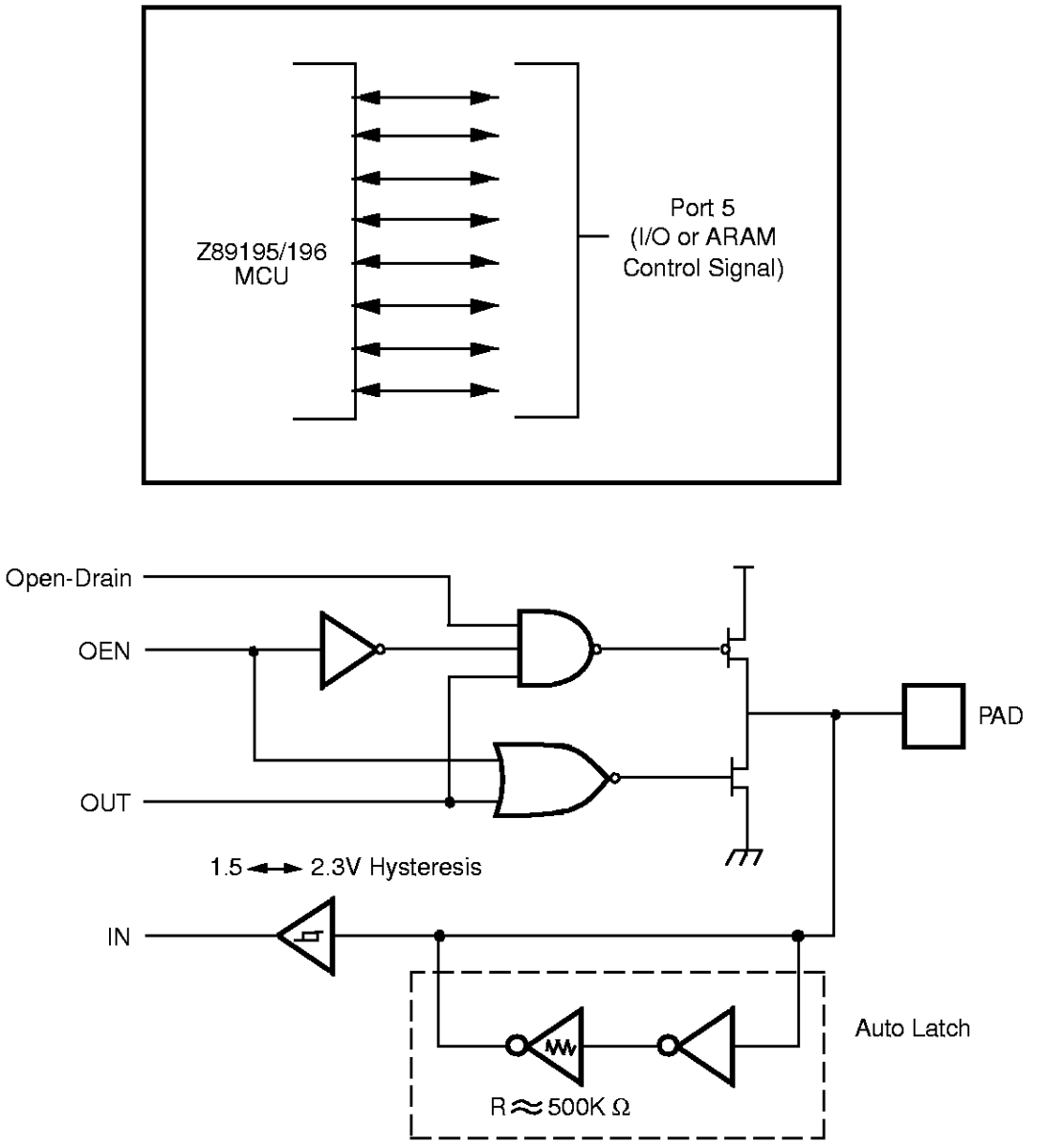


Figure 16. Port 5 Configuration

PIN FUNCTIONS (Continued)

Port 6 (P67–P60). When the Z89195's ARAM Controller function is enabled, Port 6 is used as external ARAM Address/Data signals. Refer to the section on ARAM Controller for details. Otherwise, Port 6 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 17). These I/O lines are configured under software control independently as inputs or outputs. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 6 is a bit programmable general-purpose I/O port. The control registers for Port 6 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 6 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

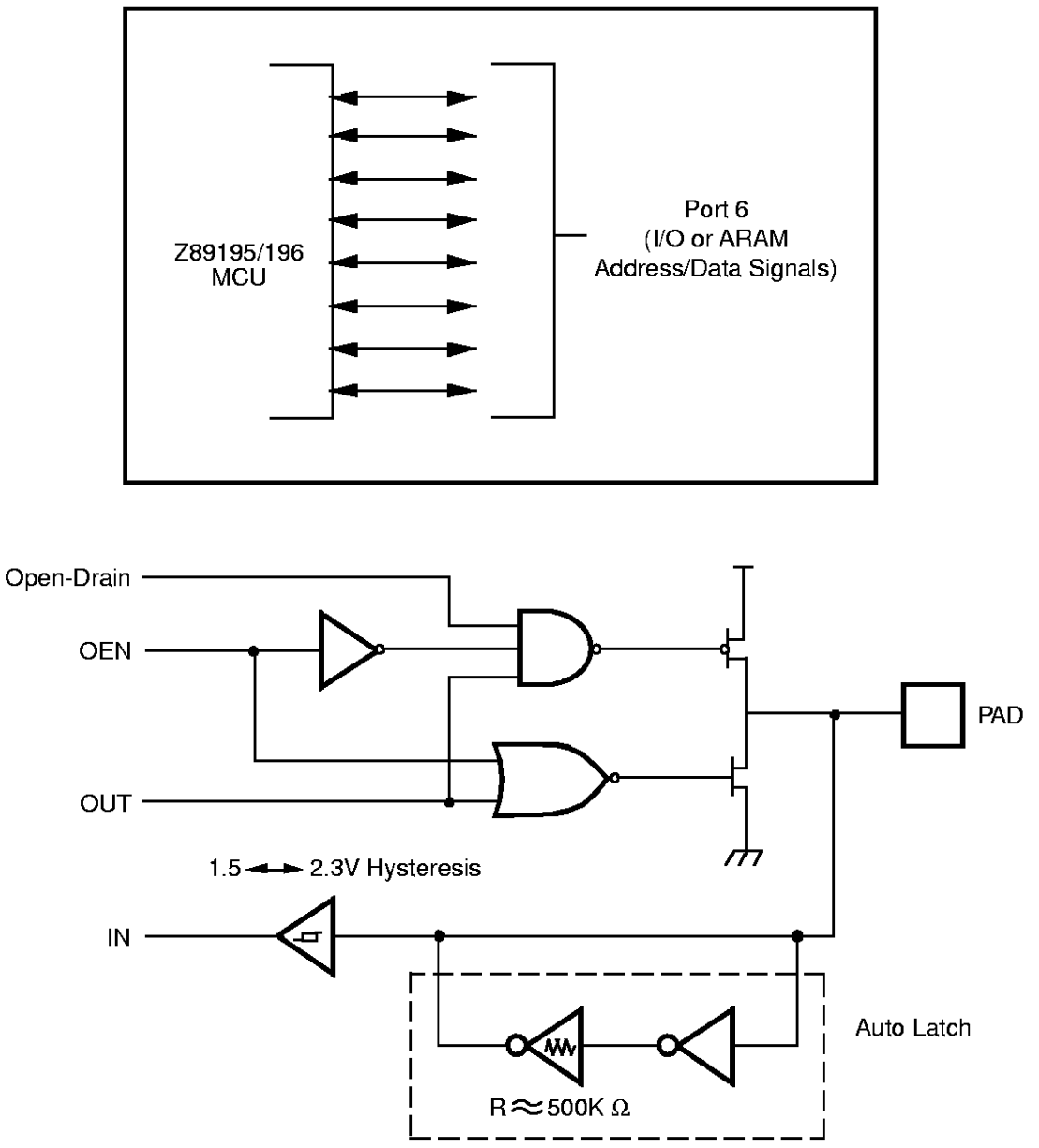


Figure 17. Port 6 Configuration

Port 7 (P77–P70). When the Z89195's ARAM Controller function is enabled, Port 7 is used as external ARAM Address/Data signals. Refer to the section on ARAM Controller for details. Otherwise, Port 7 is an 8-bit, bidirectional, CMOS-compatible I/O port (Figure 18). These I/O lines are configured under software control independently as inputs or outputs. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 7 is a bit programmable general-purpose I/O port. The control registers for Port 7 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 7 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

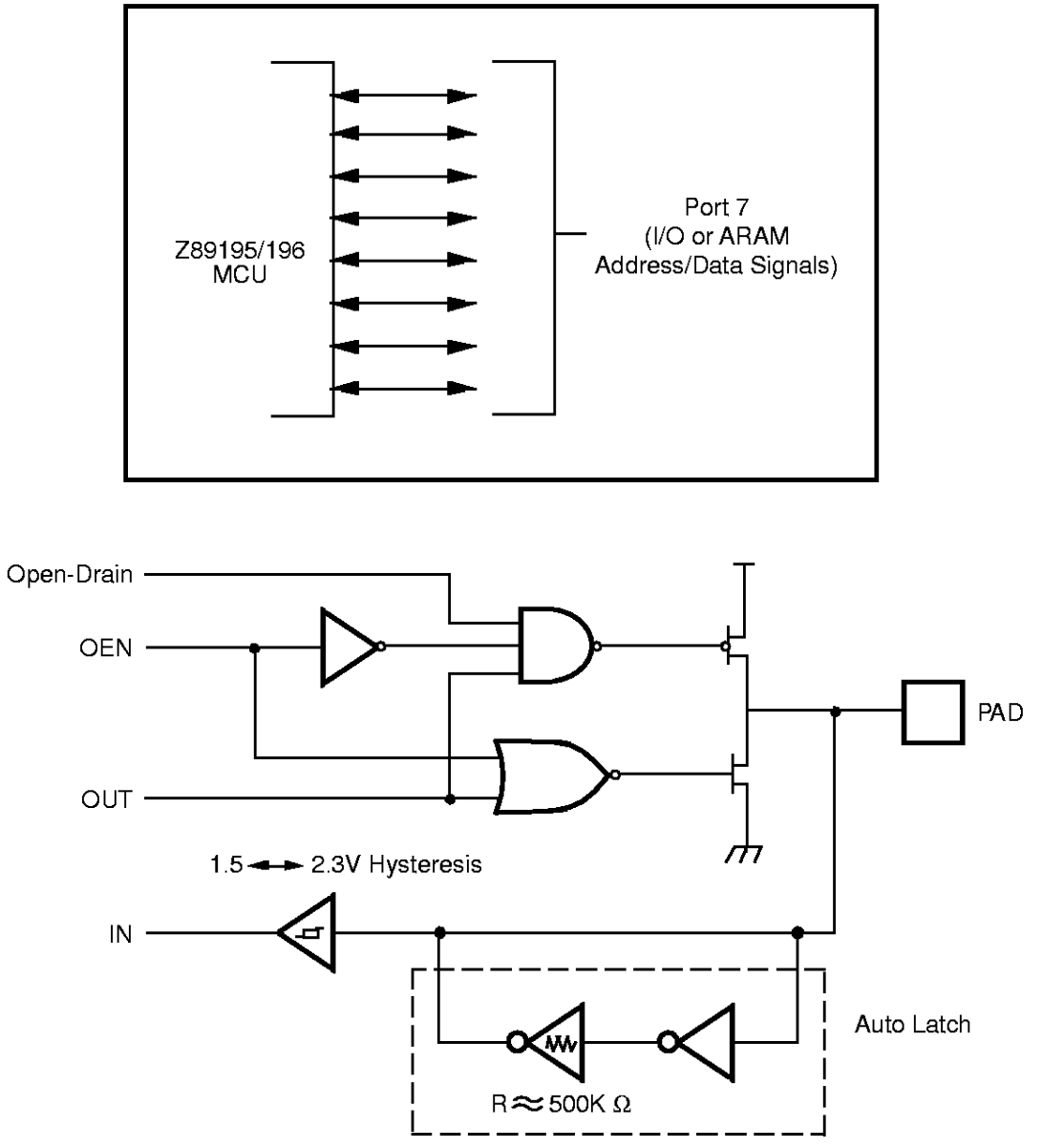


Figure 18. Port 7 Configuration

Z8 FUNCTIONAL DESCRIPTION

The Z8 core of the Z89195/196 incorporates special functions to enhance the Z8's application in a variety of voice-processing applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset

Program Memory. The Z8 addresses up to 32 KB of internal program memory and 32 KB external memory (Figure 21). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors which correspond to the five user interrupts and one DSP interrupt. Byte 12 to byte 32767 consist of on-chip mask-programmed ROM. At addresses 32768 and greater the Z8 executes external program memory. In ROMless mode, the Z8 will execute external program memory beginning at byte 12 and continuing through byte 65535.

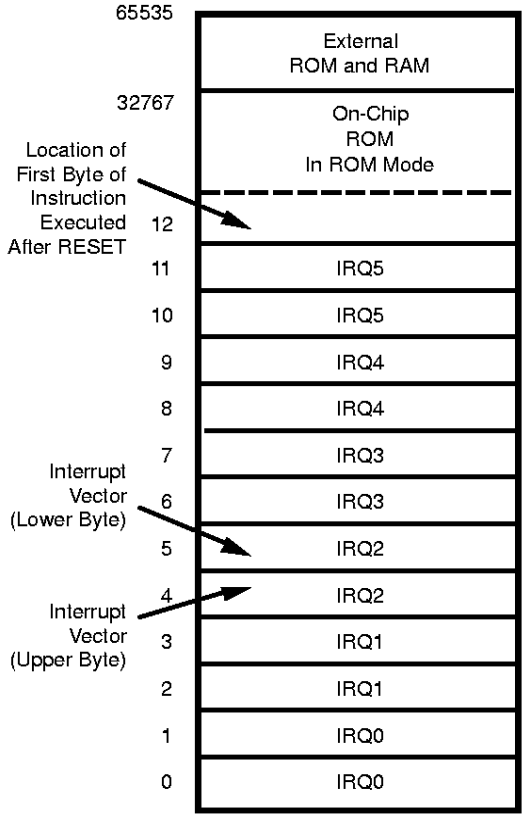


Figure 19. Program Memory

ROM Protect. The 32 KB of internal program memory for the Z8 is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents of Program Memory by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions. The ROM Protect option is mask-programmable, to be selected by the customer at the time the ROM code is submitted.

Data Memory ($\overline{DM}$). In ROM mode, the Z8 can address up to 32 KB of external data memory beginning at location 32768 (Figure 22). In ROMless mode, the Z8 can address the full 64 KB of external data memory beginning at location 12. External data memory can be included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on Port 34, is used to distinguish between data and program memory space (Table 5). The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

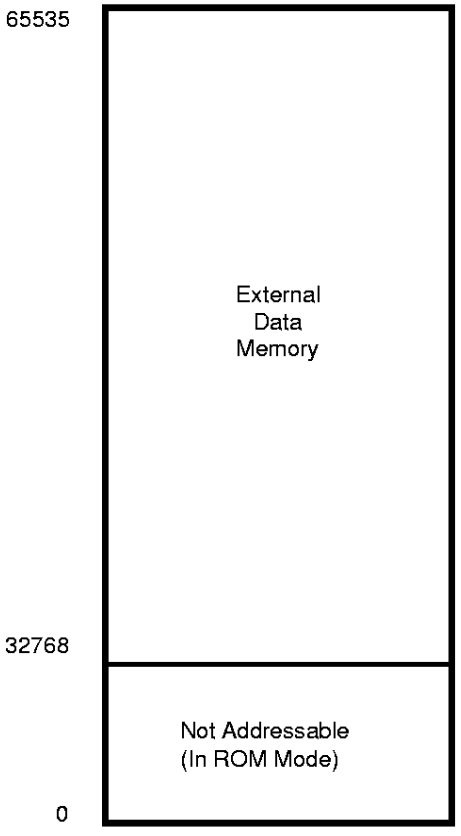


Figure 20. Data Memory Map

Register File. The standard Z8 register file consists of four I/O port registers, 236 general-purpose registers, and 15 control and status registers (R0–R3, R4–R239, and

R241–R255, respectively). The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 21). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group (Figure 24).

Note: Register Group E (Registers EF–E0) is only accessed through a working register and indirect addressing modes.

RAM Protect. The upper portion of the Z8's RAM address spaces 80H to EFH (excluding the control registers) is protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates the RAM Protect from the internal ROM code by loading a bit D6 in the IMR register to either a 0 (OFF) or a 1 (ON). A 1 in D6 indicates RAM Protect enabled.

Stack. The Z8's external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R255–R254) is used for the external stack which can reside only from 32768 to 65535 in ROM mode or 0 to 65535 in ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack residing within the 236 general-purpose registers (R239–R4). SPH can be used as a general-purpose register when using internal stack only.

Expanded Register File. The register file on the Z8 has been expanded to allow for additional system control registers and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space has been implemented as 16 banks of 16 register groups per bank (Figure 23). These register banks are known as the ERF (Expanded Register File). Bits 7–4 of register RP (Register Pointer) select the working register group. Bits 3–0 of register RP select the Expanded Register bank (Figure 23).

The SMR register, WDT Register, control and data registers for Ports 4, 5, 6 and 7, and the DSP control register are located in Bank F of the Expanded Register File. Bank B of the Expanded Register File consists of the Mailbox Interface through which the Z8 and the DSP communicate. The Phase-Locked Loop, Serial I/O and ARAM Controller registers are located in Bank A of the Extended Register File. The rest of the Expanded Register is not physically implemented and is open for future expansion.

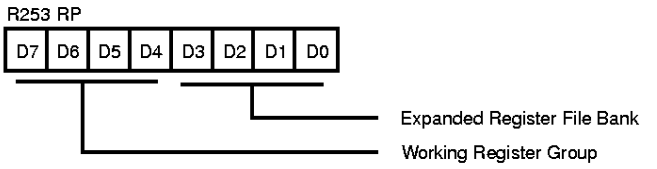


Figure 21. Register Pointer Register

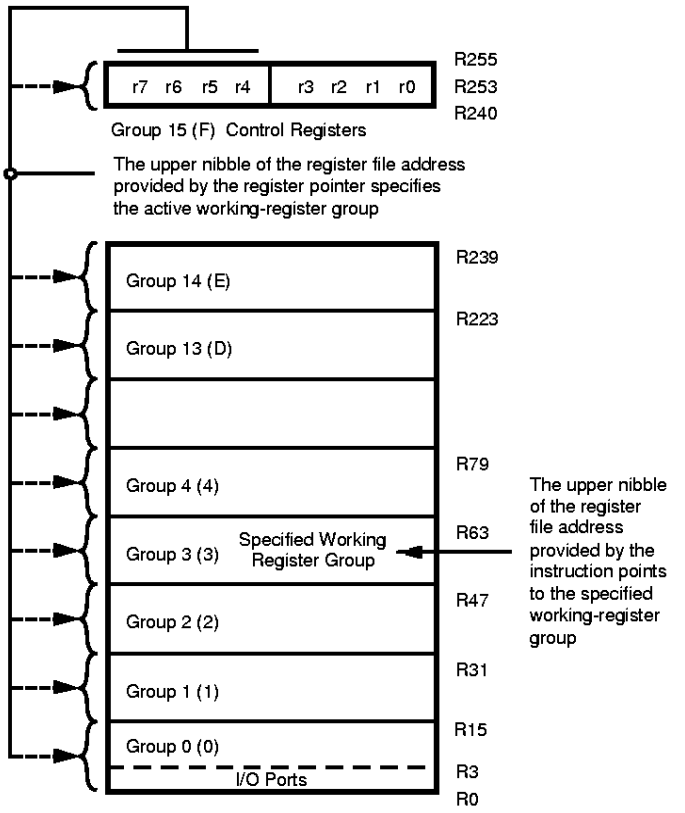


Figure 22. Register Pointer

Z8 FUNCTIONAL DESCRIPTION (Continued)

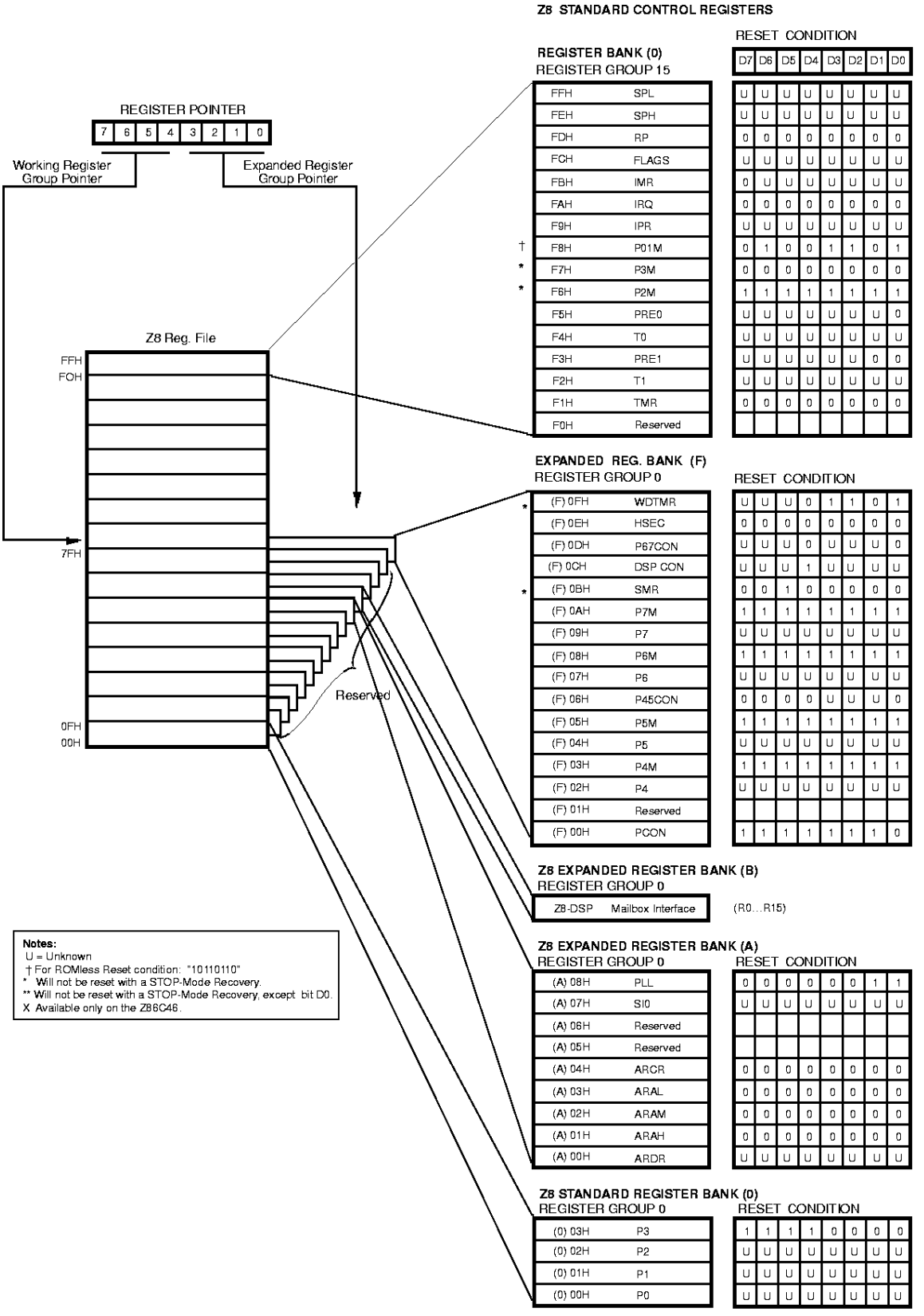


Figure 23. Expanded Register File Architecture

Phase-Locked Loop Clock Generator

An incorporated Phase-Locked Loop (PLL) circuit generates a high frequency System Clock from the 32.768 kHz crystal oscillator clock. The benefits of using a low frequency crystal for the Z89195 are low system cost, low power consumption and low EMI.

The Phase-Locked Loop (or Voltage-Controlled Oscillator, VCO) circuit can be programmed to output a System Clock frequency of either 20.48 MHz or 14.7456 MHz. Two bypass options can be invoked, either to the crystal oscillator clock, or to an external input clock CKIN.

In addition, the VCO can be programmed to stop and restart to provide low power consumption mode. At VCO stop, a user should select bypass to crystal or CKIN. At VCO restart, a software delay of 10msec must be observed before switching the System Clock back to the VCO source, in order to allow the VCO circuit to become stable.

The circuitry to switch the System Clock among these three clock sources is designed to avoid any clock glitches at frequency transitions.

The DSP core is clocked by the System Clock directly, whereas the Z8 has the option of being clocked by the System Clock divided by 2, by 4, or by 8.

Timers 0 and 1 are clocked at the same rate as the Z8, whereas Timers 2 and 3 are clocked at the same time as the DSP core.

The PLL operation is controlled by Register 08 in Bank A in Z8's Expanded Register space.

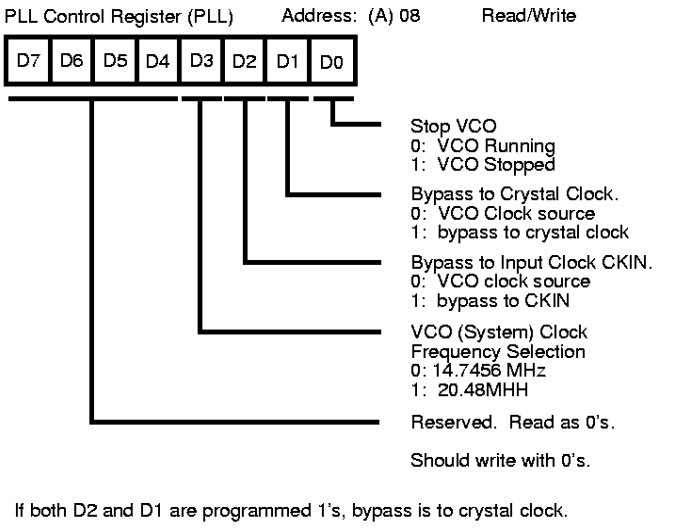


Figure 24. PLL Control Register

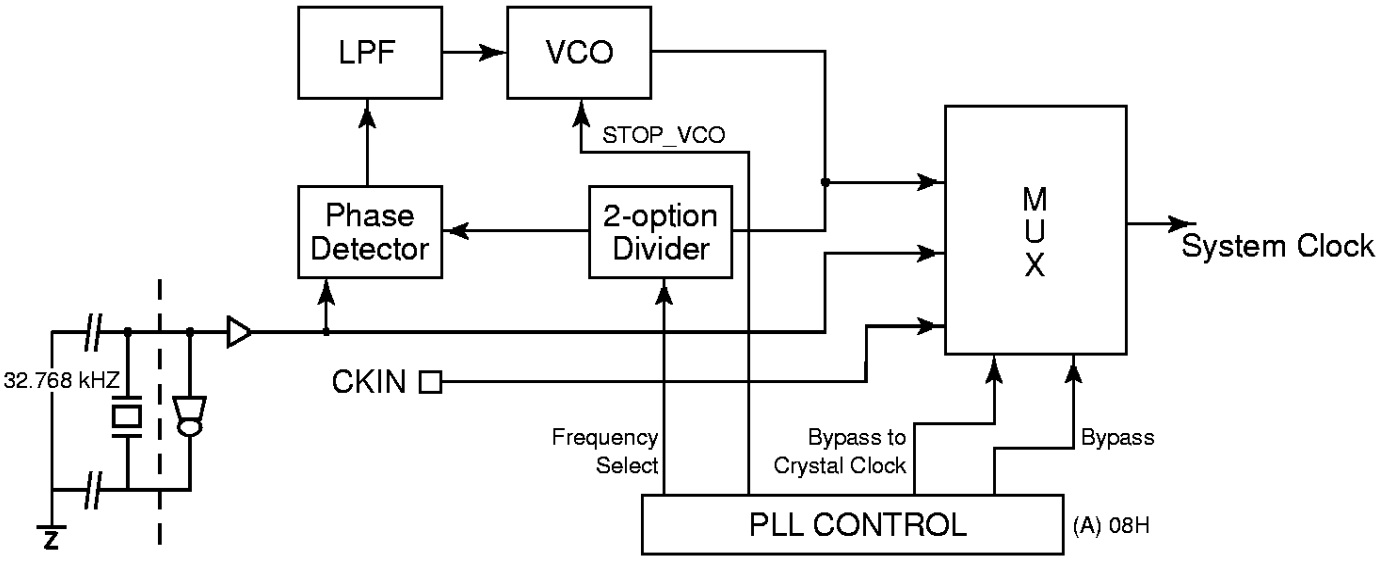


Figure 25. PLL Functional Block Diagram

Z8 FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 26). The six sources are divided as follows; three sources are claimed by Port 3 lines P33–P31, two by counter/timers, and one by the DSP (Table 6). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

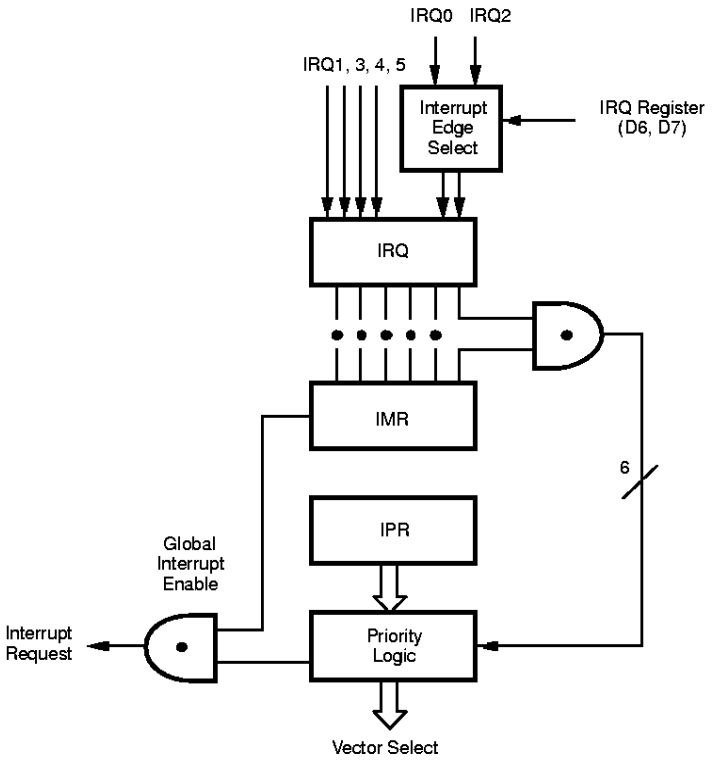


Figure 26. Interrupt Block Diagram

Table 6. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, P32, AN2, UART/SCXVR Tx	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ1	$\overline{DAV1}$, P33, UART/SCXVR Rx	2, 3	External (P33), Fall Edge Triggered
IRQ2	$\overline{DAV2}$, P31, TIN, AN1	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ3	IRQ3	6, 7	Internal (DSP activated), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, pushes the Program Counter and Status Flags to the stack, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register can be polled to determine which of the interrupt requests needs service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 7.

Table 7. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Counter/Timers. There are two 8-bit programmable counter/timers (T1,T0), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. However, the T0 prescaler is driven by the internal clock only (Figure 27).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (0 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 31. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Z8 FUNCTIONAL DESCRIPTION (Continued)

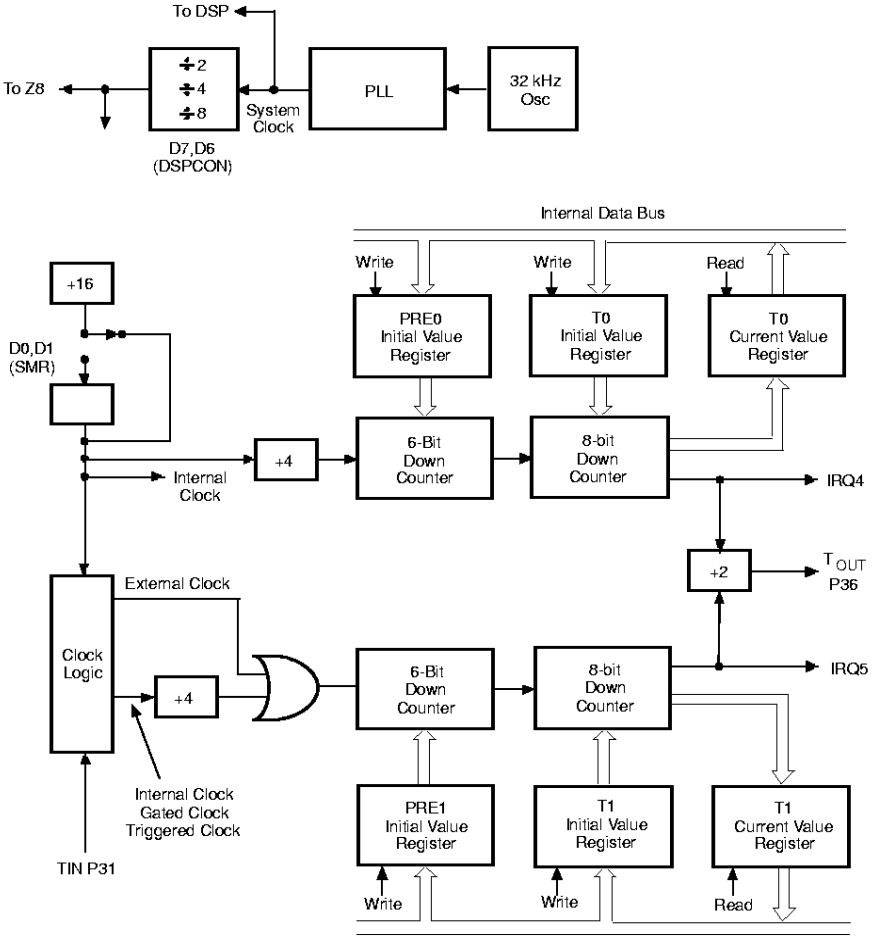


Figure 27. Counter/Timer Block Diagram

SERIAL COMMUNICATION INTERFACE

A user can elect to enable a Universal Asynchronous Receiver/Transmitter (UART), or a Self-Clocking Transceiver (SCXVR). The latter is designed for data transmission in a moderate noise environment, and mimics the function and algorithm that have been used in cordless phone applications. When either of these functions is enabled, Port 5 bit 0 (P50) is used for Receive Data Input, and Port 5 bit 1 (P51) is used for Transmit Data Output.

The Serial Communication Interface operation modes are under the control of Ports45 Control Register (P45CON), which is mapped into Z8's Extended REgister File Bank F, address 06H. Conceptually the Z8 reads received data from a Serial I/O Register (SIO), mapped into Extended Register File Bank A, address 07H. Data to be transmitted is written with the same SIO Register address.

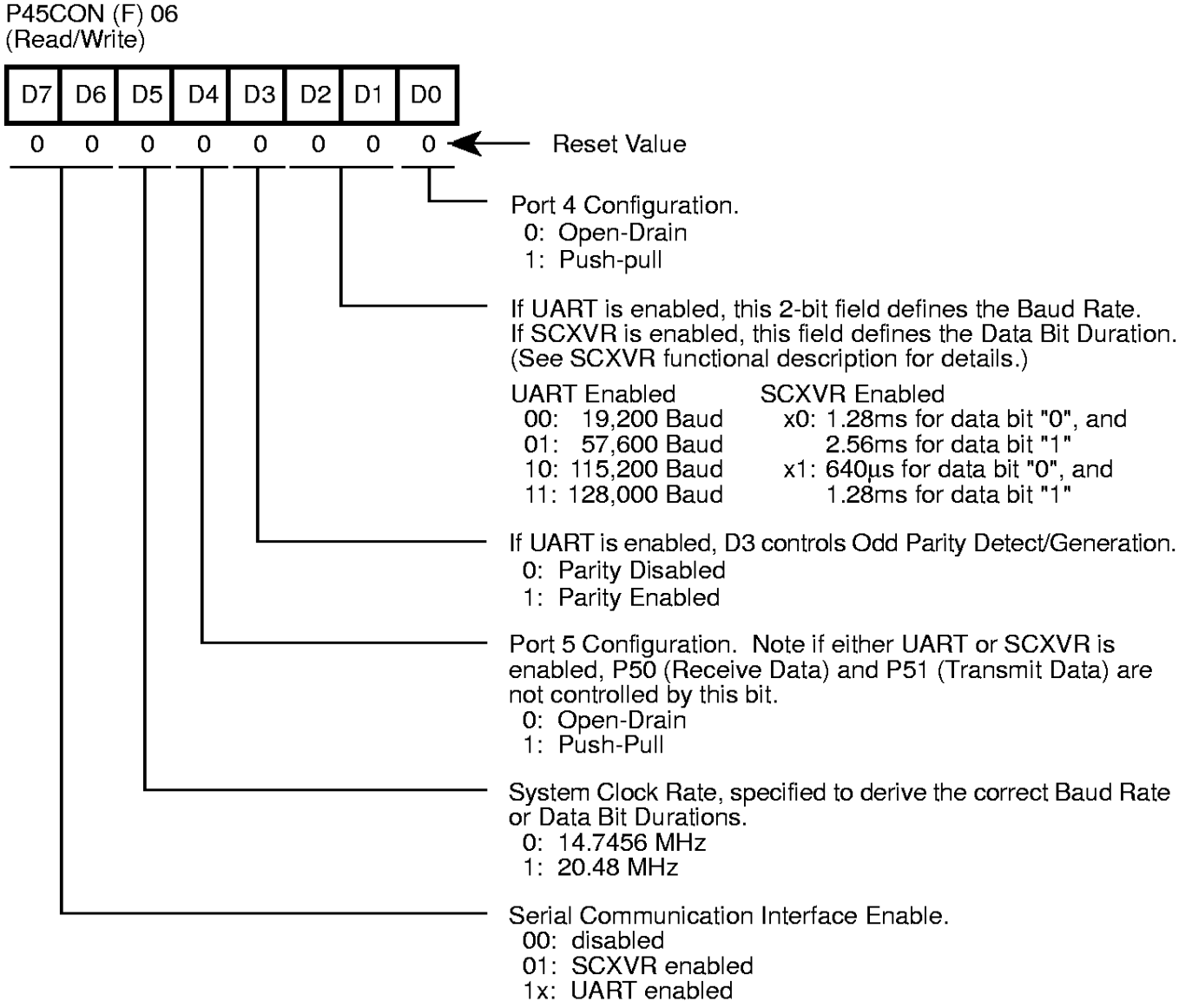


Figure 28. P45 Control Register (P45CON)

UART FUNCTIONAL DESCRIPTION (Continued)

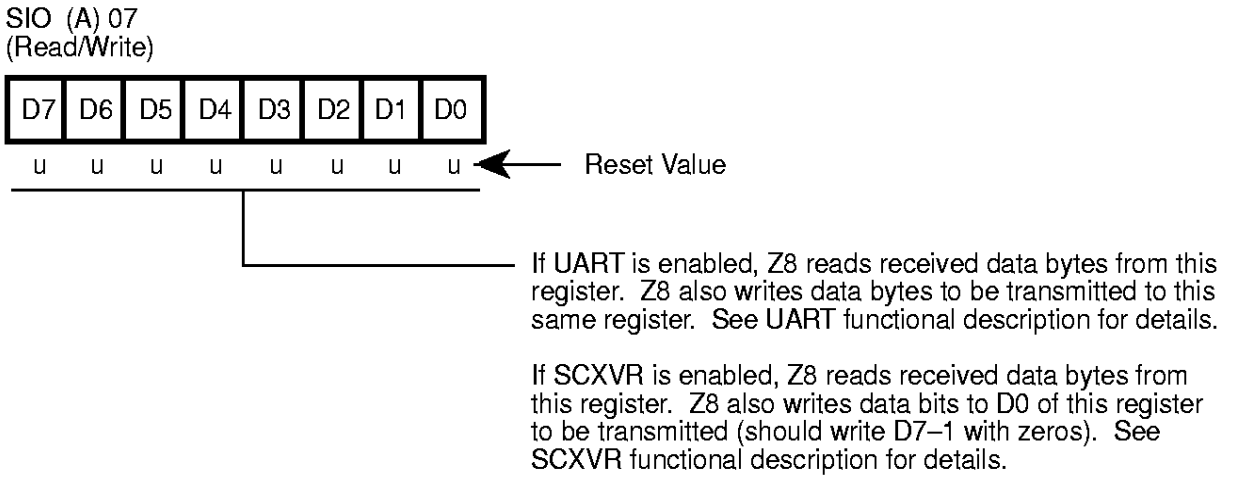


Figure 29. Serial I/O Register

UART FUNCTIONAL DESCRIPTION

Figure 30 depicts the UART block diagram. The SCI Clock Generator divides the Z89195 System Clock to output an SCI clock under the control of Ports45 Control Register (P45CON). The SCI Clock is dependent upon an enabled UART and the programmed Baud Rate or, if the SCXVR is enabled, the programmed Data Bit Duration. In the case of an enabled UART, the SCI Clock is 16X the Baud Rate.

The UART can be programmed for either 1200 or 9600 Bauds. It performs data transfers in 8-bit quantities or, with the Odd Parity Detect/Generation option enabled, in 7-bit quantities with parity flags enabled.

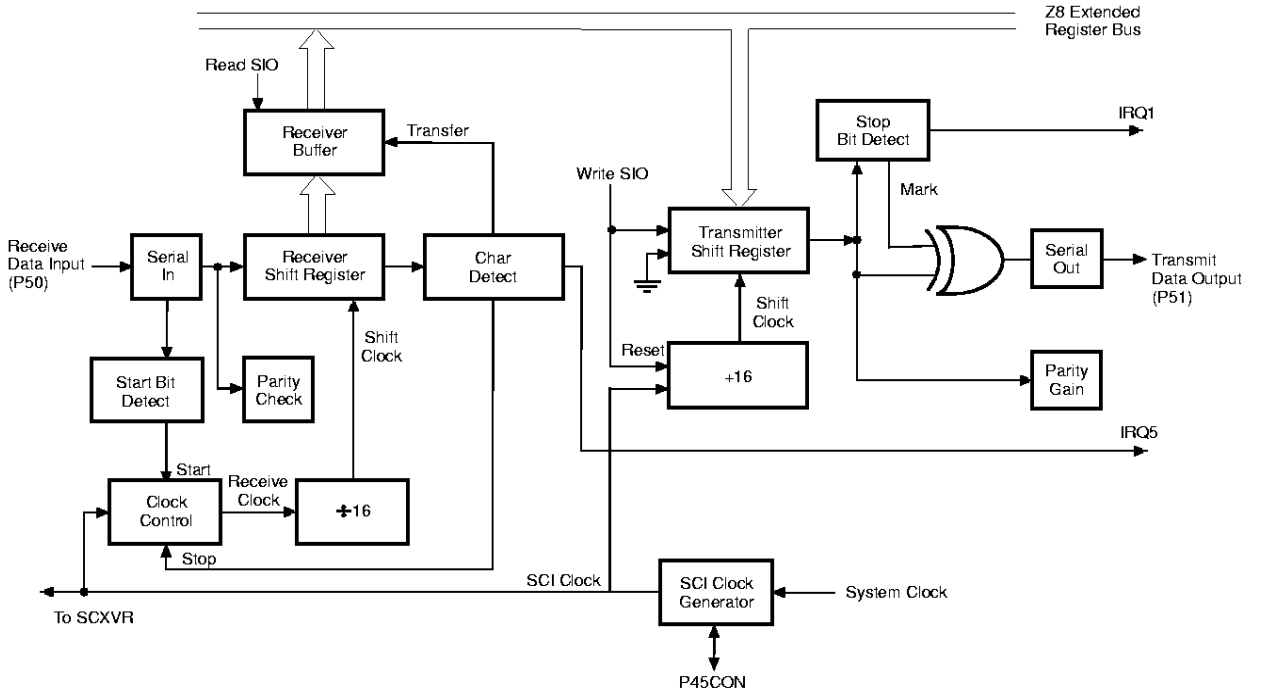


Figure 30. UART Block Diagram

The Receiver is double-buffered, having a Receiver Shift Register and a Receiver Buffer. When a character is received in the Receiver Shift Register, it is transferred to the Receiver Buffer. At the same time, interrupt IRQ0 to the Z8 is activated. If polling is used, IRQ0 bit in the Interrupt Requester Register (Bank 0, address FAH) can be examined and cleared by software. No overflow indication is provided. The Z8 must read the Receiver Buffer contents before they are replaced with the next character being shifted in. Note that Receiver Buffer is equivalent to the conceptual SIO Register at Bank A, address 07H in our earlier discussion. Receiver operation and timing are depicted in Figure 31, and data formats are shown in Figure 32. Note that a character is composed of 8 data bits, or with the Odd Parity Detect/Generation option enabled, 7 data bits plus Parity Flag (0 for no error, 1 otherwise).

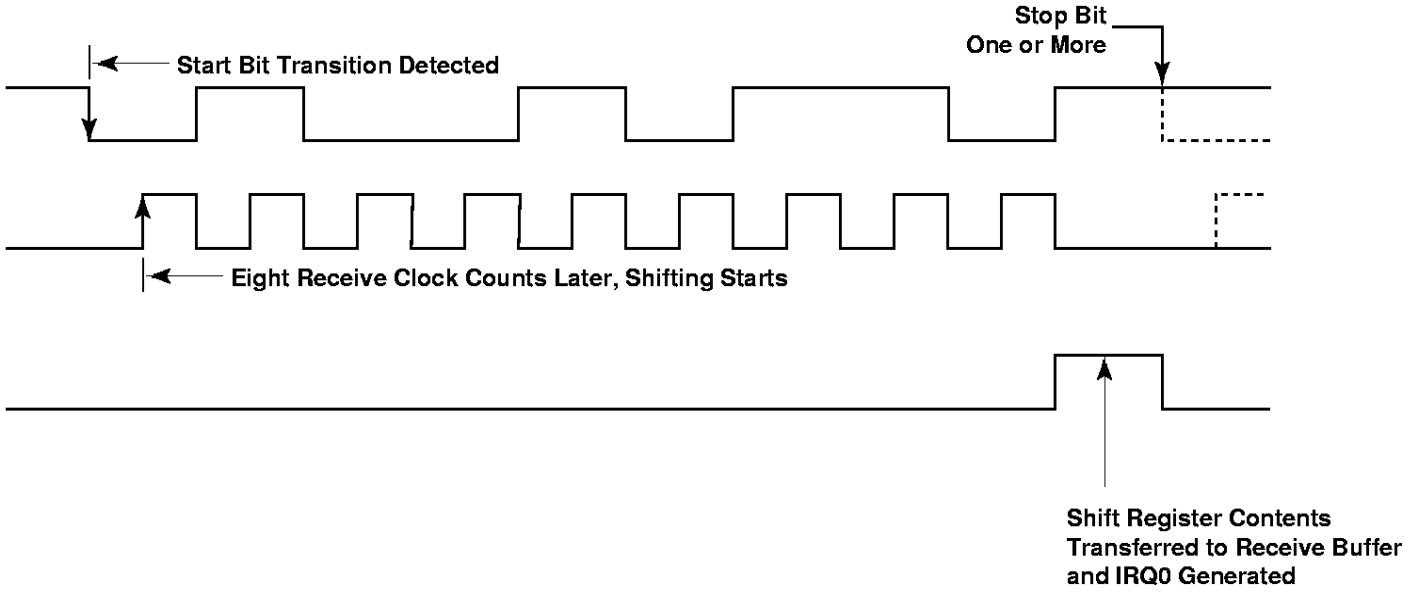


Figure 31. Receiver Operation and Timing

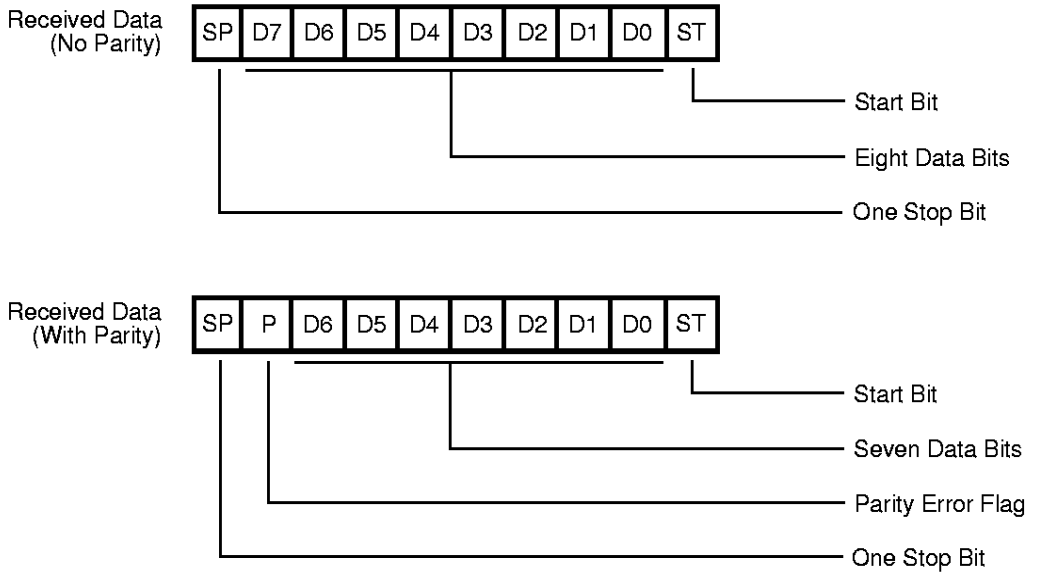


Figure 32. Receiver Data Formats

UART FUNCTIONAL DESCRIPTION (Continued)

The Transmitter is single-buffered. When the Z8 is prompted by interrupt IRQ1, it writes data for the next transmission into the Transmit Shift Register (equivalent to conceptual SIO Register at Bank A, address 07H). Alternatively, the Z8 can examine and clear IRQ1 bit in the Interrupt Request Register (Bank 0, address FAH) in polling mode. Refer to Figure 33 for transmit data formats. When data is written to the Transmit Shift Register, transmission is initiated with a Start Bit automatically inserted at the Transmit Data Output, followed by D0 through D7, then 2 Stop Bits; or if the Odd Parity Detect/Generation Option is enabled, D6 is followed by an automatically generated Odd Parity Bit, then 2 Stop Bits. When at idle, Transmit Data Output is conditioned at the Mark state (Logic 1).

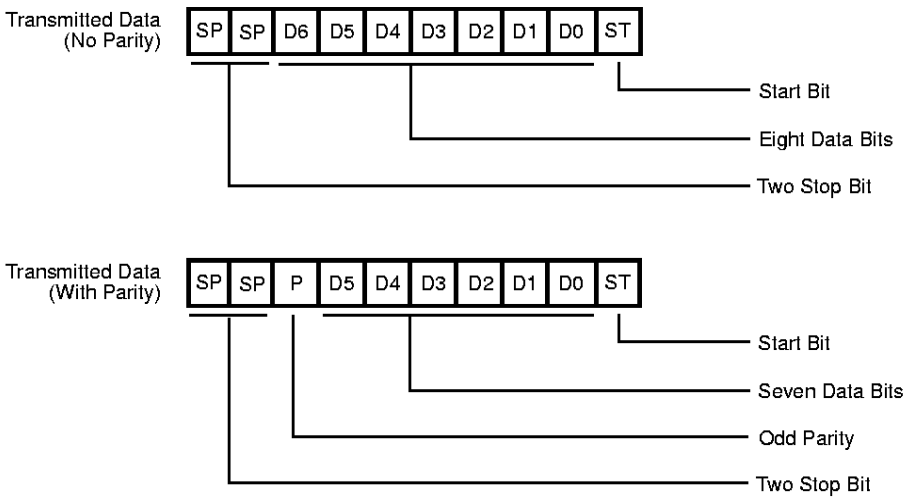


Figure 33. Transmitter Data Formats

The Transmit Shift Register can be overwritten while a current character is being shifted out, which allows a Break signal (Logic 0) to be generated easily. Z8 can write null characters to the Transmit Shift Register at rate prior to parity and stop bits are to be generated. The design is such that a new character transmission with a new start bit is initiated every time the Transmit Shift Register is written.

SCXVR FUNCTIONAL DESCRIPTION

The Self-Clocking Transceiver SCXVR is designed for serial communication in a moderate noise environment. It mimics the function and algorithm that is useful in cordless phone applications. The algorithm being implemented permits detection of data bits in the presence of phase shift and noise.

The definition for the zero (0) data bit and the one(1) data bit is shown in Figure 34. The bits are generated with a 50% duty cycle. The basic time unit is T1. A zero bit has T1 time at logic High followed by T1 time at logic Low. A one bit has 2XT1 time at logic High followed by 2XT1 time at logic Low. That is, a one bit has twice the duration of a zero bit.

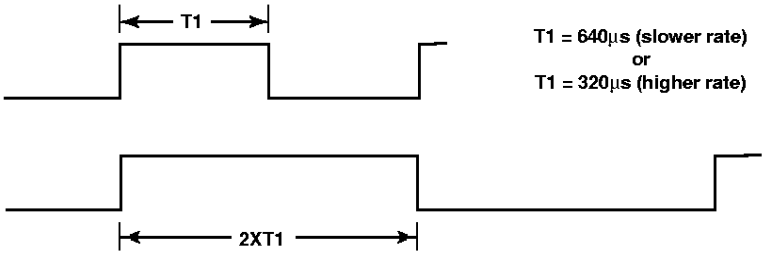


Figure 34. SXCVR Bit Definition

The SCXVR supports two bit rates. The slower bit rate has a Data Bit Duration of 1.28ms for the zero bit and 2.56ms for the one bit. The faster bit rate has a Data Bit Duration of 640µs for the zero bit and 1.28ms for the one bit.

As described earlier in the UART Functional Description, the Z89195 System Clock is divided in the SCI Clock Generator block, under the control of Ports45 Control Register (P45CON). If SCXVR is enabled, the SCI Clock Generator outputs its SCI Clock with a 5µs period, whether the System Clock in effect is 20.48MHz or 14.7456MHz. This SCI clock as well as the System Clock are inputs to SCXVR's Transmitter and Receiver.

The SCXVR Transmitter is shown in Figure 35. It is a single-bit, double-buffered configuration. The Z8 writes to the Tx Buffer a one- or zero-data bit for transmission via its Extended Register Bus, bit 0. The higher order unused bits should be written with zeroes. Note that the Tx Buffer is equivalent to the conceptual SIO Register at Bank A, address 07H in our earlier discussion. If the Transmitter is at idle, the Tx State Machine samples the Tx Buffer bit value, and enables its "1" Generate or "0" Generate block accordingly, which generates a 50-% duty cycle data bit waveform at Transmit Data Output. At the end of the Data Bit Duration in effect, the "1" Generate or "0" Generate block issues an END1 or END0 signal to Tx State Machine. At the time when Tx State Machine samples the Tx buffer value to initiate a data bit transmission, it issues an interrupt IRQ1 to the Z8, which prompts the Z8 to write a next data bit to Tx Buffer, to be transmitted immediately following the completion of the current data bit transmission. If polling is used, the Z8 can examine the IRQ1 bit in the Interrupt Request Register (Bank 0, address FAH) to service the Transmitter. If at the end of a data bit transmission and the Tx Buffer has not been updated with a new bit value, the Transmit Data Output is conditioned at logic Low.

SCXVR FUNCTIONAL DESCRIPTION (Continued)

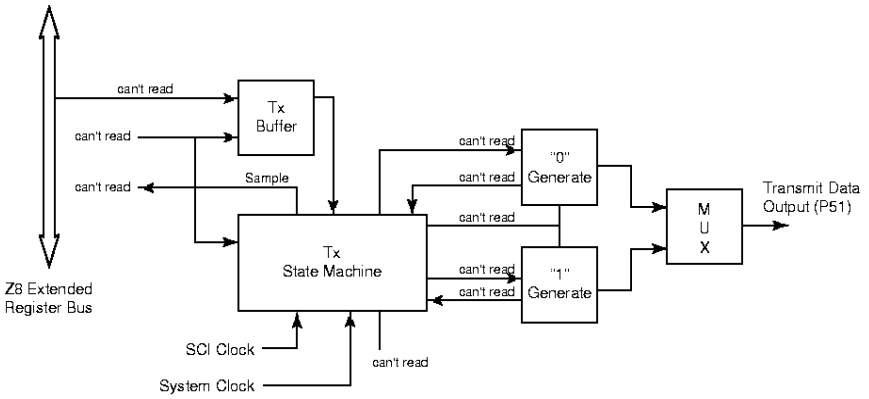


Figure 35. SCXVR Transmitter

The SCXVR Receiver is shown in Figure 36. It shifts in 8 data bits from the Receive Data Input to compose a byte and loads the byte into the Rx Buffer. Our protocol specifies the incoming byte as least significant bit first, most significant bit last. The Receiver is byte-wise double-buffered, since the Z8 can read from the Rx Buffer while a second data byte is being shifted in. Note that the Rx Buffer is equivalent to the conceptual SIO Register at Bank A, address 07H in our earlier discussion. The Receiver generates an IRQ0 interrupt to the Z8 in an interrupt-driven system. Or, if polling is used, the IRQ0 bit in the Interrupt Request Register (Bank 0, address FAH) can be examined and cleared by software.

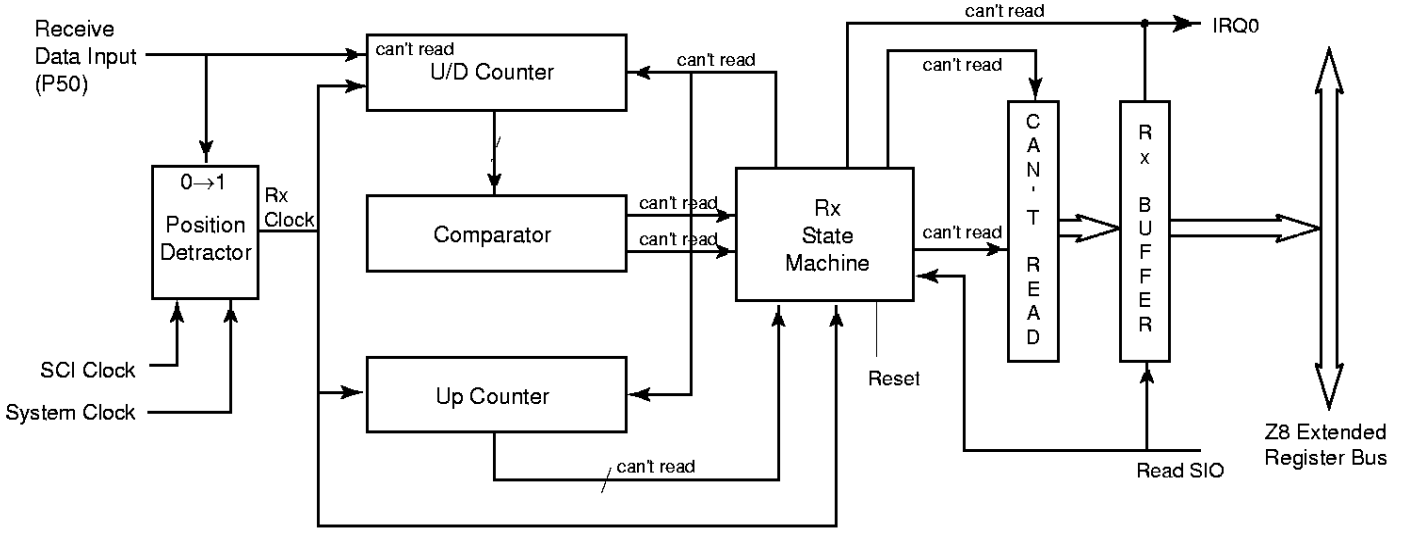


Figure 36. SCXVR Receiver

Receive Data Input is monitored by the 0→1 Transition Detector block, which holds its Rx Clock output at logic Low when in the idle state. When a 0→1 transition is detected, the Rx Clock becomes a divide-by-4 or divide-by-2 version of SCI Clock, as determined by the programmed Data Bit Duration in effect. That is, the Rx Clock is at 20µs period for the slower bit rate and at 10µs period for the higher bit rate.

This Rx Clock controls the operation of an Up/Down Counter, an Up Counter, as well as the Rx State Machine. The Receive Data Input is sampled multiple times throughout a data bit time. For example, the zero bit is sampled 32 times when it is High, and 32 times when it is Low. The one bit is sampled 64 times when it is High, and 64 times when it is Low. The bit decoding algorithm is further defined in the following steps.

1. Upon Z89195 reset, reset all registers, counters and Rx State Machine.

2. Look for a 0→1 transition on Receive Data Input to enable Rx Clock and operation for the Up/Down Counter and Up Counter.

3. When the Up Counter reaches a count of 56, check the Up/Down Counter value. If the Value is less than 16, output a zero bit. When the Up Counter reaches 60, reset the Counters. Go to Step 2.

4. If the Up/Down Counter value is not less than 16 in Step 3, continue until the Up Counter reaches 112 and recheck the Up/Down Counter value. If the value is less than 64, output a one bit, otherwise no bit is output. When the Up Counter reaches 120, reset the Counters. Go to Step 2.

The above algorithm is basically a digital filter that is initiated on a Receive Data Input 0→1 transition. The Up/Down Counter filters all of the High period and some of the Low period. There can be glitches in both of those times such that the sampling will filter them out. In addition, the duration of the High and Low periods does not need to be exact. The bits into the Receiver can be continuous. Extreme noise conditions are tolerated in the sense that the detection is reset when the Up Counter reaches 60 (higher bit rate) or 112 (lower bit rate). False 0→1 transition is tolerated as neither a one nor a zero bit is output.

ARAM CONTROLLER

The Z89195 incorporates an ARAM Controller, which allows the Z8 to access audio grade DRAMs organized in various configurations. The Controller can be programmed for access speed of either 100ns or 200ns when Z8 clock frequency is at 10.24 MHz. The Z8 reads and writes data through the Controller in byte quantities, and can address a linear space of up to 6MB. An address auto-increment feature allows the Z8-supplied address field A7–0 to be incremented by 1 after each data byte transfer. In addition, the Controller can be programmed to perform CAS-before-RAS refresh cycles to the ARAMs. Configurations being supported are listed in Table 8.

Table 8. ARAM Configurations Supported

Type	No. of Chips	Address Space
256K x 16	1	512KB
256K x 16	2	1MB
1M x 16	1	2MB
1M x 16	2	4MB
4M x 4	1	2MB
4M x 4	2	4MB
4M x 4	3	6MB

Note: Four 4Mx1 chips can be configured as one 4Mx4

When the ARAM Controller is enabled, Ports 7, 6 and a portion of Port 5 are used for address, data and control signals. These port pin assignments are shown in Table 9.

Table 9. ARAM Pin Assignments

Port Pins	256Kx16	1Mx16	4Mx4
P77	D15	D15	D3
P76	D14	D14	D2
P75	D13	D13	D1
P74	D12	D12	D0
P73	D11	D11	$\overline{CAS0}$
P72	D10	D10	A10
P71	D9	AD9	A9
P70	AD8	AD8	A8
P67	AD7	AD7	A7
P66	AD6	AD6	A6
P65	AD5	AD5	A5
P64	AD4	AD4	A4
P63	AD3	AD3	A3
P62	AD2	AD2	A2
P61	AD1	AD1	A1
P60	AD0	AD0	A0
P57	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
P56	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
P55	$\overline{RAS0}$	$\overline{RAS0}$	$\overline{RAS}$
P54	$\overline{CASL}$	$\overline{CASL}$	$\overline{CAS1}$
P53	$\overline{CASH}$	$\overline{CASH}$	$\overline{CAS2}$
P52	$\overline{RAS1}$	$\overline{RAS1}$	

ARAM CONTROLLER (Continued)

When 16-bit wide ARAMs are being used, the Controller activates $\overline{CASL}$ (CAS Low Byte) in the access cycle if the Z8-supplied address is even. If the supplied address is odd, $\overline{CASH}$ (CAS High Byte) is asserted. That is, one byte of data is read or written in each access cycle. In a single-chip configuration, only $\overline{RAS0}$ is required and pin P52 can be used as a general purpose port pin. In a 2-chip configuration, $\overline{RAS0}$ and $\overline{RAS1}$ are used to distinguish which chip is being accessed. $\overline{RAS0}$ is active for access cycles with a Z8-supplied address most significant bit at 0. Otherwise, $\overline{RAS1}$ is active. The Controller drives and inputs the contents of the multiplexed address/data bus at appropriate times in a read or late-write cycle, as well as providing the appropriate $\overline{WE}$ and $\overline{OE}$ pulses.

When 4-bit wide ARAMs are being used, the Controller appends a least significant bit to the Z8-supplied address. The Controller performs a page mode cycle to transfer two nibbles of data, with the aforementioned least significant address bit first at 0, then at 1. The first nibble of the access cycle is directed to or from the more significant half of the data byte as seen by the Z8, the second nibble as the less significant half. Page mode read or page mode late write cycles are performed. ARAM address and data buses are nonmultiplexed. Up to three ARAMs can be supported, each controlled by its own CAS signal. When not required as CAS signals, P53 and P54 can be used as general purpose port pins. Table 12 details which CAS signals are active in access cycles in the supported configurations.

Table 10. CAS Activation for 4Mx4 Configurations

No. of Chips	CAS0	CAS1	CAS2	Z8-Supplied Address 2 Most Significant Bits
1-chip	L			A20–19 = xx
2-chip	L	H		A21–20 = 0x
	H	L		A21-20 = 1x
3-chip	L	H	H	A22–21 = 00
	H	L	H	A22–21 = 01
	H	H	L	A22–21 = 1x

The ARAM Controller can be programmed to generate CAS-before-RAS refresh cycles to meet various ARAM chip specifications. For every 32.768 kHz oscillator period (30.52µs), it performs a single refresh cycle, or 2 or 4 back-to-back refresh cycles. The oscillator rate is chosen so that ARAM refreshes are independent of the Z8 clock frequency. For 16-bit wide ARAM configurations, both $\overline{CASH}$ and $\overline{CASL}$ are pulsed at the same time in the refresh cycles, and if 2-chips are configured, both $\overline{RAS0}$ and $\overline{RAS1}$ are pulsed at the same time. For 4-bit wide ARAM configurations, all the required CAS signals are pulsed at the same time. The refresh function can be disabled and enabled to accommodate time windows of heavy memory access activities. At disabling, if a refresh cycle is in progress, it will be allowed to complete. If disabling is at the midst of back-to-back refreshes, the sequence is prematurely terminated by allowing only the refresh in progress to complete. The following code sequence is suggested:

```
Disable refresh
NOP              (time for refresh, if any, to complete)
ARAM read or write
```

The ARAM Controller registers are assigned to Z8's Extended Register address space, Bank A.

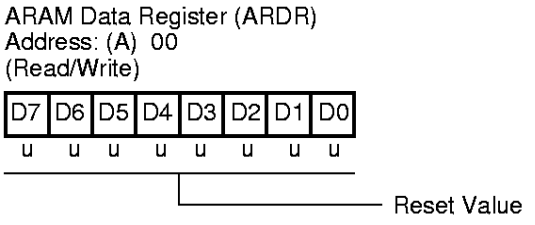


Figure 37. ARAM Data Register

Z8 reads data bytes from or write data bytes to external ARAM(s) via this register. The contents of this register are unaffected by a reset.

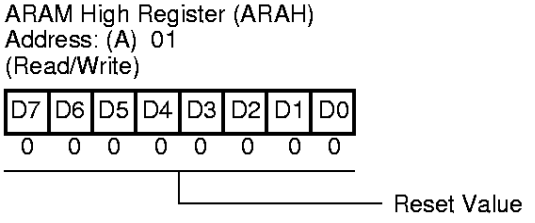


Figure 38. ARAM High Register

D7: Reserved. Read as 0, should write 0.

D6–0: Z8 Address A22–16 for 6MB address space. For smaller address space configurations, the appropriate high bit(s) should be written with 0's.

ARAM Address Mid Register (ARAM)
Address: (A) 02
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Reset Value

Figure 39. ARAM Address Mid Register

D7–0: Z8 Address A15–8.

ARAM Address Low Register (ARAL)
Address: (A) 03
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Reset Value

Figure 40. ARAM Address Low Register

D7–0: Z8 Address A7–0

ARAM Control Register (ARCR)
Address: (A) 04
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Reset Value

Figure 41. ARAM Control Register

D7: ARAM Controller Enable.
0: disable 1: enable.

D6–5: This field defines the type of ARAM chip(s) being used.
00: 256Kx16
01: 1Mx16
10: 4Mx4
11: 4Mx4, 3 chips

D4: Number of ARAM chips being used.
0: 1 chip 1: 2 chips
D4 is don't care if D7–6 are programmed 1's.

D3: ARAM Access Speed (Z8 at 10.24 MHz).
0: 200ns 1: 100ns

D2: Address Auto-Increment
0: disable 1: enable

D1–0: This field enables and defines the number of back-to-back refresh cycles to be issued every 30.52µs.
00: refresh disabled
01: 1 refresh cycle
02: 2 back-to-back refresh cycle
03: 4 back-to-back refresh cycle

When the Z8 writes to the ARAM Data Register, it starts an ARAM write cycle with addressing defined by the ARAM Address High, Mid and Low Registers. After completion of the data byte transfer, the contents of ARAM Address Low Register is incremented by 1, if the auto-increment option is selected.

When the Z8 reads from the ARAM Data Register, it reads the existing contents of that register, and an ARAM read cycle is initiated with addressing defined by the ARAM Address High, Mid and Low Registers. The new data byte is stored in ARAM Data Register, available for the Z8's next read. The contents of ARAM Address Low Register are incremented by 1, if the auto-increment option is selected.

Z8 codes should be written to allow sufficient time between data transfers, and also to account for possible refresh cycle(s) in progress, Earlier discussion on the refresh function describes how to define time windows for multiple memory access activities.

Z8 FUNCTIONAL DESCRIPTION

Port Configuration Register (PCON). The PCON register configures the comparator output on Port 3. The PCON register (Figure 42) is located in the Expanded Register File at Bank F, location 00H.

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35, and a 0 releases the Port to its standard I/O configuration.

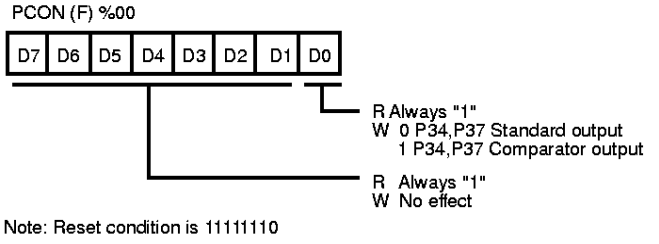


Figure 42. Port Configuration Register (PCON)

Port 4 and 5 Configuration Register (P45CON). The P45CON register configures Port 4 and Port 5, individually, to open-drain or push-pull active. This register is located in the Expanded Register File at Bank F, location 06H.

Port 4 Open-Drain (D0). Port 4 can be configured as an open-drain by resetting this bit (D0 = 0) or configured as push-pull active by setting this bit (D0 = 1). The default value is 1.

Port 5 Open-Drain (D4). Port 5 can be configured as an open-drain by resetting this bit (D4 = 0) or configured as push-pull active by setting this bit (D4 = 1). The default value is 1.

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

5. Power fail to Power OK status;
6. Stop-Mode Recovery (if D5 of SMR=1);
7. WDT time-out.

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation. It reduces the standby current to 20 µA or less. The STOP Mode is terminated by a reset only, either by WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate Sleep instruction, i.e.,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 35). All bits are Write-Only except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register group at address 0BH.

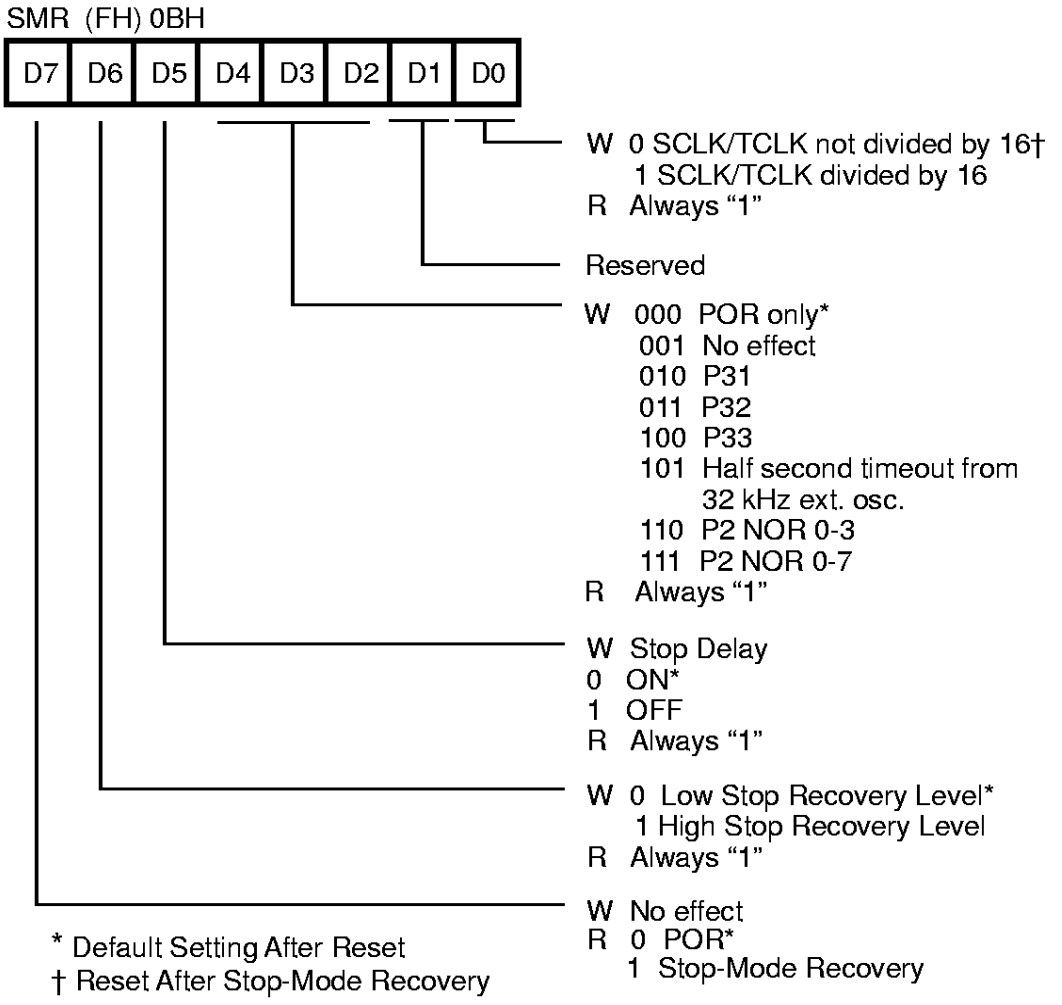


Figure 43. Stop-Mode Recovery Register (SMR)

SCLK/TCLK divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources counter/timers and interrupt logic).

Stop-Mode Recovery Source (D4–D2). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 44 and Table 11).

Z8 FUNCTIONAL DESCRIPTION (Continued)

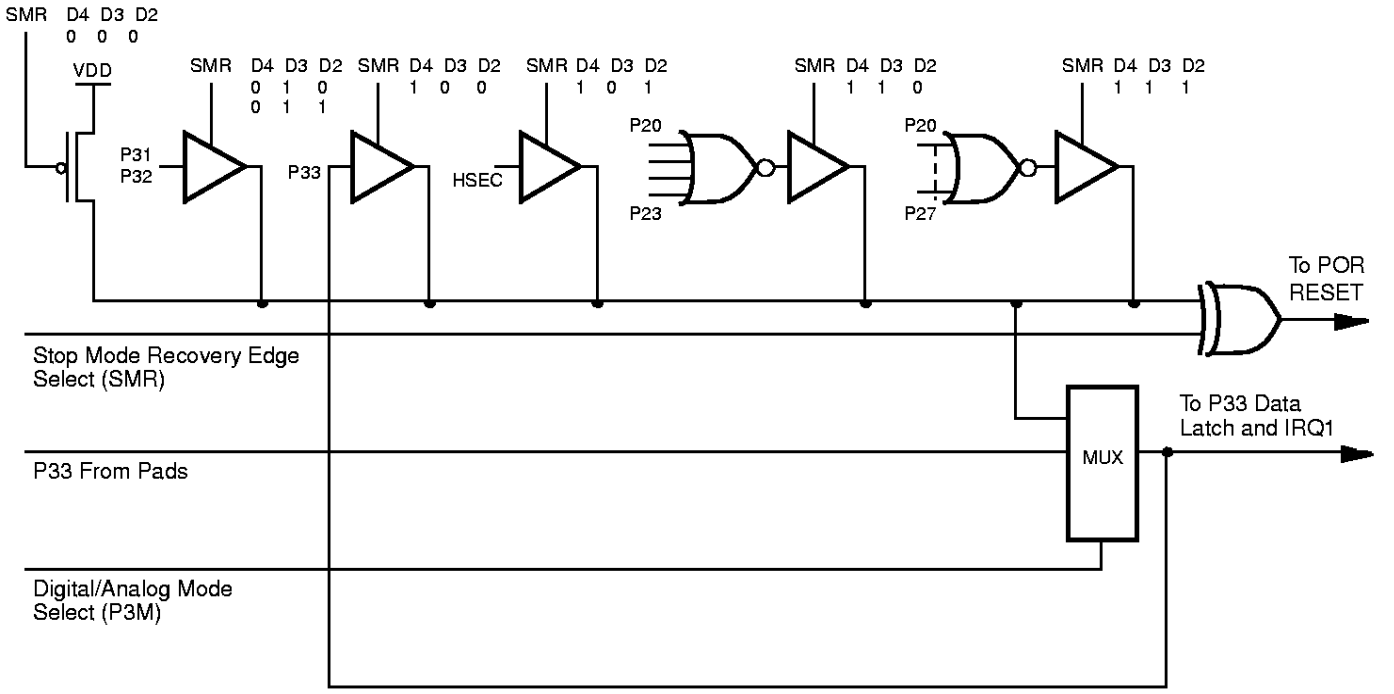


Figure 44. Stop-Mode Recovery Source

Table 11. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	No effect
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	HSEC
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). When Low, this bit disables the 5 ms $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z89195/196 from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Table 13).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active High, and is 0 (cold) on POR/WDT $\overline{\text{RESET}}$. This bit is Read-Only. It is used to distinguish between a cold or warm start.

DSP Control Register (DSPCON). The DSPCON register controls various aspects of the Z8 and the DSP. It can configure the internal system clock (SCLK) or the Z8, $\overline{\text{RESET}}$, and HALT of the DSP, and control the interrupt interface between the Z8 and the DSP (Table 12).

Table 12. DSP Control Register (F) OCH [Read/Write]

Field DSPCON (F)0CH	Position	Attrib	Value	Label
Z8_SCLK	76------	R/W	00	(OSC/8)
			01	(OSC/4)
			1x	(OSC/2)
DSP_Reset	--5-----	R		Return "0"
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--	W		No effect
		R		Return "0"
				No effect
DSP_INT2	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
Z8_IRQ3	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect

Z8 IRQ3 (D0). When read, this bit indicates the status of the Z8 IRQ3. The Z8 IRQ3 is set by the DSP by writing to D9 of DSP External Register 4 (ICR). By writing a 1 to this bit, Z8 IRQ3 is Reset.

DSP INT2 (D1). This bit is linked to DSP INT2. Writing a 1 to this bit sets the DSP INT2. Reading this bit indicates the status of the DSP INT2.

DSP RUN (D4). This bit defines the HALT Mode of the DSP. If this bit is set to 0, then the DSP clock is turned off to minimize power consumption. After this bit is set to 1, then the DSP will continue code execution from where it was halted. After a hardware reset, this bit is reset to 1.

DSP RESET (D5). Setting this bit to 1 will reset the DSP. If the DSP was in HALT Mode, this bit is automatically preset to 1. Writing a 0 has no effect.

Z8 SCLK (D7–D6). These bits define the SCLK frequency of the Z8. The oscillator can be divided by 8, 4, or 2. After a reset, both bits default to 00.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an onboard RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 37). The WDTMR register is accessible only within 64 Z8 clock cycles after POR.

Z8 FUNCTIONAL DESCRIPTION (Continued)

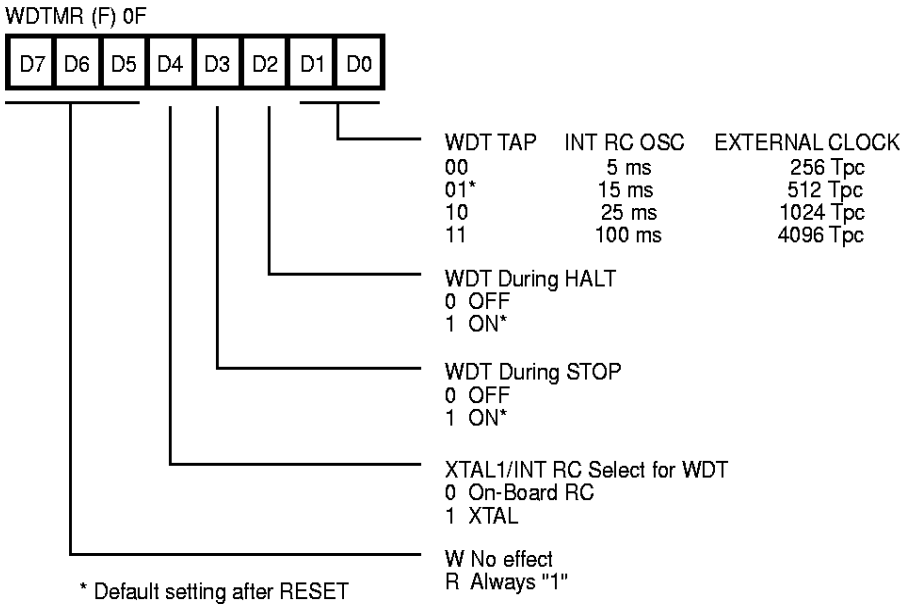


Figure 45. Watch-Dog Timer Mode Register

Half-Second Timer Status Register (HSEC). The half-second timer status register (Figure 46) is a free-running timer clocked by the external 32.768 kHz crystal. In normal operation mode, every half-second, the timer will time-out and set bit 0 (D0) of the HSEC register to 1. The user can reset this bit for real timing. In Stop mode, this timer can be used as a Stop-Mode Recovery source. Every half-second, the timer will recover the Stop mode and bit 0 of the HSEC register will be set to 1. Therefore, in Stop Mode, the user can keep real time.

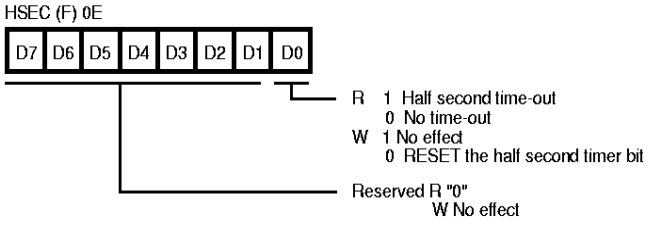


Figure 46. Half-Second Timer Status Register

WDT Time Select (D0, D1). These bits selects the WDT time period. The configuration is shown in Table 13.

Table 13. WDT Time Select

D1	D0	Time-out of Internal RC OSC	Time-out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle.
Tolerance = ±10%

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the RC oscillator.

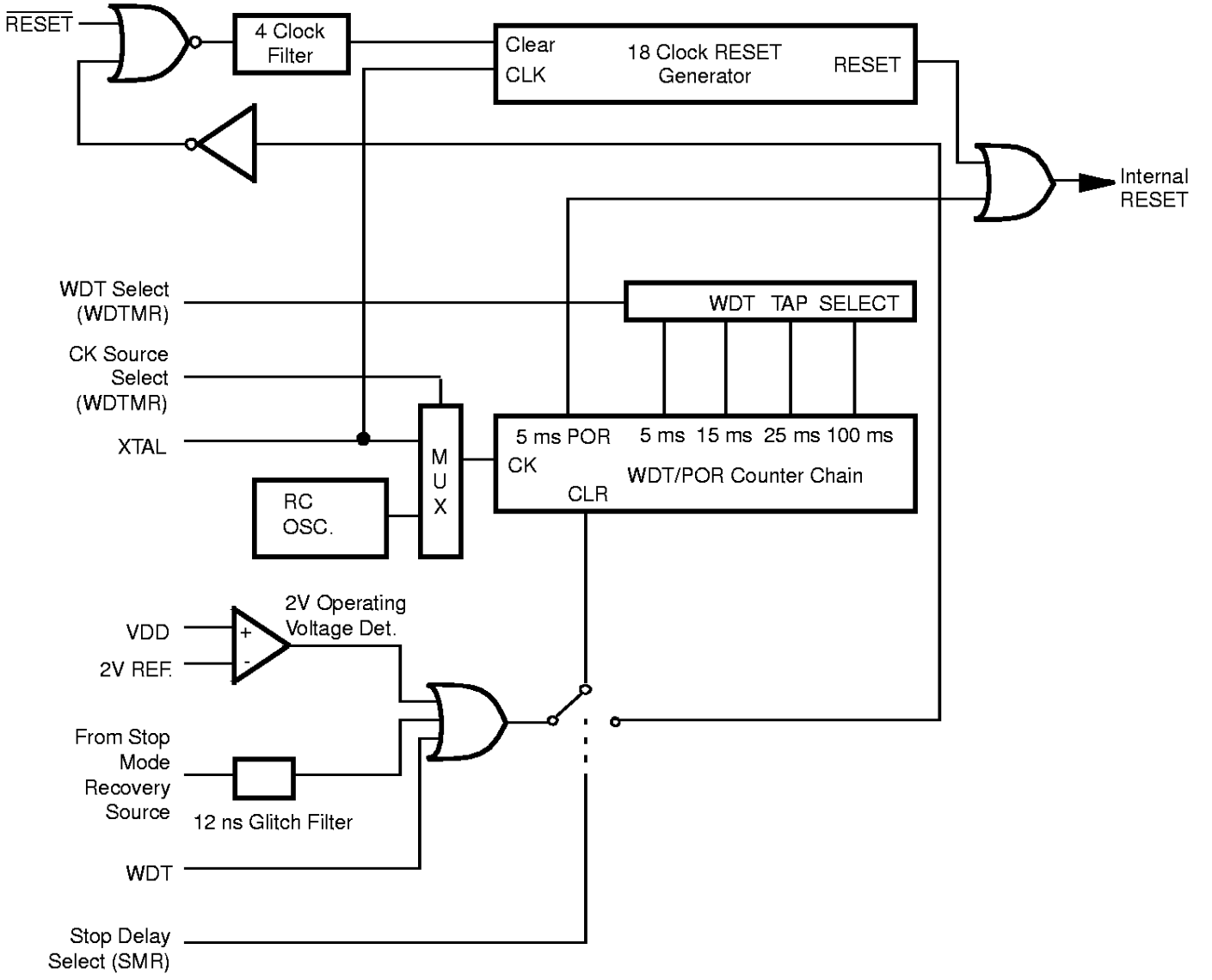


Figure 47. Resets and WDT

DSP REGISTERS DESCRIPTION

General. The DSP is a high-performance second generation CMOS Digital Signal Processor with a modified Harvard-type architecture with separate program and data ports. The design has been optimized for processing power and saving silicon space.

Registers. The DSP has eight internal registers and seven external registers. The external registers are for the A/D and D/A converters, Codec Interface, and the mailbox and interrupt interfacing between DSP to the Z8. External registers are accessed in one machine cycle, the same as internal registers.

DSP Registers

There are 15 internal and extended 16-bit registers which are defined in Table 14.

Table 14. DSP Registers

Register	Attribute	Register Definition
BUS	Read	Data-Bus
X	Read/Write	X Multiplier Input, 16-Bit
Y	Read/Write	Y Multiplier Input, 16-Bit
A	Read/Write	Accumulator, 24-Bit
SR	Read/Write	Status Register
Stack	Read/Write	Stack
PC	Read/Write	Program Counter
P	Read	Output of MAC, 24-Bit
EXT0	Read	Z8 ERF Bank B, Register 00–01 (from Z8)
	Write	Z8 ERF Bank B, Register 08–09 (to Z8)
EXT1	Read	Z8 ERF Bank B, Register 02–03 (from Z8)
	Write	Z8 ERF Bank B, Register 0A–0B (to Z8)
EXT2	Read	Z8 ERF Bank B, Register 04–05 (from Z8)
	Write	Z8 ERF Bank B, Register 0C–0D (to Z8)
EXT3	Read	Z8 ERF Bank B, Register 06–07 (from Z8)
	Write	Z8 ERF Bank B, Register 0E–0F (to Z8)
EXT4	Read/Write	DSP Interrupt Control Register
EXT5	Read	A/D Converter, Codec Interface
	Write	D/A Converter, Codec Interface
EXT6	Read/Write	Analog Control Register

EXT3–EXT0 (External Registers 3–0). These are the Mailbox Registers used by the DSP and Z8 to communicate. These four 16-bit registers correspond to the eight outgoing and eight incoming 8-bit registers in Bank B of the Z8's Expanded Register File.

EXT4 (DSP Interrupt Control Register (ICR)). This register controls the interrupts in the DSP as well as the interrupts in common between the DSP and the Z8. It is accessible by the DSP only, except for bit F and bit 9.

EXT5 (D/A, A/D and Codec Data Register). This register is used by both D/A and A/D converters, as well as the Codec Interface. The D/A converter and Codec Interface output data are loaded by writing to this register, while the A/D converter and Codec Interface input data are read from this register. The Register EXT5 is accessible only by the DSP.

EXT6 (Analog Control Register). This register controls the D/A and A/D converters and the Codec Interface. It is a read/write register accessible only by the DSP.

DSP Z8 Mail Box

To receive information from the DSP, the Z8 uses eight incoming registers which are mapped in the Z8 extended Register File (Bank B, 08 to 0F). The DSP treats these as four 16-bit registers that correspond to the eight incoming Z8 registers (Figure 48).

The Z8 can supply the DSP with data through eight outgoing registers mapped into both the Z8 Expanded Register File (Bank B, Registers 00 to 07) and the external register interface of the DSP. These registers are Read/Write and can be used as general-purpose registers of the Z8. The DSP can only read information from these registers. Since the DSP uses a 16-bit data format and the Z8 an 8-bit data format, eight outgoing registers of the Z8 correspond to four DSP registers. The DSP can only read information from the outgoing registers.

Both the outgoing registers and the incoming registers share the same DSP address (EXT3–EXT0).

Note: The Z8 can read and write to ERF Bank B R00–R07, Registers 08–0F are Read-Only from the Z8.

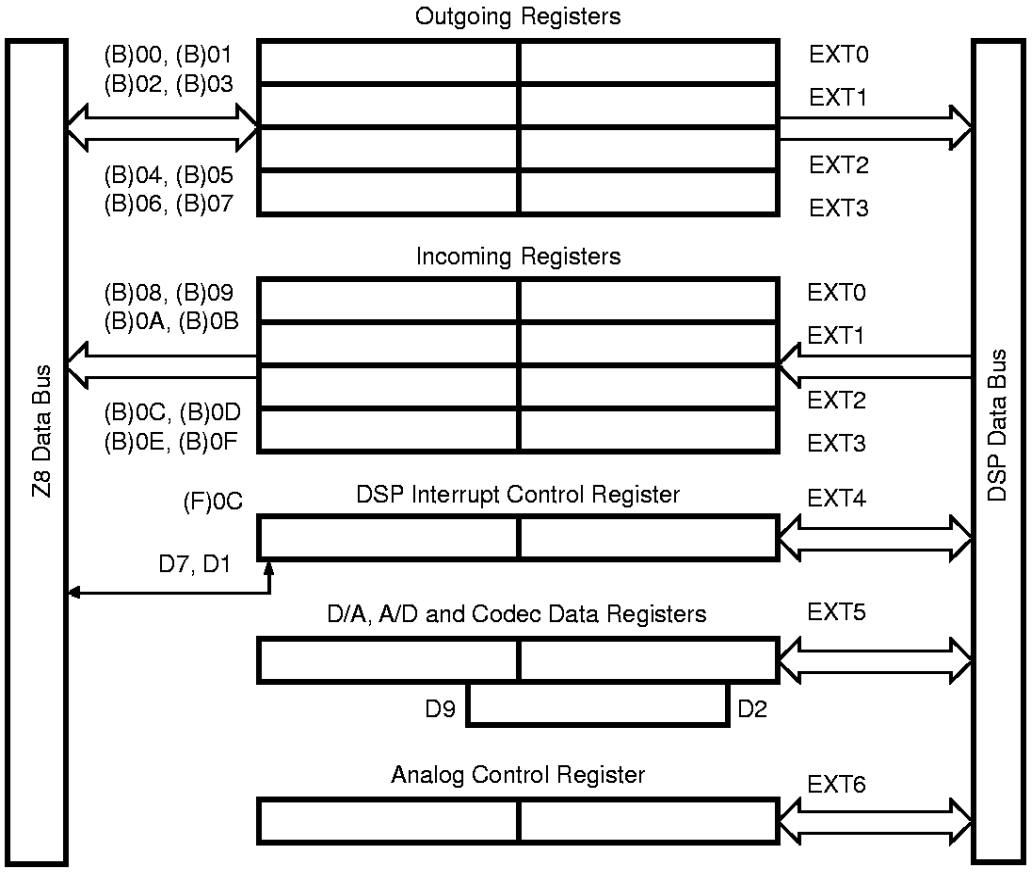


Figure 48. Z8-DSP Interface

DSP REGISTERS DESCRIPTION (Continued)

Table 15. Z8 Outgoing Registers (Read-Only from DSP)

Field	Position	Attrib	Value	Label
Outgoing [0] (B)00	76543210	R/W	%NN	(B)00DSP_ext0_hi
Outgoing [1] (B)01	76543210	R/W	%NN	(B)01DSP_ext0_lo
Outgoing [2] (B)02	76543210	R/W	%NN	(B)02DSP_ext1_hi
Outgoing [3] (B)03	76543210	R/W	%NN	(B)03DSP_ext1_lo
Outgoing [4] (B)04	76543210	R/W	%NN	(B)04DSP_ext2_hi
Outgoing [5] (B)05	76543210	R/W	%NN	(B)05DSP_ext2_lo
Outgoing [6] (B)06	76543210	R/W	%NN	(B)06DSP_ext3_hi
Outgoing [7] (B)07	76543210	R/W	%NN	(B)07DSP_ext3_lo

Table 16. Z8 Incoming Registers (Write-Only from DSP)

Field	Position	Attrib	Value	Label
Incoming [8] (B)08	76543210	R	%NN	DSP_ext0_hi
		W		No Effect
Incoming [9] (B)09	76543210	R	%NN	DSP_ext0_lo
		W		No Effect
Incoming [a] (B)0A	76543210	R	%NN	DSP_ext1_hi
		W		No Effect
Incoming [b] (B)0B	76543210	R	%NN	DSP_ext1_lo
		W		No Effect
Incoming [c] (B)0C	76543210	R	%NN	DSP_ext2_hi
		W		No Effect
Incoming [d] (B)0D	76543210	R	%NN	DSP_ext2_lo
		W		No Effect
Incoming [e] (B)0E	76543210	R	%NN	DSP_ext3_hi
		W		No Effect
Incoming [f] (B)0F	76543210	R	%NN	DSP_ext3_lo
		W		No Effect

Table 17. DSP Incoming Registers

Field	Position	Attrib	Value	Label
DSP_ext0	fedcba9876543210	R	%NNNN	(B)00, (B)01
Mail Box		W		(B)08, (B)09
DSP_ext1	fedcba9876543210	R	%NNNN	(B)02, (B)03
Mail Box		W		(B)0A, (B)0B
DSP_ext2	fedcba9876543210	R	%NNNN	(B)04, (B)05
Mail Box		W		(B)0C, (B)0D
DSP_ext3	fedcba9876543210	R	%NNNN	(B)06, (B)07
Mail Box		W		(B)0E, (B)0F

DSP Interrupts

The DSP processor has three interrupt sources (INT2, INT1, INT0) (Figure 49). These sources have different priority levels (Figure 50). The highest priority, the next lower and the lowest priority level are assigned to INT0, INT1 and INT2, respectively (Figure 51). When two interrupt requests occur simultaneously the DSP starts servicing the interrupt with the highest priority level.

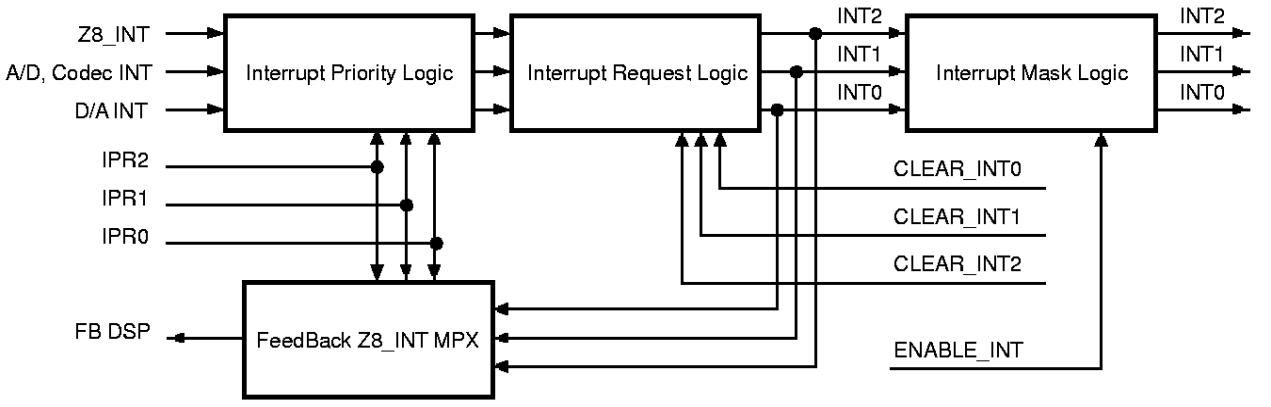


Figure 49. DSP Interrupts

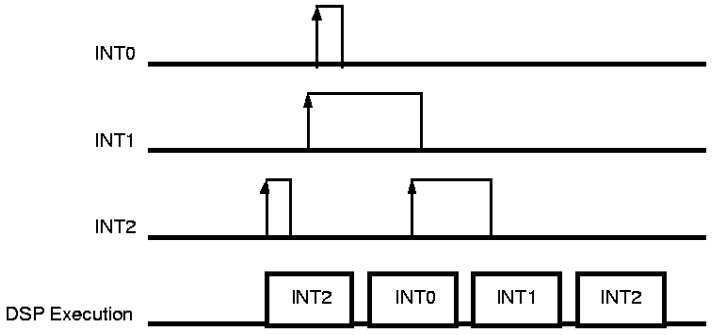


Figure 50. DSP Interrupt Priority Structure

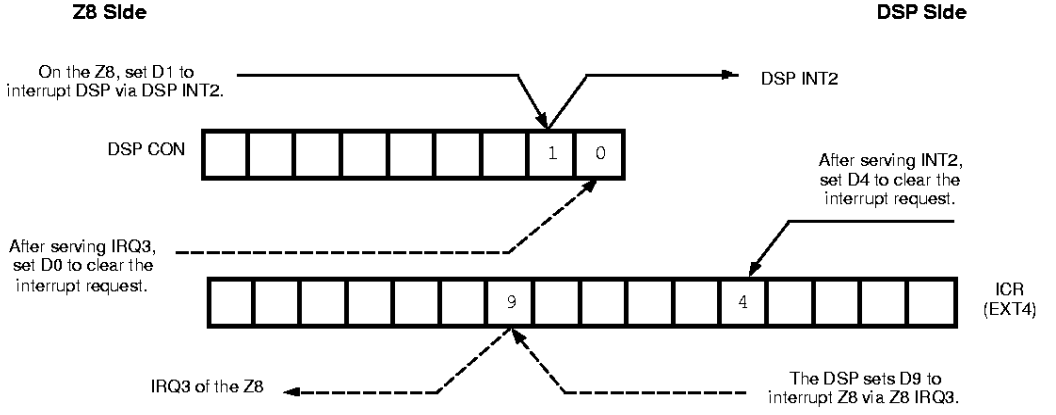


Figure 51. Interprocessor Interrupts Structure

DSP REGISTERS DESCRIPTION (Continued)

Table 18. EXT4 DSP Interrupt Control Register (ICR) Definition

Field	Position	Attrib	Value	Label
DSP_IRQ2	f---------------	R	1	Set_IRQ2
			0	Reset_IRQ2
	f---------------	W		No effect
DSP_IRQ1	-e--------------	R	1	Set_IRQ1
			0	Reset_IRQ1
	-e--------------	W		No effect
DSP_IRQ0	--d-------------	R	1	Set_IRQ0
			0	Reset_IRQ0
	--d-------------	W		No effect
DSP_MaskINT2	---c------------	R/W	1	Enable_INT2
			0	Disable_INT2
DSP_MaskINT1	----b-----------	R/W	1	Enable_INT1
			0	Disable_INT1
DSP_MaskINT0	-----a----------	R/W	1	Enable_INT0
			0	Disable_INT0
Z8_IRQ3	------9---------	R		Return "0"
	------9---------	W	1	Set_Z8_IRQ3
			0	Reset_Z8_IRQ3
DSPintEnable	-------8--------	R/W	1	Enable
			0	Disable
DSP_IPR2	--------7-------	R/W	Binary	IPR2
DSP_IPR1	---------6------	R/W	Binary	IPR1
DSP_IPR0	----------5-----	R/W	Binary	IPR0
Clear_IRQ2	-----------4----	R		Return "0"
	-----------4----	W	1	Clear_IRQ2
			0	Has_no_effect
Clear_IRQ1	------------3---	R		Return "0"
	------------3---	W	1	Clear_IRQ1
			0	No effect
Clear_IRQ0	-------------2--	R		Return "0"
	-------------2--	W	1	Clear_IRQ0
			0	No effect
Reserved	--------------10	W		No effect "0"
		R		

Interrupt Control Register (ICR). The ICR is mapped into EXT4 of the DSP (Table 18). The bits are defined as follows:

DSP_IRQ2 (Z8 Interrupt). This bit is read by both Z8 and DSP and is set only by writing to the Z8 expanded Register File (Bank F, ROC, bit 0). This bit asserts IRQ2 of the DSP and is cleared by writing to the Clear_IRQ2 bit.

DSP_IRQ1 (A/D, Codec Interrupt). This bit is read by the DSP only and is set when valid data is present at the A/D output and Codec input registers (conversion done). This bit asserts IRQ1 of the DSP and is cleared by writing to the Clear_IRQ1bit.

DSP_IRQ0 (D/A Interrupt). This bit is read by DSP only and is set by Timer3. This bit assists IRQ0 of the DSP and is cleared by writing to the Clear_IRQ0 bit.

DSP_MaskIntX. These bits are accessed by the DSP only. Writing a 1 to these locations allows the INT to be serviced, while writing a 0 masks off the corresponding INT.

Z8_IRQ3. This bit can be read by both the Z8 and the DSP but can only be set by the DSP. Addressing this location accesses bit D3 of the Z8 IRQ register, hence, this bit is not implemented in the ICR. During the interrupt service routine executed on the Z8 side, the User must reset the Z8_IRQ3 bit by writing a 1 to bit D0 of the DSPCON.

The hardware of the Z89195/196 automatically resets Z8_IRQ3 bit three instructions of the Z8 after 1 is written to its location in register bank 0F. This delay provides the timing synchronization between the Z8 and the DSP sides during interrupts. In summary, the interrupt service routine of the Z8 for IRQ3 should be finished by:

```
LD      ;       RP,#%0F
OR      ;       r12,#%01
POP     ;       RP
IRET    ;
```

DSP Enable_INT. Writing a 1 to this location enables global interrupts of the DSP while writing 0 disables them. A system Reset globally disables all interrupts.

DSP_IPRX. This three-bit group defines the Interrupt Selection logic as shown in Table 19.

Clear_IRQX. These bits are accessed by the DSP only. Writing a 1 to these locations resets the corresponding DSP_IRQX bits to 0. Clear_IRQX are virtual bits and are not implemented.

Table 19. DSP Interrupt Selection

DSP_IPR[2–0] 2 1 0	Z8_INT is switched to	A/D_INT is switched to	D/A_INT is switched to
0 0 0	INT2	INT1	INT0
0 0 1	INT1	INT2	INT0
0 1 0	INT2	INT0	INT1
0 1 1	INT1	INT0	INT2
1 0 0	INT0	INT2	INT1
1 0 1	INT0	INT1	INT2
1 1 0	Reserved	Reserved	Reserved
1 1 1	Reserved	Reserved	Reserved

DSP REGISTERS DESCRIPTION (Continued)

DSP Analog Data Registers

The D/A conversion is DSP driven by sending 10-bit data to the EXT5 of the DSP. The six remaining bits of EXT5 are not used (Figure 52).

A/D supplies 8-bit data to the DSP through the register EXT5 of the DSP. From the 16 bits of EXT5, only bits 2 through 9 are used by the A/D (Figure 53). Bits 0 and 1 are padded with zeroes. If the Codec Interface is enabled, DSP should write outgoing 8-bit data to EXT5 with bit 15 at logic 1. DSP reads incoming 8-bit data from EXT5, in sequence with A/D data (Figure 54).

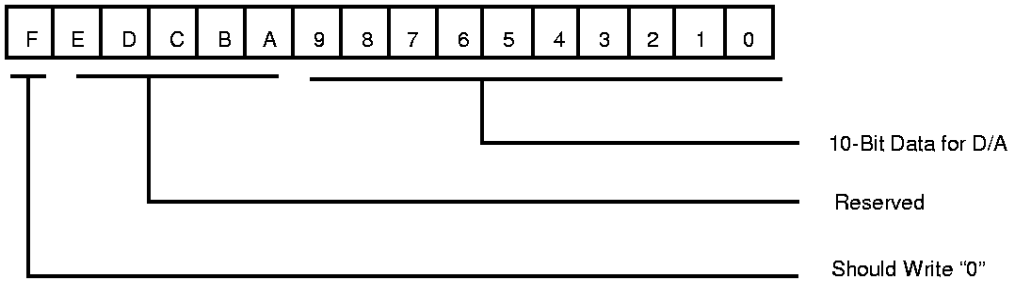


Figure 52. EXT5 Register D/A Mode Definition (Write Only)

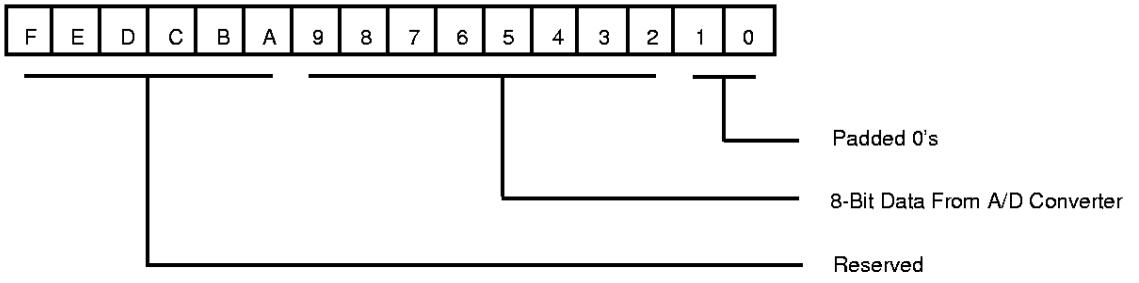


Figure 53. EXT5 Register A/D Mode Definition (Read Only)

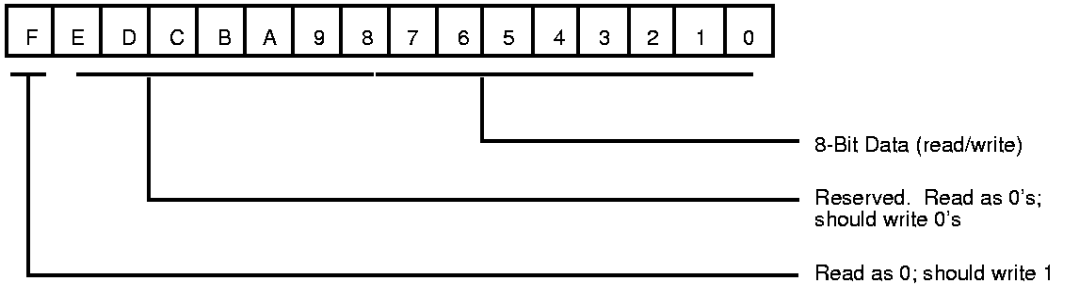


Figure 54. EXT5 Register Codec Interface Mode Definition

Analog Control Register (ACR). The Analog Control register is mapped to register EXT6 of the DSP (Table 20). This read/write register is accessible by the DSP only.

The 16-bit field of EXT6 defines modes of the D/A, A/D and Codec Interface.

Table 20. EXT6 Analog Control Register (ACR)

Field	Position	Attrib	Value	Label	20.48 MHz	14.7456 MHz*
DSP_INT0	f---------------	R/W	1	P26		
			0	Timer3		
Reset_Toggle	-e--------------	R		Return "0"		
		W	1	Reset Toggle		
			0	No effect		
Select_Sequence	--dc------------	R/W	xx	Enable A/D, Codec, Table 21; select reading		
Reserved	----ba----------	R		Return "0"		
		W		No effect		
Reserved	------9---------	R		Return "1"		
		W		No effect		
D/A_SamplingRate	-------8--------	R/W	0		16 kHz	8.04 kHz
			1		10 kHz	9.6 kHz
DSP_port (DSP1, DSP0)	--------76------	R/W		User-defined DSP outputs		
ConversionDone	----------4----	W		No effect		
		R	1	Done		
			0	Not Done		
Reserved	------------32--	R		Return "0"		
		W		No effect		
20/15 MHz Select	--------------1-	R/W	1	14.7456 MHz*		
			0	20.48 MHz†		
A/D, Codec_Sampling Rate	---------------0	R/W	1		16 kHz	16 kHz
			0		8 kHz	9.6 kHz

Notes:
* Default value
† Optional feature

DSP REGISTERS DESCRIPTION (Continued)

DSP INT0. This bit defines the source of the DSP INT0 interrupt.

Reset_Toggle. A "1" should be written to bit 'e' in order to reset the sequence. Writing 1 to bit 'e' ensures the next data read from EXT5 is the data of A/D.

Select_Sequence. Defines the A/D and Codec enabling/disabling and the sequence of reading data from these devices starting from the reset condition (Table 21).

Table 21. Select Sequence

Select Sequence		Enable/Disable		Sequence	
d	c	A/D	Codec	First	Second
0	0	Disable	Disable	N/A	N/A
0	1	Enable	Disable	A/D	N/A
1	0	Enable	Enable	A/D	Codec
1	1	Disable	Disable	N/A	N/A

D/A_Sampling Rate. This field defines the sampling rate of the D/A output. It changes the period of Timer3 interrupt and the maximum possible accuracy of the D/A Sampling Rate. (Table 22)

Table 22. D/A Data Accuracy

D/A_Sampling Rate	Sampling Rate	
Bit 8	20.48 MHz	14.7456 MHz
0	16 kHz	8.04 kHz
1	10 kHz	9.6 kHz

DSP0. DSP0 is a general-purpose output pin connected to Bit 6. This bit has no special significance and can be used to output data by writing to bit 6.

DSP1. DSP1 is a general-purpose output pin connected to Bit 7. This bit has no special significance and can be used to output data by writing to bit 7.

Conversion Done. This Read-Only flag indicates that the A/D conversion is complete. Upon reading EXT5 (A/D data), the Conversion Done flag is cleared.

A/D, Codec_Sampling Rate. This field defines the sampling rate of the A/D and Codec Interface. It changes the period of Timer2 interrupt (Table 23).

Table 23. A/D Sampling Rate

A/D_Sampling Rate	Sampling Rate	
Bit 0	20.48 MHz	14.7456 MHz
1	16 kHz	16 kHz
0	8 kHz	9.6 kHz

DSP TIMERS

Timer2 is a free running counter that divides the System Clock frequency to support different sampling rates for the A/D converter and Codec Interface. The sampling rate is defined by the Analog Control Register. Upon reaching the end of a count, the timer starts an A/D conversion and Codec data transfer. At completion, an interrupt is generated to the DSP.

Analogous to Timer2, Timer3 generates the different sampling rates for the D/A converter. Timer3 also generates an interrupt request to the DSP upon reaching its final count value (Figure 55).

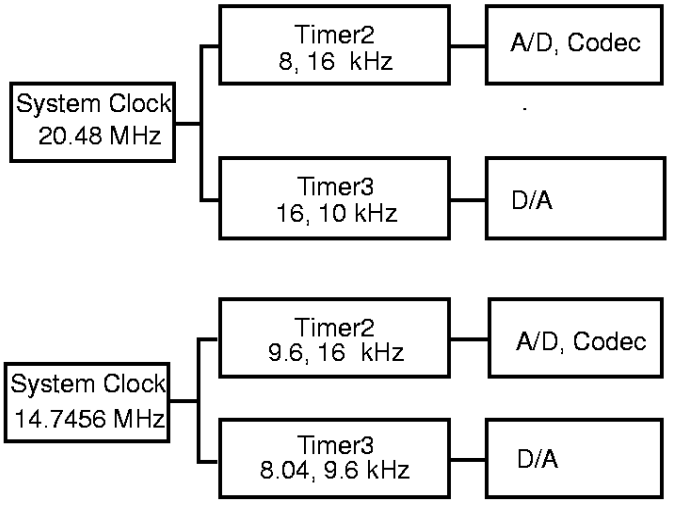


Figure 55. Timer2 and Timer3

Pulse Width Modulator (PWM)

The PWM supports different sampling rates according to the settings of bit 8 of the ACR and the System Clock frequency. The output of the PWM can be assigned to logic 1 only during the active region (which is 4/5 of the output signal period). The output will be at logic 0 for the rest of the time. An exception occurs in 10 kHz PWM, where the active region covers the whole output signal period (Figure 56). The active region is divided into 1024 time slots. In each of these time slots, the output can be set to logic 1 or logic 0.

In order to increase the effective sampling rate, the PWM employs a special technique of distributing the "logic 1" period over the active region.

The 10-bit PWM data is divided into two parts: the upper five bits (High_Val) and the lower five bits (Low_Val). The 1024 time slots in the active region are divided into 32 equal groups, with 32 time slots in each group. The first slot of each of the 32 groups represents Low_Val, while High_Val is represented by the remaining 31 time slots in each group.

For example, a value of %13a is loaded into PWM data register EXT 5:

%13a = 01 0011 1010B = 314

High_Val = 01001B = 9

Low_Val = 11010B = 26

26 out of 32 groups will then have their first slots set to logic 1. The remaining one slot in each group has nine time slots set to logic 1.

For 10 kHz PWM, the effective output frequency is 10K x 32 = 320 kHz. Figure 57 illustrates the waveform by using a 6-bit PWM data (3-bit High_Val and 3-bit Low_Val).

DSP TIMERS (Continued)

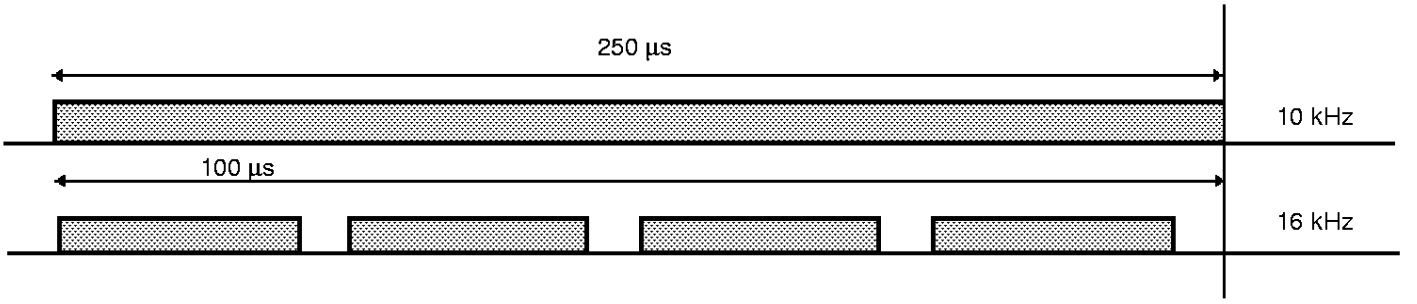


Figure 56. PWM Waveform (shaded area shows the active region)

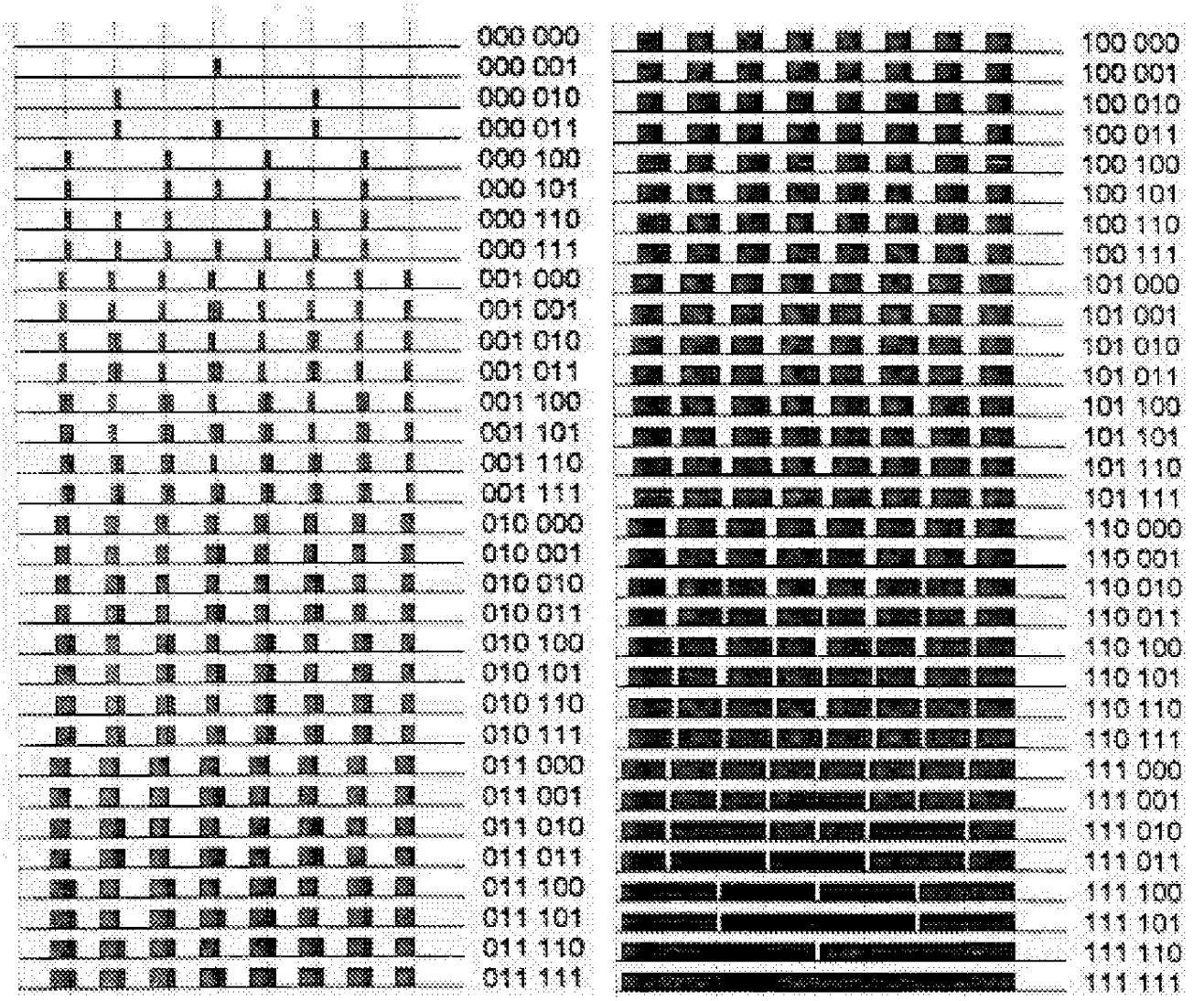


Figure 57. PWM Waveform of the Active Region (for a 6-bit PWM data)

A/D CONVERTER (ADC)

Analog to Digital Converter

The A/D converter is an 8-bit half flash converter which uses two reference resistor ladders for its upper four bits (MSBs) and lower four bits (LSBs) conversion (Figure 58). Two reference voltage pins, VREF+ (High) and VREF– (Low), are provided for external reference voltage supplies. During the sampling period, the converter is auto-zeroed before starting the conversion time depending on the System Clock frequency and the selection of the A/D sampling rate (Figure 59). The sampling rates are 10 or 16 kHz (System Clock = 20.48 MHz) in order to provide oversampling. The rates are software controlled by the ACR (DSP EXT6 Register). Timer2 supports the ADC. The maximum conversion time is 2 µs.

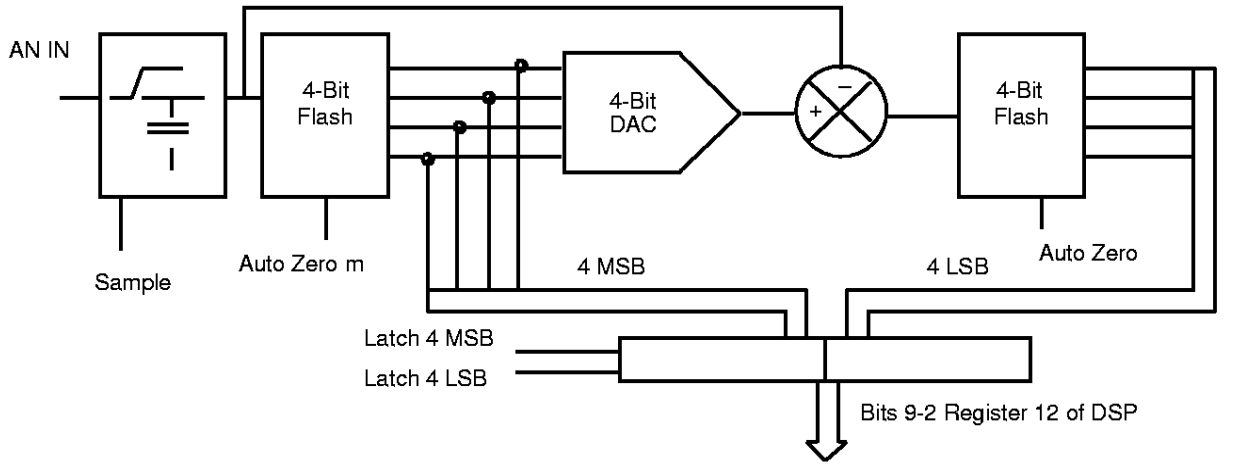


Figure 58. A/D Converter

To begin conversion, enable the A/D by writing to the appropriate bit in the Analog Control Register (ACR).

The ADC can be disabled for low power consumption when not in use.

Though the ADC functions for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time can also take slightly longer due to smaller input signals.

A/D CONVERTER (ADC) (Continued)

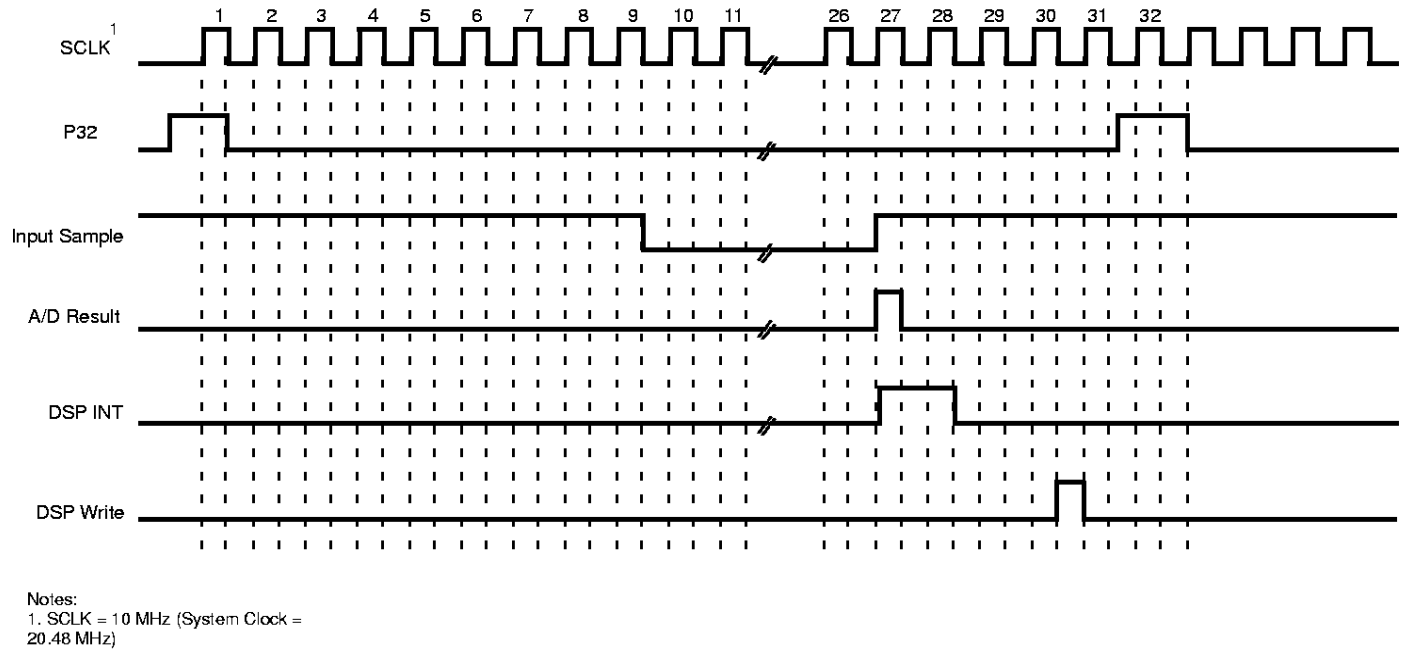


Figure 59. ADC Timing Diagram

Figure 60 shows the input circuit of the ADC. When conversion starts, the analog input voltage from the input is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Shunting 31 parallel internal resistances of the analog switches and simultaneously charging 31 parallel 1 pF capacitors is equivalent to a 400 Ohms input impedance in parallel with a 31 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. Input source resistances up to 2 Kohms can be used under normal operating conditions without any degradation of the input settling time. For larger input source resistance, longer conversion cycle times can be required to compensate the input settling time problem. V_{REF} is set using the V_{REF} + pin.

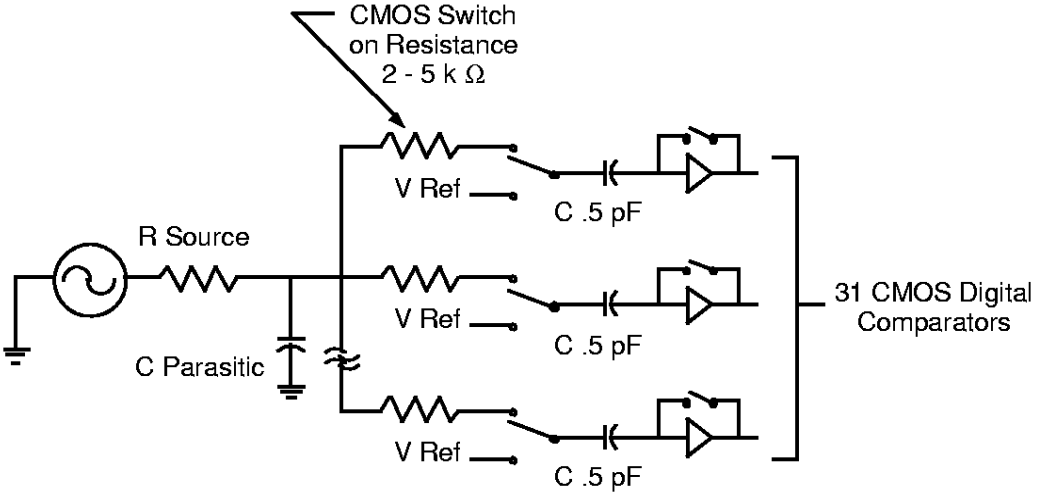


Figure 60. Input Impedance of ADC

CODEC INTERFACE (CODEC)

The single-channel Codec Interface must be enabled together with the A/D Converter. They share the same sampling rate. Each time an A/D conversion takes place, the Codec Interface performs an 8-bit data in, 8-bit data out iteration. A single interrupt prompts the DSP to service both of these functions. Refer to the Analog Control Register description on writing and reading for these blocks. Timing for the Codec Interface channel is shown in Figure 61.

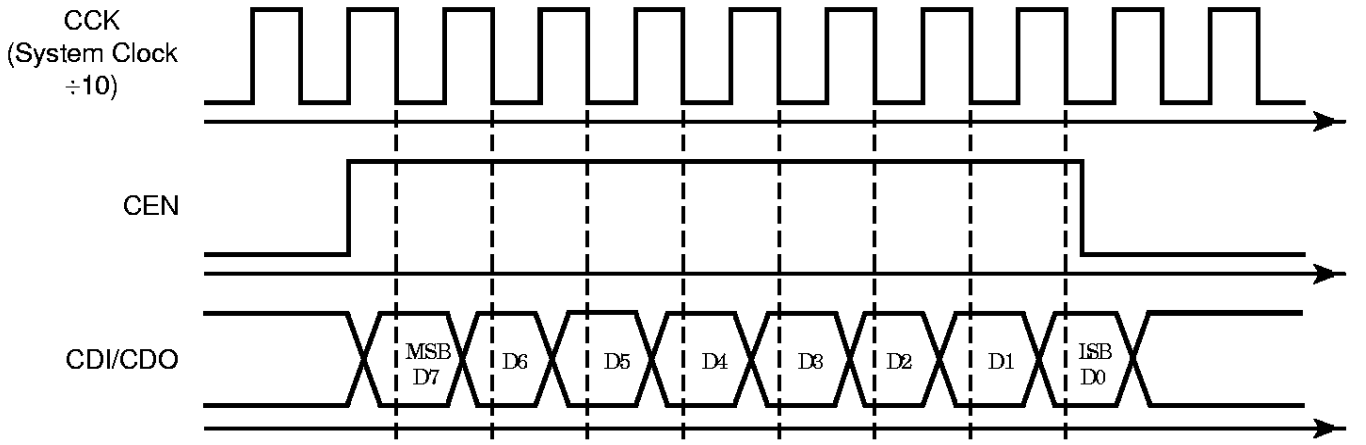


Figure 61. Codec Interface Timing

Z8 EXPANDED REGISTER FILE REGISTERS

Expanded Register Bank A

PLL Control Register (PLL) Address: (A) 08 Read/Write

D7	D6	D5	D4	D3	D2	D1	D0

Stop VCO
0: VCO Running
1: VCO Stopped

Bypass to Crystal Clock.
0: VCO Clock source
1: bypass to crystal clock

Bypass to Input Clock CKIN.
0: VCO clock source
1: bypass to CKIN

VCO (System) Clock Frequency Selection
0: 14.7456 MHz
1: 20.48MHH

Reserved. Read as 0's.

Should write with 0's.

If both D2 and D1 are programmed 1's, bypass is to crystal clock.

Figure 62. PLL Control Register

SIO (A) 07
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
u	u	u	u	u	u	u	u

← Reset Value

If UART is enabled, Z8 reads received data bytes from this register. Z8 also writes data bytes to be transmitted to this same register. See UART functional description for details.

If SCXVR is enabled, Z8 reads received data bytes from this register. Z8 also writes data bits to D0 of this register to be transmitted (should write D7–1 with zeros). See SCXVR functional description for details.

Figure 63. Serial I/O Register

(A) 06

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Figure 64. Reserved

(A) 05

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Figure 65. Reserved

ARAM Control Register (ARCR)
Address: (A) 04
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Reset Value

D7: ARAM Controller Enable.
0: disable 1: enable.

D6–5: This field defines the type of ARAM chip(s) being used.
00: 256Kx16
01: 1Mx16
10: 4Mx4
11: 4Mx4, 3 chips

D4: Number of ARAM chips being used.
0: 1 chip 1: 2 chips
D4 is don't care if D7–6 are programmed 1's.

D3: ARAM Access Speed (Z8 at 10.24 MHz).
0: 200ns 1: 100ns

D2: Address Auto-Increment
0: disable 1: enable

D1–0: This field enables and defines the number of back-to-back refresh cycles to be issued every 30.52µs.
00: refresh disabled
01: 1 refresh cycle
02: 2 back-to-back refresh cycle
03: 4 back-to-back refresh cycle

Figure 66. ARAM Control Register

ARAM Address Low Register (ARAL)
Address: (A) 03
(Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Reset Value

Figure 67. ARAM Address Low Register

ARAM Address Mid Register (ARAM)
Address: (A) 02
(Read/Write)

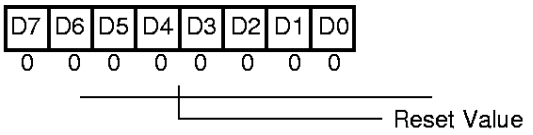


Figure 68. ARAM Address Mid Register

ARAM High Register (ARAH)
Address: (A) 01
(Read/Write)

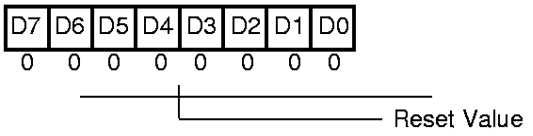


Figure 69. ARAM High Register

ARAM Data Register (ARDR)
Address: (A) 00
(Read/Write)

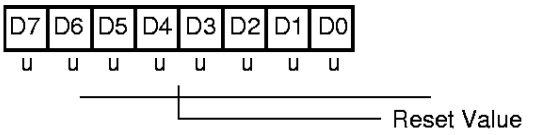


Figure 70. ARAM Data Register

Z8 EXPANDED REGISTER FILE REGISTERS (Continued)

Expanded Register Bank B

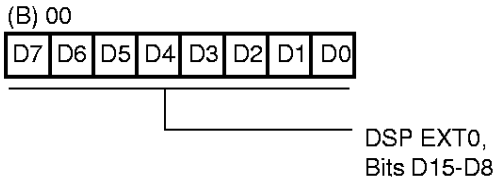


Figure 71. Outgoing Register to DSP EXT0 (High Byte) (B) 00H [Read/Write]

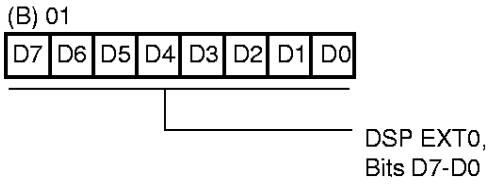


Figure 72. Outgoing Register to DSP EXT0 (Low Byte) (B) 01H [Read/Write]

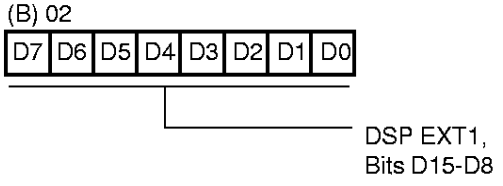


Figure 73. Outgoing Register to DSP EXT1 (High Byte) (B) 02H [Read/Write]

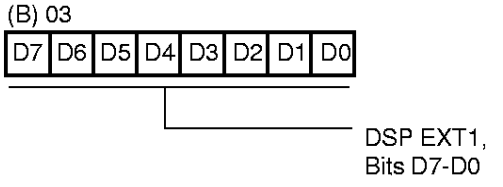


Figure 74. Outgoing Register to DSP EXT1 (Low Byte) (B) 03H [Read/Write]

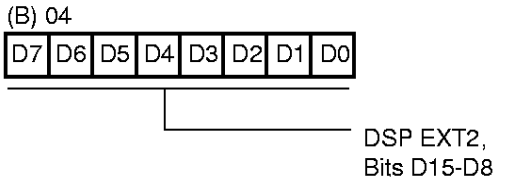


Figure 75. Outgoing Register to DSP EXT2 (High Byte) (B) 04H [Read/Write]

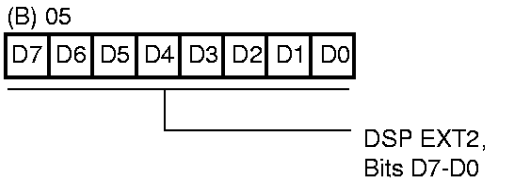


Figure 76. Outgoing Register to DSP EXT2 (Low Byte) (B) 05H [Read/Write]

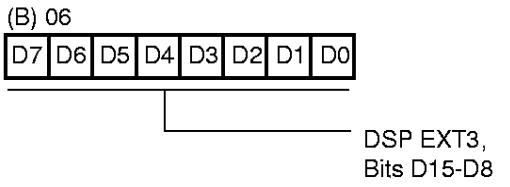


Figure 77. Outgoing Register to DSP EXT3 (High Byte) (B) 06H [Read/Write]

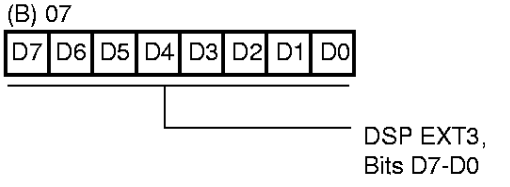


Figure 78. Outgoing Register to DSP EXT3 (Low Byte) (B) 07H [Read/Write]

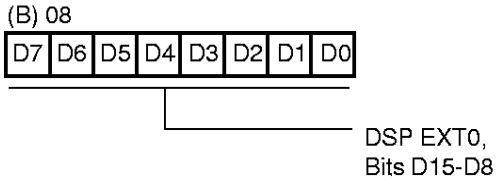


Figure 79. Incoming Register from DSP EXT0 (High Byte) (B) 08H [Read-Only]

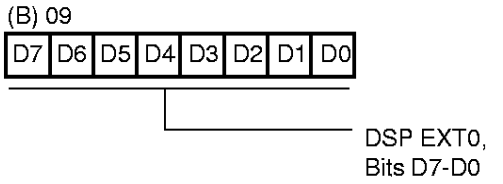


Figure 80. Incoming Register from DSP EXT0 (Low Byte) (B) 09H [Read-Only]

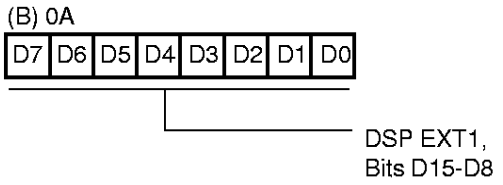


Figure 81. Incoming Register from DSP EXT1 (High Byte) (B) 0AH [Read-Only]

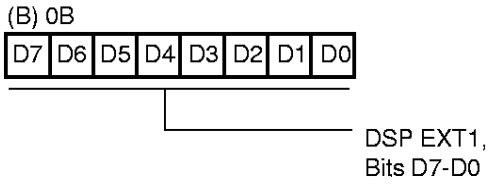


Figure 82. Incoming Register from DSP EXT1 (Low Byte) (B) 0BH [Read-Only]

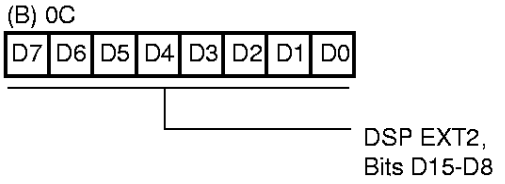


Figure 83. Incoming Register from DSP EXT2 (High Byte) (B) 0CH [Read-Only]

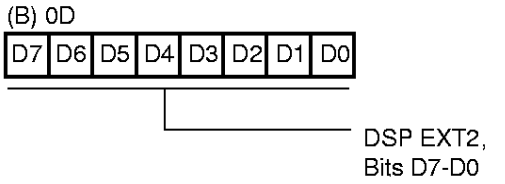


Figure 84. Incoming Register from DSP EXT2 (Low Byte) (B) 0DH [Read-Only]

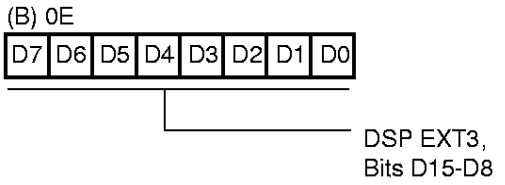


Figure 85. Incoming Register from DSP EXT3 (High Byte) (B) 0EH [Read-Only]

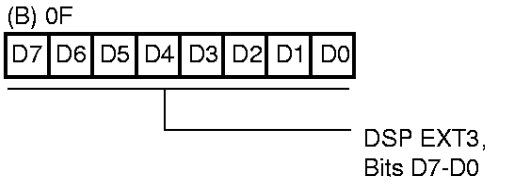


Figure 86. Incoming Register from DSP EXT3 (Low Byte) (B) 0FH [Read-Only]

Z8 EXPANDED REGISTER FILE REGISTERS (Continued)

Expanded Register Bank F

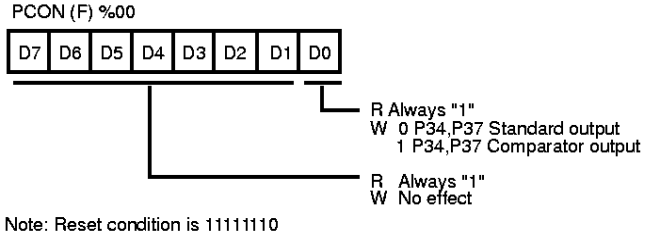


Figure 87. Port Configuration Register (PCON) (F) 00H [Write-Only]

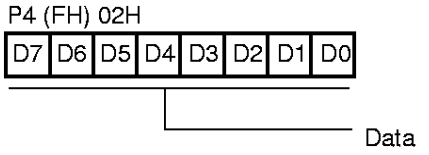


Figure 88. Port 4 Data Register (F) 02H [Read/Write]

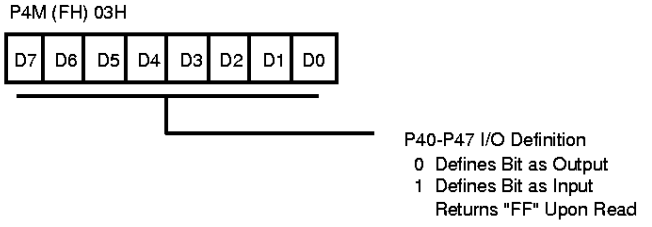


Figure 89. Port 4 Mode Register (F) 03H [Write-Only]

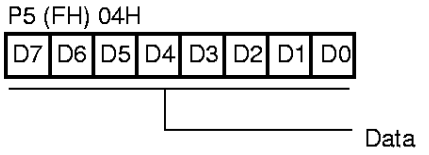


Figure 90. Port 5 Data Register (F) 04H [Read/Write]

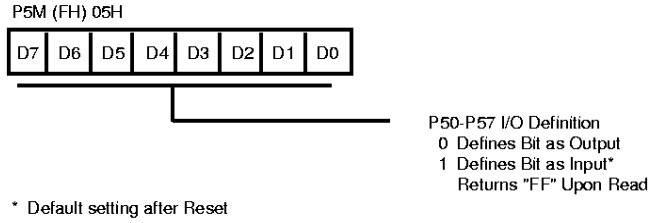


Figure 91. Port 5 Mode Register (F) 05H [Write-Only]

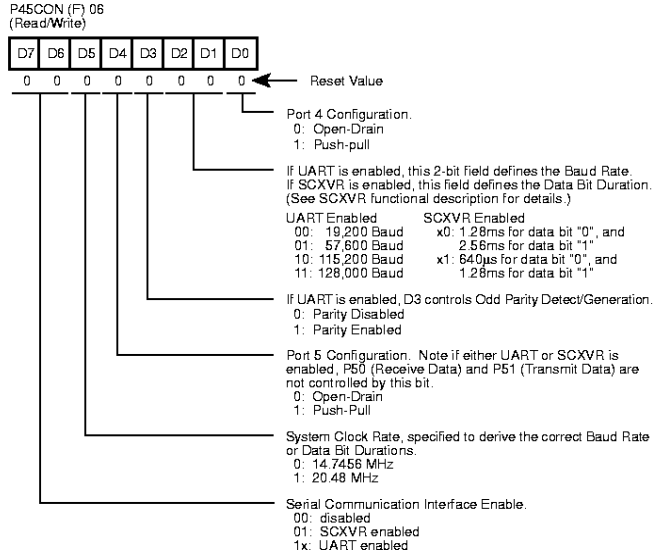


Figure 92. Port 4 and 5 Configuration Register (F) 06H [Write-Only]

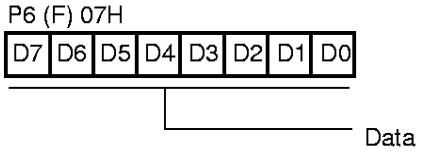


Figure 93. Port 6 Data Register (F) 07H [Read/Write]

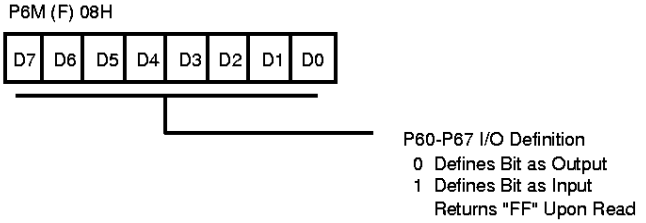


Figure 94. Port 6 Mode Register (F) 08H [Write-Only]

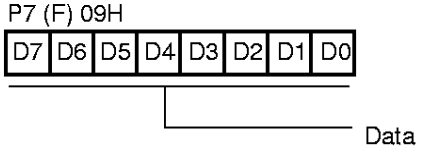


Figure 95. Port 7 Data Register (F) 09H [Read/Write]

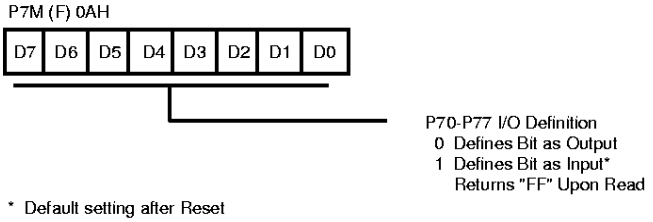


Figure 96. Port 7 Mode Register (F) 0AH [Write-Only]

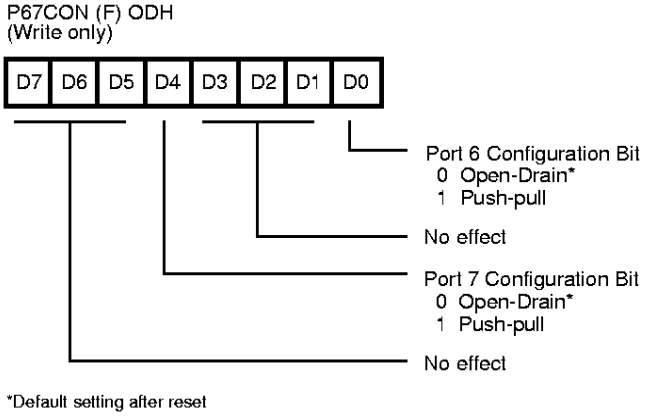


Figure 97. Port 6 and 7 Configuration Register (F) 0DH [Write-Only]

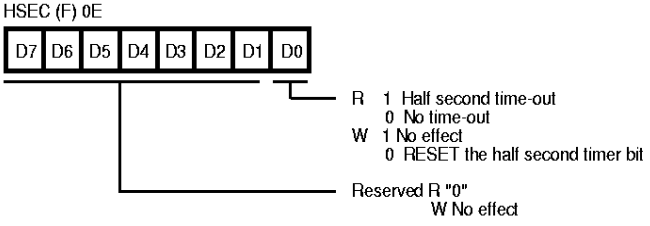


Figure 98. Half-Second Timer Status Register

Z8 EXPANDED REGISTER FILE REGISTERS (Continued)

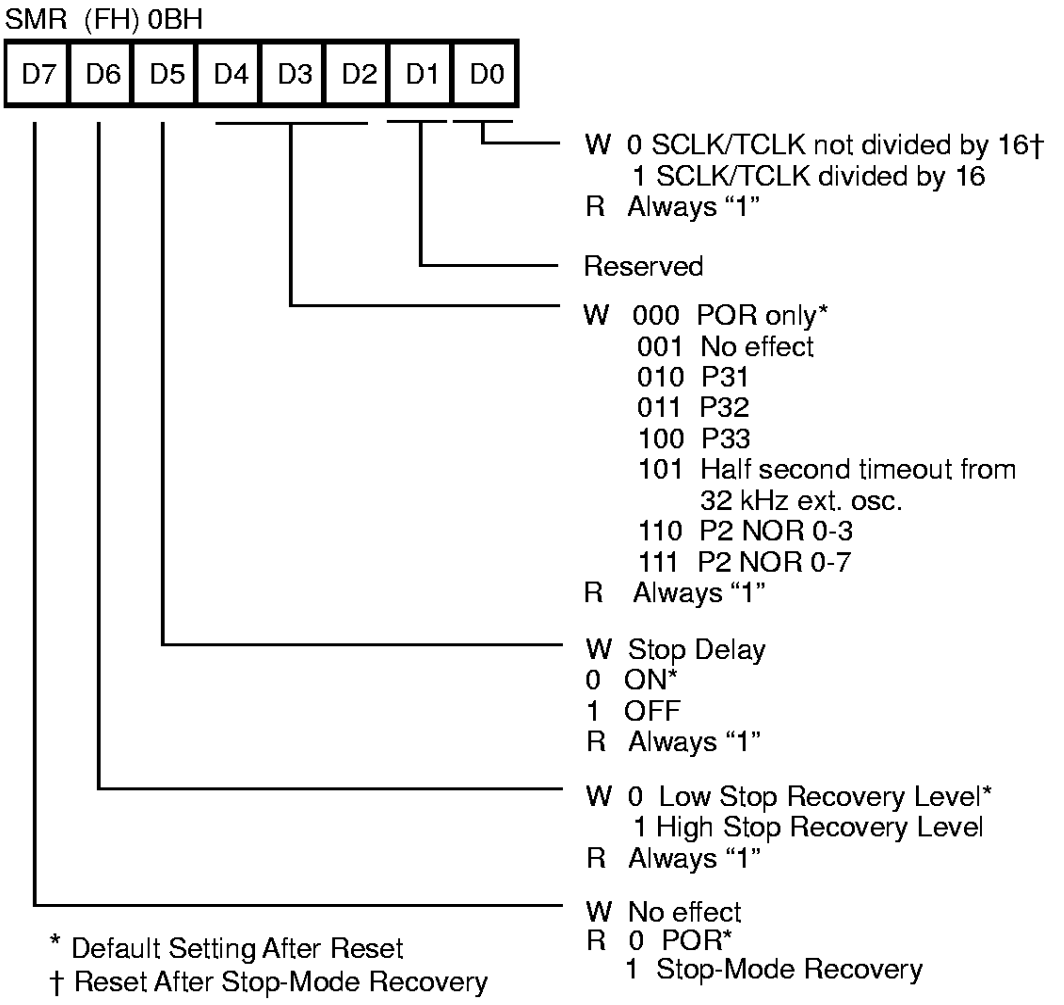


Figure 99. Stop-Mode Recovery Register (SMR)
(F) 0BH [Read/Write]

Table 24. DSP Control Register (F) 0CH [Read/Write]

Field DSPCON (F) 0CH	Position	Attributes	Value	Label
Z8_SCLK	76------	R/W	00	OSC/8
			01	OSC/4
			1x	OSC/2
DSP_Reset	--5-----	R		Return "0"
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--		xx	
				Return "0"
				No effect
IntFeedback	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect

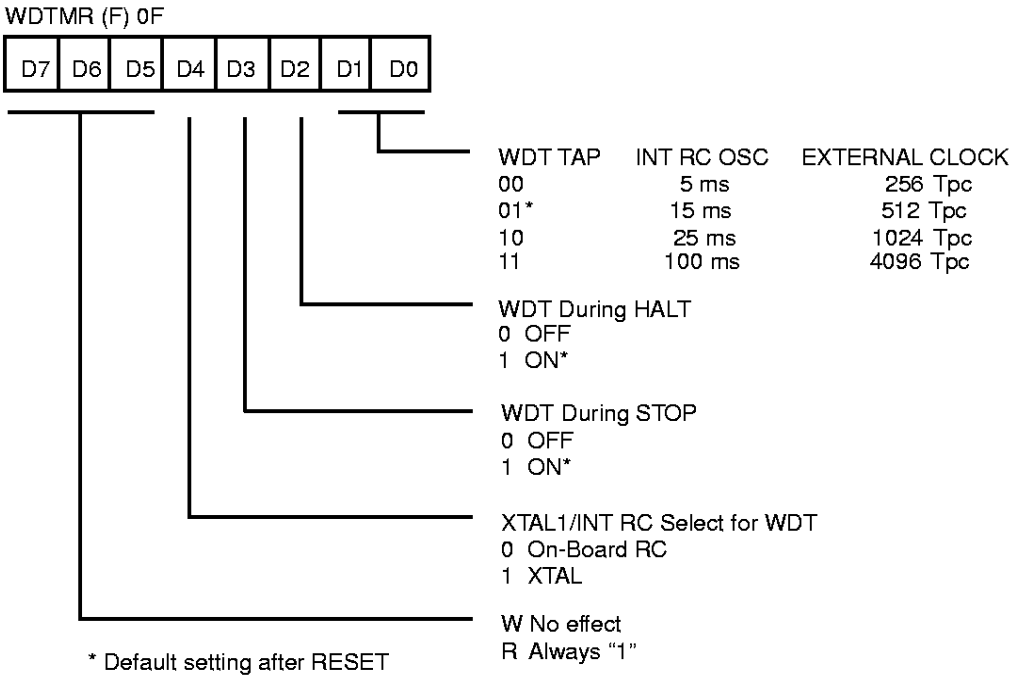


Figure 100. Watch-Dog Timer Mode Register (F) 0FH [Read/Write]

Z8 CONTROL REGISTERS

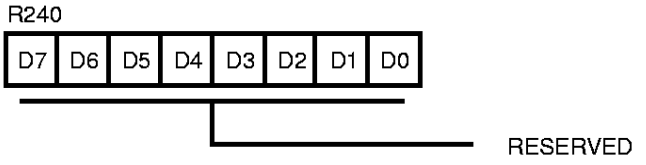


Figure 101. Reserved (F0H)

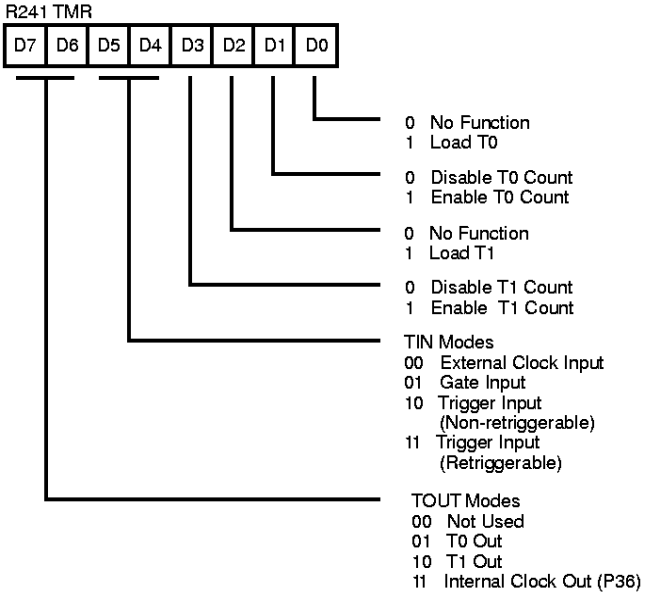


Figure 102. Timer Mode Register (F1H: Read/Write)

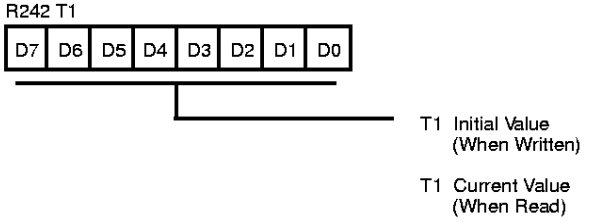


Figure 103. Counter/Timer 1 Register (F2H: Read/Write)

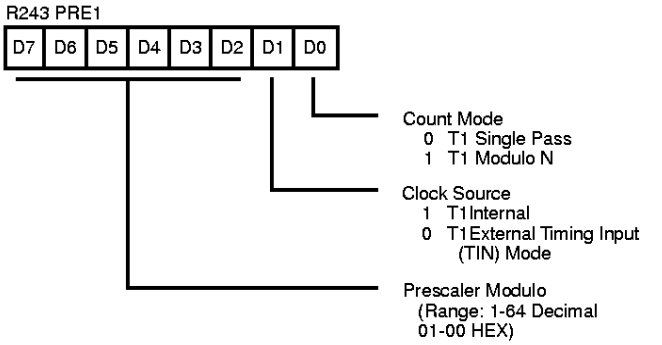


Figure 104. Prescaler 1 Register (F3H: Write-Only)

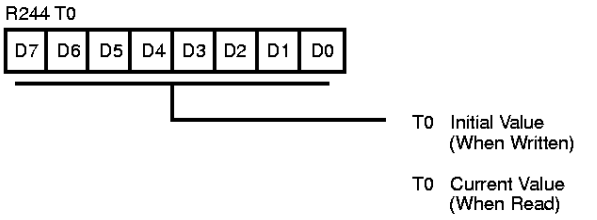


Figure 105. Counter/Timer 0 Register (F4H: Read/Write)

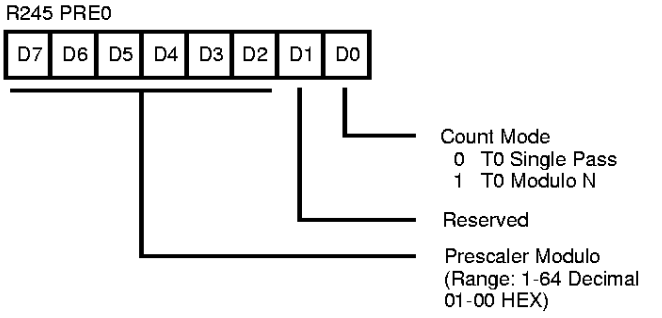


Figure 106. Prescaler 0 Register (F5H: Write-Only)

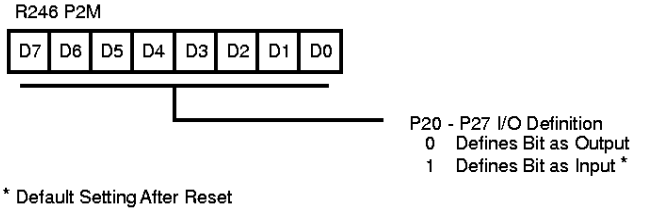


Figure 107. Port 2 Mode Register (F6H: Write-Only)

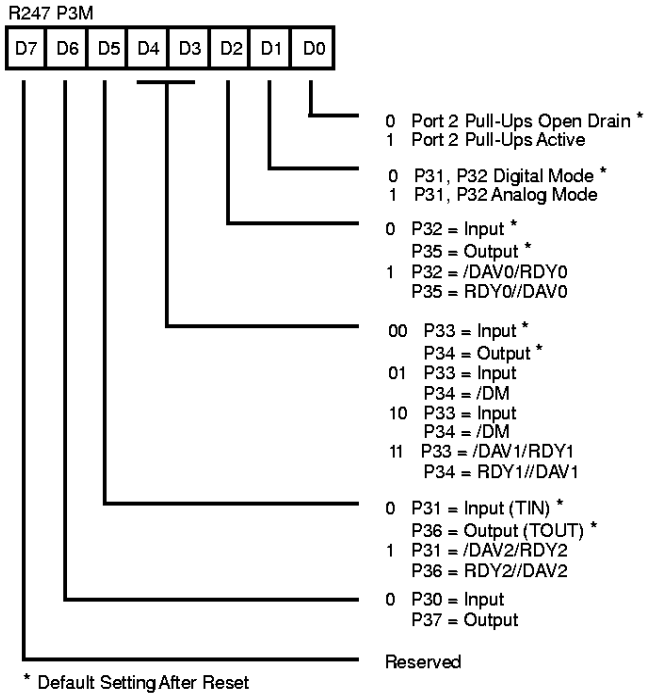


Figure 108. Port 3 Mode Register (F7H: Write-Only)

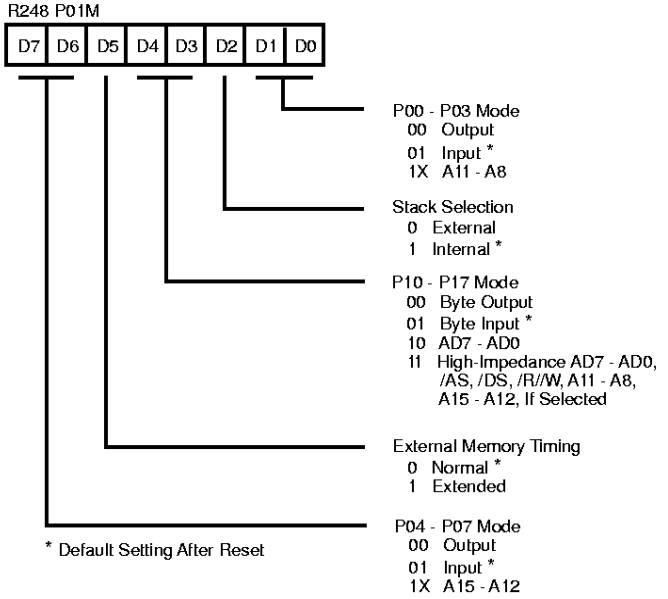


Figure 109. Port 0 Mode Register (F8H: Write-Only)

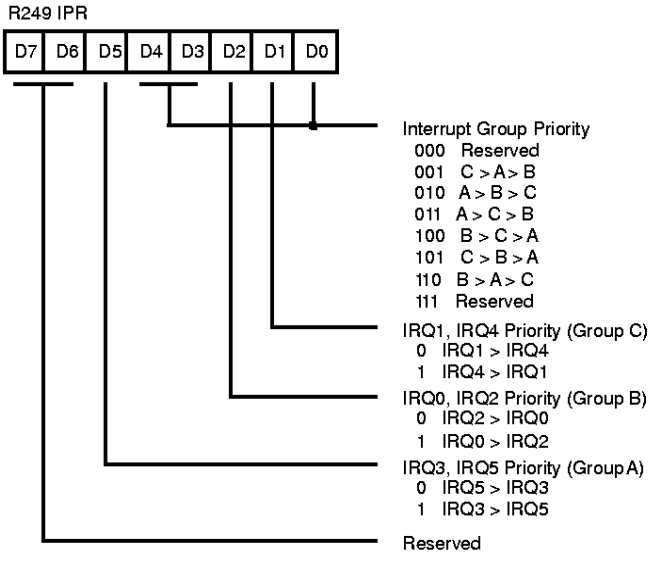


Figure 110. Interrupt Priority Register (F9H: Write-Only)

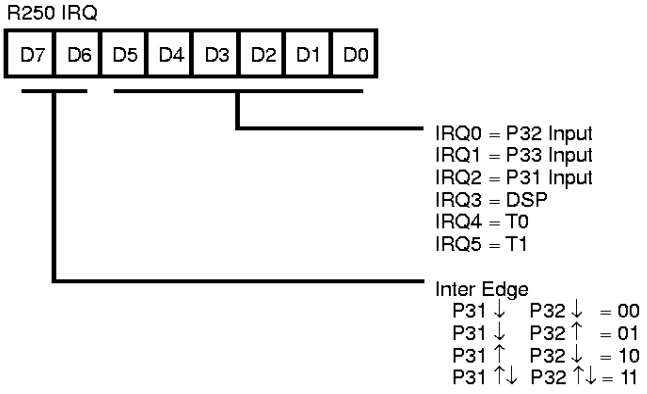


Figure 111. Interrupt Request Register (FAH: Read/Write)

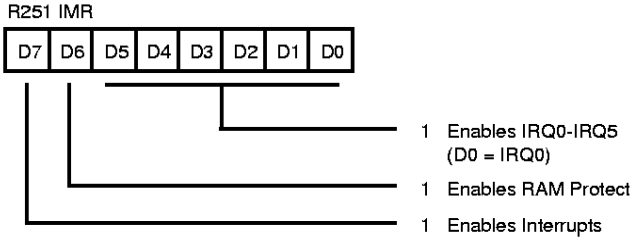


Figure 112. Interrupt Mask Register (FBH: Read/Write)

Z8 CONTROL REGISTERS (Continued)

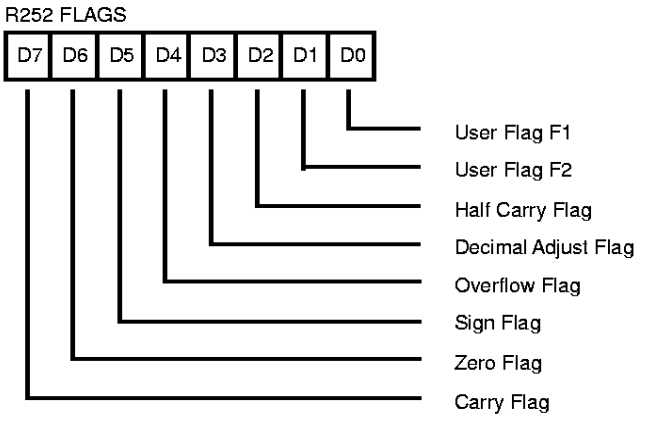


Figure 113. Flag Register (FCH: Read/Write)

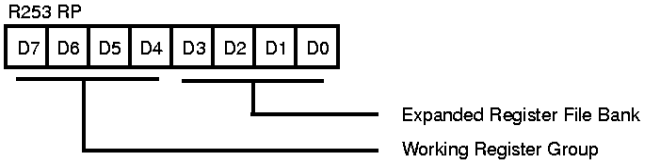


Figure 114. Register Pointer (FDH: Read/Write)

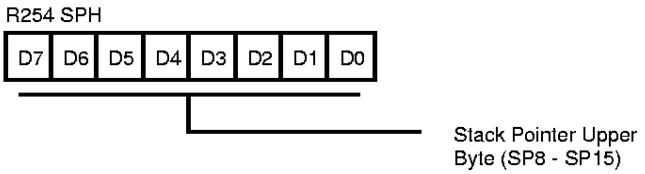


Figure 115. Stack Pointer High (FEH: Read/Write)

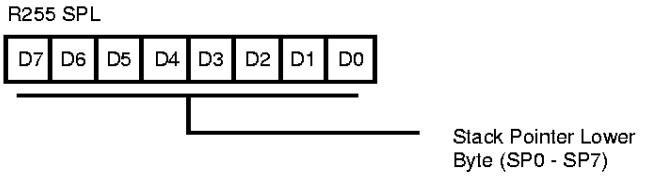


Figure 116. Stack Pointer Low (FFH: Read/Write)

PACKAGE INFORMATION

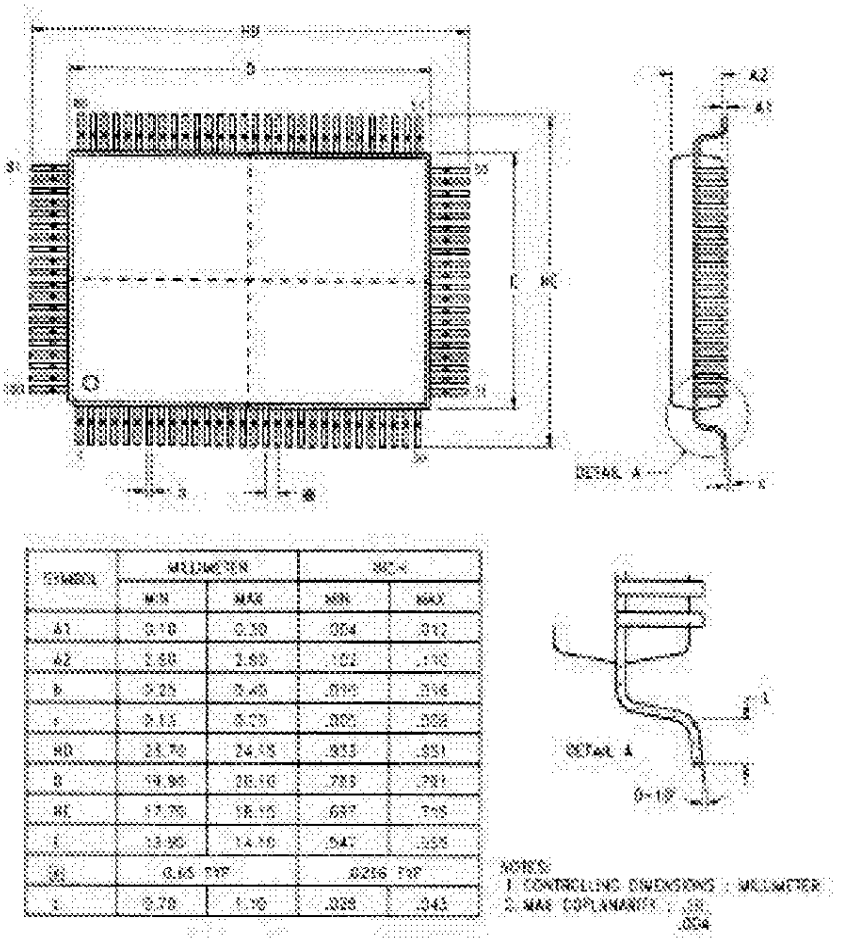
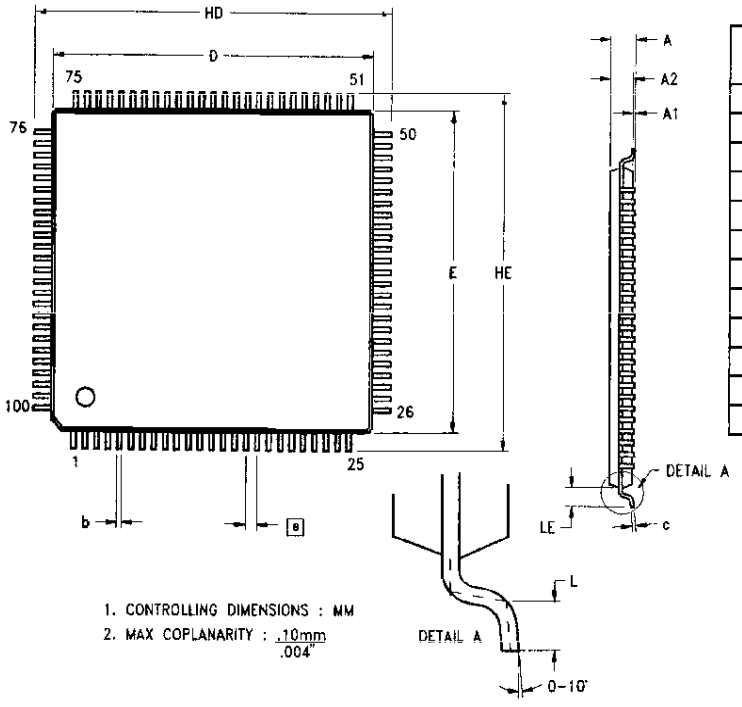


Figure 117. 100-Pin QFP Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

Figure 118. 100-Pin VQFP Package Diagram