SYNCHRONOUS DRAM MODULE

MT4LSDT1632U – 64MB
MT8LSDT1632U – 64MB
MT8LSDT3232U – 128MB
MT8LSDT6432U – 256MB

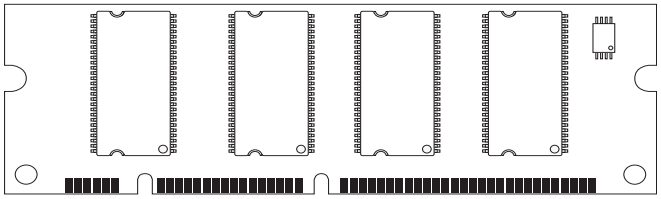
For the latest data sheet, please refer to the Micron® Web site: www.micron.com/products/modules

Features

- 100-pin, dual in-line memory module (DIMM)
- PC 100- and PC133-compliant
- 64MB (16 Meg x 32) , 128MB (32 Meg x 32), and 256MB (64 Meg x 32)
- Utilizes 125 MHz and 133 MHz SDRAM components
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
  64MB and 128 MB modules; 64ms, 4,096-cycle refresh (15.625µs refresh interval); 256MB modules; 64ms, 8,192-cycle refresh (7.81µs refresh interval)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

Figure 1: 100-Pin DIMM (MO-161)

Standard 1.15in. (29.21mm)



Options — Marking

- Frequency / CAS Latency — Y
  - 133 MHz (7.5ns) / CL = 3 — -75
  - 125 MHz (8ns) / CL = 3 — -8
  - 100 MHz (10ns) / CL = 2 — -10
- PCB
  Standard 1.15in. (29.21mm)

Table 1: Timing Parameters

CL = CAS (READ) latency

MODULE MARKING	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2	CL = 3		
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-8	125 MHz	6ns	6ns	2ns	1ns
-10	100 MHz	9ns	7.5ns	2ns	1ns

Table 2: Address Table

MODULE DENSITY	MT4LSDT1632U	MT8LSDT1632U	MT8LSDT3232U	MT8LSDT6432U
Refresh Count	4K	4K	4K	8K
Device Banks	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)
Device Configuration	128Mb (16 Meg x 8)	64Mb (8 Meg x 8)	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)
Device Row Addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)	8K (A0–A12)
Device Column Addressing	1K (A0–A9)	512 (A0–A8)	1K (A0–A9)	1K (A0–A9)
Module Ranks	1 (S0#, S2#)	2 (S0#, S2#; S1#, S3#)	2 (S0#, S2#; S1#, S3#)	2 (S0#, S2#; S1#, S3#)

Table 3: Part Numbers

PART NUMBER	MODULE DENSITY	CONFIGURATION	SYSTEM BUS SPEED
MT4LSDT1632UG-75__	64MB	16 Meg x 32	133 MHz
MT4LSDT1632UY-75__	64MB	16 Meg x 32	133 MHz
MT4LSDT1632UG-8__	64MB	16 Meg x 32	125 MHz
MT4LSDT1632UY-8__	64MB	16 Meg x 32	125 MHz
MT4LSDT1632UG-10__	64MB	16 Meg x 32	100 MHz
MT4LSDT1632UY-10__	64MB	16 Meg x 32	100 MHz
MT8LSDT1632UG-75__	64MB	16 Meg x 32	133 MHz
MT8LSDT1632UY-75__	64MB	16 Meg x 32	133 MHz
MT8LSDT1632UG-8__	64MB	16 Meg x 32	125 MHz
MT8LSDT1632UY-8__	64MB	16 Meg x 32	125 MHz
MT8LSDT1632UG-10__	64MB	16 Meg x 32	100 MHz
MT8LSDT1632UY-10__	64MB	16 Meg x 32	100 MHz
MT8LSDT3232UG-75__	128MB	32 Meg x 32	133 MHz
MT8LSDT3232UY-75__	128MB	32 Meg x 32	133 MHz
MT8LSDT3232UG-8__	128MB	32 Meg x 32	125 MHz
MT8LSDT3232UY-8__	128MB	32 Meg x 32	125 MHz
MT8LSDT3232UG-10__	128MB	32 Meg x 32	100 MHz
MT8LSDT3232UY-10__	128MB	32 Meg x 32	100 MHz
MT8LSDT6432UG-75__	256MB	64 Meg x 32	133 MHz
MT8LSDT6432UY-75__	256MB	64 Meg x 32	133 MHz
MT8LSDT6432UG-8__	256MB	64 Meg x 32	125 MHz
MT8LSDT6432UY-8__	256MB	64 Meg x 32	125 MHz
MT8LSDT6432UG-10__	256MB	64 Meg x 32	100 MHz
MT8LSDT6432UY-10__	256MB	64 Meg x 32	100 MHz

NOTE:

1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4LSDT1632UG-8B1.

Table 4: Pin Assignment Front (100-Pin DIMM)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
	VSS	13	A0	26	VSS	38	DQ16
2	DQ0	14	A2	27	CKE0	39	DQ17
3	DQ1	15	A4	28	WE#	40	DQ18
4	DQ2	16	A6	29	S0#	41	DQ19
5	DQ3	17	A8	30	S2#	42	VDD
6	VDD	18	A10	31	VDD	43	DQ20
7	DQ4	19	BA1	32	NC	44	DQ21
8	DQ5	20	A12/NC	33	NC	45	DQ22
9	DQ6	21	VDD	34	NC	46	DQ23
10	DQ7	22	NC	35	NC	47	VSS
11	DQMB0	23	RFU	36	VSS	48	SDA
12	VSS	24	RFU	37	DQMB2	49	SCL
		25	CK0			50	VDD

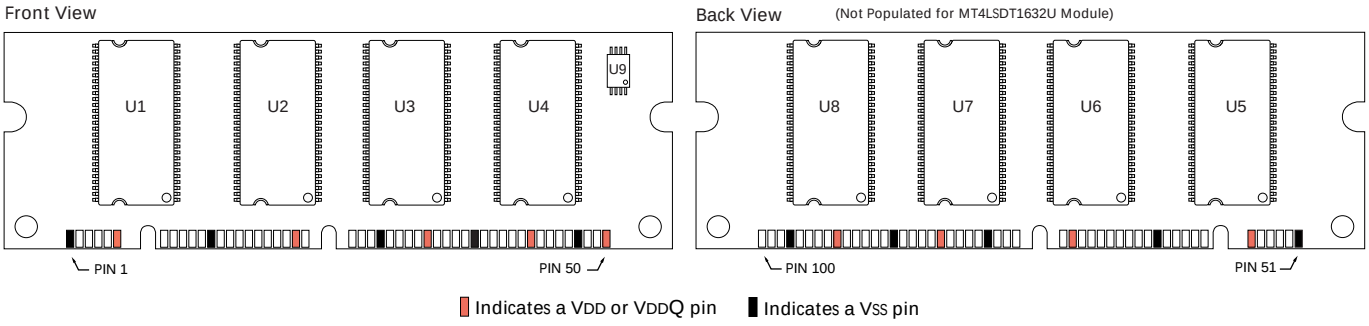
Table 5: Pin Assignment Back (100-Pin DIMM)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL

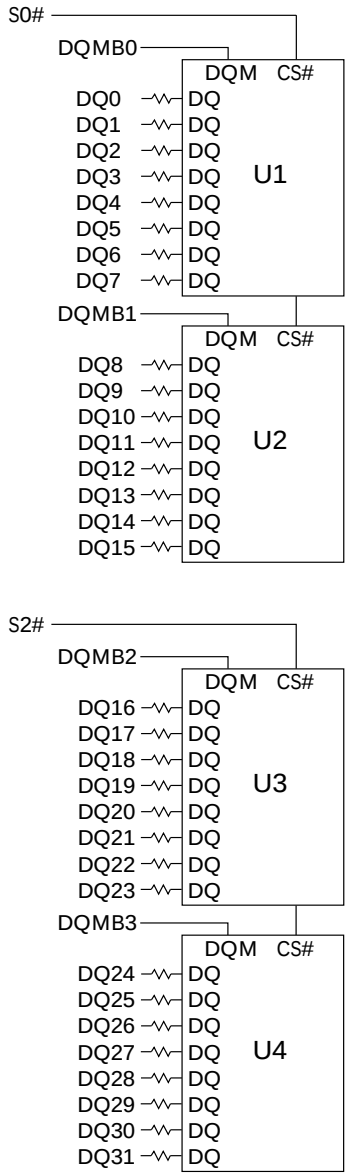
NOTE:

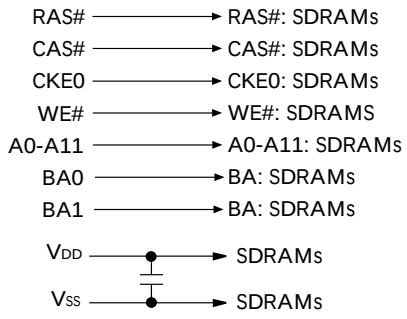
1. Pin 20 is A12 for 256MB module; for all others NC.

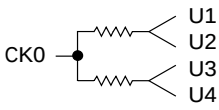
Pin Locations (100-Pin DIMM)

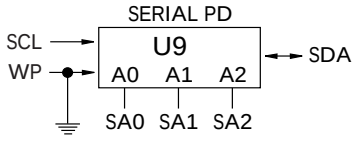


		Input	Command Inputs: RAS#, CAS# and WE# (along with S#) define the command being entered.
25, 75	CK0, CK1	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
27, 77	CKE0, CKE1	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
29, 30, 79, 80	S0#–S3#	Input	Chip Select: S# enables (registered LOW) or disables (registered HIGH) the the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
11, 37, 61, 87	DQMB0–DQMB3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
19, 68	BA0, BA1	Input	Device Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
13, 14, 15, 16, 17, 18, 20 (256MB), 63, 64, 65, 66, 67, 69	A0–A11 (64MB, 128MB) A0–A12 (256MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
2–5, 7–10, 38–41, 43–46, 52–55, 57–60, 88–91, 93–96	DQ0–DQ31	Input/ Output	Data I/Os: Data bus.
48	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 21, 31, 42, 50, 56, 71, 81, 92	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	V_{SS}	Supply	Ground.
23, 24, 74	RFU	–	Reserved for Future Use: These pins should be left unconnected.
20 (64MB, 128MB), 22, 32–35, 70, 78, 82–85	NC	–	Not connected.







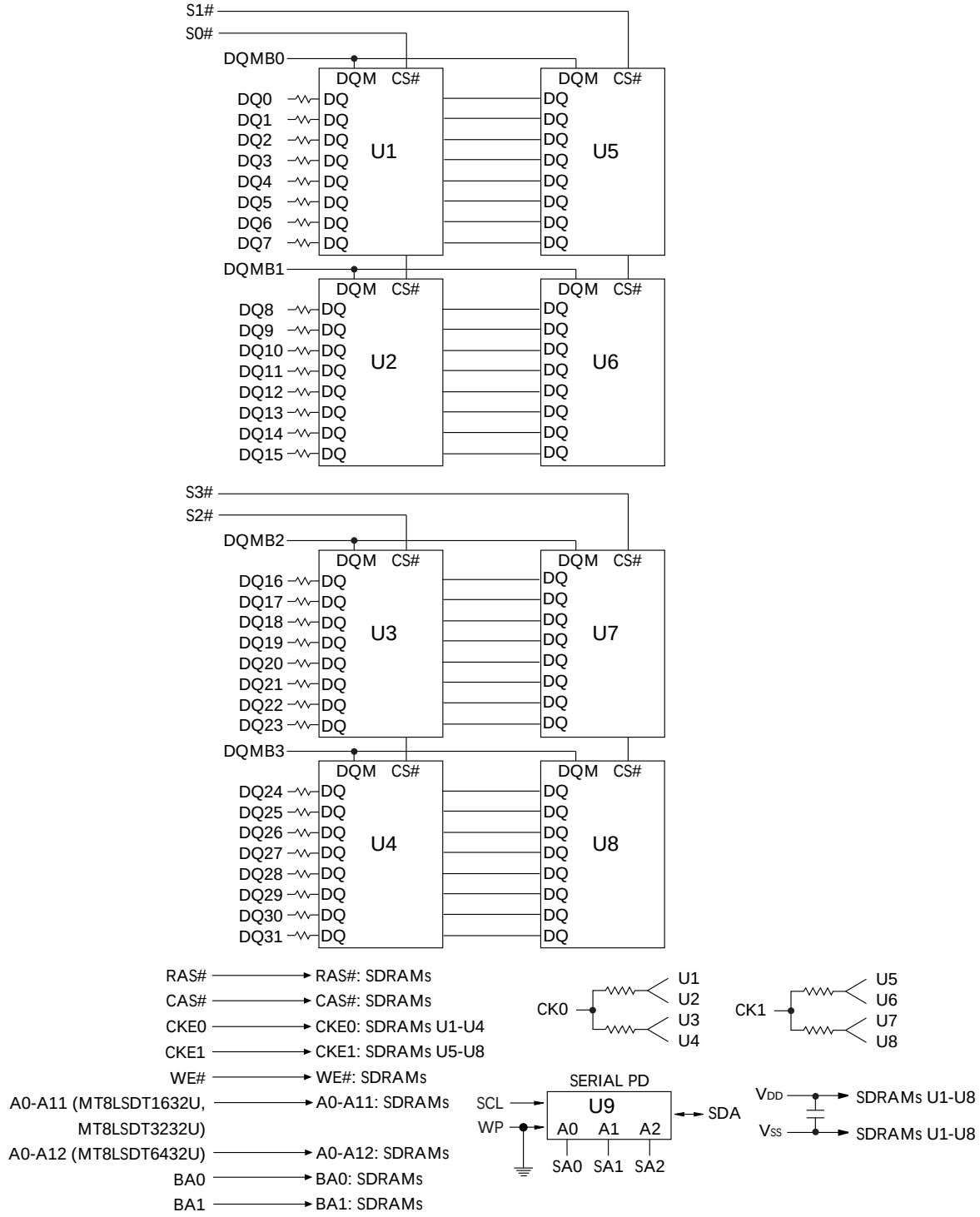


1. All resistor values are 10Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

Standard modules use the following SDRAM devices:
MT48LB16M8A2TG (MT4LSDT1632U)

Lead-free modules use the following SDRAM devices:
MT48LB16M8A2P (MT4LSDT1632U)

(MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U)



Ω

MT48LC8M8A2TG (MT8LSDT1632U); MT48LC16M8A2TG (MT8LSDT3232U); MT48LC32M8A2TG (MT8LSDT6432U)

Lead-free modules use the following SDRAM devices:
MT48LC8M8A2P (MT8LSDT1632U); MT48LC16M8A2P (MT8LSDT3232U); MT48LC32M8A2p (MT8LSDT6432U)

General Description

The MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U are high-speed CMOS, dynamic random-access, 64MB, 128MB and 256MB memory modules organized in a x32 configuration. These modules use SDRAM devices which are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0–A11 [MT4LSDT1632U, MT8LSDT1632U, and MT8LSDT3232U]; or A0–A12 [MT8LSDT6432U]). The address bits registered coincident with the READ or WRITE command (A0–A8 MT4LSDT1632U; A0–A9 MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U]). are used to select the starting device column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n*

^{2}C bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

DD and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

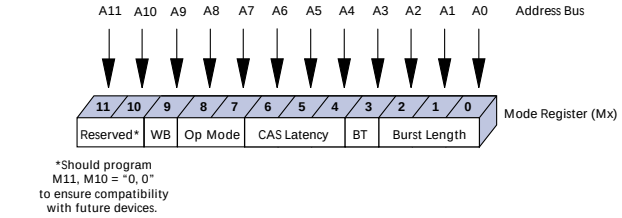
Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

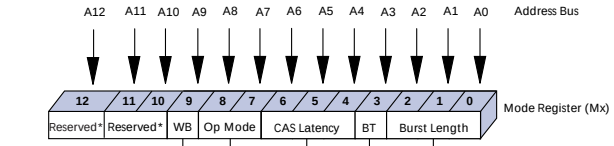
Mode Register Definition

Mode Register Definition Diagram

MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U



MT8LSDT6432U



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Burst Length

in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 7, Burst Definition Table, on page 9. The block is uniquely selected by A1–A*i*

i

i

i

Burst Type

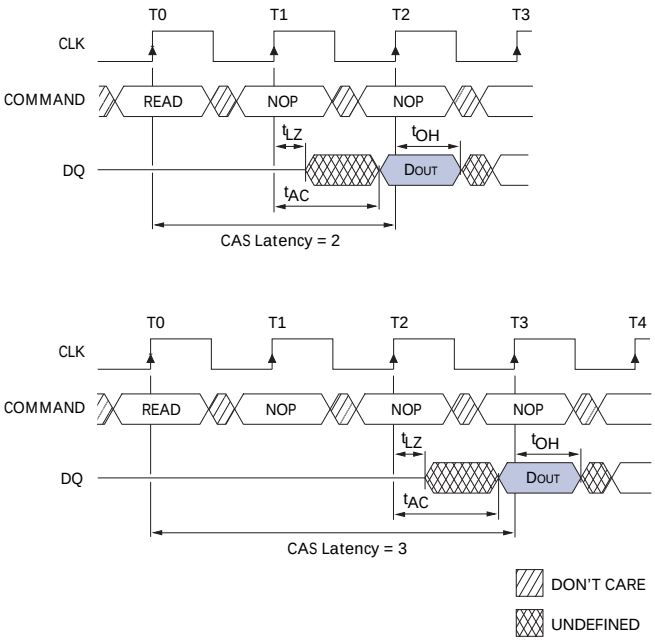
TABLE 7: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
	A0		
	A1 A0		
	A2 A1 A0		
	(location 0-*y*)	Cn, Cn + 1, Cn + 2, Cn + 3, Cn + 4. . . Cn - 1, Cn . . .	Not supported

NOTE:

1. For full-page accesses: y = 512 (MT4LSDT1632U); y = 1,024 (128Mb-based MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U).
2. For a burst length of two, A1–A select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A select the unique column to be accessed, and mode register bit M3 is ignored.
8. = 8 for MT8LSDT1632U
   i = 9 for MT4LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U

CAS Latency Diagram



CAS Latency

m

n + *m*. The DQ will start driving as a result of the clock edge one cycle earlier (- 1), and provided that the relevant access times are met, the data will be valid by clock edge . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQ will start driving after T1 and the data will be valid by T2, as shown in Figure , Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.. Table 8, CAS Latency Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Write Burst Mode

Table 8: CAS Latency Table

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
	≤	≤
	≤	≤
	≤	≤

Commands

Table 9: Commands and DQMB Operation Truth Table

NAME (FUNCTION)	S#	RAS#	CAS#	WE#	DQMB	ADDR	DQ	NOTES
		X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select device bank and activate row)	L	L	H	H	X	Bank/ Row	X	3
READ (Select device bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0–A11 define the op-code written to the Mode Register. For MT8LSDT6432U, A12 should be driven LOW.
3. A0–A11 (MT4LSDT1632U, MT8LSDT1632U, MT8LSDT3232U), or A0–A12 (MT8LSDT6432U) provide row address and BA0 and BA1 determine which device bank is made active.
4. A0–A8 (MT4LSDT1632U) or A0–A9 (MT8LSDT1632U, MT8LSDT3232U, and MT8LSDT6432U) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0 and BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0 and BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQ during WRITE (zero-clock delay) and READ (two-clock delay).

Absolute Maximum Ratings

SS . . . . . -1V to +4.6V
Voltage on Inputs, NC, or I/O Pins
Relative to VSS . . . . . -1V to +4.6V

Operating Temperature
T_{OPR} (Commercial - ambient) . . . . . 0°C to +65°C
Storage Temperature (plastic) . . . . . -55°C to +150°C

DC Electrical Characteristics and Operating Conditions – Single-Rank Module

SS; VDD = +3.3V ±0.3V

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
		VDD	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		VIH	2	VDD + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		VIL	-0.3	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	WE#, RAS#, CAS#, A0-A11, BA0–BA1, CK, CKE	II1	-20	20	µA	33
	S#	II2	-10	10	µA	33
	DQMB	II3	-5	5	µA	33
OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ VOUT ≤ VDD	DQ	IOZ	-5	5	µA	33
OUTPUT LEVELS: Output High Voltage (IOUT = -4mA)		VOH	2.4	–	V	
Output Low Voltage (IOUT = 4mA)		VOL	–	0.4	V	

Notes: 1notes appear on page 18; VDD = +3.3V ±0.3V

SUPPLY VOLTAGE		VDD	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		VIH	2	VDD + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs		VIL	-0.3	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	WE#, RAS#, CAS#, A0-A12, BA0–BA1	II1	-40	40	µA	33
	CK, CKE	II2	-20	20	µA	33
	S#, DQMB	II3	-10	10	µA	33
OUTPUT LEAKAGE CURRENT: DQ disabled; 0V ≤ VOUT ≤ VDD	DQ	IOZ	-10	10	µA	33
OUTPUT LEVELS: Output High Voltage (IOUT = -4mA)		VOH	2.4	–	V	
Output Low Voltage (IOUT = 4mA)		VOL	–	0.4	V	

DD Specifications and Conditions –Conditions – MT4LSDT1632U

			MAX				
PARAMETER/CONDITION		**SYMBOL**	**-75**	**-8**	**-10**	**UNITS**	**NOTES**
$^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}	115	600	560	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		I_{DD2}	2	8	8	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after ^{t}RCD met; no accesses in progress		I_{DD3}	45	200	160	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		I_{DD4}	140	600	560	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	I_{DD5}	210	1,240	1,080	mA	3, 12
	^{t}RFC = 15.625µs	I_{DD6}	3	12	12	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}	1	8	8	mA	4

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 18; $V_{DD} = V_{DD}Q$ = +3.3V ±0.3V

OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		$I_{DD1}{}^{a}$	115	468	388	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		$I_{DD2}{}^{b}$	2	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after ^{t}RCD met; no accesses in progress		$I_{DD3}{}^{a}$	45	188	148	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		$I_{DD4}{}^{a}$	140	568	488	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	$I_{DD5}{}^{b}$	210	1,680	1,520	mA	3, 12
	^{t}RFC = 15.625µs	$I_{DD6}{}^{b}$	3	24	24	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		$I_{DD7}{}^{b}$	1	8	8	mA	4

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.

b - Value calculated reflects all module ranks in this operating condition.

DRAM components only; notes: 1, 5, 6, 11, 13; notes appear on page 18; VDD, VDDQ = +3.3V ±0.3V

OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}[a]	150	608	568	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		I_{DD2}[b]	2	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after ^{t}RCD met; no accesses in progress		I_{DD3}[a]	50	208	168	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		I_{DD4}[a]	150	608	568	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	I_{DD5}[b]	310	2,480	2,160	mA	3, 12
	^{t}RFC = 15.625µs	I_{DD6}[b]	3	24	24	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}[b]	2	16	16	mA	4

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
b - Value calculated reflects all module ranks in this operating condition.

DRAM components only; notes: 1, 5, 6, 11, 13;notes appear on page 18; VDD, VDDQ = +3.3V ±0.3V

OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $^{t}RC = {}^{t}RC$ (MIN)		I_{DD1}[a]	125	508	508	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; all device banks idle; CKE = LOW		I_{DD2}[b]	2	16	16	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; all device banks active after ^{t}RCD met; no accesses in progress		I_{DD3}[a]	40	168	168	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; continuous burst; READ or WRITE; all device banks active		I_{DD4}[a]	135	548	548	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	$^{t}RFC = {}^{t}RFC$ (MIN)	I_{DD5}[b]	270	2,160	2,160	mA	3, 12
	^{t}RFC = 7.8125µs	I_{DD6}[b]	3.5	28	28	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}[b]	2.5	20	20	mA	4

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in power-down mode.
b - Value calculated reflects all module ranks in this operating condition.

Note: 1; this parameter is sampled; V_{DD} =+3.3V ±0.3V; f = 1 MHz; notes appear on page 18

Input Capacitance: Address and Command	C_{I1}	10	15.2	pF
Input Capacitance: CK	C_{I2}	10	14	pF
Input Capacitance: S#	C_{I3}	5	7.6	pF
Input Capacitance: DQMB#	C_{I4}	2.5	3.8	pF
Input/Output Capacitance: DQ	C_{IO}	4	6	pF

Note: 1; this parameter is sampled; V_{DD} =+3.3V ±0.3VV; f = 1 MHz; notes appear on page 18

Input Capacitance: Address and Command	C_{I1}	20	30.4	pF
Input Capacitance: CKE	C_{I2}	10	15.2	pF
Input Capacitance: CK	C_{I3}	10	14	pF
Input Capacitance: S#, DQMB#	C_{I4}	5	7.6	pF
Input/Output Capacitance: DQ	C_{IO}	8	12	pF

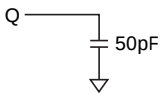
Notes: 5, 6, 8, 9, 11, 31; notes appear on page 18; SDRAM component specifications

Access time from CLK (positive edge)	CL = 3	^tAC		5.4		6		7.5	ns	
	CL = 2	^tAC		6		6		9	ns	
Address hold time		^tAH	0.8		1		1		ns	
Address setup time		^tAS	1.5		2		2		ns	
CLK high-level width		^tCH	2.5		3		3		ns	
CLK low-level width		^tCL	3		3		3		ns	
Clock cycle time	CL = 3	^tCK	7.5		8		10		ns	6
	CL = 2	^tCK	10		10		15		ns	6
CKE hold time		^tCKH	0.8		1		1		ns	
CKE setup time		^tCKS	1.5		2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		2		2		ns	
Data-in hold time		^tDH	0.8		1		1		ns	
Data-in setup time		^tDS	1.5		2		2		ns	
Data-out high-impedance time	CL = 3	^tHZ		5.4		5.4		6	ns	7
	CL = 2	^tHZ		5.4		6		6	ns	7
Data-out low-impedance time		^tLZ	1		1		2			
Data-out hold time (load)		^tOH	3		3		3		ns	7
Data-out hold time (no load)		^tOHN	1.8		1.8		1.8		ns	7
ACTIVE to PRECHARGE command period		^tRAS	44	120,000	50	120,000	60	120,000	ns	32
ACTIVE to ACTIVE command period		^tRC	66		70		90		ns	
AUTO REFRESH period		^tRCAR	20		70		90		ns	8
ACTIVE to READ or WRITE delay		^tRCD	15		20		30		ns	
Refresh period (4,096 cycles)		^tREF		64		64		64	ns	
PRECHARGE command period		^tRP	20		20		30		ns	
ACTIVE bank A to ACTIVE bank B command period		^tRRD	20		20		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	1	1.2	ms	
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7ns		1 CLK + 7n		ns	
			15		15		15		ns	9
Exit SELF REFRESH to ACTIVE command		^tXSR	75		80		90		ns	12

Notes: 5, 6, 8, 9, 11, 31; notes appear on page 18

READ/WRITE command to READ/WRITE command		^tCCD	1	1	1	^tCK	6
CKE to clock disable or power-down entry mode		^tCKED	1	1	1	^tCK	7
CKE to clock enable or power-down exit setup mode		^tPED	1	1	1	^tCK	7
DQM to input data delay		^tDQD	0	0	0	^tCK	6
DQM to data mask during WRITEs		^tDQM	0	0	0	^tCK	6
DQM to data high-impedance during READs		^tDQZ	2	2	2	^tCK	6
WRITE command to input data delay		^tDWD	0	0	0	^tCK	6
Data-in to ACTIVATE command		^tDAL	5	4	4	^tCK	8, 9
Data-in to precharge		^tDPL	2	2	2	^tCK	9, 10
Last data-in to BURST STOP command		^tBDL	1	1	1	^tCK	6
Last data-in to new READ/WRITE command		^tCDL	1	1	1	^tCK	6
Last data-in to PRECHARGE command		^tRDL	2	2	2	^tCK	9, 10
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^tMRD	2	2	2	^tCK	11
Data-out to high-impedance from PRECHARGE command	CL = 3	^tROH	3	3	3	^tCK	6
	CL = 2	^tROH	2	2	2	^tCK	6

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz; T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T_A ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the ISV crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10; ^{t}CK = 7.5ns for -8.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7.5ns for -8; and 7ns for -10 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -75 at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -8, CL = 3 and ^{t}CK = 7.5ns; for -10, CL = 2 and ^{t}CK = 10ns.
30. CKE is HIGH during refresh command period ^{t}RFC (MIN), otherwise CKE is LOW. The $I_{DD}6$ limit is actually a nominal value and does not result in a fail value.
31. Refer to device data sheet for timing waveforms.
32. The value of ^{t}RAS used in -13E speed grade modules is calculated from ^{t}RC - ^{t}RP.
33. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7, Data Validity, and Figure 8, Definition of Start and Stop).

SPD Start Condition

SPD Stop Condition

SPD Acknowledge

Data Validity

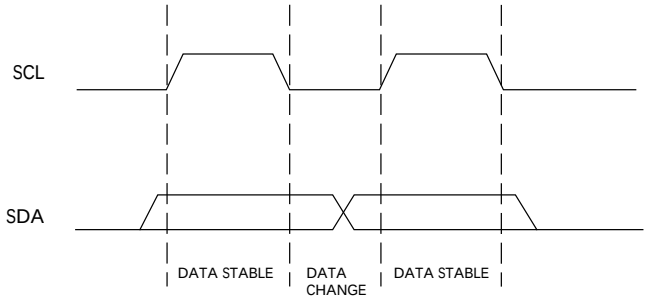


Figure 8: Definition of Start and Stop

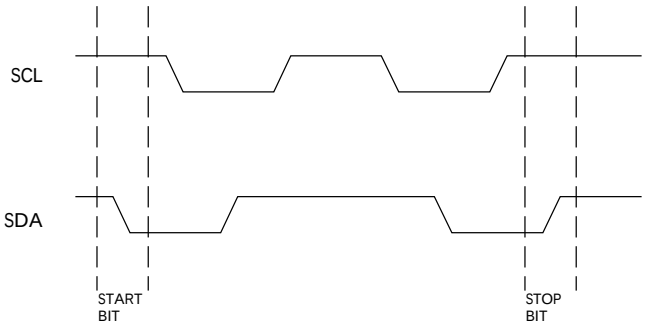


Figure 9: Acknowledge Response from Receiver

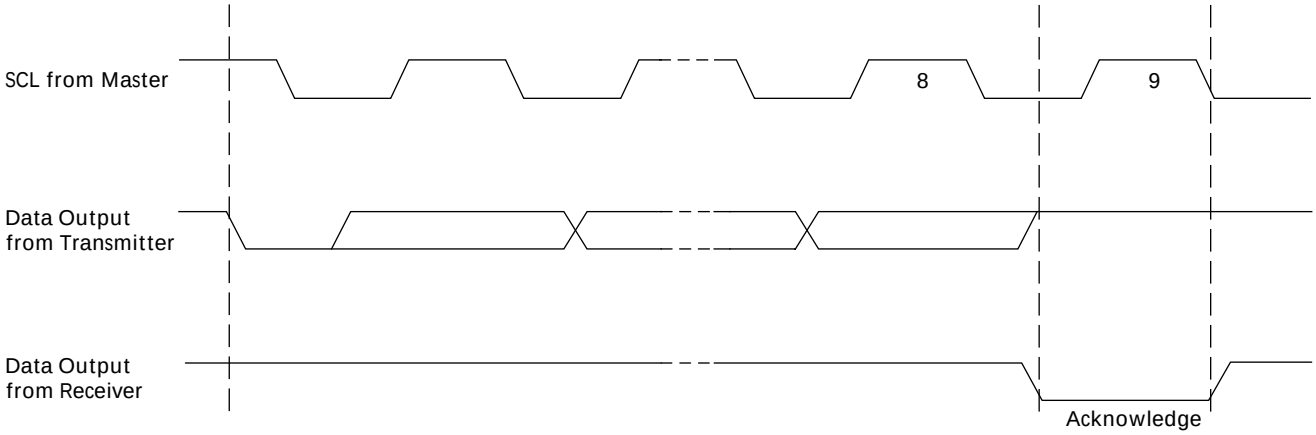


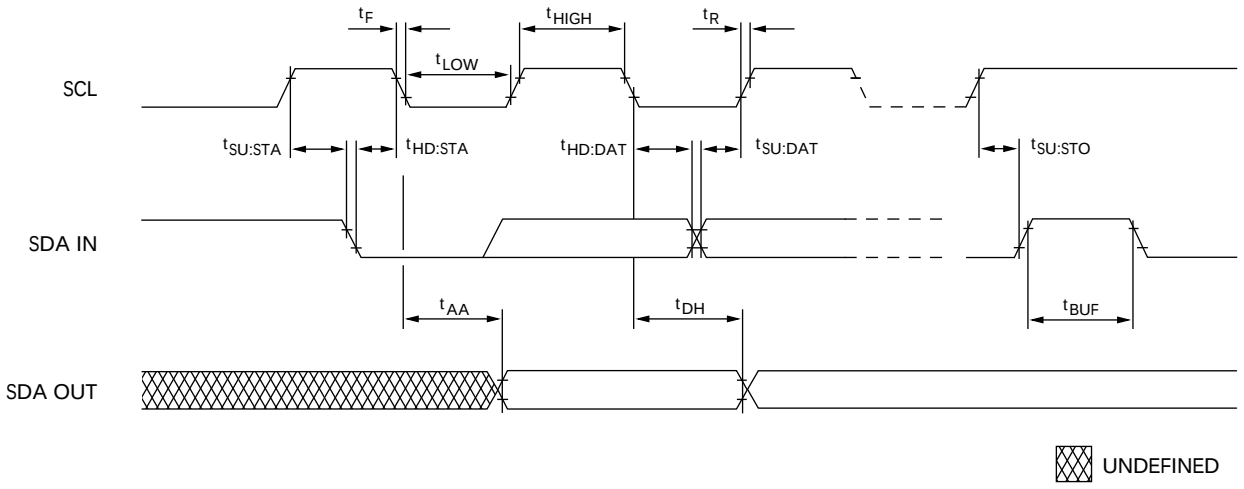
Table 20: EEPROM Device Select Code

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
								—
								—

Table 21: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
		H or VIL	1	Start, Device Select, RW = 1
RandomAddressRead	0	VIH or VIL	1	Start, Device Select, RW= 0, Address
	1	VIH or VIL		RESTART, Device Select, RW= 1
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = 0
Page Write	0	VIL	≤ 16	START, Device Select, RW = 0

Figure 10: SPD EEPROM



All voltages referenced to V_{SS}; V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
		x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{DD} or V_{SS}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

NOTE:

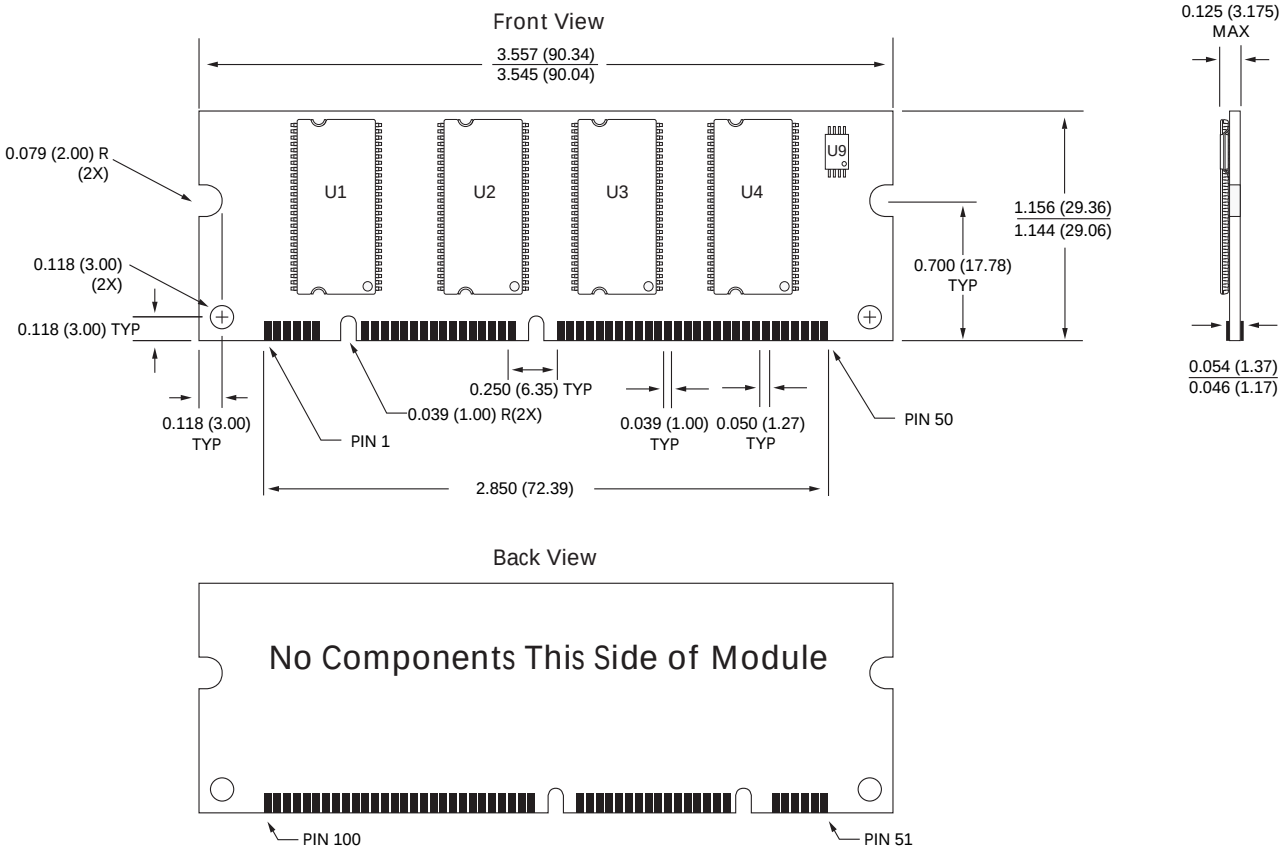
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

0	Number of Bytes Used By Micron	128	80	80	80	80
1	Total Number of SPD Memory Bytes	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses	12 or 13	0C	0C	0C	0D
4	Number of Column Addresses	9 or 10	0A	09	0A	0A
5	Number of Module Ranks	1 or 2	01	02	02	02
6	Module Data Width	32	20	20	20	20
7	Module Data Width (Continued)	0	00	00	00	00
8	Module Voltage Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 3)	10ns (-10) 8ns (-8) 7.5ns (-75)	A0 80 75	A0 80 75	A0 80 75	A0 80 75
10	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 3)	7.5ns (-10) 6ns (-8) 7.5ns (-75)	75 60 54	75 60 54	75 60 54	75 60 54
11	Module Configuration Type	None	00	00	00	00
12	Refresh Rate/type	15.62µs or 7.81µs/Self	80	80	80	82
13	SDRAM Width (Primary SDRAM)	8	08	08	08	08
14	Error-checking SDRAM Data Width	0	00	00	00	00
15	Minimum Clock Delay, ^{t}CCD	1 ^{t}CK	01	01	01	01
16	Burst Lengths Supported	1, 2, 4, 8, Page	8F	8F	8F	8F
17	Number of Banks on SDRAM Device	4	04	04	04	04
18	CAS Latencies Supported	2, 3	06	06	06	06
19	CS Latency	0	01	01	01	01
20	WE Latency	0	01	01	01	01
21	SDRAM Module Attributes	Unbuffered	00	00	00	00
22	SDRAM Device Attributes: General	Attributes	0E	0E	0E	0E
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	15ns (-10) 10ns (-8, -75)	F0 A0	F0 A0	F0 A0	F0 A0
24	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 2)	9ns (-10) 6ns (-8, -75)	90 60	90 60	90 60	90 60
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1)	Not Supported	00	00	00	00
26	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 1)	Not Supported	00	00	00	00

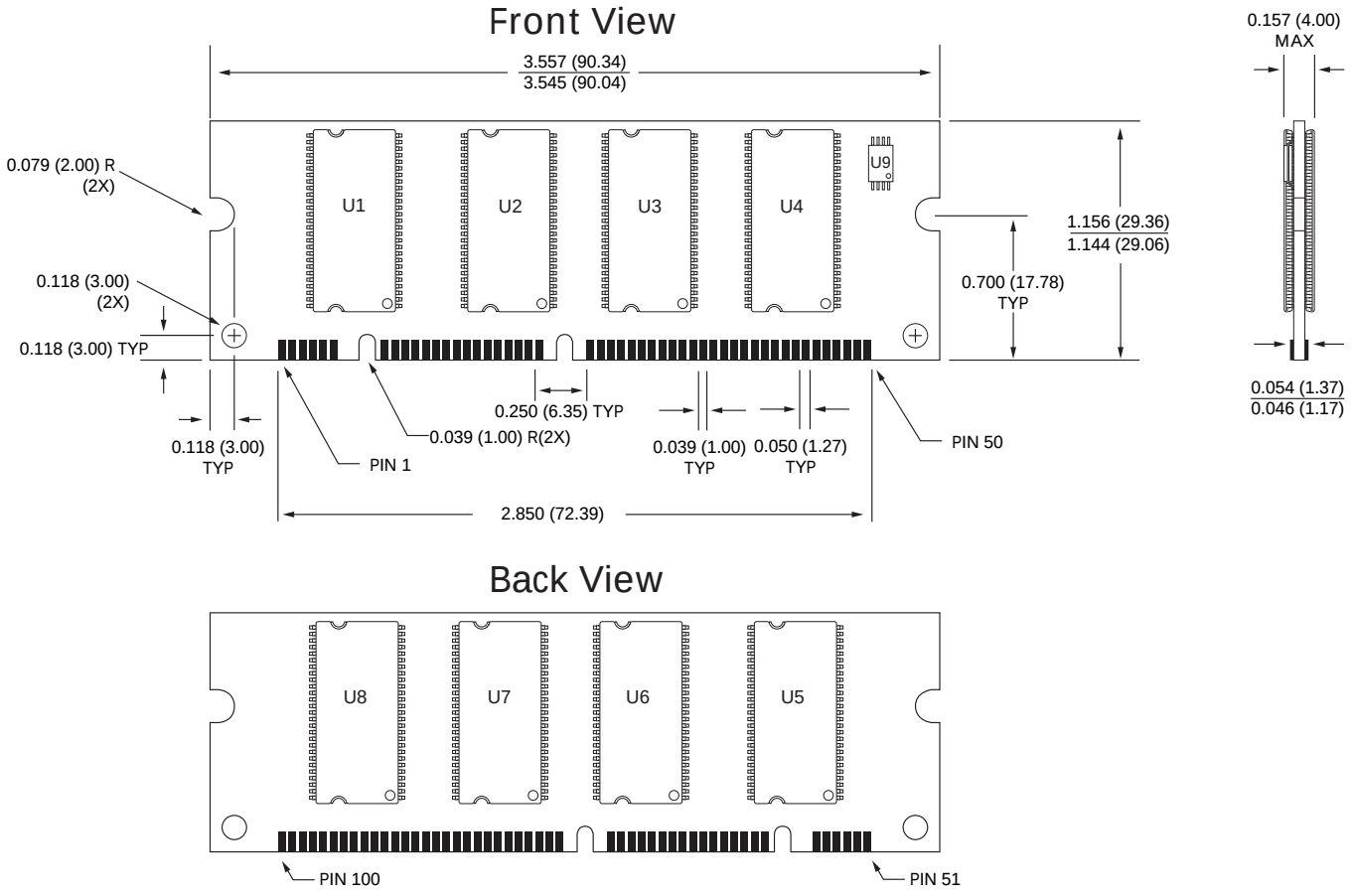
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

27	Minimum Row Precharge Time, ^{t}RP	30ns (-10) 20ns (-8, -75)	1E 14	1E 14	1E 14	1E 14
28	Minimum Row Active To Row Active, ^{t}RRD	20ns (-10, -8) 15ns (-75)	14 0F	14 0F	14 0F	14 0F
29	Minimum RAS# to CAS# Delay, ^{t}RCD	30ns (-10) 20ns (-8, -75)	1E 14	1E 14	1E 14	1E 14
30	Minimum RAS# Pulse Width, ^{t}RAS	60ns (-10) 50ns (-8) 44ns (-75)	3C 32 2C	3C 32 2C	3C 32 2C	3C 32 2C
31	Module Rank Density	32MB 64MB 128MB	10	8	10	20
32	Command/Address Setup, ^{t}AS	2ns (-10, -8) 1.5ns (-75)	20 15	20 15	20 15	20 15
33	ommand/AddressS Hold, ^{t}AH	1ns (-10, -8) 0.8ns (-75)	10 8	10 8	10 8	10 8
34	Data Signal Input Setup, ^{t}DS	2ns (-10, -8) 1.5ns (-75)	20 15	20 15	20 15	20 15
35	Data Signal Input Hold, ^{t}DH	1ns (-10, -8) 0.8ns (-75)	10 8	10 8	10 8	10 8
36-40	Reserved Bytes	–	00	00	00	00
41	Device Minimum Active/Auto-Refresh Time, ^{t}RC	66ns (-75) 71ns (-8) 66ns (-10)	42 46 5A	42 46 5A	42 46 5A	42 46 5A
42–61	Reserved Bytes	–	00	00	00	00
62	SPD Revision	REV. 2	02	02	02	02
63	Checksum for Bytes 0-62	(-75) (-8) (-10)	AB FC E3	A3 F4 DB	AC FD E4	BF 10 F7
64	Manufacturer's JEDEC ID Code	MICRON		2C	2C	2C
65-71	Manufacturer's JEDEC ID Code (Cont.)			FF	FF	FF
72	Manufacturing Location	1–12		01–0C	01–0C	01–0C
73-90	Module Part Number (ASCII)			Variable Data	Variable Data	Variable Data
91	PCB Identification Code	1-9		01-09	01-09	01-09
92	Identification Code (Cont.)	0		00	00	00
93	Year of Manufacture in BCD			Variable Data	Variable Data	Variable Data
94	Week of Manufacture in BCD			Variable Data	Variable Data	Variable Data
95-98	Module Serial Number			Variable Data	Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)			–	–	–



NOTE:

All dimensions in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



NOTE:

All dimensions in inches (millimeters); —— or typical where noted.

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