

T-41-55

LR3668

CMOS V Driver LSI for 2/3" CCD

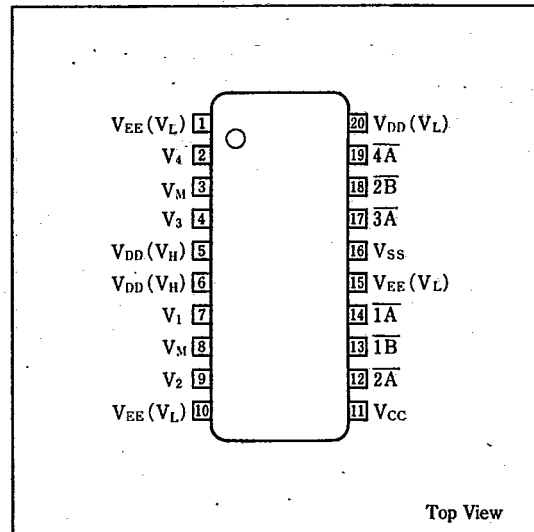
Description

The LR3668 is a CMOS V driver LSI for 2/3" CCD which provides the voltage conversion from CMOS level (0 to +5V) to (-6 to +7V) and impedance conversion functions.

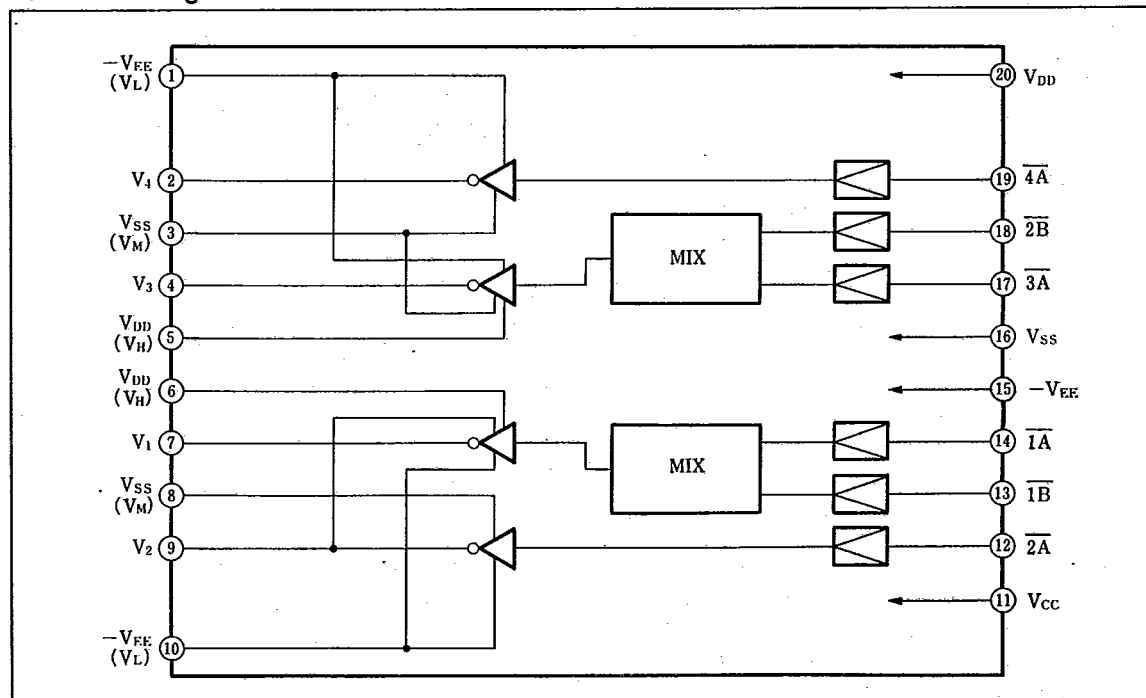
Features

1. Low power consumption
2. Internal four circuits
3. 3-level output
4. 20-pin mini flat package

Pin Connections



Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	$V_{SS}-0.3$ to $V_{SS}+6$	V
	V_{DD}	$V_{SS}-0.3$ to $V_{SS}+8$	V
	V_{EE}	$V_{SS}-7$ to $V_{SS}-0.3$	V
	V_M	V_{EE} to V_{DD}	V
Input voltage	V_I	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	-20 to +70	°C
Storage temperature	T_{str}	-55 to +150	°C

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{DD}	5.4	6.0	7.0	V
	V_{EE}	-6.0	-5.0	-4.0	V
	V_M	0		3.0	V
Input voltage	V_I	0		V_{CC}	V
Operating frequency	NTSC PAL	f	15.734		kHz
			15.625		
Operating temperature	T_{opr}	-20		+70	°C

■ Switching Characteristics

($CL=2700pF$, $V_{CC}=5V$, $V_{DD}=6V$, $V_{EE}=-5V$,
 $V_M=0$ to $3V$, $T_a=-20$ to $70^\circ C$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output rise time	t_{rM}			500	ns
	t_{rH}			500	ns
Output fall time	t_{fM}			500	ns
	t_{fL}			500	ns
Propagation Low time	t_{pHL}			1000	ns
	t_{pIL}			1000	ns
Propagation High time	t_{pLH}			1000	ns
	t_{pHH}			1000	ns

See test circuit

* Input rise and fall time : t_r and $t_f=20ns$

Electrical Characteristics

($V_{CC}=5V$, $V_{DD}=6V$, $V_{EE}=-5V$, $V_M=0V$, $T_a=-20$ to $+70^\circ C$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "Low" voltage	V_{IL}		0		1.0	V	1
Input "High" voltage	V_{IH}		4.0		5.0	V	
Input "Low" current	I_{IL}	$V_{IL}=0V$			1	μA	
Input "High" current	I_{IH}	$V_{IH}=5V$			1	μA	
Output "Low" current	I_{OL}	$V_{OL}=-4.5V$	1.0			mA	2
Output "High" current	I_{OH}	$V_{OH}=5.5V$	1.0			mA	3
Output "Medium" current	I_{OML}	$V_{OML}=-0.5V$	0.5			mA	2
	I_{OMH}	$V_{OMH}=0.5V$	0.5			mA	
Output "Low" voltage	V_{OL}	$ I_{OL} < 1 \mu A$			-4.95	V	3
Output "High" voltage	V_{OH}	$ I_{OH} < 1 \mu A$	5.95			V	
Output "Medium" voltage	V_{OML}	$ I_{OML} < 1 \mu A$			-0.05	V	2
	V_{OMH}	$ I_{OMH} < 1 \mu A$	0.05			V	
Static current consumption	I_{CC}	All inputs Low V_{CC}			200	μA	
	I_{DD}	All inputs Low V_{DD}			200	μA	
	I_{EE}	All inputs Low V_{EE}			200	μA	
Power consumption	I_{DD1}	During operation at NTSC and PAL system		20	50	mW	4

Note 1 : Applied to all input pins.

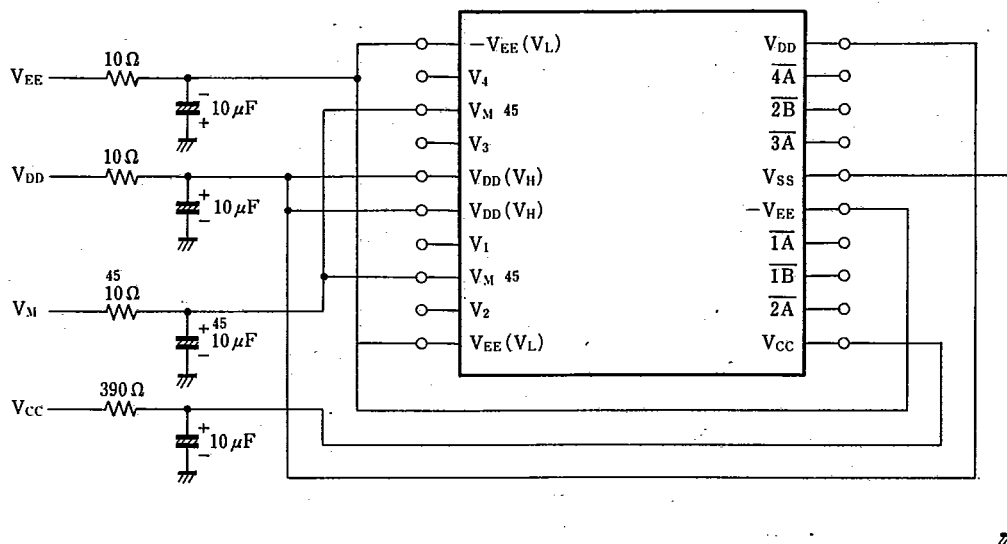
Note 2 : Applied to all output pins.

Note 3 : Applied to output pins V_1 and V_3 .

Note 4 : It is the same test input pattern as for switching characteristics.

Referenced to $V_{SS}=0V$, See test circuit.

Test Circuit (for switching characteristics and electrical characteristics)



■ Cautions

- 1) $10\ \mu\text{F}$ of capacitor should be applied between the power supply as below and the V_{SS} .
- 2) Resistors should be applied to pins in series as below.
 - a) $390\ \Omega$ to V_{CC}
 - b) $10\ \Omega$ to V_H and V_{DD}
 - c) $10\ \Omega$ to V_L and V_{DD}
 - d) $10\ \Omega$ to V_M

■ Timing Chart

