W671300 SERIES

3.3V VoIP RINGING SLIC SERIES

PRELIMINARY DATA SHEET

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Revision 0.5

1. GENERAL DESCRIPTION

The 3.3V family of Ringing Subscriber Line Interface Circuits (RSLIC), collected under the W671300 series, support interfacing to analog Plain Old Telephone Service (POTS) lines. On board ringing generation supports short and medium loop lengths, up to 5,000 ft at the highest operating voltage of -100V. This makes the devices are ideal for emerging customer premises equipment applications such as VoIP gateways, VoIP enabled DSL or Cable Modems as well as Analog Telephone Adapters. Furthermore the family contains seven different product variations, offering the flexibility to match performance to individual system requirements. All variations, however, are distinguished by low power consumption, particularly in standby modes.

The W671300 series allow extensive parameters to be programmed, including the loop current limit, the transient loop current limit, Ring Trip and Switch Hook Detect thresholds. Integrated test and diagnostic features are also offered on selected products to support loopback testing as well as line measurement tests.

Winbond also offers a 3V A-Law/μ-Law CODEC solution (W681310). Using this CODEC in conjunction with the W671300 series completes the termination of the analog POTS line and provides a cost-effective solution to support the complete BORSCHT feature requirements.

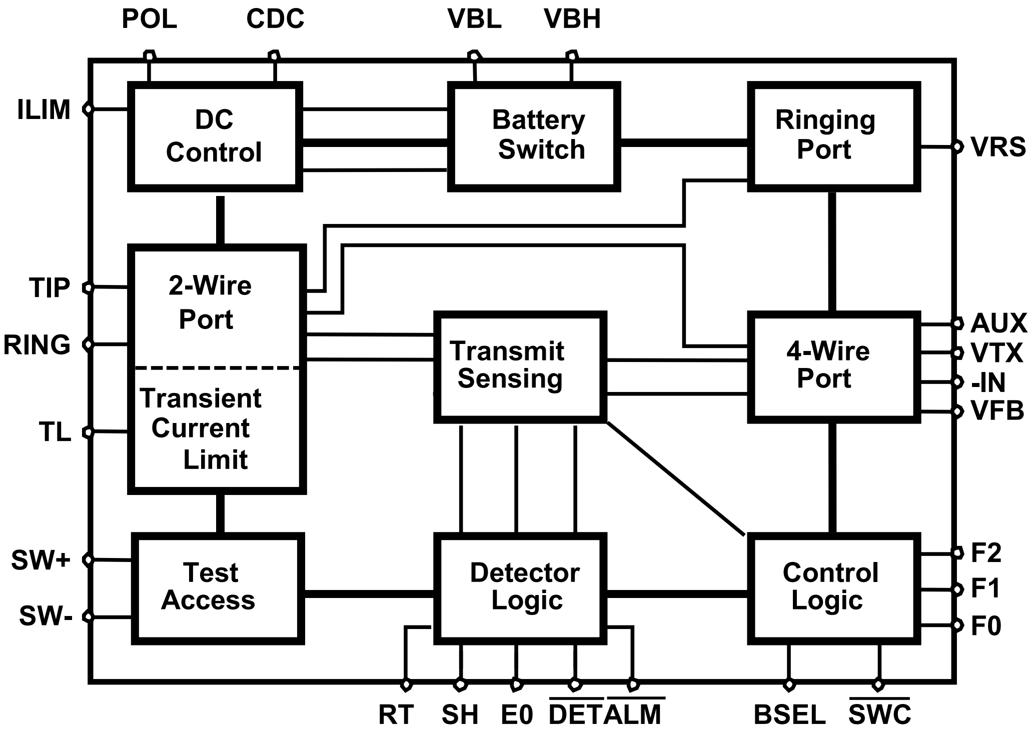
2. FEATURES

- 3.3V Operation
- On board Ringing Generation
- Low Standby Power Consumption (75V, 65mW)
- Programmable Transient Current Limit
- Low Idle Channel noise
- Low External Component Count
- Integrated MTU DC Characteristics
- Silent Polarity Reversal
- Balanced and Unbalanced Ringing
- Thermal Shutdown with Alarm Indicator
- Smooth Off Hook Performance
- Pulse Metering and On-hook Transmission
- Tip Open Ground Start Operation
- Package Options: PLCC and reduced footprint QFN

APPLICATIONS

- Voice Over Internet Protocol (VoIP)
- Cable Modems
- Voice Over DSL (VoDSL) Modems
- Short Loop Access Platforms
- Remote Subscriber Units
- IP PBX
- Analog Terminal Adapters
- Fiber to the Home (FTTH) equipment

3. BLOCK DIAGRAM



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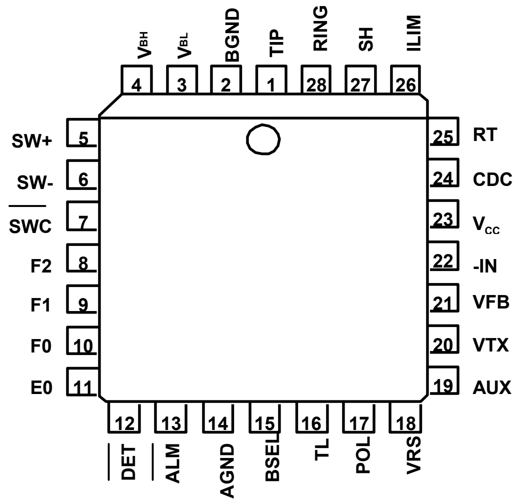
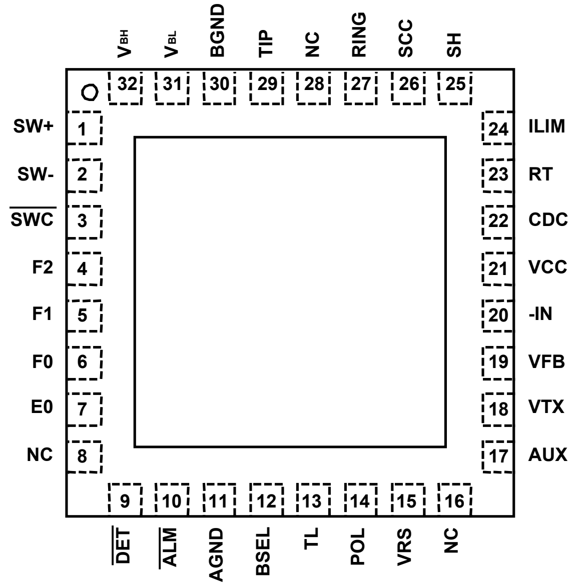
PLCC Top View



QFN Top View



6. PIN DESCRIPTION

Pin Name	Pin # PLCC	Pin # QFN	Functionality
TIP	1	29	Tip power amplifier output.
BGND	2	30	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND. This ground must be connected to the same potential as AGND.
VBL	3	31	Low Battery supply connection.
VBH	4	32	High Battery supply connection for the most negative battery.
SW+	5	1	Uncommitted Switch positive terminal.
SW-	6	2	Uncommitted Switch negative terminal.
$\overline{\text{SWC}}$	7	3	Switch Control Input. This TTL compatible input controls the uncommitted switch, with a logic “0” enabling the switch and logic “1” disabling the switch.
F2	8	4	Mode Control Input - MSB. Pins F2-F0 TTL inputs control the various modes of operation of the device.
F1	9	5	Mode Control Input. (see F2 above)
F0	10	6	Mode Control Input. (see F2 above)
E0	11	7	Detector Output Selection Input. TTL input controling the multiplexing of the Switch Hook Detector (E0=1) and Ground Key Detector (E0=0) comparator outputs to the $\overline{\text{DET}}$ output based upon the state at the F2-F0 pins (see the Device Operating Modes table in section 7).
$\overline{\text{DET}}$	12	9	Detector Output - This TTL output provides on-hook/off-hook status of the loop based upon the selected operating mode (F2-F0 pins). The detected output will either be Switch Hook, Ground Key or Ring Trip. $\overline{\text{DET}}$ will be latched low following a ring trip and unlatched by changing logic state.
$\overline{\text{ALM}}$	13	10	Thermal Shutdown Alarm. Signals internal die temperature has exceeded safe operating temperature (approximately 175^{o}C) and the device has been powered down automatically.
AGND	14	11	Analog Ground Reference. This pin should be externally connected to BGND.
BSEL	15	12	Selects between high battery (BSEL=”1”) and low battery (BSEL=”0”).
TL	16	13	Transient Current Limit programming resistor
POL	17	14	Polarity Reversal Time programming capacitor
VRS	18	15	Ringing Signal Input - Analog input for driving 2-wire interface while in Ring Mode.
AUX	19	17	Auxilliary Input – float if not used.
VTX	20	18	Transmit Output Voltage – Output of impedance matching amplifier, AC couples to CODEC.
VFB	21	19	Feedback voltage for impedance matching. This voltage is scaled to accomplish impedance matching. The CFB capacitor connects between this pin and the -IN pin. It needs to be non-polarized for proper device operation in the Reverse Active mode. Ceramic surface mount capacitors (1206 body style) are available with a 6.3V voltage rating. These can be used for CFB since it is internally limited to approximately ±3V.
-IN	22	20	Impedance matching amplifier summing node. Resistor R_{IN} needs to be as close to the -IN pin as possible to minimize parasitic capacitance.

Pin Name	**Pin # PLCC**	**Pin # QFN**	**Functionality**
VCC	23	21	Positive voltage power supply, +3.3V.
CDC	24	22	DC Biasing Filter Capacitor connects between this pin and VCC. The CDC capacitor may be either polarized or non polarized with a 6.3V voltage rating.
RT	25	23	Ring Trip filter network.
ILIM	26	24	Loop Current Limit programming resistor.
SH	27	25	Switch hook detection threshold programming resistor.
SCC	-	26	Substrate Common Connection - Connect this pin to VBH Supply. Used to connect the die substrate and the thermal heatsink plane of the QFN package.
RING	28	27	Ring power amplifier output.

7. FUNCTIONAL DESCRIPTION

7.1. DESING EQUATIONS

7.1.1. Switch Hook Detect

The switch hook detect threshold is set by a single external resistor, R_{SH} calculated as follows.

$$R_{SH} = 600 / I_{SH} \qquad \textbf{(EQ. 1)}$$

The term I_{SH} is the desired DC loop current threshold. The loop current threshold programming range is from 5mA to 15mA ($40k\Omega < R_{SH} < 120k\Omega$).

7.1.2. Ground Key Detect

The Ground Key Detector senses a DC current imbalance between the Tip and Ring terminals when the ring terminal is connected to ground. The Ground Key Detect threshold is not externally programmable and is internally fixed to 12 mA regardless of the switch hook threshold.

7.1.3. Ring Trip Detect

The Ring Trip Detect threshold is set by a single external resistor, R_{RT}. I_{RT} should be set between the peak ringing current and the peak off hook current while still ringing.

$$R_{RT} = 1800 / I_{RT} \qquad \textbf{(EQ. 2)}$$

In addition, the Ring Trip current must be set below the transient current limit, including tolerances. The capacitor C_{RT}, in parallel with R_{RT}, will set the Ring Trip response time.

7.1.4. Loop Current Limit

The loop current limit of the device is programmed by the external resistor R_{IL}. The value of R_{IL} can be calculated as follows.

$$R_{IL} = \frac{1760}{I_{LIM}} \qquad \textbf{(EQ. 3)}$$

The term I_{LIM} is the desired loop current limit, programmable between 15mA and 45mA ($39k\Omega < R_{IL} < 117k\Omega$).

7.1.5. Transient Current Limit

The drive current capability of the output tip and ring amplifiers is determined by an output current limit circuit and is externally programmable at pin TL. This is output current limit is separate from the DC loop current limit function. The current limit circuit works in both the source and sink direction, with an internally fixed offset to prevent the current limit functions from turning on simultaneously. The current limit function is provided by sensing line current and reducing the voltage drive to the load when the externally set threshold is exceeded, hence forcing a constant source or sink current.

7.1.5.1. Transient Source Current Programming

The source current is externally programmed as shown below.

$$R_{TL} = \frac{1780}{I_{SRC}} \qquad \text{(EQ. 4)}$$

For example a source current limit setting of 95mA is programmed with a 18.7kΩ resistor connected between pin TL and ground. This setting determines the maximum amount of current which flows from Tip to Ring during an off-hook event until the DC loop current limit responds. In addition this setting also determines the amount of current which will flow from Tip or Ring when external battery faults occur.

7.1.5.2. Transcient Sink Current Programming

The sink current limit is internally offset 20% higher than the externally programmed source current limit setting.

$$I_{SNK} = 1.20 \times I_{SRC} \qquad \text{(EQ. 5)}$$

If the source current limit is set to 95mA, the sink current limit will be 114mA. This setting will determine the maximum current that flows into Tip or Ring when external ground faults occur.

7.1.5.3. Understanding Transient Current Limit

Each tip and ring amplifier is designed to limit source current and sink current. The diagram below shows the functionality of the circuit for the case of limiting the source current. A similar diagram applies to the sink current limit with current polarity changed accordingly.

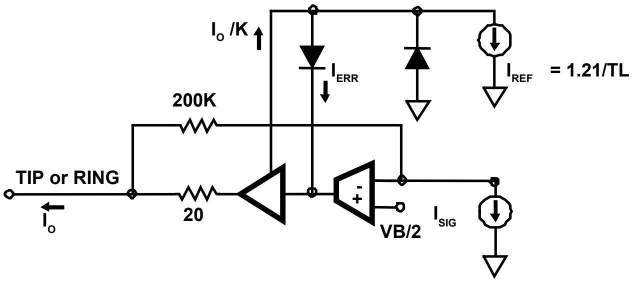


FIGURE 1: CURRENT LIMIT FUNCTIONAL DIAGRAM

During normal operation, the error current (I_{ERR}) is zero and the output voltage is determined by the signal current (I_{SIG}) multiplied by the 200 KΩ feedback resistor. With the current polarity as shown for I_{SIG}, the output voltage moves positive with respect to half battery. Assuming the amplifier output is driving a load at a more negative potential, the amplifier output will source current.

During excessive output source current flow, the scaled output current (I_O/K) exceeds the reference current (I_{REF}) forcing an error current (I_{ERR}). With the polarity as shown the error current subtracts from the signal current, which reduces the amplifier output voltage. By reducing the output voltage the source current to the load is decreased and the output current is limited.

7.1.5.4. Setting the Propoer Transient Current Limit

Since this feature programs the maximum output current of the device, the setting must be high enough to allow for detection of Ring Trip or programmed off-hook loop current, whichever is greater.

To allow for proper Ring Trip operation, the transient current limit setting should be set at least 25% higher than the peak Ring Trip current setting. Setting the transient current 25% higher should account for programming tolerances of both the Ring Trip threshold and the transient current limit.

If loop current is larger than Ring Trip current (Low REN applications) then the transient current limit should be set at least 35% higher than the loop current setting. The slightly higher offset accounts for the slope of the loop current limit function.

Attention to detail should be exercised when programming the transient current limit setting. If Ring Trip detect does not occur while ringing, re-examine the transient current limit and Ring Trip threshold settings.

7.1.6. DC Loop Feed

The feedback mechanism for monitoring the DC portion of the loop current is the loop detector. A low pass filter is used in the feedback to block voice band signals from interfering with the loop current limit function. The pole of the low pass filter is set by the external capacitor C_{DC} and its value should be 4.7µF, 6.3V rated polarized or non-polarized capacitor.

Most applications will operate the device from low battery while off-hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads or long loops, Tip will be near -4V and Ring will be near V_{VBL} + 5V. The following diagram illustrates the DC feed characteristic.

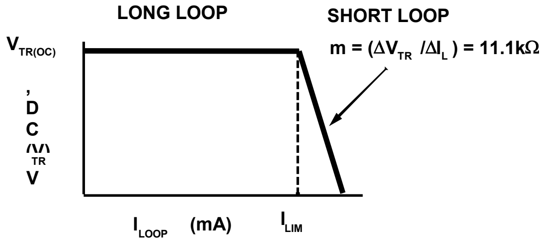


FIGURE 2: DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 9 \qquad \text{(EQ. 6)}$$

The curve of Figure 3 illustrates the actual loop current for a given set of loop conditions. The loop conditions are determined by the low battery voltage and the DC loop impedance. The DC loop impedance is the sum of the protection resistance, copper loop resistance (ohms/foot) and the telephone off hook DC resistance.

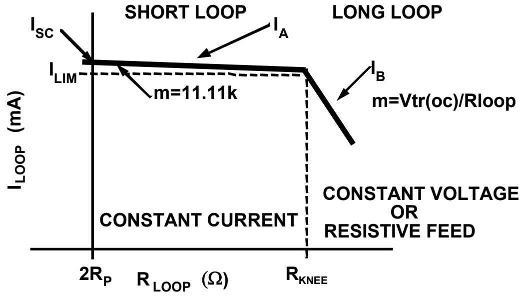


FIGURE 3: I_{LOOP} -VS- R_{LOOP} LOAD CHARACTERISTIC

The slope of the feed characteristic and the battery voltage define the maximum loop current on the shortest possible loop as the short circuit current I_{SC}.

$$I_{SC} = I_{LIM} + \frac{V_{TR(OC)} - 2R_P I_{LIM}}{11.11k} \qquad \text{(EQ. 7)}$$

The term I_{LIM} is the programmed current limit, $1760/R_{IL}$. The line segment I_A represents the constant current region of the loop current limit function.

$$I_A = I_{LIM} + \frac{V_{TR(OC)} - R_{LOOP} I_{LIM}}{11.11k} \qquad \text{(EQ. 8)}$$

Process variations in the W671300 Family effect the I_{LIM} and 11.11kΩ slope in the above equation. All units are tested with: a 300Ω load across tip and ring, V_{BAT}=-24V and I_{LIM} set to 25mA. The equation can be used to predict the ideal current at this setting (25.76mA). All units are tested to be within ±8.5% of this ideal value (23.57mA to 27.95mA).

The maximum loop impedance for a programmed loop current is defined as R_{KNEE}.

$$R_{KNEE} = \frac{V_{TR(OC)}}{I_{LIM}} \qquad \text{(EQ. 9)}$$

When R_{KNEE} is exceeded, the device will transition from constant current feed to constant voltage, resistive feed.

The line segment I_B represents the resistive feed portion of the load characteristic.

$$I_B = \frac{V_{TR(OC)}}{R_{LOOP}} \qquad \text{(EQ. 10)}$$

7.1.7. Impedance Matching

The impedance of the device is programmed with the external component R_S. R_S is the gain setting resistor for the Transmit Amplifier that provides impedance matching. If complex impedance matching is required, then a complex network can be substituted for R_S.

The feedback mechanism for monitoring the AC portion of the loop current consists of two amplifiers, the Sense Amplifier (SA) and the Transmit Amplifier (TA). The AC feedback signal is used for impedance synthesis. A detailed model of the AC feedback loop is provided below.

The gain of the transmit amplifier, set by R_S, determines the programmed impedance of the device. The capacitor C_{FB} blocks the DC component of the loop current. The ground symbols in the model represent AC grounds, not actual DC potentials.

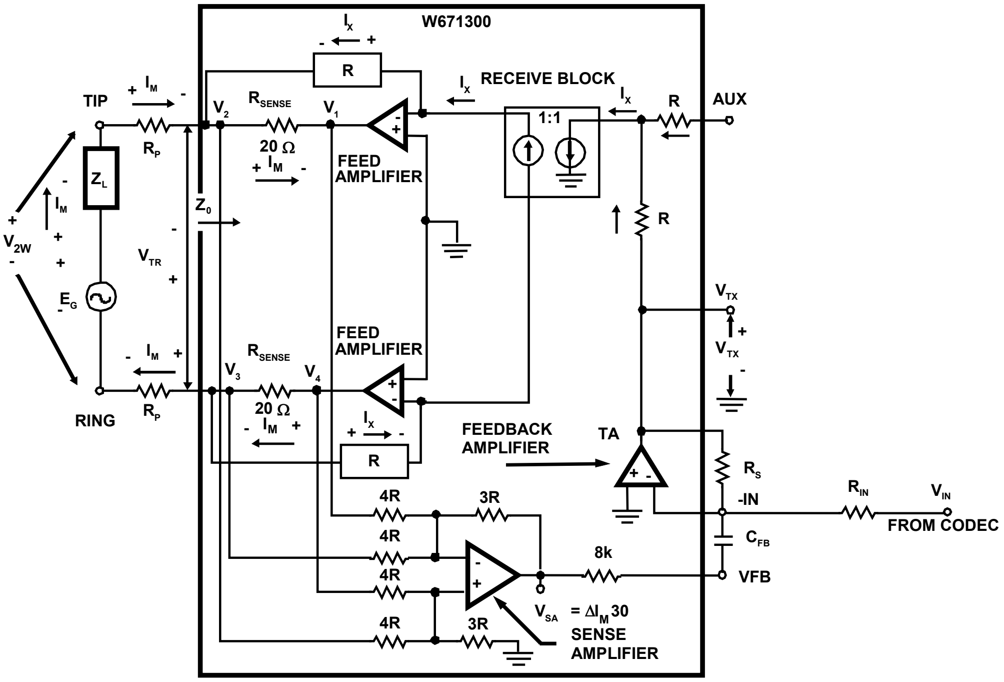


FIGURE 4: AC SIGNAL TRANSMISSION MODEL

The Sense Amplifier is configured as a 4 input differential amplifier with a gain of 3/4. The voltage at the output of the sense amplifier (V_{SA}) is calculated using superposition. $V_{SA}1$ is the voltage resulting from V1, $V_{SA}2$ is the voltage resulting from V2 and so on (as shown in the AC signal transmission model above).

$$V_{SA}1 = -\frac{3}{4}(V_1) \qquad \text{(EQ. 11)}$$

$$V_{SA}2 = \frac{3}{4}(V_2) \qquad \text{(EQ. 12)}$$

$$V_{SA}3 = -\frac{3}{4}(V_3) \qquad \text{(EQ. 13)}$$

$$V_{SA}4 = \frac{3}{4}(V_4) \qquad \text{(EQ. 14)}$$

$$V_{SA} = [(V_2 - V_1) + (V_4 - V_3)]\frac{3}{4} = [\Delta V + \Delta V]\frac{3}{4} \qquad \text{(EQ. 15)}$$

Where ΔV is equal to $I_M R_{SENSE}$ ($R_{SENSE} = 20\Omega$)

$$V_{SA} = 2(\Delta I_M \times 20)\frac{3}{4} = \Delta I_M 30 \qquad \text{(EQ. 16)}$$

The voltage at VTX is equal to:

$$V_{TX} = -V_{IN}\left(\frac{R_S}{R_{IN}}\right) - V_{SA}\left(\frac{R_S}{8k}\right) = -V_{IN}\left(\frac{R_S}{R_{IN}}\right) - (\Delta I_M 30)\left(\frac{R_S}{8k}\right) \qquad \text{(EQ. 17)}$$

V_{TR} is defined in Figure [4], note polarity assigned to V_{TR}:

$$V_{TR} = 2(V_{TX}) = 2\left(V_{IN}\left(\frac{R_S}{R_{IN}}\right) + (\Delta I_M 30)\left(\frac{R_S}{8k}\right)\right) \qquad \text{(EQ. 18)}$$

Setting V_{IN} equal to zero in the above equation, defining $Z_O = -V_{TR}/\Delta I_M$ and substituting it into the equation will enable the user to determine the required feedback to match the line impedance at V_{2W} as shown in the following equation.

$$Z_O = \frac{1}{133.33}R_S \qquad \text{(EQ. 19)}$$

7.1.7.1. 2-Wire Impedance Matching

Z_O is the source impedance of the device and is defined as:

$$Z_O = Z_L - 2R_P \qquad \text{(EQ. 20)}$$

Z_L is the line impedance and R_P is the external protection resistor. R_S is defined as:

$$R_S = 133.33(Z_L - 2R_P) \qquad \text{(EQ. 21)}$$

7.1.7.2 Complex Impedance Synthesis

Substituting the impedance programming resistor, R_S, with a complex programming network provides complex impedance synthesis.

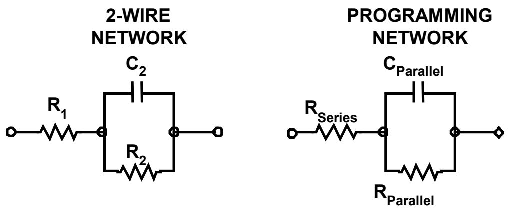


FIGURE 5: COMPLEX PROGRAMMING NETWORK

The reference designators in the programming network match the evaluation board. The component R_S has a different design equation than the R_S used for resistive impedance synthesis. The design equations for each component are provided below.

$$R_{Series} = 133.3 \times (R_1 - 2(R_P)) \qquad \text{(EQ. 22)}$$

$$R_{Parallel} = 133.3 \times R_2 \qquad \text{(EQ. 23)}$$

$$C_{Parallel} = C_2 / 133.3 \qquad \text{(EQ. 24)}$$

Node Equation at AUX input, Figure 4.

$$I_X = \frac{AUX}{R} + \frac{V_{TX}}{R} \qquad \text{(EQ. 25)}$$

Substituting equation [17] for VTX with AUX =0 and ΔI_M= $-V_{2W}/Z_L$ gives us equation [26]. Note: AUX input is not used.

Substituting equation [17] into equation [21]

$$I_X = \frac{V_{TX}}{R} = -\frac{V_{IN}}{R}\left(\frac{R_S}{R_{IN}}\right) - \left(\frac{V_{2w}30}{Z_L}\right)\left(\frac{R_S}{R8k}\right) \qquad \text{(EQ. 26)}$$

Loop Equation at feed amplifiers and load.

$$I_XR - V_{TR} + I_XR = 0 \qquad \textbf{(EQ. 27)}$$

Substituting equation [26] into equation [27]

$$V_{TR} = -2V_{IN}\left(\frac{R_S}{R_{IN}}\right) + \left(\frac{2V_{2w}30}{Z_L}\right)\left(\frac{R_S}{8k}\right) \qquad \textbf{(EQ. 28)}$$

Substituting equation [19] for R_S/8k in equation [28].

$$V_{TR} = -2V_{IN}\left(\frac{R_S}{R_{IN}}\right) + \left(\frac{2V_{2w}30}{Z_L}\right)\left(\frac{133.33Z_O}{8k}\right) \qquad \textbf{(EQ. 29)}$$

Simplifying.

$$V_{TR} = -2V_{IN}\left(\frac{R_S}{R_{IN}}\right) + \left(\frac{V_{2w}}{Z_L}\right)(Z_O) \qquad \textbf{(EQ. 30)}$$

Loop Equation at Tip/Ring interface

$$V_{2W} - I_M2R_P + V_{TR} = 0 \qquad \textbf{(EQ. 31)}$$

Substitute equation [30] into equation [31] and combine terms

$$V_{2W}\left[\frac{Z_L + Z_O + 2R_P}{Z_L}\right] = 2V_{IN}\frac{R_S}{R_{IN}} \qquad \textbf{(EQ. 32)}$$

where:

V_{IN} = The input voltage at the -IN pin through resistor R_{IN}.

AUX = Auxiliary input of RSLIC. Not used for AC gains.

V_{SA} = An internal node voltage (a function of the loop current and the output of the Sense Amplifier).

I_X = SLIC Internal current (difference between the input receive current and the feedback current).

I_M = The AC metallic current.

R_P = A protection resistor (typical 49.9Ω).

R_S = An external resistor/network for matching the line impedance.

V_{TR} = The tip to ring voltage at the output pins of the SLIC.

V_{2W} = The tip to ring voltage including the voltage across the protection resistors.

Z_L = The line impedance.

Z_O = The source impedance of the device.

7.1.7.3. 4-wire to 2-wire Gain

4-wire to 2-wire gain across the Ringing SLIC is equal to the V_{2W} divided by the input voltage V_{IN}, (see Figure [4] above). The receive gain is calculated using equation [32] above.

Equation [33] expresses the receive gain (V_{IN} to V_{2W}) in terms of network impedances. From equation [21], the value of R_S was set to match the line impedance (Z_L) to the device plus the protection resistors (Z_0 + $2R_P$). This results in a 4-wire to 2-wire gain equal to R_S/R_{IN}, as shown below.

$$G_{4-2} = \frac{V_{2W}}{V_{IN}} = 2\left(\frac{R_S}{R_{IN}}\right)\frac{Z_L}{Z_L + Z_O + 2_{RP}} = 2\frac{Z_L}{Z_L + Z_L} = \frac{R_S}{R_{IN}}$$

(EQ. 33)

7.1.7.4. 2-wire to 2-wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with V_{IN} = 0, (reference Figure [4] above).

$$\underline{\textbf{Loop}}$$

$$-E_G + Z_L I_M + 2R_P I_M - V_{TR} = 0$$

(EQ. 34)

From equation [30] with V_{IN} = 0

$$V_{TR} = \frac{Z_O V_{2W}}{Z_L}$$

(EQ. 35)

Substituting equation [35] into Equation [34] and simplify.

$$E_G = -V_{2W}\left[\frac{Z_L + 2R_P + Z_O}{Z_L}\right]$$

(EQ. 36)

Substituting equation [19] into Equation [17] (V_{IN} =0) and defining $\Delta I_M = -V_{2W}/Z_L$ results in the following equation.

$$V_{TX} = \frac{V_{2W}}{2}\left[\frac{Z_L - 2R_P}{Z_L}\right]$$

(EQ. 37)

Combining the two preceding equations results in the following.

$$G_{2\text{-}4} = \frac{V_{TX}}{E_G} = -\frac{Z_L - 2R_P}{2(Z_L + 2R_P + Z_O)} = -\frac{Z_O}{2(Z_L + 2R_P + Z_O)} \qquad \text{(EQ. 38)}$$

A more useful form of the equation is rewritten in terms of V_{TX}/V_{2W}. A voltage divider equation is written to convert from E_G to V_{2W} as shown below.

$$V_{2W} = \left(\frac{Z_O + 2_{RP}}{Z_L + Z_O + 2_{RP}}\right) E_G \qquad \text{(EQ. 39)}$$

Substituting $Z_L = Z_O + 2_{RP}$ and rearranging in terms of E_G yields the following.

$$E_G = 2V_{2W} \qquad \text{(EQ. 40)}$$

Substituting this into equation [38] results in a description for 2-wire to 4-wire gain which is a function of the synthesized input impedance of the SLIC and the protection resistors.

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{2W}} = -\left(\frac{Z_O}{(Z_L + 2R_P + Z_O)}\right) = 0.416 \qquad \text{(EQ. 41)}$$

If Z_L is 600Ω, Z_O is programmed with R_S to be 498.76Ω (66.5kΩ/133.33), and R_P is equal to 49.9Ω. This results in a 2-wire to 4-wire gain of 0.416 or -7.6dB.

When the protection resistors are set to zero, the transmit gain is -6dB.

7.1.7.5. Transhybrid Gain

The transhybrid gain is defined as the 4-wire to 4-wire gain (G_{44}).

$$G_{44} = G_{42} \times G_{24} = -\left(\frac{R_S}{R_{IN}}\right)\left(\frac{Z_O}{Z_L + 2R_P + Z_O}\right) \qquad \text{(EQ. 42)}$$

7.1.8. Understanding Phase Across the Ringing SLIC

7.1.8.1. 4-Wire to 2-Wire Phase

The phase of a signal through the device depends upon whether the source is driving the signal 4-wire to 2-wire or 2-wire to 4-wire.

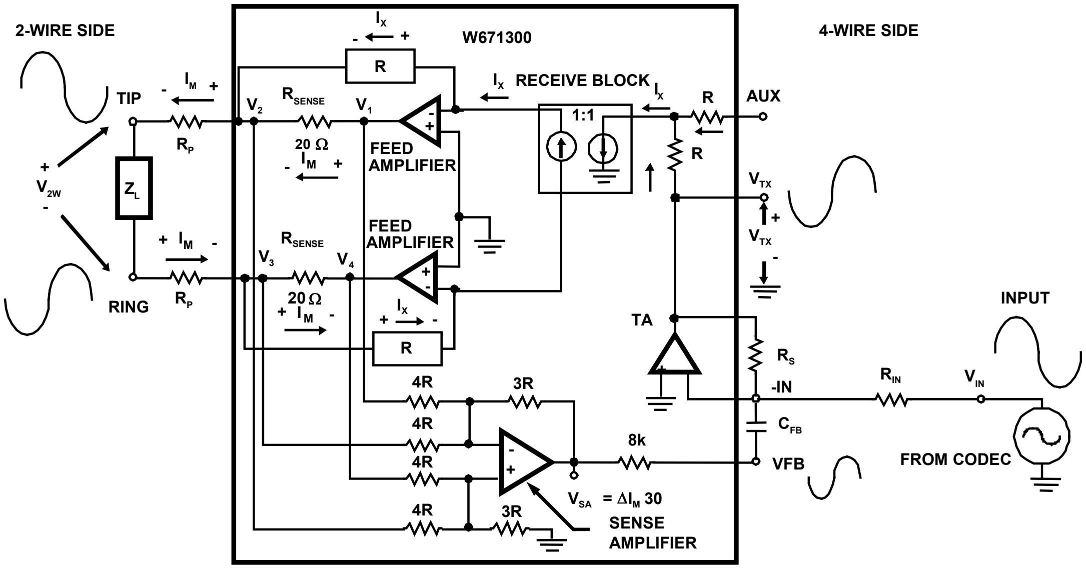


FIGURE 6: 4-WIRE TO 2-WIRE SIGNAL PHASE ACROSS THE DEVICE

The diagram illustrates the phase of the input signal across the device when the signal is applied at the -IN pin through the R_{IN} resistor. The Transmit Amplifier (TA) inverts the signal 180 degrees at the VTX pin. The feedback around the tip amplifier inverts the signal again on the tip lead. The input signal will cause AC loop current to flow through the 20Ω sense resistors in the direction from V1 to V2 and V3 to V4. This results in an inverted signal (referenced from tip) on the VSA and hence the VFB pin. This out-of-phase signal is the signal used by the feedback path to match the line impedance of the 2-wire side.

7.1.8.2. 2-Wire to 4-Wire Phase

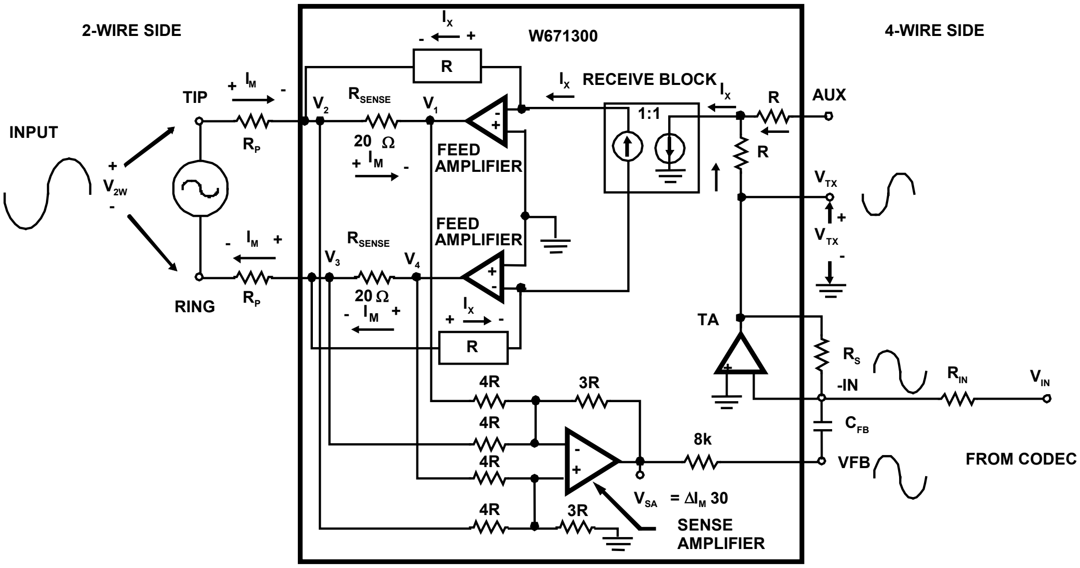


FIGURE 7: 2-WIRE TO 4-WIRE SIGNAL PHASE ACROSS THE DEVICE

The diagram above illustrates the phase of the input signal across the device when the signal is applied across tip and ring. When driving the 2-wire side with a source the device looks like a pre-determined impedance (programmed with resistor RS). The current flows through the 20Ω sense resistors in the direction V2 to V1 and V4 to V3. This results in a non-inverted signal (referenced from tip) on the VSA and hence the VFB pin. This signal is then inverted by the TA amplifier and the signal appearing on the VTX putput is out of phase with the signal on tip.

7.1.8.3. Summary

4-Wire to 2-Wire (V_{IN} to V_{2W}) is 180° out of phase.

2-Wire to 4-Wire (V_{2w} to V_{TX}) is 180° out of phase.

4-Wire to 4-Wire (V_{IN} to V_{TX}) is 180° out of phase.

7.2. OPERATING MODES

The operation of the W671300 Family may best be understood by examining the various operating modes. The following table gives an overview of those modes and the members of the W671300 family to which they apply. A detailed description of each mode will follow.

TABLE 1: DEVICE OPERATING MODES

MODE	F2	F1	F0	E0 = 1	E0 = 0	W671310	W671320	W671330	W671340	W671352	W671361	W671370 W671371
Low Power Standby	0	0	0	SHD	GKD	●	●	●	●	●	●	●
Forward Active	0	0	1	SHD	GKD	●	●	●	●	●	●	●
Unbalanced Ringing	0	1	0	RTD	RTD							●
Reverse Active	0	1	1	SHD	GKD	●	●	●	●	●	●	●
Ringing	1	0	0	RTD	RTD	●	●	●	●	●	●	●
Forward Loop Back	1	0	1	SHD	GKD	●	●	●	●		●	●
Tip Open	1	1	0	SHD	GKD	●	●	●	●		●	●
Power Denial	1	1	1	n/a	n/a	●	●	●	●	●	●	●

Notes: SHD: Switch Hook Detector; GKD: Ground Key Detector; RTD: Ring Trip Detect

7.2.1. LOW POWER STANDBY MODE

The Low Power Standby mode (LPS, 000) should be used during idle line conditions. The device is designed to operate from the high battery during this mode. Most of the internal circuitry is powered down, resulting in low power dissipation. If the 2-wire (tip/ring) DC voltage requirements are not critical during idle line conditions, the device may also be operated from the low battery. Operation from the low battery will further decrease the standby power dissipation.

TABLE 2: DEVICE INTERFACES DURING LOW POWER STANDBY

INTERFACE	ON	OFF	NOTES
Receive		X	AC transmission, impedance matching and ringing are disabled during this mode.
Ringing		X	
Transmit		X	
2-Wire	X		Amplifiers disabled
Loop Detect	X		Switch hook or ground key

7.2.1.1. 2-Wire Interface

During Low Power Standby, the tip and ring amplifiers are turned off to conserve power and the 2-wire interface is maintained with internal switches and voltage references. The device will provide Maintenance Termination Unit (MTU) compliance, loop current and loop supervision. Figure 3 represents the internal circuitry providing the 2-wire interface during Low Power Standby.

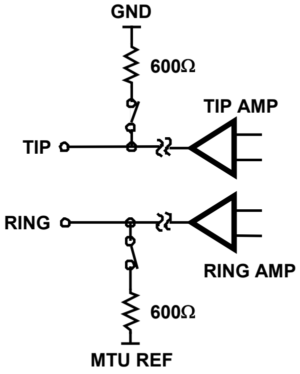


FIGURE 8: LPS 2-WIRE INTERFACE CIRCUIT DIAGRAM

7.2.1.2. Maintenance Terminal Unit (MTU) Compliance

MTU compliance places DC voltage requirements on the 2-wire terminals during idle line conditions. The voltage is expressed as the difference between Tip and Ring. The minimum idle voltage is 42.75V. The high side of the MTU range is 56V.

The Tip voltage is held near ground through a 600Ω resistor and switch. The Ring voltage is limited to a maximum of -56V (by MTU REF) when operating from either the high or low battery. A switch and 600Ω resistor connect the MTU reference to the Ring terminal. When the high battery voltage exceeds the MTU reference of -56V, the Ring terminal will be clamped by the internal reference (typically -54V). The same Ring relationships apply when operating from the low battery voltage. For high battery voltages (V_{BH}) less than or equal to the internal MTU reference threshold:

$$V_{RING} = V_{BH} + 5 \qquad \text{(EQ. 43)}$$

7.2.1.3. Loop Current

During Low Power Standby, the device will provide current to a load. The current path is through resistors and switches, and will be a function of the off hook loop resistance (R_{LOOP}) which includes the off hook phone resistance and copper loop resistance. The current available during Low Power Standby is determined by the following equation.

$$I_{LOOP} = (-1 - (-54)) / (600 + 600 + R_{LOOP}) \qquad \text{(EQ. 44)}$$

Internal current limiting of the standby switches will limit the maximum current to approximately 20 mA.

Another loop current related parameter is longitudinal current capability. The longitudinal current capability is reduced. The reduction in longitudinal current capability is a result of disabling the Tip and Ring amplifiers.

7.2.1.4. On-hook Power Dissipation

The On-hook power dissipation of the device during Low Power Standby is determined by the operating voltages and quiescent currents and is calculated using the following equation.

$$P_{LPS} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \qquad \text{(EQ. 45)}$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an On-hook mode. Some applications may specify a standby current which may be a charging current required for some modern telephone electronics.

7.2.1.5. Standby Current Power Dissipation

Any standby line current, I_{SLC}, introduces an additional power dissipation term P_{SLC}. The following equation illustrates that the power contribution is zero when the standby line current is zero.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| - 54 + 1 + I_{SLC} x1200) \qquad \text{(EQ. 46)}$$

If the battery voltage is less than -54V (the MTU clamp is off), the standby line current power contribution reduces to the following.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| + 1 + I_{SLC} x1200) \qquad \text{(EQ. 47)}$$

Most applications do not specify charging current requirements during standby. When specified, the typical charging current may be as high as 5 mA**.**

7.2.2. FORWARD ACTIVE MODE

The Forward Active mode (FA, 001) is the primary AC transmission mode of the device. On-hook transmission, DC loop feed and voice transmission are supported during Forward Active. Loop supervision is provided by either the Switch Hook Detector (E0 = 1) or the Ground Key Detector (E0 = 0). The device may be operated from either high or low battery for on-hook transmission and low battery for loop feed.

7.2.2.1. On-Hook Transmission

The primary purpose of On-hook transmission is to support caller ID and other advanced signalling features. The transmission over load level while On-hook is $1V_{PEAK}$.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V. For battery voltages less than -60V, the Ring voltage is a function of the battery voltage and is calculated as follows.

$$V_{RING} = V_{BH} + 5 \qquad \text{(EQ. 48)}$$

Loop supervision is provided by the Switch Hook Detector at the $\overline{DET}$ output. When $\overline{DET}$ goes LOW, the low battery should be selected for DC loop feed and voice transmission.

7.2.2.2. Feed Architecture

The design implements a voltage feed/current sense architecture. The device controls the voltage across Tip and Ring though sensing of load current. Internal resistors (R_{CS}) are placed in series with Tip and Ring outputs to provide the current sensing. The diagram below illustrates the concept.

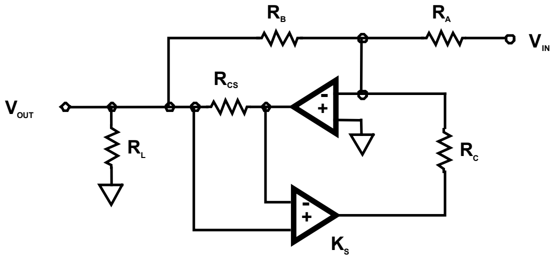


FIGURE 9: VOLTAGE FEED CURRENT SENSE DIAGRAM

By monitoring the current at the amplifier output, a negative feedback mechanism sets the output voltage for a defined load. The amplifier gains are set by resistor ratios (R_A, R_B, R_C) providing all the performance benefits of matched resistors. The internal sense resistor, R_{CS}, is much smaller than the gain resistors and is typically 20Ω for this device. The feedback mechanism, K_S, represents the amplifier configuration providing the negative feedback.

7.2.2.3. Transhybrid Balance

The final step in completing the impedance synthesis design is calculating the necessary gains for transhybrid balance. The AC feedback loop produces an echo at the V_{TX} output of the signal injected at V_{IN}. The echo must be cancelled to maintain voice quality. Most applications will use a summing amplifier in the CODEC front end as shown below to cancel the echo signal.

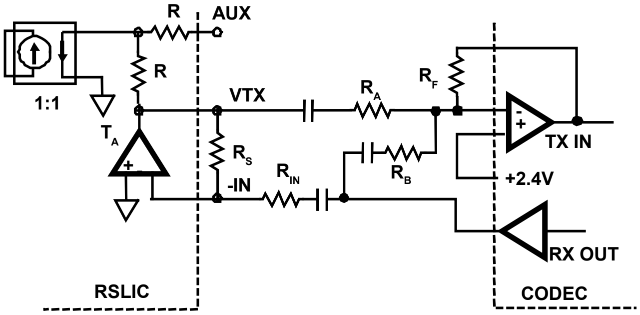


FIGURE 10: TRANSHYBRID BALANCE INTERFACE

The resistor ratio, R_F/R_A, provides the final adjustment for the transmit gain, G_{TX} (V_{2W} to PCMi). The transmit gain is calcualted using the following equation.

$$G_{TX} = -G_{24}\left(\frac{R_F}{R_A}\right) = -\left(\frac{Z_O}{(Z_L + 2R_P + Z_O)}\right)\left(\frac{R_F}{R_A}\right) \qquad \text{(EQ. 49)}$$

Most applications set $R_F = R_A$, making the device 2-wire to 4-wire gain equal the transmit gain. Typically R_A is greater than 20kΩ to prevent loading of the device transmit output. The Value of the RF resistor should be greater than the minimum load specification of the CODECs internal amplifier.

The resistor ratio, R_F/R_B, is determined by the transhybrid gain of the device, G_{44}. R_F is previously defined by the transmit gain requirement and R_B is calculated using the following equation.

$$R_B = \frac{R_A}{G_{44}} = R_A\left(\frac{R_{IN}}{R_S}\right)\left(\frac{Z_L + 2R_P + Z_O}{Z_O}\right) \qquad \text{(EQ. 50)}$$

7.2.2.4. Power Dissipation

The power dissipated by the device during on-hook transmission is strictly a function of the quiescent currents for each supply voltage during Forward Active operation.

$$P_{FAQ} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \qquad \text{(EQ. 51)}$$

Off-hook power dissipation is increased above the quiescent power dissipation by the DC load. If the loop length is less than or equal to R_{KNEE}, the device is providing constant current, I_A, and the power dissipation is calculated using the following equation.

$$P_{FA(IA)} = P_{FA(Q)} + (V_{BL} x I_A) - (R_{LOOP} x I^2{}_A) \qquad \text{(EQ. 52)}$$

If the loop length is greater than R_{KNEE}, the device is operating in the constant voltage, resistive feed region. The power dissipated in this region is calculated using the following equation.

$$P_{FA(IB)} = P_{FA(Q)} + (V_{BL} x I_B) - (R_{LOOP} x I^2{}_B) \qquad \text{(EQ. 53)}$$

Since the current relationships are different for constant current versus constant voltage, the region of device operation is critical to valid power dissipation calculations.

7.2.3. REVERSE ACTIVE MODE

The Reverse Active mode (RA, 011) provides the same functionality as the Forward Active mode. On-hook transmission, DC loop feed and voice transmission are supported. Likewise loop supervision is provided by either the Switch Hook Detector (E0 = 1) or the Ground Key Detector (E0 = 0). The device may be operated from either high or low battery.

During Reverse Active the Tip and Ring DC voltage characteristics exchange roles. That is, Ring is typically 4V below ground and Tip is typically 4V more positive than battery. Otherwise, all feed and voice transmission characteristics are identical to Forward Active.

7.2.3.1. Silent Polarity Reversal

Changing from Forward Active to Reverse Active or vice versa is referred to as polarity reversal. Many applications require slew rate control of the polarity reversal event. Requirements range from minimizing crosstalk to protocol signalling.

The device uses an external low voltage capacitor, C_{POL}, to set the reversal time. Once programmed, the reversal time will remain nearly constant over various load conditions. In addition, the reversal timing capacitor is isolated from the AC loop, so loop stability is not impacted.

The internal circuitry used to set the polarity reversal time is shown below.

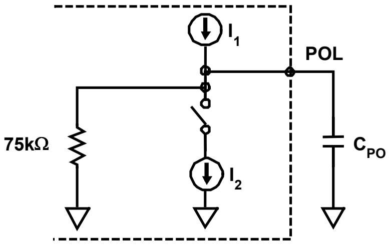


FIGURE 11: REVERSAL TIMING CONTROL

During Forward Active, the current from source I1 charges the external timing capacitor C_{POL} and the switch is open. The internal resistor provides a clamping function for voltages on the POL node. During Reverse Active, the switch closes and I2 (roughly twice I1) pulls current from I1 and the timing capacitor. The current at the POL node provides the drive to a differential pair which controls the reversal time (Δtime) according to the following relationship.

$$C_{POL} = \frac{\Delta time}{75000} \qquad \text{(EQ. 54)}$$

Polarized capacitors may be used for C_{POL} as the low voltage at the POL pin and minimal voltage excursion of ±0.75V, are well suited to such capacitors.

7.2.3.2. Power Dissipation

The power dissipation equations for Forward Active operation described above also apply to Reverse Active operation.

7.2.4. RINGING MODE

The Ringing mode (RNG, 100) provides linear amplification to support a variety of ringing waveforms. A programmable Ring Trip function provides loop supervision and auto disconnect upon Ring Trip. The device is designed to operate from the high battery during this mode.

7.2.4.1. Architecture

The device provides linear amplification to the signal applied to the Ringing Signal Input, VRS. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in the following figure.

The voltage gain from the VRS input to the TIP output is 40V/V. The resistor ratio provides a gain of 8 and the current mirror provides a gain of 5. The voltage gain from the VRS input to the RING output is -40V/V.

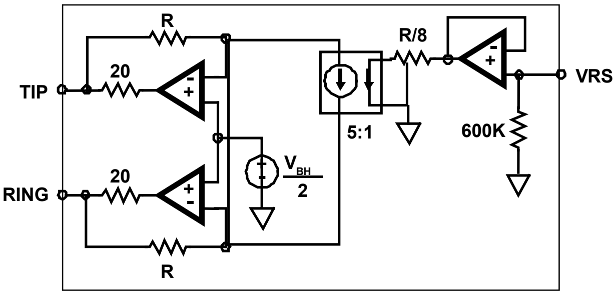


FIGURE 12: LINEAR RINGING MODEL

The equations for the TIP and RING outputs during ringing are provided below.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \qquad \text{(EQ. 55)}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \qquad \text{(EQ. 56)}$$

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs are available during ringing. This feature allows for DC offsets as part of the ringing waveform.

7.2.4.2. Ringing Signal Input

The Ringing Signal Input, VRS, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling of the ring signal. The VRS input is enabled only during the Ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum signal swing at VRS to achieve full scale ringing is approximately $2.4V_{P-P}$. The low signal levels are compatible with the output voltage range of the CODEC.

7.2.4.3. Logic Control

Ringing patterns consist of silent intervals. The ringing to silent pattern is called the ringing cadence. During the silent portion of ringing, the device can be programmed to any other operating mode. The most likely candidates are Low Power Standby or Forward Active. Depending on system requirements, the low or high battery may be selected.

Loop supervision is provided with the Ring Trip Detector. The Ring Trip Detector senses the change in loop current when the phone is taken off hook. The loop detector full wave rectifies the ringing current, which is then filtered with external components R_{RT} and C_{RT}. The resistor R_{RT} sets the trip threshold and the capacitor C_{RT} sets the trip response time. Most applications will require a trip response time of less than 150ms.

Three very distinct actions occur when the device detects a Ring Trip. First, the $\overline{\text{DET}}$ output is latched LOW. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the VRS input is disabled, removing the ring signal from the line. Third, the device is internally forced to the Forward Active mode.

7.2.4.4. Power Dissipation

The power dissipation during ringing is dictated by the load driving requirements and the ringing waveform. The key to valid power calculations is the correct definition of average and RMS currents. The average current defines the high battery supply current. The RMS current defines the load current.

The cadence provides a time averaging reduction in the peak power. The total power dissipation consists of the ringing power, P_r, and the silent interval power, P_s.

$$P_{RNG} = P_r \times \frac{t_r}{t_r + t_s} + P_s \times \frac{t_s}{t_r + t_s} \qquad \text{(EQ. 57)}$$

The terms t_R and t_S represent the cadence where t_R is the ringing interval and t_S the silent interval. The typical cadence ratio $t_R : t_S$ is 1 : 2.

The quiescent power of the device in the Ringing mode is defined as follows.

$$P_{r(Q)} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \qquad \text{(EQ. 58)}$$

The total power during the ringing interval is the sum of the quiescent power and loading power:

$$P_r = P_{r(Q)} + V_{BH} \times I_{AVG} - \frac{V_{RMS}^2}{Z_{REN} + R_{LOOP}} \qquad \text{(EQ. 59)}$$

For sinusoidal waveforms, the average current, I_{AVG}, is defined as follows.

$$I_{AVG} = \left(\frac{2}{\pi}\right) \frac{V_{RMS} \times \sqrt{2}}{Z_{REN} + R_{LOOP}} \qquad \text{(EQ. 60)}$$

The silent interval power dissipation will be determined by the quiescent power of the selected operating mode.

7.2.5. UNBALANCED RINGING MODE

The W671370 and W671371 also offer an Unbalanced Ringing mode (010). This feature is important for those Analog PBX Trunk Lines that require the Tip terminal to be held near ground for the duration of the ringing bursts. The Tip terminal is offset to 0V using an internal current source that is applied to the inverting input of the Tip amplifier. This reduces the differential ringing gain to 40V/V. The Ring terminal will center at VBH/2 and swing from -VBH to ground. As in Balanced Ringing mode, off-hook detection is accomplished by sensing the peak current and comparing it to a preset threshold. This allows the same sensing, comparing and threshold circuitry to be used in both Ringing and Unbalanced Ringing modes. This mode of operation does not require any additional external components.

7.2.6. FORWARD LOOP BACK MODE

The Forward Loop Back mode (FLB, 101) provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. The device is intended to operate from only the low battery during this mode.

7.2.6.1. Architecture

When the Forward Loop Back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers.

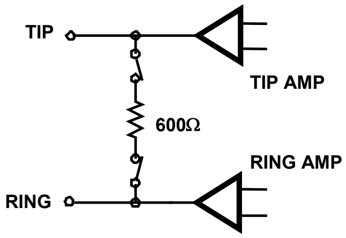


FIGURE 13: FORWARD LOOP BACK INTERNAL TERMINATION

7.2.6.2. DC Verification

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{\text{DET}}$ LOW, indicating the presence of loop current. In addition, the $\overline{\text{ALM}}$ output will also go LOW. In this mode this does not indicate a thermal alarm condition. Rather, proper logic operation is verified in the event of a thermal shutdown. In addition to verifying device functionality, toggling the logic outputs verifies the interface to the system controller.

7.2.6.3. AC Verification

The entire AC loop of the device is active during the Forward Loop Back mode. Therefore a 4-wire to 4-wire level test capability is provided. Depending on the transhybrid balance implementation, test coverage is provided by a one-step or two-step process (see Figure 6).

System architectures which cannot disable the transhybrid function require a two-step process. The first step would be to send a test tone to the device while on-hook and not in Forward Loop Back mode. The return signal would be the test level times the gain of the transhybrid amplifier (R_F/R_B). Since the device would not be terminated, cancellation would not occur. The second step would be to program the device to Forward Loop Back mode and resend the test tone. The return signal would be much lower in amplitude than the first step, indicating the device was active and the internal termination attenuated the return signal.

System architectures which disable the transhybrid function can achieve test coverage with a single step. Once the transhybrid function is disabled, program the device for Forward Loop Back mode and send the test tone. The return signal level is determined by the 4-wire to 4-wire gain of the device.

7.2.7. TIP OPEN MODE

The Tip Open mode (110) is intended for compatibility for some PBX interfaces. Used during idle line conditions, the device does not provide transmission. Loop supervision is provided by either the Switch Hook Detector (E0 = 1) or the Ground Key Detector (E0 = 0). The Ground Key Detector will be used in most applications. The device may be operated from either high or low battery.

7.2.7.1. Functionality

During Tip Open operation, the Tip switch is disabled and the Ring switch is enabled. The minimum Tip impedance is 30kΩ. The only active path through the device will be the Ring switch.

In keeping with the MTU characteristics of the device, Ring will not exceed -56V when operating from the high battery. Though MTU does not apply to tip open, safety requirements are satisfied.

7.2.8. POWER DENIAL MODE

The Power Denial Mode (111) will shutdown the entire device except for the logic interface. Loop supervision is not provided. This mode may be used as a sleep mode or to shut down in the presence of a persistent thermal alarm. Switching between high and low battery will have no effect during Power Denial.

7.2.8.1. Functionality

During Power Denial, both the Tip and Ring amplifiers are disabled, representing high impedances. The voltages at both outputs are near ground.

7.2.8.2. Thermal Shutdown

In the event the safe die temperature is exceeded, the $\overline{\text{ALM}}$ output will go LOW and $\overline{\text{DET}}$ will go HIGH and the part will automatically shut down. When the device cools, $\overline{\text{ALM}}$ will go HIGH and $\overline{\text{DET}}$ will reflect the loop status. If the thermal fault persists, $\overline{\text{ALM}}$ will go LOW again and the part will shut down. Programming Power Denial will permanently shutdown the device and stop the self-cooling cycling.

7.3. BATTERY SWITCHING

The integrated battery switch selects between the high battery and low battery. The battery switch is controlled with the logic input BSEL. When BSEL is a logic HIGH, the high battery is selected and when a logic LOW, the low battery is selected. All operating modes of the device can operate from high or low battery except Forward Loop Back.

7.3.1. Functionality

The logic control is independent of the operating mode decode. Independent logic control provides maximum flexibility and will support all application configurations.

When changing device operating states, battery switching should occur simultaneously with or prior to changing the operating mode. In most cases, this will minimize overall power dissipation and prevent glitches on the $\overline{\text{DET}}$ output.

The only external component required to support the battery switch is a diode in series with the VBH supply lead. In the event that high battery is removed, the diode allows the device to transition to low battery operation.

7.3.2. Low Battery Operation

All off-hook operating conditions should use the low battery. The prime benefit will be reduced power dissipation. The typical low battery for the device is -24V. However this may be increased to support longer loop lengths or high loop current requirements. Standby conditions may also operate from the low battery if MTU compliance is not required, further reducing standby power dissipation.

7.3.3. High Battery Operation

Other than ringing, the high battery should be used for standby conditions which must provide MTU compliance. During standby operation the power consumption is typically 85mW with -100V battery. If ringing requirements do not require full 100V operation, then a lower battery will result in lower standby power.

7.3.4. High Voltage Decoupling

The 100V rating of the device will require a capacitor of higher voltage rating for decoupling. Suggested decoupling values for all device pins are 0.1µF. Standard surface mount ceramic capacitors are rated at 100V. For applications driven by low cost and small size, the decoupling scheme shown below could be implemented.

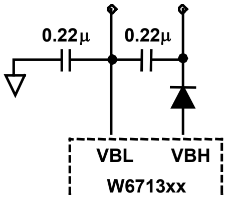


FIGURE 14: ALTERNATE DECOUPLING SCHEME

It is important to place the external diode between the VBH pin and the decoupling capacitor. Attaching the decoupling capacitor directly to the VBH pin will degrade the reliability of the device. This applies to both single and stacked and decoupling arrangements.

If VBL and VBH are tied together to override the battery switch function, then the external diode is not needed and the decoupling may be attached directly to VBH.

7.4. UNCOMMITTED SWITCH

The uncommitted switch is a three terminal device designed for system flexibility. The Switch Control logic input, $\overline{\text{SWC}}$, allows switch operation regardless of device operating mode. The switch is activated by a logic LOW. The positive and negative terminals of the switch are labeled SW+ and SW- respectively.

7.4.1. Relay Driver

The uncommitted switch may be used as a relay driver by connecting SW+ to the relay coil and SW- to ground. The switch is designed to have a maximum on voltage of 0.6V with a load current of 45mA.

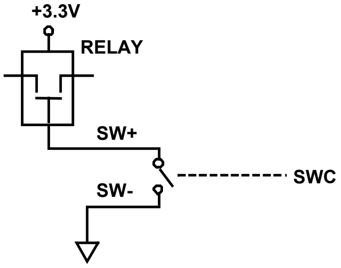


FIGURE 15: EXTERNAL RELAY SWITCHING

Since the device provides the ringing waveform, the relay functions which may be supported include subscriber disconnect, test access or line interface bypass. An external snubber diode is not required when using the uncommitted switch as a relay driver.

7.4.2. Test Load

The switch may be used to connect test loads across Tip and Ring. The test loads can provide external test termination for the device. Proper connection of the uncommitted switch to Tip and Ring is shown below.

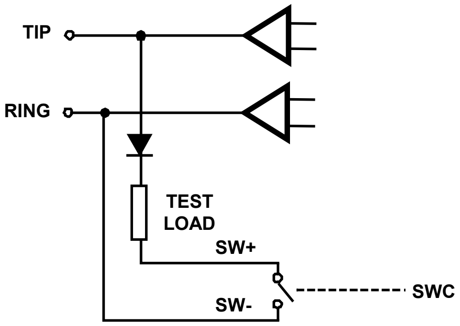


FIGURE 16: TEST LOAD SWITCHING

The diode in series with the test load blocks current from flowing through the uncommitted switch when the polarity of the Tip and Ring terminals are reversed. In addition to the Reverse Active mode, the polarity of Tip and Ring are reversed for half of the ringing cycle. With independent logic control and the blocking diode, the uncommitted switch may be continuously connected to the Tip and Ring terminals.

8. TIMING DIAGRAMS

As the W671300 family is a completely analog technology there are no timing diagrams.

9. ABSOLUTE MAXIMUM RATINGS

9.1. ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Condition	Value
Maximum Supply Voltages	V_{CC} = -0.5V to +7V $V_{CC} – V_{BH}$ = 110V Uncommitted Switch Voltage = -110V
Maximum Tip/Ring Negative Voltage Pulse [1]	V_{BH} -15V
Maximum Tip/Ring Positive Voltage Pulse [1]	+8V
ESD (Human Body Model)	1000V

Notes:

[1] Characterized with 2 x 10µs, and 10 x 1000µs first level lightning surge waveforms (GR-1089-CORE).

9.2. OPERATING CONDITIONS

Condition	Value
Temperature Ranges	Industrial (W6713x**0**): -40°C to 85°C Commercial (W6713x**1**): 0°C to 85°C Other (W6713x**2**): 0°C to 75°C
Positive Power Supply (V_{CC})	+3.3V, ±10%
Low Battery Power Supply (V_{BL})	-16V to -52V, ±5%
High Battery Power Supply (V_{BH})	W671310/30/71: V_{BL} to –100V, ±5% W671320/40: V_{BL} to –85V, ±10% W671352/61: V_{BL} to –75V, ±10%
Uncommitted Switch (loop back or relay driver)	+5V to –100V

9.3. THERMAL INFORMATION

Condition	Value	
Thermal Resistance (Typical)	Θ_{JA} (°C/W)	Θ_{JC} (°C/W)
PLCC [1]	53	N/A
QFN [2]	26	1
Maximum Junction Temperature Plastic	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s) (PLCC – Lead Tips Only)	300°C	

Notes:

[1] θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

[2] θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features . θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside.

9.4. DIE CHARACTERISTICS

Condition	Value
Substrate Potential	V_{BH}
Process	Bipolar-DI

CAUTION:
Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

10. ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified, T_A = -40°C to 85°C for industrial grade and T_A = 0°C to 85°C for commercial grade, V_{BL} = -24V, V_{BH} = -100V, -85V or -75V, V_{CC} = +3.3V, AGND = BGND = 0V, loop current limit = 25mA. All AC transmission parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300 Hz to 3.4 kHz. Protection resistors = 0Ω.

10.1. RINGING PARAMETERS

Parameter	Conditions	Min	Typ	Max	Units
VRS Input Impedance [1]		450	-	-	kΩ
Differential Ringing Gain [2]	Balanced Ringing, VRS to 2-Wire, $R_{LOAD} = \infty$	78	80	82	V/V
	Unbalanced Ringing, VRS to 2-Wire, $R_{LOAD} = \infty$	38	40	42	V/V
Centering Voltage Accuracy	Tip, Referenced to $V_{BH}/2 + 0.5$ [3]	-	± 2.5	-	V
	Ring, Referenced to $V_{BH}/2 + 0.5$	-	± 2.5	-	V
Open Circuit Ringing Voltage	Balanced Ringing, VRS Input = $0.840V_{RMS}$	-	67	-	V_{RMS}
	Unbalanced Ringing, VRS Input = $0.840V_{RMS}$	-	33.5	-	V_{RMS}
Ringing Voltage Total Distortion	R_L = 1.3 kΩ, $V_{T-R} = \|V_{BH}\| -5$	-	-	4.0	%
4-Wire to 2-Wire Ringing Off Isolation	Active Mode, Referenced to VRS Input	-	90	-	dB
2-Wire to 4-Wire Transmit Isolation	Ringing Mode Referenced to the Differential Ringing Amplitude	-	80	-	dB

Notes:

[1]. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

[2]. Differential Ringing Gain is measured with VRS = 0.795VRMS for -100V devices, VRS = 0.663 VRMS for -85V devices and VRS = 0.575VRMS for -75V devices.

[3]. For Unbalanced Ringing the Tip terminal is offset to 0V and the Ring terminal is centered at Vbh/2 + 0.5V.

10.2. AC TRANSMISSION PARAMETERS

Parameters	Conditions	Min	Typ	Max	Units
Auxiliary Input Impedance [1]		160	-	-	kΩ
Transmit Output Impedance [1]		-	-	1	Ω
4-Wire Port Overload Level	THD = 1%	-	1	-	V_{PK}
2-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PK}
2-Wire Return Loss	300Hz	-	24	-	dB
	1kHz	-	40	-	dB
	3.4kHz	-	21	-	dB
2-Wire Longitudinal Balance [2, 3] 300Hz to 1kHz	Forward Active W671310/20	58	62	-	dB
	Forward Active W671330/40/52	53	59	-	dB
2-Wire Longitudinal Balance [2, 3] 1kHz to 3.4kHz	Forward Active W671310/20	54	58	-	dB
	Forward Active W671330/40/52	53	58	-	dB
4-Wire Longitudinal Balance [2, 3] 300Hz to 1kHz	Forward Active W671310/20	58	67	-	dB
	Forward Active, W671330/40/52	53	64	-	dB
4-Wire Longitudinal Balance [2, 3] 1kHz to 3.4kHz	Forward Active W671310/20	54	66	-	dB
	Forward Active, W671330/40/52	53	63	-	dB
2-Wire to 4-Wire Level Linearity 4-Wire to 2-Wire Level Linearity Referenced to -10 dBm	+3 to -40 dBm, 1kHz	-	±0.025	-	dB
	-40 to -50 dBm, 1kHz	-	±0.050	-	dB
	-50 to -55 dBm, 1kHz	-	±0.100	-	dB
Longitudinal Current Capability Per Wire [1]	OHT Active	20	-	-	mA_{RMS}
4-Wire to 2-Wire Insertion Loss		-0.20	0.00	+0.20	dB
2-Wire to 4-Wire Insertion Loss		-6.22	-6.02	-5.82	dB
4-Wire to 4-Wire Insertion Loss		-6.22	-6.02	-5.82	dB
Forward Active Idle Channel Noise [3]	2-Wire C-Message, T = 25°C	-	10	13	dBrnC
	4-Wire C-Message, T = 25°C	-	4	7	dBrnC
Reverse Active Idle Channel Noise [3]	2-Wire C-Message, T = 25°C	-	10	13	dBrnC
	4-Wire C-Message, T = 25°C	-	4	7	dBrnC

Notes:

[1] *These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.*

[2] *Longitudinal Balance is tested per IEEE455-1985, with 368Ω per Tip and Ring terminal.*

[3] These parameters are tested 100% at room temperature. These parameters are guaranteed not tested across temperature via statistical characterization and design.

10.3. DC PARAMETERS

Parameters	Conditions	Min	Typ	Max	Units
Off Hook Loop Current Limit	Programming Accuracy (1% Programming Resistor)	-8.5	-	+8.5	%
	Programming Range	15	-	45	mA
Off Hook Transient Current Limit	Programming Accuracy (1% Programming Resistor)	-10	-	+10	%
	Programming Range	40	-	100	mA
Loop Current During Low Power Standby	Forward Polarity Only	18	-	26	mA
Open Circuit Voltage (|Tip - Ring|)	V_{BL} = -16V	-	8.0	-	V_{DC}
	V_{BL} = -24V	14	15.5	17	V_{DC}
	V_{BH} > -60V	43	49	-	V_{DC}
Low Power Standby, Open Circuit Voltage (Tip - Ring)	V_{BL} = -48V	-	44.5	-	V_{DC}
	V_{BH} > -60V	43	51.5	-	V_{DC}
Absolute Open Circuit Voltage	V_{RG} in LPS and FA; V_{TG} in RA; V_{BH} > -60V	-	-53	-56	V_{DC}

10.4. TEST ACCESS FUNCTIONS

Parameters	Conditions	Min	Typ	Max	Units
Switch On Voltage	I_{OL} = 45 mA	-	0.20	0.60	V
Loopback Max Battery (V_{BL} or V_{BH})		-	-	52	V

10.5. LOOP DETECTORS & SUPERVISORY FUNCTIONS

Parameters	Conditions	Min	Typ	Max	Units
Switch Hook Programming Range		5	-	15	mA
Switch Hook Programming Accuracy	(1% Programming Resistor)	-10	-	+10	%
Dial Pulse Distortion		-	1.0	-	%
Ring Trip Comparator Threshold		1.12	1.25	1.37	V
Ring Trip Programming Current Accuracy	(1% Programming Resistor)	-10	-	+10	%
Ground Key Threshold		-	12	-	mA
E0 Transition, $\overline{\text{DET}}$ Output Delay		-	20	-	µs
Thermal Alarm Output	IC Junction Temperature	-	175	-	oC

10.6. LOGIC INPUTS (F0, F1, F2, E0, $\overline{\text{SWC}}$, BSEL)

Parameters	Conditions	Min	Typ	Max	Units
Input Low Voltage		-	-	0.8	V
Input High Voltage		2.0	-	-	V
Input Low Current	$V_{IL} = 0.4V$	-20	-10	-	µA
Input High Current	$V_{IH} = 2.4V$	-	-	1	µA

10.7. LOGIC OUTPUTS ($\overline{\text{DET}}$, $\overline{\text{ALM}}$)

Parameters	Conditions	Min	Typ	Max	Units
Output Low Voltage	$I_{OL} = 5$ mA	-	.15	0.4	V
Output High Voltage	$I_{OH} = 100$ µA	2.4	2.8	-	V

10.8. SUPPLY CURRENTS

Parameters	Conditions	Min	Typ	Max	Units
Low Power Standby, BSEL = 1	I_{CC}	-	3.9	6.0	mA
	I_{BH}	-	0.66	0.90	mA
Forward or Reverse Active, BSEL = 0	I_{CC}	-	4.9	6.5	mA
	I_{BL}		1.2	2.5	mA
Forward Active, BSEL = 1	I_{CC}	-	7.0	9.5	mA
	I_{BL}	-	0.9	2.0	mA
	I_{BH}	-	2.2	3.0	mA
Ringing, BSEL = 1 (Balanced Ringing, 100)	I_{CC}	-	6.4	9.0	mA
	I_{BL}	-	1.0	1.3	mA
	I_{BH}	-	2.0	3.0	mA
Ringing, BSEL = 1 (Unbalanced Ringing, 010)	I_{CC}	-	9.3		mA
	I_{BL}	-	1.0	1.3	mA
	I_{BH}	-	2.4	3.0	mA
Forward Loopback, BSEL = 0	I_{CC}	-	10.3	13.5	mA
	I_{BL}	-	23.5	32	mA
Tip Open, BSEL = 1	I_{CC}	-	3.8	5.5	mA
	I_{BL}	-	0.4	1.0	mA
	I_{BH}	-	0.6	1.0	mA
Power Denial, BSEL = 0 or 1	I_{BH}	-	0.4	0.6	mA
	I_{CC}	-	4.0	6.0	mA
	I_{BL}	-	0.4	1.0	mA

10.9. ON-HOOK POWER DISSIPATION [1]

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Forward or Reverse	V_{BL} = -24V	-	55	-	mW
Low Power Standby	V_{BH} = -100V	-	85	-	mW
	V_{BH} = -85V	-	75	-	mW
	V_{BH} = -75V	-	65	-	mW
Ringing	V_{BH} = -100V	-	250	-	mW
	V_{BH} = -85V	-	230	-	mW
	V_{BH} = -75V	-	225	-	mW

Notes:

[1]. *The power dissipation is based on actual device measurements and will be less than worst case calculations based on data sheet supply current limits.*

10.10. OFF HOOK POWER DISSIPATION [1]

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Forward or Reverse	V_{BL} = -24V	-	305	-	mW

Notes:

[1]. *The power dissipation is based on actual device measurements and will be less than worst case calculations based on data sheet supply current limits.*

10.11. POWER SUPPLY REJECTION RATIO

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Units**
V_{CC} to 2-Wire	f = 300Hz	-	40	-	dB
	f = 1kHz	-	35	-	dB
	f = 3.4kHz	-	28	-	dB
V_{CC} to 4-Wire	f = 300Hz	-	45	-	dB
	f = 1kHz	-	43	-	dB
	f = 3.4kHz	-	33	-	dB
V_{BL} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	30	-	dB
V_{BL} to 4-Wire	300Hz ≤ f ≤ 3.4kHz	-	35	-	dB
V_{BH} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	33	-	dB
V_{BH} to 4-Wire	300Hz ≤ f ≤ 1kHz	-	40	-	dB
	1kHz ≤ f ≤ 3.4kHz	-	45	-	dB

11. TYPICAL APPLICATION CIRCUIT

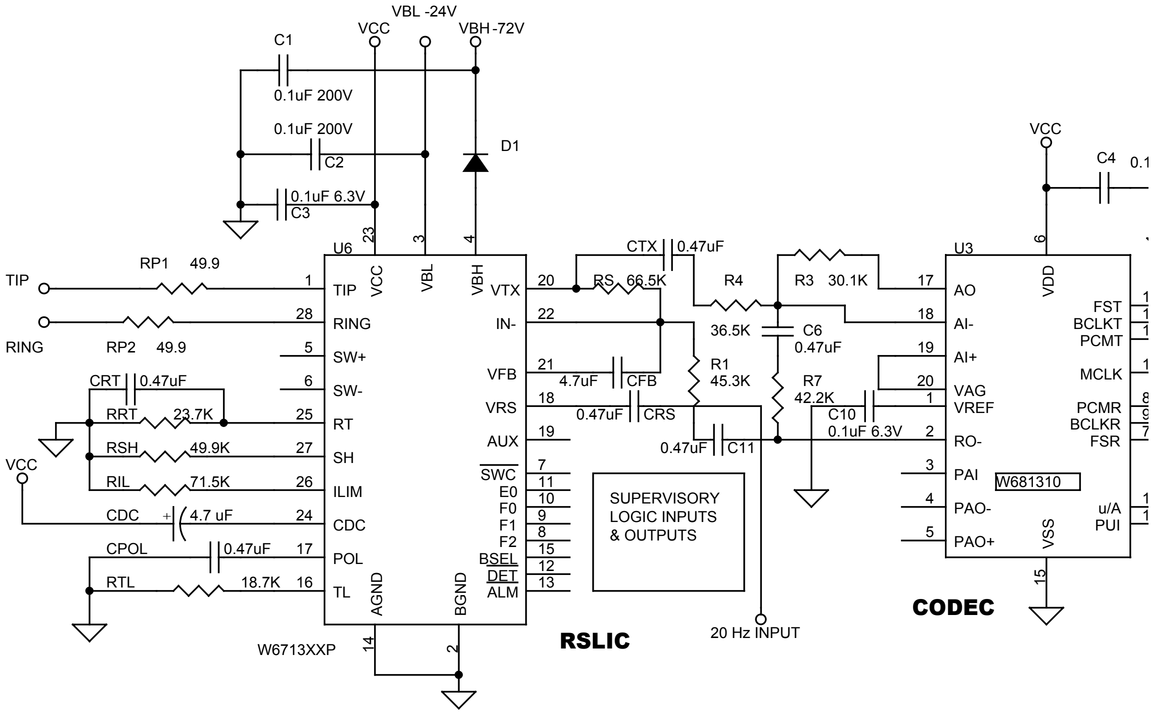
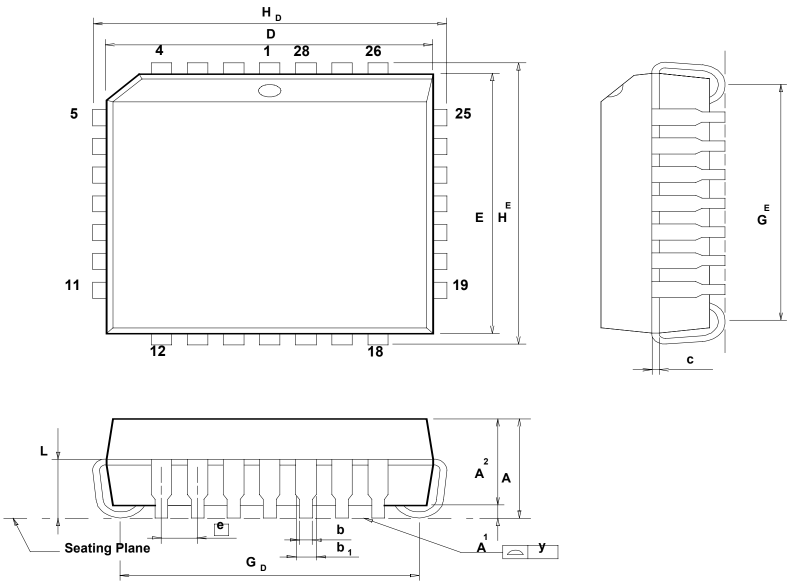


FIGURE 17: CODEC PLUS RSLIC APPLICATION DIAGRAM

12. PACKAGE SPECIFICATION

12.1. 28L PLCC

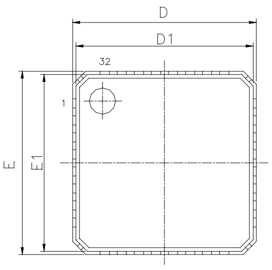


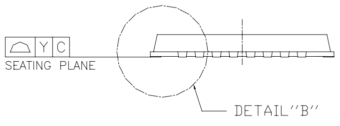
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.185	——	——	4.70
A_1	0.020	——	——	0.51	——	——
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.448	0.453	0.458	11.38	11.51	11.63
E	0.448	0.453	0.458	11.38	11.51	11.63
$\boxed{e}$	0.050 BSC			1.27 BSC		
G_D	0.390	0.410	0.430	9.91	10.41	10.92
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.480	0.490	0.500	12.91	12.45	12.70
H_E	0.480	0.490	0.500	12.91	12.45	12.70
L	0.090	0.100	0.110	2.29	2.54	2.79
y	——	——	0.004	——	——	0.10

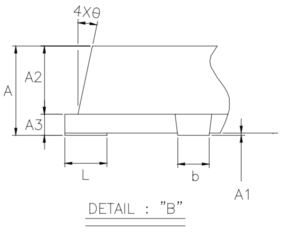
Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Inch
4. General appearance spec. should be based on final visual inspection spec.

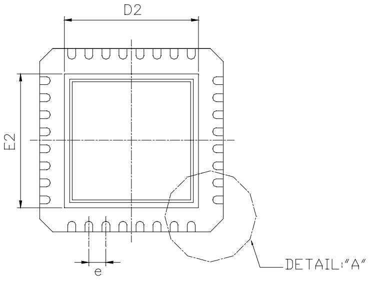
12.2. 32L QFN PACKAGE

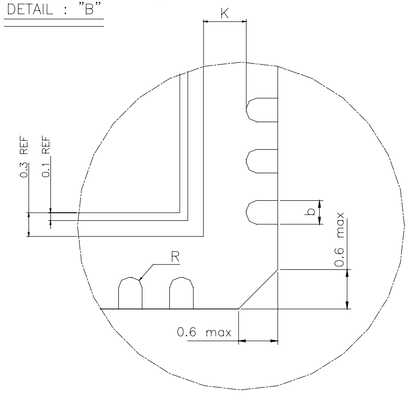






DETAIL : "B"





DETAIL : "A"

Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	4.96	5.11	5.26	0.195	0.201	0.207
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
E2	4.96	5.11	5.26	0.195	0.201	0.207
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.13	---	---	0.005	---	---
K	0.20	---	---	0.008	---	---
θ	0°	---	12°	0°	---	12°

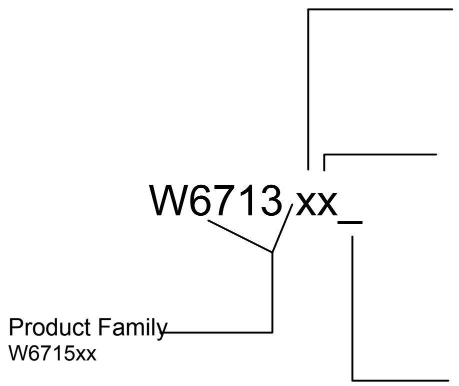
*D2,*E2:By die size difference.

12.2.1. Special Considerations for the QFN Package

The Quad Flatpack No-lead (QFN) package offers a significant footprint reduction (65%) and improved thermal performance with respect to the 28 lead PLCC. To realize the thermal enhancements and maintain the high voltage (-100V) performance, the exposed pad on the bottom of the QFN package should be soldered to a power/heat sink plane that is electrically connected to Substrate Common Connection (SCC) pin. The heat is distributed evenly across the board by way of the heat sink plane. This is accomplished by using conductive thermal vias.

13. ORDERING INFORMATION

Product Number Descriptor Key



Battery Voltage / Longnitudinal Balance:

	100V	85V	75V
58dB	**1/7**	**2**	
53dB	**3**	**4**	**5/6**

Temperature Range:

0 = -40°C to 85°C
1 = 0°C to 85°C
2 = 0°C to 75°C

Package Type:

P = 28-Lead Plastic Leaded Chip Carrier Package (PLCC)
Y = 32-Lead Quad Flat No Lead Package (QFN)

When ordering the W671300 series of devices, please refer to the following part numbers.

PART NUMBER	HIGH BATTERY (VBH)			LONGITUDINAL BALANCE		FULL TEST	TEMP. RANGE °C	PACKAGE
	100V	85V	75V	58dB	53dB			
W671310P	●			●		●	-40 to 85	PLCC 28
W671320P		●		●		●	-40 to 85	PLCC 28
W671330P	●				●	●	-40 to 85	PLCC 28
W671340P		●			●	●	-40 to 85	PLCC 28
W671352P			●		●		0 to 75	PLCC 28
W671352Y			●		●		0 to 75	QFN 32
W671361P			●		●	●	0 to 85	PLCC 28
W671361Y			●		●	●	0 to 85	QFN 32
W671371P	●				●	●	0 to 85	PLCC 28
W671371Y	●				●	●	0 to 85	QFN 32

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	March 2004	All	Preliminary Specifications

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