4705B/4705BX

ARITHMETIC LOGIC REGISTER STACK

FAIRCHILD CMOS MACROLOGIC™

DESCRIPTION — The Arithmetic Logic Register Stack (ALRS) is designed to implement accumulators in high performance microprogrammed digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0-A_2). The result of the operation is loaded into the same RAM location and simultaneously, is loaded into the Output Register making it available at the 3-state output data bus.

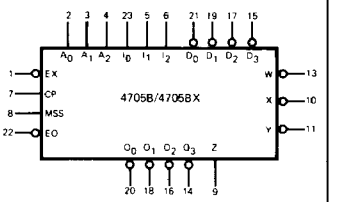
The 4705B/4705BX operates on four bits of data but features are provided for expansion to longer word lengths. Carry propagate and carry generate facilities are provided for an external carry lookahead where maximum operating speed is required. In applications where high-speed arithmetic is not needed, ripple expansion may also be implemented. The 4705B/4705BX provides three status signals: Zero, Negative and Overflow. These qualify the result of an operation. The 4705B/4705BX is fully compatible with all CMOS families. The 4705B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V. The 4705BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **VERY LOW POWER DISSIPATION**
- **EIGHT ACCUMULATORS IN A SINGLE PACKAGE**
- **HIGH SPEED—3.8 MHz MICROINSTRUCTION RATE TYPICALLY AT V_{DD}=10V**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES STATUS — ZERO, NEGATIVE, AND OVERFLOW**
- **3-STATE OUTPUTS**
- **SLIM 24-PIN PACKAGE**

PIN NAMES

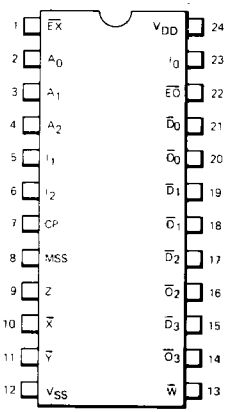
$\overline{D}_0$ - $\overline{D}_3$	Data Inputs (Active LOW)
A_0 - A_2	Address Instruction Inputs
I_0 - I_2	ALU Instruction Inputs
MSS	Most Significant Slice Input (Active HIGH)
CP	Clock Input
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Data Outputs (Active LOW)
$\overline{W}$	Ripple Carry Outputs (Active LOW)
$\overline{X}$	Carry Propagate Output
$\overline{Y}$	Carry Generate Output
Z	Zero Status Output (Active HIGH, Open Collector)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM

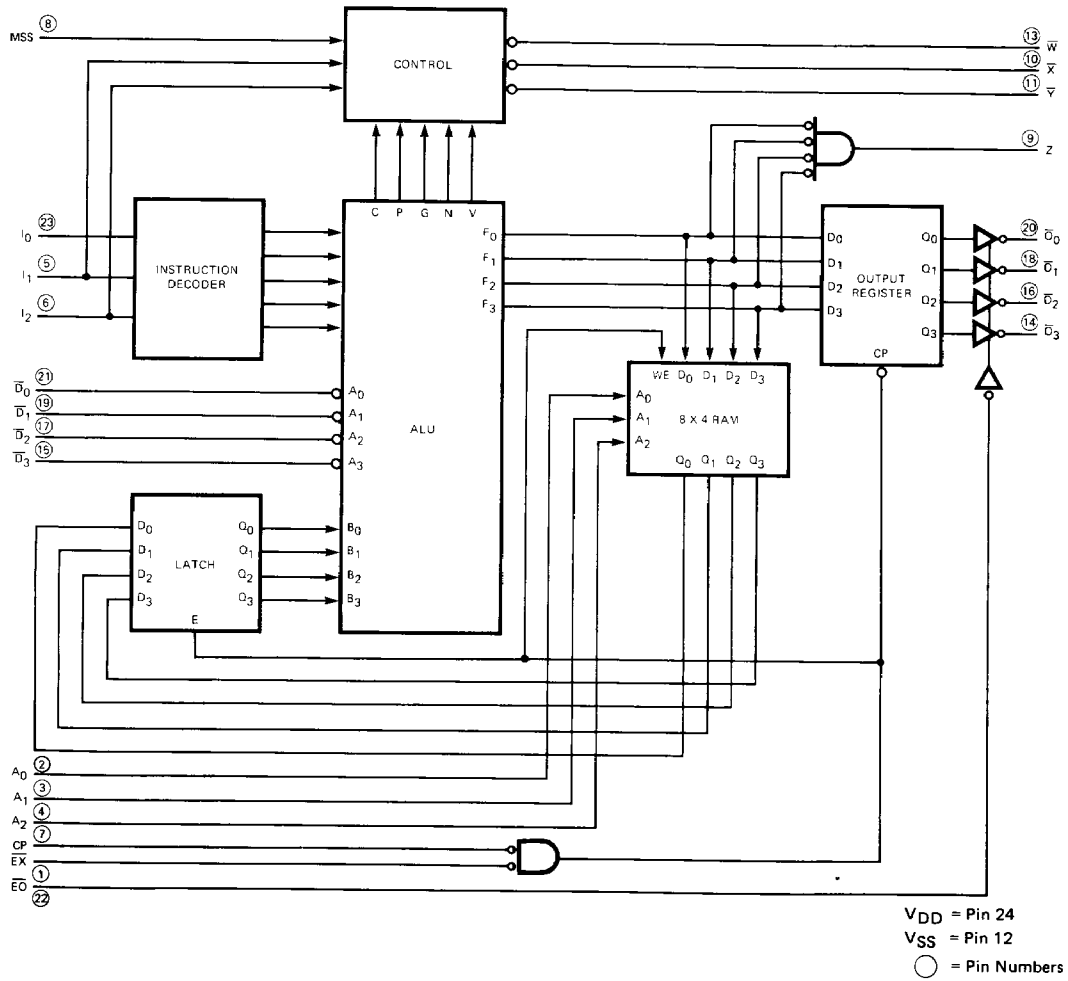


TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2 I_1 I_0	INTERNAL OPERATION	
L L L	R_X plus D-Bus plus 1 → R_X	Accumulate
L L H	R_X plus D-Bus → R_X	Accumulate
L H L	R_X • D-Bus → R_X	Logical AND
L H H	D-Bus → R_X	Load
H L L	R_X → Output Register	Output
H L H	R_X + D-Bus →	Logical OR
H H L	R_X ⊕ D-Bus → R_X	Exclusive OR
H H H	D-Bus → R_X	Load Complement

H = HIGH Level L = LOW Level

NOTES:

1. R_X is the RAM location addressed by A_0-A_2.
2. The result of any operation is always loaded into the Output Register.

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 4705B/4705BX Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an Instruction Decoder, Control Logic and a 4-bit Output Register.

The ALU receives the active LOW input data ($\overline{D}_0$–$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and Output Register. The active LOW output data ($\overline{O}_0$–$\overline{O}_3$) is obtained from the Output Register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level EO disables the buffers (high impedance state).

The instruction bus for the 4705B/4705BX consists of two fields, A and I; A_0–A_2 specify the desired location of the RAM and I_0–I_2 specify the desired function to be performed. *Table 1* lists instruction code assignments. Thus, the 4705B/4705BX provides eight accumulators (R_0–R_7) and eight different operations may be performed on any of these accumulators. The I_0–I_2 inputs are decoded by the Instruction Decoder to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: Carry Out (C), Carry Propagate (P), Carry Generate (G), Negative (N) and Overflow (V) status. The control logic manipulates the status signals as a function of I_0–I_2 and a control input MSS. A HIGH on the MSS input declares the most significant slice in a 4705B/4705BX array (the MSS can be tied directly to V_{DD}). All devices, except the most significant 4705B/4705BX should have a LOW level (ground) on the MSS input. The control logic generates three device outputs ($\overline{W}$, $\overline{X}$ and $\overline{Y}$) for arrayed operation. An all zero result from the ALU is decoded and presented at the open collector Zero (Z) output.

The I_0 input serves a dual purpose. For arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 4705B/4705BX expansion schemes.

Operation – The 4705B/4705BX operates on a single clock. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$–$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0–I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. The A lines must obviously be held stable during this time. On the LOW-to-HIGH transition of the CP, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

EXPANSION – The 4705B/4705BX is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 4705B/4705BX provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 4705B/4705BX's. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices. The Z output is open drain and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four 4705B/4705BX's. The MSS input is tied to V_{DD} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-field and I-field. A-field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, it assumes the state of the I_0 input. Thus, in *Figure 1*, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 inputs together to form the I-field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

The $\overline{X}$ output of device 4 is LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP. *Figure 2* shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 4582B in addition to the four 4705B/4705BX's in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs together with the I_0 input of device 1 from the I-field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the 4582B Carry Outputs (C_{n+x},C_{n+z} respectively). Also the P and G inputs of

4582B are connected to $\overline{X}$ and $\overline{Y}$ outputs of the 4705B/4705BX as shown. The control logic in the 4705B/4705BX (see block diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs as well as the Carry Generate and Carry Propagate outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ output of device 4 is the carry output from the array. Also note that the I_0 input of device 1 is not only an instruction input but also provides the carry input to the array so the I_0 input of device 1 must be connected to the appropriate 4582B input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 4705B/4705BX forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ outputs on all except the most significant slice. An examination of the 4582B logic reveals that whenever P is LOW and G is HIGH the associated carry output is the same as the carry input. Thus, in *Figure 2* devices 2, 3, and 4 will assume the logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent Negative and Overflow from the array.

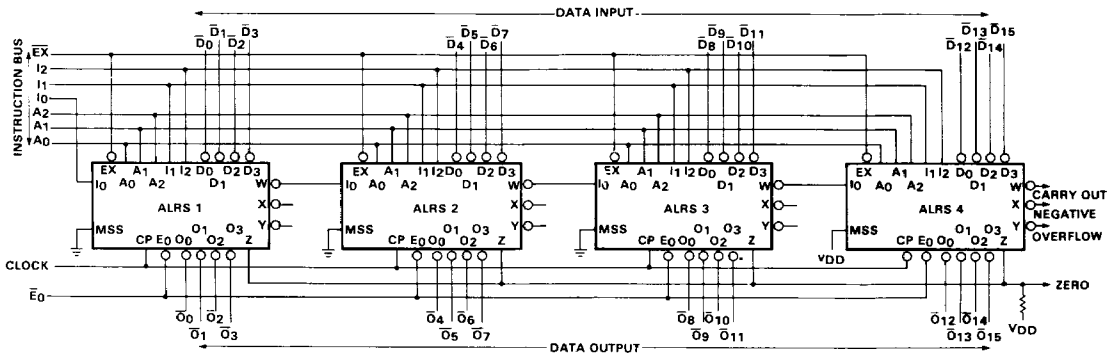


Fig. 1
RIPPLE CARRY EXPANSION

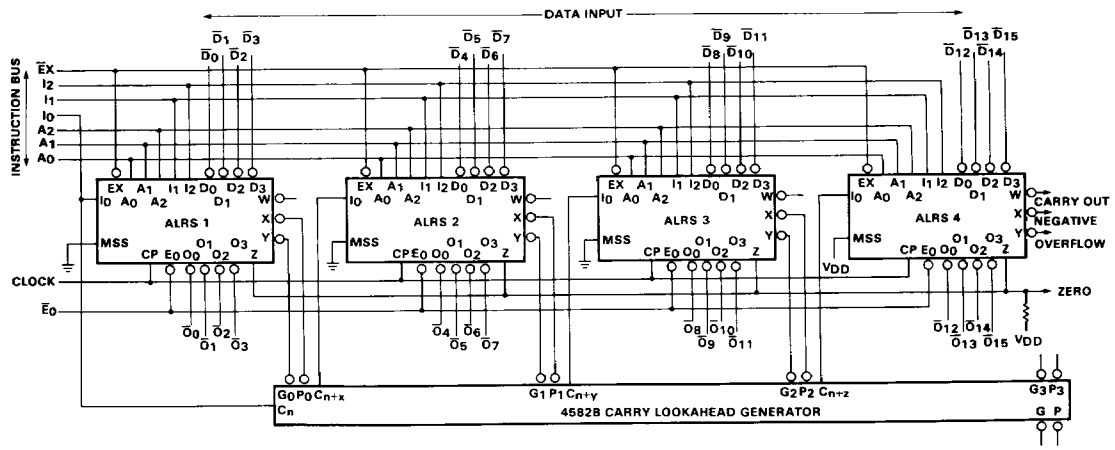


Fig. 2
CARRY LOOKAHEAD EXPANSION

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 3)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS} $\overline{EO}$ = V_{DD}
											- 12		MAX	
		XM									-0.4		MIN, 25°C	
											- 12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35		MIN, 25°C	
					250			500			1000		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} = 0 V, T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (Note 6)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		163	326		71	142		50	100	ns	$\overline{EO}$ = $\overline{EX}$ = V_{SS}
t_{PHL}	CP to $\overline{O}_n$		174	348		70	140		49	98		
t_{PLH}	Propagation Delay,		120	240		55	110		39	78	ns	I_1 or I_2 = V_{DD}
t_{PHL}	I_0 to $\overline{W}$		139	278		56	112		40	80		
t_{PLH}	Propagation Delay,		251	502		101	202		71	142	ns	I_1 or I_2 = V_{SS}
t_{PHL}	$\overline{D}_n$ to $\overline{W}$		186	372		61	122		43	86		
t_{PLH}	Propagation Delay,		382	764		150	300		105	210	ns	MSS = V_{DD}
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		363	726		140	280		98	196		I_1 = I_2 = V_{SS}
t_{PLH}	Propagation Delay,		161	322		58	116		41	82	ns	MSS = I_1 = I_2 =
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		239	478		90	180		63	126		V_{SS}
t_{PLH}	Propagation Delay,		211	422		96	192		68	136	ns	MSS = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{X}$, $\overline{Y}$		266	532		109	218		77	154		
t_{PLH}	Propagation Delay,		360	720		179	358		126	262	ns	R_L = 1kΩ to
t_{PHL}	$\overline{D}_n$ to Z		251	502		95	190		67	134		V_{DD}
t_{PLH}	Propagation Delay,		198	396		83	166		59	118	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to $\overline{W}$		226	452		87	174		61	122		
t_{PLH}	Propagation Delay,		152	304		73	146		52	104	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{W}$		252	504		104	208		73	146		
t_{PLH}	Propagation Delay,		317	634		123	246		87	174	ns	I_1 = I_2 = MSS =
t_{PHL}	$\overline{D}_3$ to $\overline{X}$		401	802		152	304		107	214		V_{DD}
t_{PLH}	Propagation Delay,		397	794		161	322		113	226	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		538	1076		213	426		150	300		V_{SS}
t_{PLH}	Propagation Delay,		527	1054		205	410		144	288	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		668	1336		269	538		189	378		MSS = V_{DD}
t_{PLH}	Propagation Delay,		519	1038		202	404		142	284	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$		695	1380		279	558		196	392		V_{DD}
t_{PLH}	Propagation Delay,		556	1112		229	458		161	322	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{W}$		415	830		161	322		113	226		
t_{PLH}	Propagation Delay,		512	1024		236	472		166	332	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to Z		618	1236		245	490		172	344		
t_{PLH}	Propagation Delay,		143	286		71	142		50	100	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{X}$, $\overline{Y}$		338	676		134	268		94	188		MSS = V_{DD}
t_{PLH}	Propagation Delay,		171	342		85	170		60	120	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to $\overline{X}$, $\overline{Y}$		304	608		118	236		83	166		MSS = V_{DD}
t_{PLH}	Propagation Delay,		370	740		186	392		131	262	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to Z		276	552		109	218		77	154		
t_{PLH}	Propagation Delay,		298	596		155	310		109	218	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to Z		177	354		70	140		49	98		
t_{PZH}	Output Enable		71	142		36	72		26	52	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	Time		58	116		27	54		19	38		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable		71	142		40	80		28	56	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	Time		79	158		42	84		30	60		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition		95	190		54	108		38	76	ns	C_L = 50 pF
t_{THL}	Time		67	134		27	54		19	38		

Notes on following page.

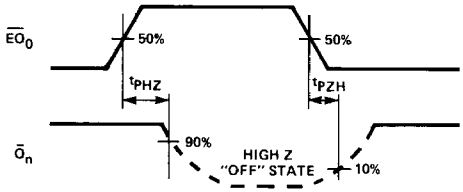
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: (Cont'd)

V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 4)

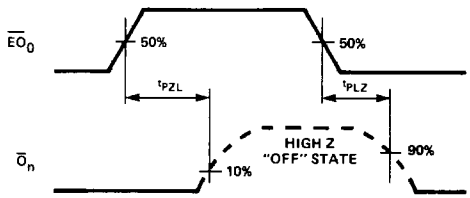
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (Note 6)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{CW}	Minimum Clock Period	1018	509		526	263		370	185		ns	C_L = 50 pF, R_L = 200 kΩ, $\overline{EX}$ = V_{SS}
$t_WCP(L)$	CP Minimum Pulse Width (LOW)	214	107		102	51		72	36		ns	
$t_WCP(H)$	CP Minimum Pulse Width (HIGH)	484	242		222	111		156	78		ns	
t_s	Set-UP Time, $\overline{EX}$ to CP	326	163		198	99		134	67		ns	
t_h	Hold Time, $\overline{EX}$ to CP	20	0		15	0		10	0			
t_s	Set-Up Time, A_n to CP	452	226		168	84		118	59		ns	
t_h	Hold Time, A_n to CP	20	0		15	-1		10	0			
t_s	Set-Up Time, $\overline{D}_n$ to CP	500	250		198	99		140	70		ns	
t_h	Hold Time, $\overline{D}_n$ to CP	-35	-69		-11	-21		-8	-15			
t_s	Set-Up Time, I_n to CP	502	251		224	112		158	79		ns	
t_h	Hold Time, I_n to CP	-29	-57		-12	-23		-9	-17			
f_{MAX}	Input Count Frequency (Note 1)	0.98	1.97		1.9	3.8		2.47	4.94		MHz	

NOTES:
1. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
2. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V and 3 μs at V_{DD} = 15 V.
3. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
4. Propagation Delays and Output transition times are graphically described in this section under 4000B Series CMOS Family Characteristics.
5. The Internal Clock is generated from CP and $\overline{EX}$. The Internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW. For timing considerations the $\overline{EX}$, CP two input active LOW AND gate is considered to exhibit no propagation delay. Actual timing requirements are referenced to the external CP and $\overline{EX}$ inputs.
6. Input Transition Times ≤ 20 ns.

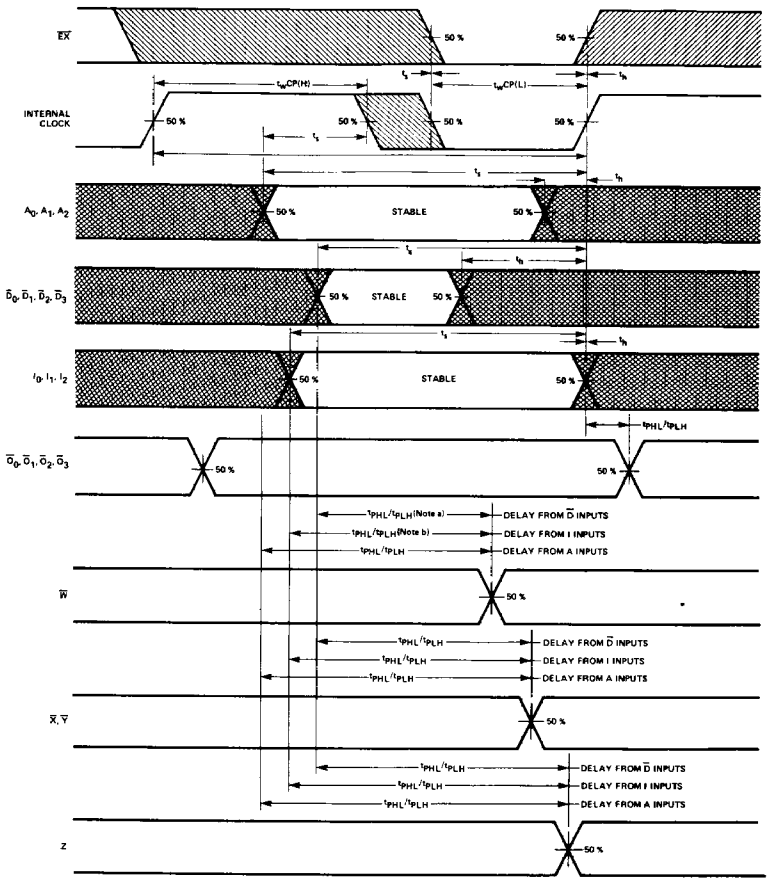
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



PROPAGATION DELAYS, A_n to Z, I_n to Z, $\overline{D}_n$ to Z, A_n to $\overline{X}$, $\overline{Y}$, I_n to $\overline{X}$, $\overline{Y}$, $\overline{D}_n$ to $\overline{X}$, $\overline{Y}$, A_n to $\overline{W}$, I_n to $\overline{W}$, $\overline{D}_n$ to $\overline{W}$, I_n to $\overline{O}_n$ SET-UP AND HOLD TIMES $\overline{EX}$ TO CP, A_n TO CP, $\overline{D}_n$ to CP, I_n to CP, MINIMUM INTERNAL CLOCK PULSE

NOTES:
a. Delay for logical operation (I_1 or I_2 = HIGH)
b. Delay for arithmetic operation (I_1 = I_2 = LOW)
c. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.