

TC74HC590AP/AF

8-BINARY COUNTER/REGISTER WITH 3-STATE OUTPUTS

The TC74HC590A is a high speed CMOS 8-BIT COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

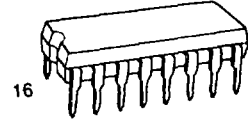
The internal counter counts on the positive going edge of Counter Clock (CCK) when Counter Clock Enable (CCKEN) is low. When Counter Clear (CCLR) is low, the internal counter is cleared asynchronously to the clock.

Data in the internal counter are loaded into the register at positive going edge of Register Clock (RCK), and the register outputs are controlled by enable input (G).

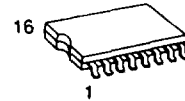
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed $f_{MAX}=62\text{MHz}$ (Typ.) at $V_{CC}=5\text{V}$
- Low Power Dissipation $I_{CC}=4\mu\text{A}$ (Max.) at $T_a=25^\circ\text{C}$
- High Noise Immunity $V_{NH}=V_{NL}=28\% V_{CC}$ (Min.)
- Output Drive Capability 15 LSTTL Loads For QA~QH
10 LSTTL Loads For RCO
- Symmetrical Output Impedance $|I_{OH}|=I_{OL}=6\text{mA}$ (Min.)
For QA~QH
 $|I_{OH}|=I_{OL}=4\text{mA}$ (Min.)
For RCO
- Balanced Propagation Delays $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range $V_{CC}(\text{opr})=2\text{V}\sim 6\text{V}$
- Pin and Function Compatible with 74LS590

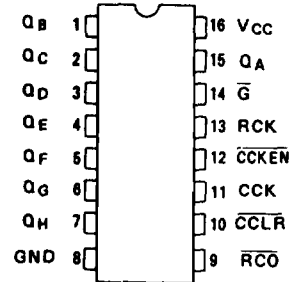


P (DIP 16-P-300A)



F (SOP 16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

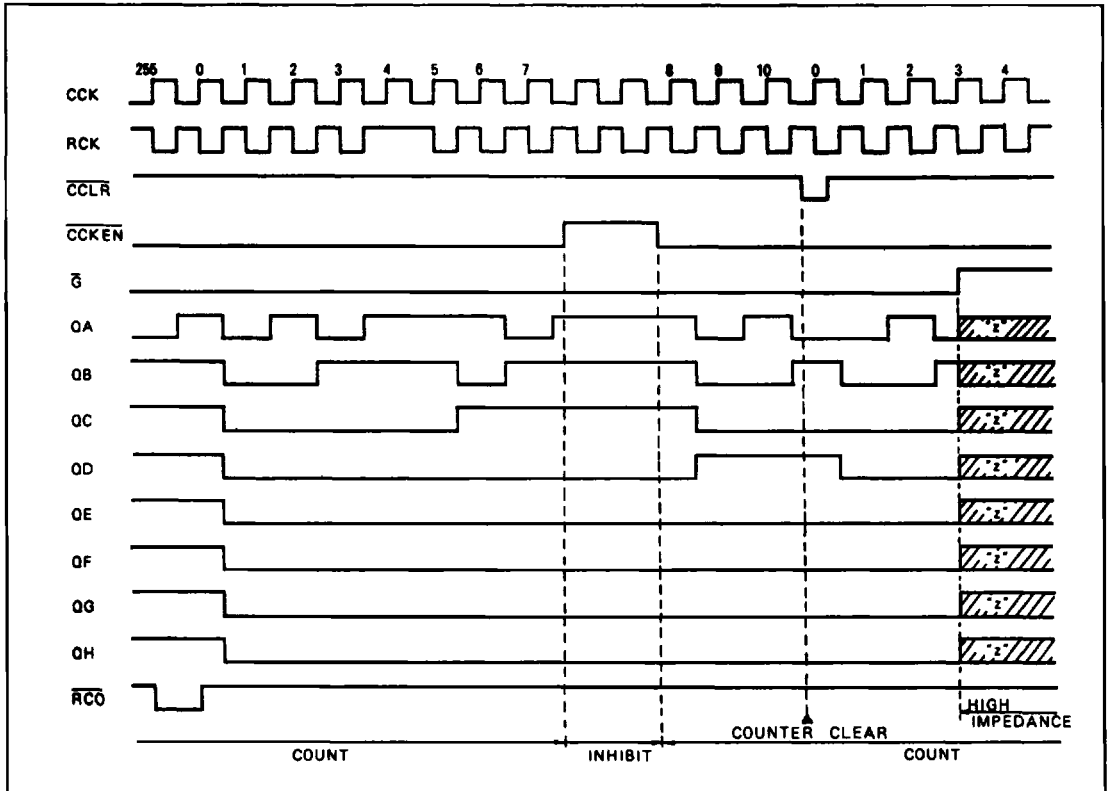
TRUTH TABLE

INPUT					FUNCTION
G	RCK	CCLR	CCKEN	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	\uparrow	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	\downarrow	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	\uparrow	ADVANCE ONE COUNT.
X	X	H	L	\downarrow	NO COUNT
X	X	H	H	X	NO COUNT

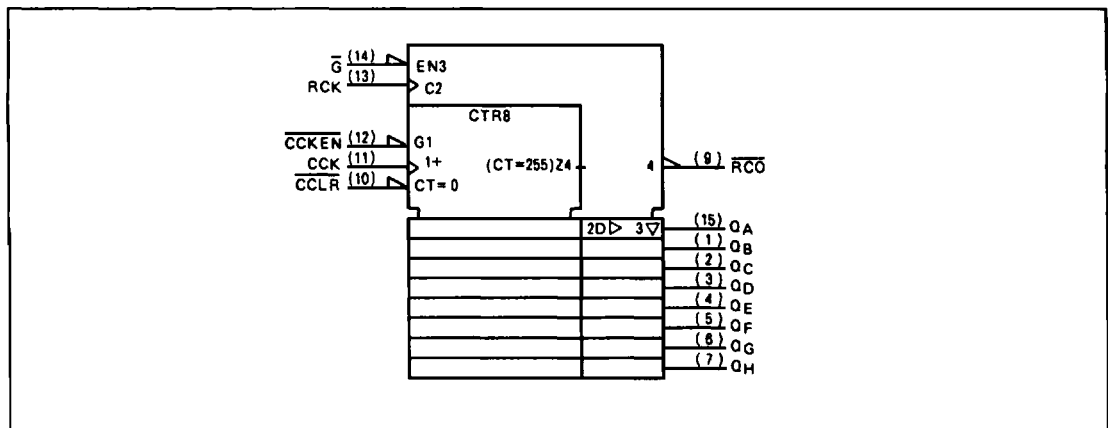
X: Don't care

$RCO=QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'$
(QA'~QH': Internal outputs of the counter)

TIMING CHART

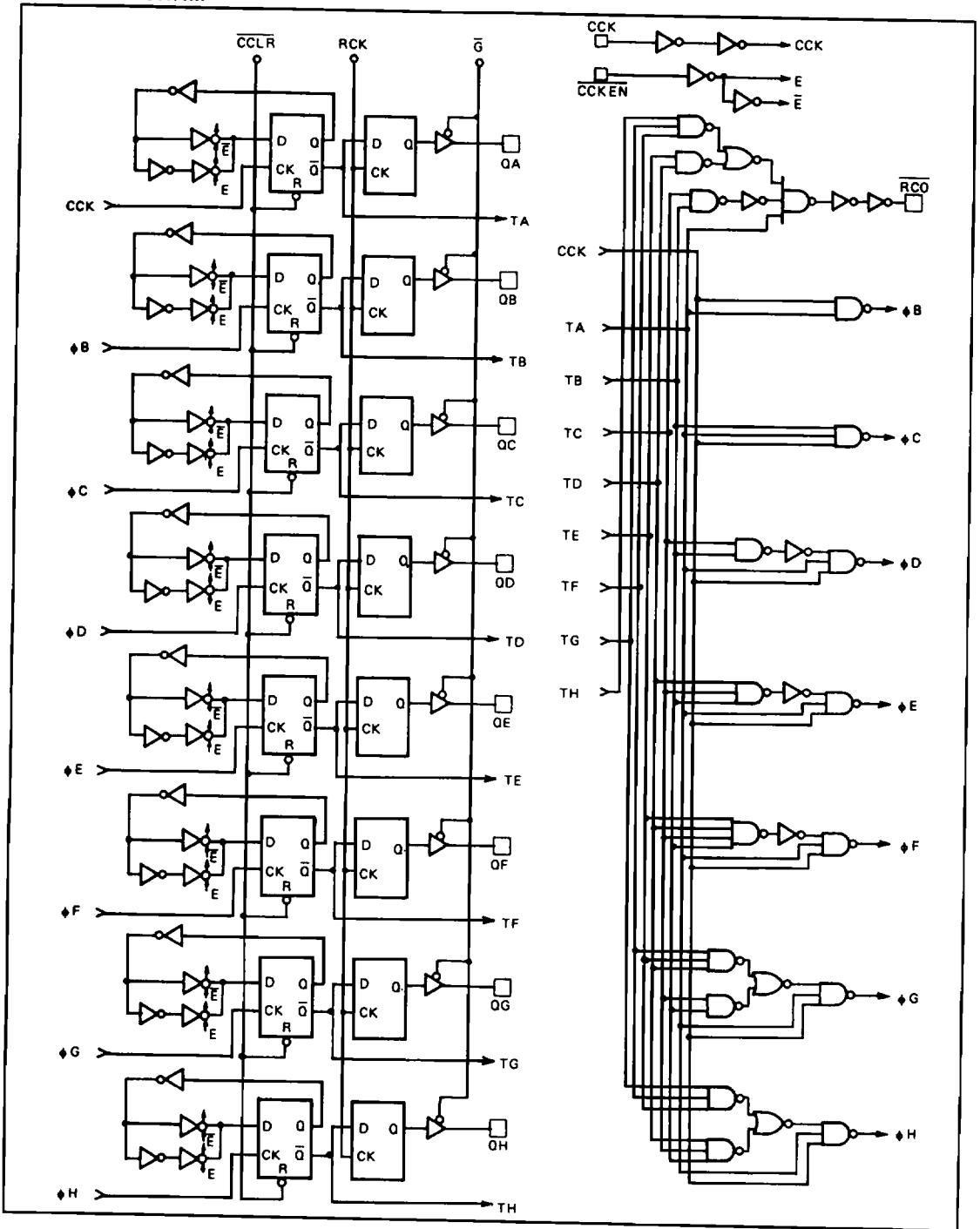


IEC LOGIC SYMBOL

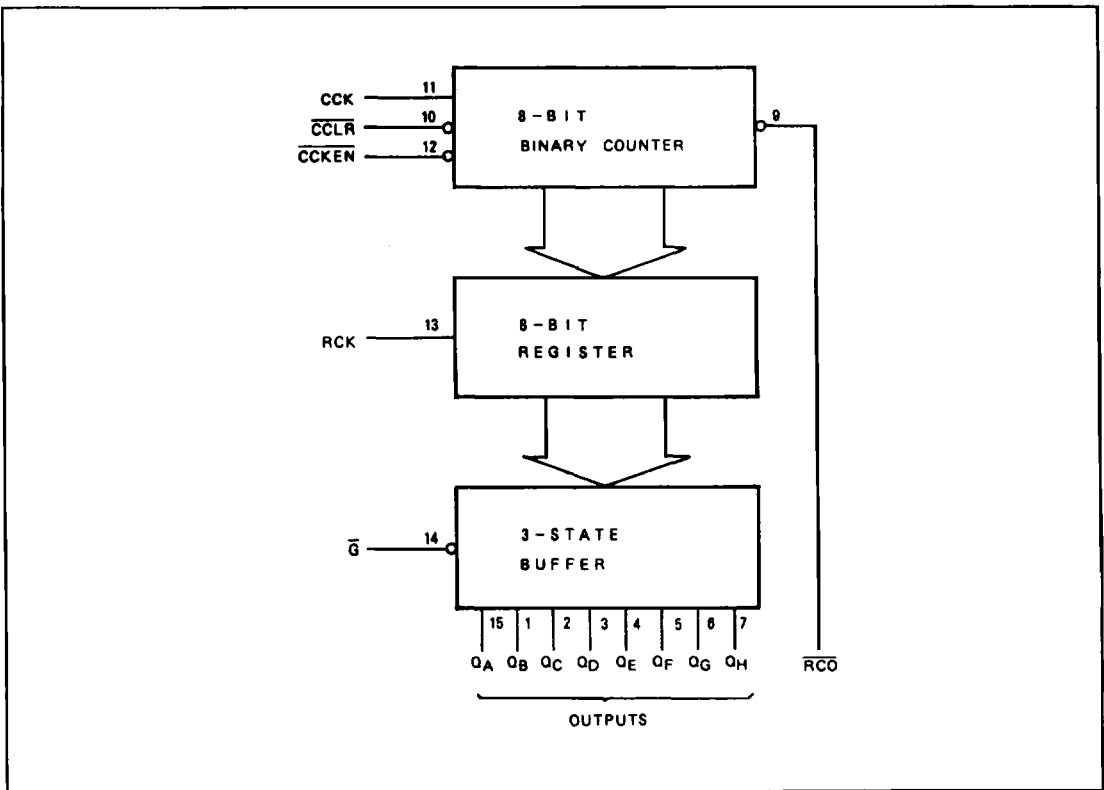


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LOGIC DIAGRAM



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (RCO) ($Q_A \sim Q_H$)	I_{OUT}	±25 ±35	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)~/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 ($V_{CC} = 2.0\text{V}$) 0 ~ 500 ($V_{CC} = 4.5\text{V}$) 0 ~ 400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT			
				MIN.	TYP.	MAX.	MIN.	MAX.				
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V			
			4.5	3.15	-	-	3.15	-				
			6.0	4.2	-	-	4.2	-				
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V			
			4.5	-	-	1.35	-	1.35				
			6.0	-	-	1.8	-	1.8				
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V		
				4.5	4.4	4.5	-	4.4	-			
				6.0	5.9	6.0	-	5.9	-			
				RCO	$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	-		4.13	-
					$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	-		5.63	-
				$Q_A \sim Q_H$	$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	-		4.31	-
$I_{OH} = -7.8 \text{ mA}$	6.0	5.68	5.80		-	5.63	-					
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V		
				4.5	-	0.0	0.1	-	0.1			
				6.0	-	0.0	0.1	-	0.1			
				RCO	$I_{OL} = 4 \text{ mA}$	4.5	-	0.17	0.26		-	0.33
					$I_{OL} = 5.2 \text{ mA}$	6.0	-	0.18	0.26		-	0.33
				$Q_A \sim Q_H$	$I_{OL} = 6 \text{ mA}$	4.5	-	0.17	0.26		-	0.33
$I_{OL} = 7.8 \text{ mA}$	6.0	-	0.18		0.26	-	0.33					
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.5	-	±5.0	μA			
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.1	-	±1.0				
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	-	-	-	4.0	-	40.0				

TIMING REQUIREMENTS (Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	T _a =25°C		T _a =-40 ~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	-	75	95	ns
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Pulse Width (CCLR)	$t_{W(L)}$		2.0	-	75	95	
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Set-up Time (CCKEN-CCK)	t_s		2.0	-	100	125	
			4.5	-	20	25	
			6.0	-	17	21	
Minimum Set-up Time (CCK-RCK)	t_s		2.0	-	200	250	
			4.5	-	40	50	
			6.0	-	34	43	
Minimum Hold Time	t_h		2.0	-	0	0	
			4.5	-	0	0	
			6.0	-	0	0	
Minimum Removal Time (CCLR)	t_{rem}		2.0	-	75	95	
			4.5	-	15	19	
			6.0	-	13	16	
Clock Frequency	f		2.0	-	6	5	MHz
			4.5	-	33	26	
			6.0	-	39	31	

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AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (RCO)	t _{TLH} t _{THL}		-	4	8	ns
Propagation Delay Time (CCK-RCO)	t _{pLH} t _{pHL}		-	18	28	
Propagation Delay Time (CCK-RCO)	t _{pLH}		-	20	30	
Maximum Clock Frequency	f _{MAX}		32	62	-	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V _{CC}	T _a = 25°C			T _a = -40 ~ 85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Qn)	t _{TLH} t _{THL}		50	2.0	-	25	60	-	75	ns
				4.5	-	7	12	-	15	
				6.0	-	6	10	-	13	
Output Transition Time (RCO)	t _{TLH} t _{THL}		50	2.0	-	30	75	-	95	
				4.5	-	8	15	-	19	
				6.0	-	7	13	-	16	
Propagation Delay Time (CCK-RCO)	t _{pLH} t _{pHL}		50	2.0	-	75	163	-	205	
				4.5	-	22	33	-	41	
				6.0	-	17	28	-	35	
Propagation Delay Time (CCLR-RCO)	t _{pLH}		50	2.0	-	78	175	-	220	
				4.5	-	23	35	-	44	
				6.0	-	18	30	-	37	
Propagation Delay Time (RCK-Qn)	t _{pLH} t _{pHL}		50	2.0	-	62	145	-	180	
				4.5	-	19	29	-	36	
				6.0	-	15	25	-	31	
			150	2.0	-	78	185	-	230	
				4.5	-	24	37	-	46	
				6.0	-	19	31	-	39	
Output Enable time	t _{pZL} t _{pZH}	R _L = 1 kΩ	50	2.0	-	43	105	-	130	
				4.5	-	14	21	-	26	
				6.0	-	12	18	-	22	
			150	2.0	-	58	150	-	190	
				4.5	-	19	30	-	38	
				6.0	-	16	26	-	33	
Output Disable time	t _{pLZ} t _{pHZ}	R _L = 1 kΩ	50	2.0	-	33	105	-	130	
				4.5	-	16	21	-	26	
				6.0	-	12	18	-	22	
Maximum Clock Frequency	f _{MAX}		50	2.0	6	12	-	5	-	
				4.5	30	51	-	24	-	
				6.0	35	80	-	28	-	
Input Capacitance	C _{IN}				-	5	10	-	10	pF
Power Dissipation Capacitance	C _{PD(1)}				-	-	-	-	-	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(OP)} = C_{ID} \cdot V_{CC} \cdot f_N + I_{CC}$$