

**SPEED/PACKAGE AVAILABILITY**

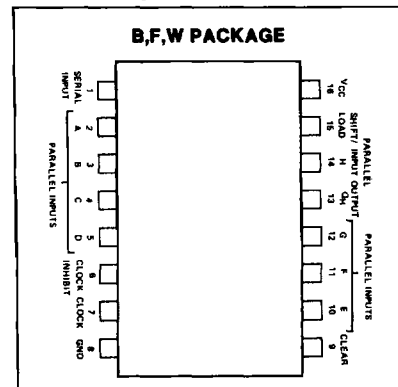
54 F,W 74 B

**TRUTH TABLE**

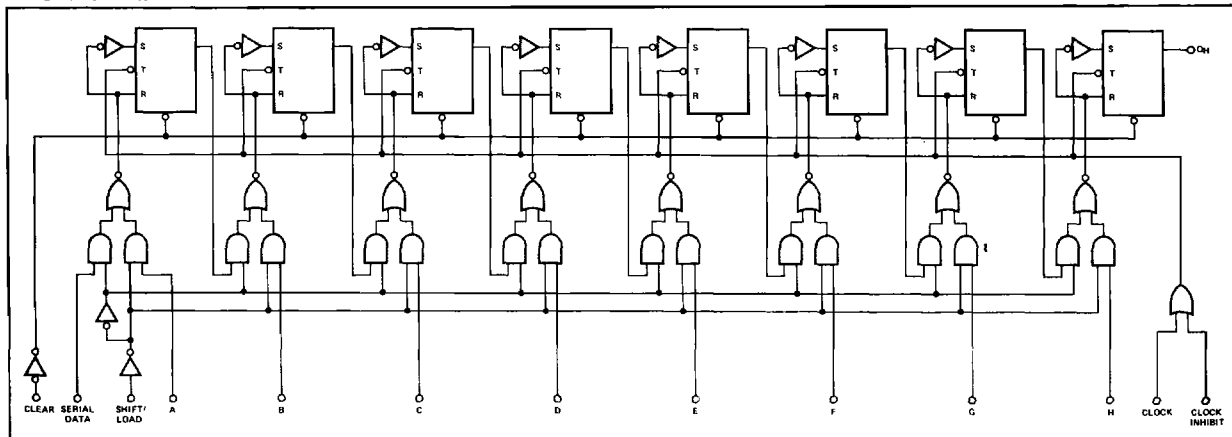
INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/LOAD	INHIBIT	CLOCK	SERIAL	PARALLEL	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>H</sub>
					A...H			
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>AO</sub>	Q <sub>BO</sub>	Q <sub>HO</sub>
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>AO</sub>	Q <sub>BO</sub>	Q <sub>HO</sub>

H = high level (steady state), L = low level (steady state)  
 X = irrelevant (any input, including transitions)  
 ↑ = transition from low to high level  
 a...h = the level of steady state input at inputs A thru H, respectively.  
 Q<sub>AO</sub>, Q<sub>BO</sub>, Q<sub>HO</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.  
 Q<sub>An</sub>, Q<sub>Gn</sub> = the level of Q<sub>A</sub> or Q<sub>G</sub>, respectively, before the most recent ↑ transition of the clock.

**PIN CONFIGURATION**

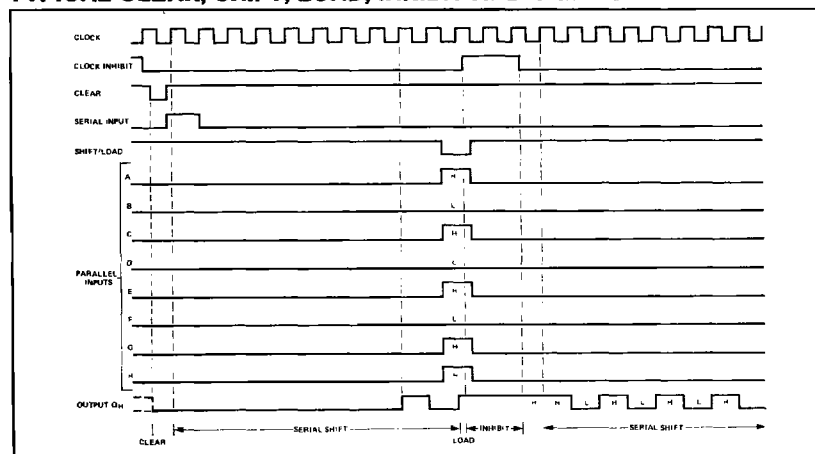


**LOGIC DIAGRAM**



**LOGIC**

**TYPICAL CLEAR, SHIFT, LOAD, INHIBIT AND SHIFT SEQUENCE**

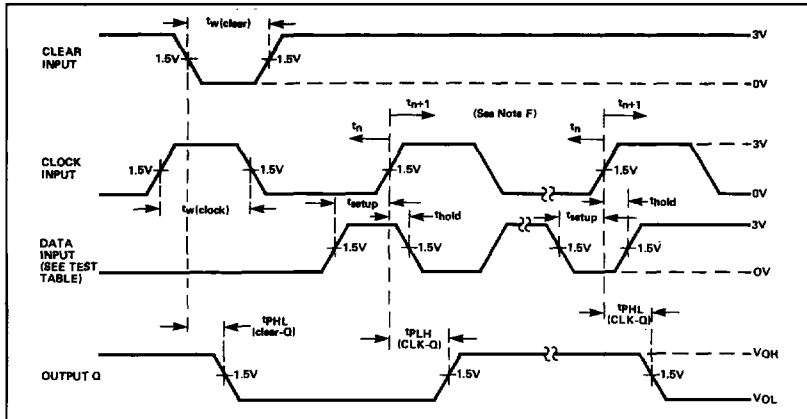


**SWITCHING CHARACTERISTICS**  $V_{CC} = 5V, T_A = 25^\circ C$

TEST CONDITIONS			54/74			UNIT
			$C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	
$f_{Count}$ Count frequency			25	35		MHz
$t_w(\text{Clock or Clear})$ Width of clock or clear pulse			20			ns
$t_{Setup}$ Input setup time	Mode Control Data		30			ns
$t_{Hold}$ Input hold time			20			ns
Propagation delay time						
$t_{PLH}$ Low-to-high	Clock		8	17	26	ns
$t_{PHL}$ High-to-low			8	20	30	
$t_{PHL}$ High-to-low	Clear			23	35	

Load circuit and typical waveforms are shown at the front of section.

**PARAMETER MEASUREMENT INFORMATION**



- A. The clock pulse has the following characteristics:  $t_w(\text{clock}) \geq 20 \text{ ns}$  and  $PRR = 1 \text{ MHz}$ . The clear pulse has the following characteristics:  $t_w(\text{clear}) \geq 20 \text{ ns}$  and  $t_{hold} = 0 \text{ ns}$ . When testing  $I_{max}$ , vary the clock PRR.
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. A clear pulse is applied prior to each test.
- E. Propagation delay times ( $t_{PLH}$  and  $t_{PHL}$ ) are measured at  $t_n+1$ . Proper shifting of data is verified at  $t_n+8$  with a functional test.
- F.  $t_n$  = bit time before clocking transition  
 $t_n+1$  = bit time after one clocking transition  
 $t_n+8$  = bit time after eight clocking transitions