National Semiconductor

NM27LC64
65,536-Bit (8k x 8) Low Current CMOS EPROM

General Description

The NM27LC64 is a 8k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NC27LC64 consumes a mere 12.5 mW (typical) in CMOS, and 25 mW (typical) in TTL, at 3 MHz.

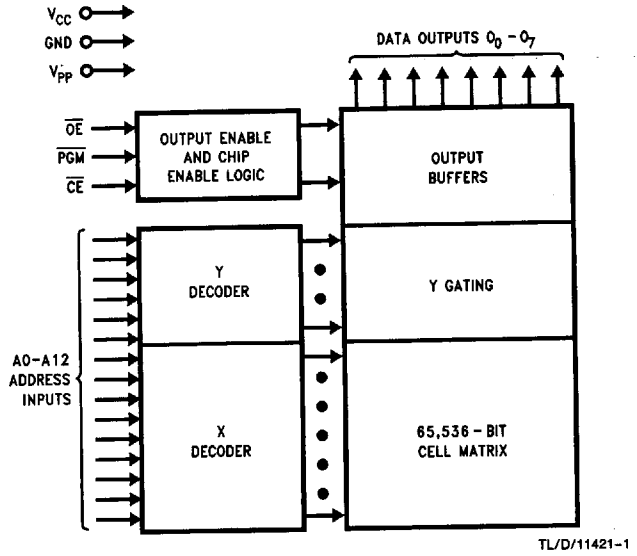
The NM27LC64 is one among a family of Power Miser (PM) products from National Semiconductor catering to the increasing low current demands of the market.

Offered in the JEDEC Pinout, this device is a replacement for high power devices, while also providing an upgrade path to higher densities.

Features

- Low power consumption
  - — 5V operation
  - — 4.5 mA (max) active
  - — 100 μA (max) standby
- 170 ns access time
- High reliability with EPI processing
  - — Latch-up immunity to 200 mA
  - — ESD protection exceeds 2000V
- JEDEC standard pin configuration
- Silicon Signature
- Manufacturer's identification code

Block Diagram



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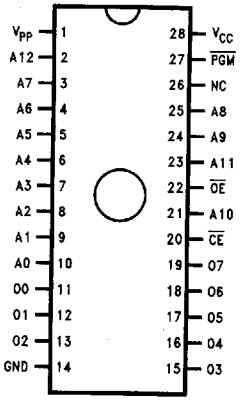
Pin Names

Symbol	Description
A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

Connection Diagrams

27LC010	27LC512	27LC256
XX/V_{PP}		
A16		
A15	A15	V_{PP}
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O0	O0	O0
O1	O1	O1
O2	O2	O2
GND	GND	GND

DIP
NM27LC64



27LC256	27LC512	27LC010
		V_{CC}
		XX/PGM
V_{CC}	V_{CC}	XX
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
OE	OE/V_{PP}	OE
A10	A10	A10
CE/PGM	CE/PGM	CE
O7	O7	O7
O6	O6	O6
O5	O5	O5
O4	O4	O4
O3	O3	O3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27LC64 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC64 Q, N, 120	120
NM27LC64 Q, N, 150	150
NM27LC64 Q, N, 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC64 QE, NE, 120	120
NM27LC64 QE, NE, 150	150
NM27LC64 QE, NE, 200	200

Ordering Information

NM 27 LC 64 Q E 200

- **National Memory** — NM
- **EPROM** — 27
- **Low Current** — LC
- **Size** — 64
  - 64 = 64k
  - 256 = 256k
  - 512 = 512k
- **Package** — Q
  - Q = Ceramic DIP
  - N = Plastic DIP, OTP
- **Operating Temperature Range** — E
  - Blank = Commercial
  - E = Extended
- **Access Time** — 200
  - 200 = 200 ns

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%

READ OPERATION

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Type	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND				10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$				10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 3 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA	Comm'l		5	6.3	mA
			Ind'l		5	7	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA, (*Figures 1* and *2*)	Comm'l		2	3	mA
			Ind'l		2	3.5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$			0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$			0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$				10	μA
V_{IL}	Input Low Voltage			−0.1		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA		2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA				0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA		V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	150		200		250		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

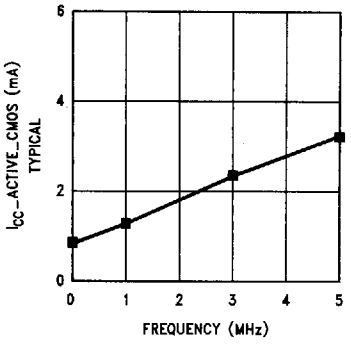

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FIGURE 1. I_{CC} Active CMOS vs Frequency
$V_{CC} = V_{PP} = 5.0V$, Temperature = 25°C

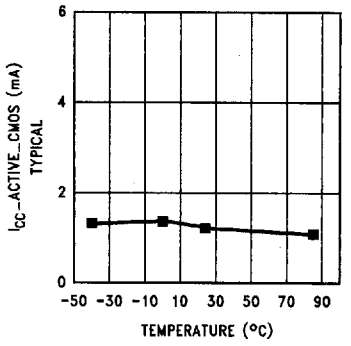

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FIGURE 2. I_{CC} Active CMOS vs Temperature
$V_{CC} = V_{PP}$ 5.0V, Frequency = 1 MHz

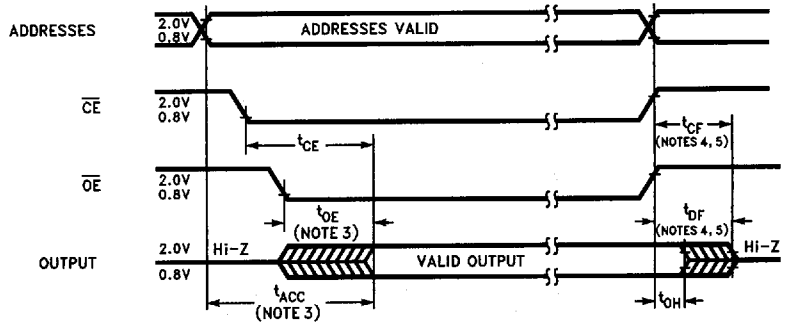
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45V to 2.4V
		Timing Measurement Reference Level	(Note 10)
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

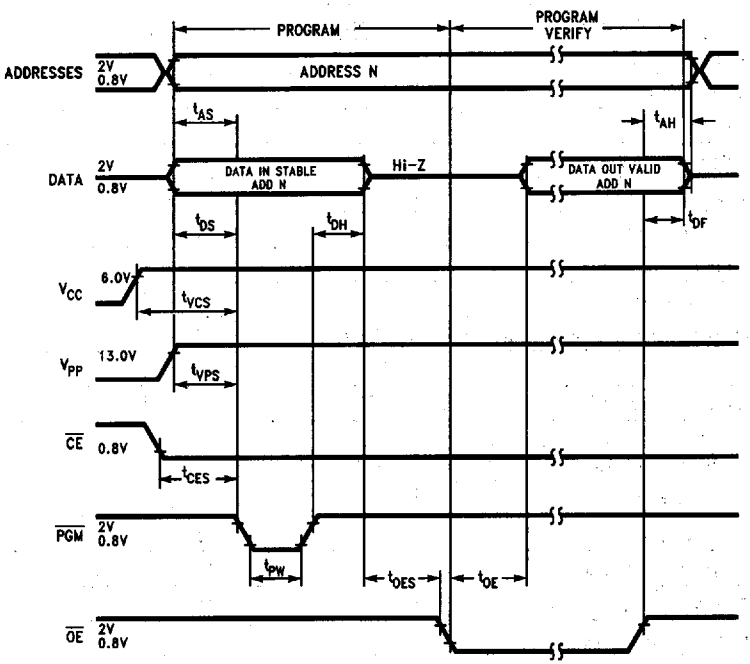
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs: $V_{IL} =$ GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Interactive Programming Algorithm Flow Chart

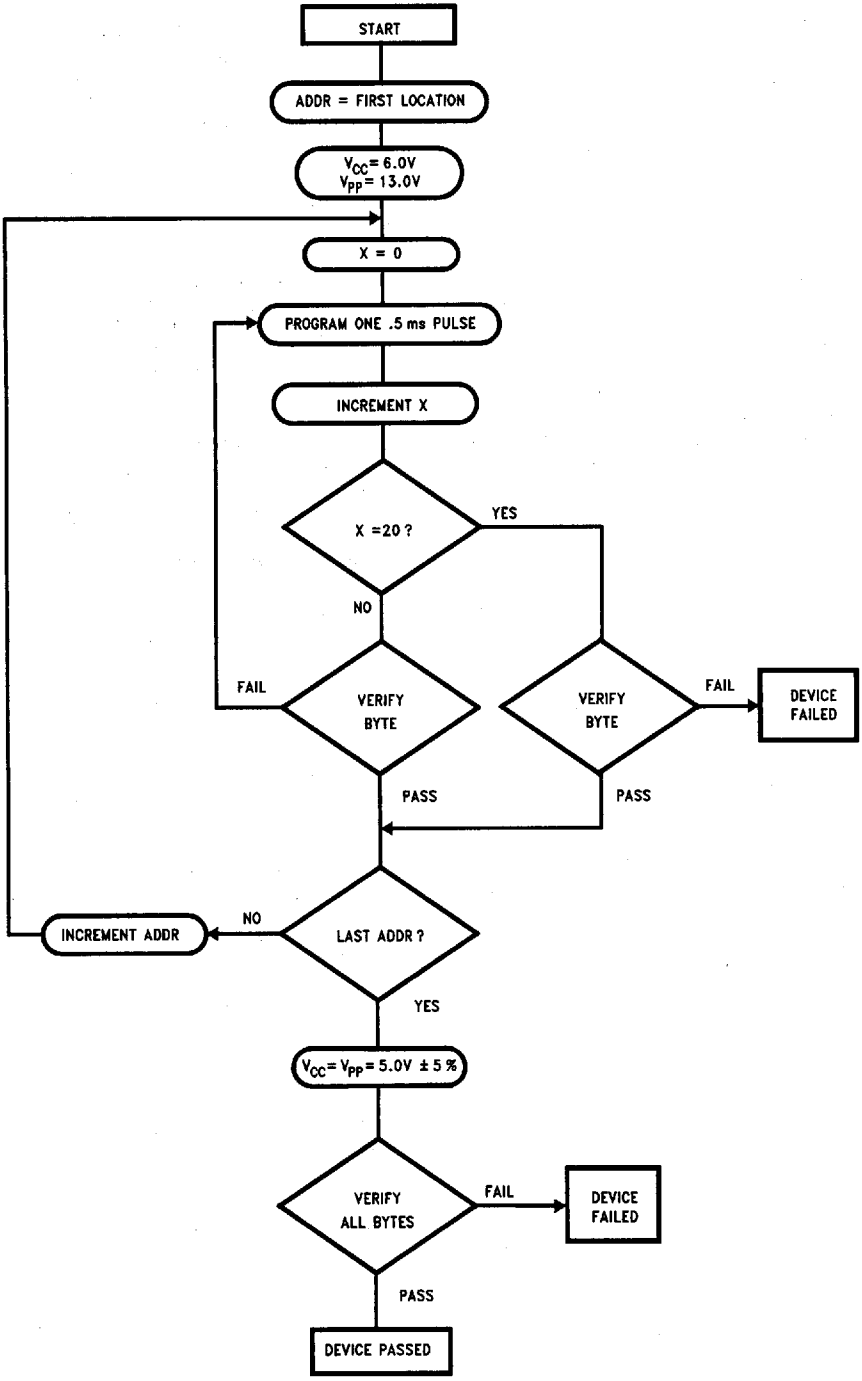

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FIGURE 3

Functional Description

DEVICE OPERATION

The six modes of operation of the NM27LC64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NM27LC64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NM27LC64 has a standby mode which reduces the active power dissipation by 97%, from 34.65 mW to 0.55 mW. The NM27LC64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NM27LC64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NM27LC64.

Initially, all bits of the NM27LC64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NM27LC64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NM27LC64 is designed to be programmed with interactive programming *(Figure 3)*, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NM27LC64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NM27LC64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM27LC64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NM27LC64s. If an application requires erasing and reprogramming, the NM27LC64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NM27LC64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NM27LC64 may be common. A TTL low level program pulse applied to an NM27LC64's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NM27LC64. A TTL high level $\overline{CE}$ input inhibits the other NM27LC64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NM27LC64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NM27LC64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM27LC64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NM27LC64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NM27LC64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NM27LC64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2