1 CHANNEL SWITCHED MODE CONSTANT CURRENT CONTROLLER E522.31/33

PRODUCTION DATA - JUL 21, 2016

RoHS compliant

Features

- Switched-Mode, PWM LED Controller
- 5V to 55V input voltage range, up to 80V boosted output voltage
- Boost-, SEPIC, Buck-Boost- or Buck Topology supported
- Constant Current Regulation implemented
- High-Precision Differential High-Side Sense up to 60V
- High-Frequency PWM Dimming Capability for constant LED Color
- Analog 10:1 Dimming Capability for LED Binning
- Integrated Softstart
- Advanced Error Detection (e.g. Over-Voltage, Open-Load Detection, different Shorts or GND Loss)
- Integrated Automotive LDOs for 5V & 3.3V
- AEC-Q100 Qualified
- Junction temperature range -40°C to +150°C

Applications

- Automotive LED lighting Applications (daytime running light, indicator, front- and rear light, interior lighting etc.)
- General Indoor and Outdoor Lighting and -Signals
- TFT Backlighting
- General Current driven Applications

General Description

E522.31 and E522.33 are part of a family of fixed frequency switched-mode high voltage LED power supplies and controllers with high efficiency. Integrated high-side sensing allows topologies related to the supply input (Boost-to-Battery) or to GND (Boost-to-GND).

The device is suitable for operation in boost-, buck-boost-, SEPIC- and buck-topologies, particularly in harsh automotive environments.

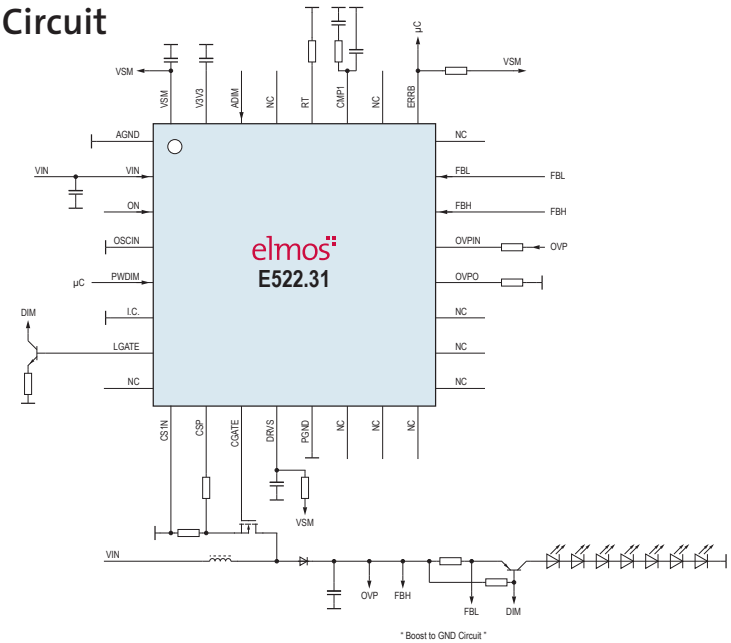
The constant switching frequency is adjustable up to 600kHz by an external resistor or can be synchronized in Master-Slave configurations with other devices.

Multiple control- and monitoring functions, e.g. short- and open load detection, over-temperature shutdown and under-voltage lockout are implemented.

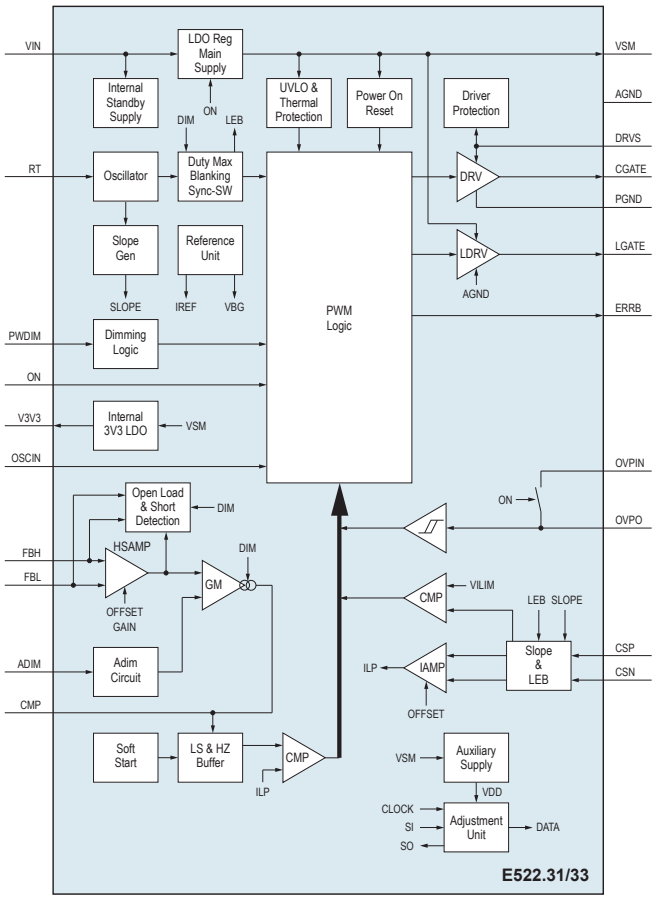
Ordering Information

Ordering-No.	Oscillator Spectrum	Softstart Ramping	Package
E52231A61C	spread	Slow Ramping (SR)	QFN32L5
E52231A61CXFR	spread	Fast Ramping (FR)	QFN32L5
E52233A61C	narrow	Slow Ramping (SR)	QFN32L5
E52233A61CXFR	narrow	Fast Ramping (FR)	QFN32L5

Typical Application Circuit

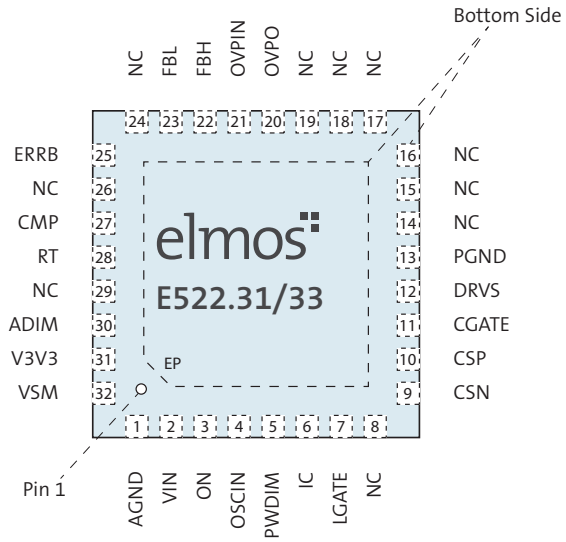


Functional Diagram



Pin Configuration

Top View



Note: *Not to scale, EP Exposed die pad*

Pin Description

Pin	Name	Type [1)]	Description
1	AGND	S	Analog Ground. Ground pin for analog blocks. Make a short, low impedance connection between this pin and GND.
2	VIN	HV_S	High voltage supply input. Bypass with low ESR capacitance to GND.
3	ON	HV_A_I	Control input to activate/disable the IC. CMOS compatible logic input with high-voltage capability and pulldown current.
4	OSCIN	D_I	5V & 3.3V compatible input pin with pulldown current for synchronization to external clock. Solder to GND to use RT defined internal oscillator. If used, a resistor matching the applied input frequency has to be connected to RT (see RT pin description).
5	PWDIM	D_I	PWM dimming input with pullup current to V3V3. For constant LED color, PWM is used to control brightness. 5V CMOS compatible as well as open-drain compatible input. If not needed, solder this pin to V3V3 for continuous operation.
6	IC		Reserved for factory use. Connect to AGND in application
7	LGATE	D_O	Dimming output for regulation circuit. Low Side Gate driver output to conrol N-channel MOSFET types. If not needed leave this pin open.
8	NC		Not connected
9	CSN	A_I	Negative low-side converter current sense input. The negative biased shunt resistor terminal is connected to this pin.
10	CSP	A_I	Positive low-side converter current sense input. The positive biased shunt resistor terminal is connected to this pin.
11	CGATE	D_O	Low-Side switch gate driver output. Connect the gate of the external logic level N-channel MOSFET to this pin.
12	DRVS	S	Gate driver supply voltage. Connect a low ESR ceramic capacitor between this pin and PGND. Connect either VSM via a decoupling resistor or an external voltage source to this pin.
13	PGND	S	Power Ground. Ground pin for CGATE high power drivers. Make a short, low-impedance connection to GND
14	NC		Not connected
15	NC		Not connected
16	NC		Not connected
17	NC		Not connected
18	NC		Not connected
19	NC		Not connected
20	OVPO	A_IO	Over voltage protection output. Connect the low-side resistor of over-voltage protection feedback to this pin.
21	OVPIN	HV_A_I	Over voltage protection input. Connect the high side of an external resistor divider for over voltage protection to this pin.
22	FBH	HV_A_I	Positive high-side feedback input for regulation circuit. Connect the positive terminal of sensing shunt resistor to this pin. For good regulation, keep the connection to the shunt as short as possible.
23	FBL	HV_A_I	Negative high-side feedback input for regulation circuit. Connect the negative terminal of sensing shunt resistor to this pin. For good regulation, keep the connection to the shunt as short as possible.
24	NC		Not connected.
25	ERRB	D_O	Open-drain error output. Low-impedant in case of Open Load, short circuit or over-temperature events.
26	NC		Not connected.

Pin	Name	Type [1)]	Description
27	CMP	A_IO	Error amplifier compensation. Connect the compensation circuit to this pin.
28	RT	A_IO	Oscillator control. For free-running operation, connect a resistor between this pin and AGND. If an external synchronization clock is applied to OSCIN, the according resistor must be applied at RT.
29	NC		Not connected.
30	ADIM	A_I	Analog dimming input. The input voltage at this pin controls the LED current sensing at FBH and FBL. To use internal reference voltage solder to V3V3.
31	V3V3	S	3.3V regulator output. Connect to AGND with a ceramic capacitance of typ. 1µF.
32	VSM	S	Internal 5V low drop regulator output. Bypass this pin to AGND with a ceramic capacitance of typ. 1µF. Additionally, the VSM voltage can be connected to DRVS via a decoupling resistor so supply the CGATEx drivers.
-	EP	S	Exposed Die Pad Connect to AGND

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

ESD:

More details according this topic are described in the "ESD" chapter.

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Condition	Symbol	Min	Max	Unit
High Voltage Supply Input VIN		V_{VIN}	-0.3	55	V
High Voltage Supply Input VIN, transient	t_{MAX} = 500ms	$V_{VIN,TRAN}$	-0.3	60	V
Voltage at pin FBH		V_{FBH}	-0.3	60	V
Voltage at pin FBL		V_{FBL}	-0.3	60	V
Differential Voltage between Feedback Pins FBH & FBL	t_{MAX} < 1h [1)]	$V_{FBH-FBL,MAX}$	-60	60	V
Voltage at pin OVPIN		V_{OVPIN}	-0.3	80	V
Voltage at pin OVPO		V_{OVPO}	-0.3	V_{V3V3}	V
Voltage at pin ADIM		V_{ADIM}	-0.3	V_{V3V3}	V
Voltage at pin PWDIM		V_{PWDIM}	-0.3	V_{VSM}	V
Voltage at pin RT		V_{RT}	-0.3	V_{V3V3}	V
Input current at pin RT		I_{RT}	-2	2	mA
Voltage at pin ON		V_{ON}	-0.3	55	V
Voltage at pin VSM		V_{VSM}	-0.3	5.5	V
Output current at pin VSM	V_{VIN} > 5.5V ON = '1'	I_{VSM}	-65	0	mA
Voltage at pin OSCIN		V_{OSCIN}	-0.3	V_{VSM}	V
Averaged Output Current at pin CGATE		$I_{CGATE,AVG}$		40	mA
Average Output Current at pin LGATE		$I_{LGATE,AVG}$		2	mA
Voltage at pin ERRB		V_{ERRB}	-0.3	7.5	V
Input Current at pin ERRB		I_{ERRB}	0	5	mA
Voltage at pin CSN and CSP		V_{CS}	-0.3	V_{V3V3}	V
Voltage at pin V3V3		V_{V3V3}	-0.3	3.6	V
Current at pin V3V3	V_{VSM} = 5V	I_{V3V3}	-25	0	mA
Voltage at pin DRVS		V_{DRVS}	-0.3	7.5	V
Voltage at pin CMP		V_{CMPX}	-0.3	V_{V3V3}	V
PGND to AGND		V_{PGND}	-0.3	0.3	V
ESD Protection at all pins	AECQ-100 HBM	V_{ESD}	-2	2	kV
Thermal resistance (junction to case) QFN32L5		R_{T_J-C}		5	K/W
Junction temperature		T_J	-40	150	°C
Ambient temperature	packaged devices	T_A	-40	125	°C
Storage temperature, soldered	soldered device	T_{S1}	-40	150	°C
Storage temperature, unsoldered	un-soldered device	T_{S2}	-40	125	°C
Total Power Dissipation		P_{TOT}		1500	mW

1) Absolute maximum ratings V_{FBH} and V_{FBL} must not be exceeded

2 ESD Protection

Description	Condition	Symbol	Min	Max	Unit
ESD HBM	HBM [1)]	$V_{PINS-ALL}$	±2	-	kV
ESD CDM at corner pins	CDM [2)]	$V_{PINS\ EDGE}$	±0.75	-	kV
ESD CDM at all other pins	CDM [2)]	$V_{PINS-OTHER}$	±0.5	-	kV

Note: Test point defined as tested pin to supply.
1) According to AEC-Q 100-002, Human Body Model, 1.5kΩ resistance, 100pF capacitance.
2) According to AEC-Q 100-011, Charged Device Model, pulse rise time (10% to 90%) <400ps, 1Ω resistance.

3 Recommended Operating Conditions

Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified. All voltages are referred to ground (0V). Typical Parameters are given for V_{VIN}= 14V and T_J = +25 °C.
Currents flowing into the circuit have positive values.
The first electrical potential connected to the IC must be GND to avoid excessive current flow in other pins.

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply voltage VIN		V_{IN}	5.5	14	55	V
Voltage at pin FBL		V_{FBL}	4		56	V
Voltage at pin FBH		V_{FBH}	V_{FBL}	V_{FBL}+ 200m	V_{FBL}+ 400m	V
Voltage at pin OVPIN		V_{OVPIN}			80	V
Voltage at pin OVPO		V_{OVPO}			3	V
Resistance from OVPO to GND		R_{OVPO}	10	20	33	kΩ
External Reference at pin ADIM		$V_{ADIM,EXREF}$	0.24		2.4	V
Voltage at pin ADIM for internal Reference Voltage		$V_{ADIM,INTREF}$	V_{V3V3}- 0.25	V_{V3V3}		V
Voltage at Dimming Inputs PWDIM		V_{PWDIM}	0		V_{VSM}	V
RT Current to define fOSC		I_{RT}	-24		-10	µA
Resistance from RT to GND		R_{RT}	50		120	kΩ
Voltage at pin ON		V_{ON}	0		55	V
Resistor to supply DRVS using VSM		$R_{VSM,DRVS}$	1		3	Ω
Sink impedance of external open drain at PWDIM		Z_{PWDIM}			2	kΩ
Average Output Current at pin CGATE	SMPS Frequency x ext. Gatecharge driven	I_{CGATE}			25	mA
Average Output Current at pin LGATE	Dimming Frequency x Gatecharge at LGATE	I_{LGATE}			2	mA
Input Current at pin ERRB		I_{ERRB}	0		3	mA
External Synchronization Frequency applied to pin OSCIN		f_{OSCIN}	225		650	kHz
Voltage at pin CSP		V_{CSP}	0		400	mV
Voltage at pin CSN to AGND	1)	V_{CSN}		0		mV
Voltage at pin DRVS		V_{DRVS}	4.75	V_{VSM}	7.5	V
Junction temperature		T_J	-40		+150	°C
Ambient temperature		T_A	-40		+125	°C
Capacitance at VSM to AGND	ESR < 0.6Ω	C_{VSM}	0.8	1	2	µF
Capacitance at pin VIN to GND	ESR < 0.1Ω	C_{VIN}	47	120		µF
Capacitance from pin V3V3 to AGND	ESR < 0.6Ω	C_{V3V3}	0.8	1	2	µF
Capacitance from DRVS to PGND	ESR < 0.1Ω ESL < 5 nH	C_{DRVS}	1	2.2		µF
Maximum Total Capacitance at pins OVPIN and OVPO		C_{OVP}			20	pF
PGND to AGND	1)	V_{PGND}		0		V

1) Pins must be soldered to PCB GND potential

4 Electrical Characteristics

(V_{VIN} = +5.5V to +55V, T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VIN} = +14V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply						
Supply voltage at VIN		V_{IN}	5.5	14	55	V
Sleep Mode Current Consumption	ON = '0' V_{VIN}=14V T_J=25°C	$I_{VIN,SLEEP}$		8		µA
Active VIN Supply Current	ON = '1' no switching	$I_{VIN,ACTIVE}$		2.2	3.7	mA
Nominal Output voltage at VSM	ON = '1' V_{VIN} = 14V	$V_{VSM,NOM}$	4.75	5	5.25	V
Low-Drop Voltage of VSM	V_{VIN}=5.2V I_{VSM}=50mA [1]	$V_{VSM,LDO}$	4.7			V
Reset Threshold relative to nominal V_{VSM}	V_{VSM} rising	$V_{VSM,RESH}$		0.925		$V_{VSM,NOM}$
External VSM Current [2]	ON = High, V_{VIN} = 6 ... 55V	$I_{VSM,EXT}$	-40			mA
External V3V3 Current [2]	ON='1' V_{VSM} > 4.75V	$I_{V3V3,EXT}$	-15			mA
Short Current Limitation of VSM Regulator	V_{VIN} = 14V V_{VSM} = 0V	$I_{VSM,SHORT}$	65	110		mA
V3V3 Voltage Regulator Output	ON = '1' V_{VSM} > 4.75V	$V_{V3V3,NOM}$	3.13	3.3	3.47	V
Reset Threshold relative to nominal V_{V3V3}	V_{V3V3} rising	$V_{V3V3,RESH}$		0.925		$V_{V3V3,NOM}$
Short Current Limitation V3V3 Regulator	V_{VSM}>4.7V V_{V3V3} = 0V	$I_{V3V3,SHORT}$	20	55		mA
Reset threshold of DRVS input, relative to VSM	V_{VSM}>$V_{VSM,RESH}$ V_{DRVS} rising	$V_{DRVS,RESH}$		0.92		V_{VSM}
Reset threshold of DRVS input, relative to VSM	V_{VSM}>$V_{VSM,RESH}$ V_{DRVS} falling	$V_{DRVS,RESL}$		0.85		V_{VSM}
Enable Threshold at pin ON	V_{VIN}=14V	$V_{ON,ENA}$	1.4	1.5	1.6	V
Disable Hysteresis at pin ON	V_{VIN}=14V	$V_{ON,HYST}$		18		mV
Pulldown Current at pin ON	V_{VIN} = 14V V_{ON} = 1.5V	$I_{ON,PD}$	5	10		µA
Thermal Shutdown Junction Temperature	T_J rising	$T_{J,OFF}$		160		°C
Hysteresis of Thermal Shutdown	T_J falling [3]	$T_{J,OFF,HYST}$		25		°C
Oscillator						
Upper Oscillator Frequency Setting	R_{RT} = 50kΩ	$f_{OSC,INT,H}$	564	600	636	kHz
Lower Oscillator Frequency Setting	R_{RT} = 120kΩ	$f_{OSC,INT,L}$	235	250	265	kHz

1) Overall current at VSM voltage regulator, including IC current consumption
2) The sum of external currents at voltage regulators must not exceed 40mA
3) Not production tested

Electrical Characteristics (continued)

(V_{VIN} = +5.5V to +55V, T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VIN} = +14V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
RT Resistor Range for Internal Oscillator Operation [1]	f_{OSCIN} = 0 Hz	$R_{RT,INT}$	50		120	kΩ
OSCIN External Frequency Range [2]		$f_{OSCIN,EXT}$	225		650	kHz
Minimum High or Low Pulsewidth at OSCIN for Synchronization		$T_{PULSE,MIN,OSCIN}$	660			ns
RT Resistor Range for external Clock Synchronization	225kHz ≤ $f_{OSC,IN}$ ≤ 650kHz	$R_{RT,EXT}$	47		137	kΩ
Tracking between R_{RT} and OSCIN frequency for external Oscillator Synchronization	[2]	$R_{RT,OSCIN}$	-5		5	%
Typical Range for Spread Spectrum Modulation of internal Oscillator	f_{OSCIN} = 0 Hz only valid for E522.31	f_{SPREAD}	-40		40	kHz
Digital Dimming Logic						
Minimum PWDIM Pulse Width	[3]	$T_{PWDIM,MIN}$	2			µs
PWDIM Frequency		f_{PWDIM}	20	400	2000	Hz
Timeout for CMP and Softstart Reset	PWDIM = '0'	$T_{PWM,TIMEOUT}$		64		ms
LGATE Pullup Resistance	I_{LGATE} = -5mA T_J = 25°C	$R_{ON,LGATEH}$		30		Ω
LGATE Pulldown Resistance	I_{LGATE} = 5mA T_J = 25°C	$R_{ON,LGATEL}$		18		Ω
Average Current in LGATE	$I_{LGATE,AVG} = f_{PWDIM} \times Q_{GATECHARGE} + I_{LGATE,DC}$	$I_{LGATE,AVG}$			2	mA
Pullup Current at PWDIM to V3V3	V_{PWDIM} = 1V	$I_{PWDIM,PU}$	-100	-80	-60	µA
High Threshold at PWDIM	V_{PWDIM} rising	$V_{PWDIM,H}$		2.1		V
Low Threshold at PWDIM	V_{PWDIM} falling	$V_{PWDIM,L}$		1.2		V
Typical Delay by Internal Softstart Ramp (standard setting)	PWDIM = '1' (E52231A61C, E52233A61C) [4] [5]	$t_{SOFTSTART}$		7.5		ms
Rising Voltage Slope at CMP during Softstart (standard setting)	PWDIM = '1' (E52231A61C, E52233A61C) [5]	$dV/dt_{CMP,START1}$		200		mV / ms
Typical Delay by Internal Softstart Ramp (fast setting)	PWDIM = '1' (E52231A61CXFR, E52233A61CXFR) [4] [5]	$t_{SOFTSTART,FAST}$		3.75		ms
Rising Voltage Slope at CMP during Softstart (fast setting)	PWDIM = '1' (E52231A61CXFR, E52233A61CXFR) [5]	$dV/dt_{CMP,START2}$		400		mV / ms

1) E522.31 drives typical 1.2V to the RT node

2) The external input frequency must be matched to the frequency given by R_{RT} to detect a valid OSCIN signal

3) Note that the delays in external dimming circuit or magnetic components may limit the dimming pulse width above the E522.3x limit

4) The time given is the typical delay that is necessary to reach a sufficiently high CMP voltage to regulate a typical application. May vary depending on implementation details

5) Not production tested

Electrical Characteristics (continued)

(V_{VIN} = +5.5V to +55V, T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VIN} = +14V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Analog Dimming and Highside Sense						
ADIM Input Voltage Range	External voltage reference applied	$V_{ADIM,EXT}$	0.24		2.4	V
Internal Reference Voltage for FBH,FBL	$V_{ADIM} = V_{V3V3}$	$V_{ADIM,INT}$	192	200	208	mV
ADIM Pull-Down Current to AGND	V_{ADIM} = 1V	$I_{ADIM,PD}$		0.75		µA
Under-voltage Threshold for ADIM		$V_{ADIM,ERR}$		160		mV
Gain from ADIM to FBH/FBL		$A_{ADIM,FB}$		1/6		
Linearity Error of ADIM to FBH/FBL Gain	0.6V ≤ V_{ADIM} ≤ 2.4V [1]	$L_{ADIM,FB}$			3	%
Input voltage at FBL pin	V_{VIN} = 14V	V_{FBL}	4		56	V
Input voltage at FBH input	V_{VIN} = 14V	V_{FBH}	V_{FBL}		V_{FBL}+0.4	V
Highside Feedback Amplifier Input Currents	$I_{FB} = I_{FBH}+I_{FBL}$ $V_{FBH} = V_{FBL}$ = 14V	I_{FB}		125		µA
Undervoltage Detection at FBL and FBH	[3]	$V_{FB,UV}$		3.8	4	V
Error detection delay after falling edge at PWDIM	Evaluation of V_{FBH} - V_{FBL} during dimming	$t_{ERR,DIM}$	14	16		µs
Error Detection Threshold Voltage after falling edge at PWDIM	Evaluation of V_{FBH}-V_{FBL} during dimming	$V_{ERR,DIM}$		50		mV
Inner Current Regulation Loop						
Positive low-side Shunt Sense Input Voltage	Voltage V_{CSP} referred to GND	V_{CSP}			400	mV
Average Pull-Up Current at CSP	V_{CSP} = 0V	$I_{CSP,PU}$		-20	-5	µA
Pull-Down Current at CSN		$I_{CSN,PD}$		5		µA
Over-Current Protection Threshold at CSP		$V_{CSP,OCP}$		425		mV
Pull-Up On-Resistance of CGATE	V_{DRVS} = 5V I_{CGATE} = -100mA T_J = 25°C	$R_{ON,CGATEH}$		1.6		Ω
Pull-Down On-Resistance of CGATE	V_{DRVS} = 5V I_{CGATE} = 100mA T_J = 25°C	$R_{ON,CGATEL}$		1.2		Ω
Average Current in CGATE	$I_{CGATE,AVG} = f_{OSC} \times Q_{GATECHARGE}$ [2]	$I_{CGATE,AVG}$			25	mA
Minimum current consumption at DRVS	V_{CGATE} = 0V T_J = 25°C	$I_{DRVS,MIN}$	7	15		µA
CGATE On-Pulse Width during Over-Current Condition	V_{CSP} ≥ 500 mV [4]	T_{OFF}		130		ns
Maximum CGATE Dutycycle	$V_{CMP} = V_{V3V3}$ Softstart finished	$DC_{CGATE,MAX}$		89		%

1) For reference voltages at ADIMx below 0.6V the linearity error may scale to higher values
2) Value limited to avoid excessive current flow in VSM regulator, see also „1 Absolute Maximum Ratings“
3) Consider this parameters espesially for SEPIC or Flyback topologies
4) Not production tested

Electrical Characteristics (continued)

(V_{VIN} = +5.5V to +55V, T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VIN} = +14V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Outer Regulation Loop						
Transconductance differential Voltage $V_{FBH-FBL}$ to CMP	T_J = 25°C	GM		4000		µS
Openloop DC Gain from $V_{FBH-FBL}$ to CMP	3)	A_{DC}		85		dB
Maximum Input / Output Current at CMP	T_J = 25°C V_{CMP} = 1.5V	$I_{CMP,MAX}$		40		µA
Leakage Current at CMP during Dimming	V_{PWDIM} = 0V $T_J \leq$ 85°C V_{CMP} = 1.5V 3)	$I_{CMP,LEAK}$		1	30	nA
Under-voltage protection at CMP		$V_{OVERDR,CMP}$		160		mV
Over-Voltage Protection						
Input Voltage at OVPIN pin		V_{OVPIN}			80	V
Input voltage at OVPO pin		V_{OVPO}			V_{V3V3}	V
Over-Voltage Protection Threshold	1)	$V_{OVPO,OFF}$	1.16	1.20	1.24	V
Sleep / Dimming Leakage Current at OVPIN	V_{OVPIN} = 5 ... 80V, T_J = 25°C V_{ON}=0V or V_{PWDIM}=0	$I_{LEAK,OVPIN}$			0.1	µA
Active Current Flow into OVPIN	$I_{ACTIVE,OVPIN} = V_{OUT}/(R_{OVPIN}+R_{OVPO})$ 2)	$I_{ACTIVE,OVPIN}$			130	µA
Over-Voltage Detection Delay	PWDIM = '1' ON = '1' 3)	$t_{OVP,DETECT}$		10	25	µs
ERRB Output						
Output Voltage of active ERRB	I_{ERRB} = 3mA Error detected	$V_{ERRB,L}$		200	400	mV
ERRB Leakage Current	T_J < 150°C No Error detected	$I_{ERRB,Z}$			5	µA
Minimum ERRB Low Pulse Width	Error detected	$t_{ERRB,ON}$	0.8	1		ms

1) Hysteresis is provided by internal minimum pulse width of ERRB signal of typ. 1ms
2) The parameter V_{OUT} describes the output voltage of the converter in a typical application
3) Not production tested

5 Functional Description

5.1 General

The E522.3x family is a versatile high voltage controller family for LED drivers. They can be configured for buck from battery, buck-boost, SEPIC or boost topologies, either to VIN or GND.

This flexibility combined with the high supply voltage of 55V, the very large output voltage range and the possibility to drive high power LED arrays makes the E522.3x family ideal for

LED lighting applications
Automotive environment, e.g. headlight control
Residential and outdoor lighting applications

The E522.3x family consists of E522.31/33 for one LED chain and E522.32/34 for two LED chains. In all two channel family members the Switch Mode Power Supplies are 180° out of phase for reduced EMI. Digital PWM and analog dimming for each LED channel are independent and can be adjusted separately.

For further reduction of electromagnetic emission E522.31/32 are running with spread spectrum local oscillator. The spread spectrum is only applied if there is no input frequency at OSCIN.

The internal low-drop regulators VSM and V3V3 can be used to supply external low-power components with a total current consumption up to 15mA(E522.32/34)and 40mA(E522.31/33) at 5V (VSM) and 3.3V (V3V3) supply.

The internal oscillator can be configured for free-running mode with fixed frequency, controlled by a resistor at the RT pin, or synchronized by an external clock input at OSCIN (Slave mode in a Master-Slave configuration).

The LED controllers support PWM dimming for LED brightness control without color change and analog dimming for adjusting the LED initial current. The PWM of E522.3x dimming allows a wide dimming ratio of >1000:1 at PWM frequencies up to 400Hz.

5.2 Supply

The supply generates all necessary voltages to operate E522.3x from VIN. Furthermore supervision of V_{VIN}, V_{VSM}, V_{V3V3} and device temperature are performed.

The VSM low-drop voltage regulator provides 5V for peripheral structures and CGATE driver. It is controlled by the ON pin and the internal temperature supervision. For proper stabilization use typ. 1µF ceramic capacitance (X7R recommended).

V3V3 voltage regulator is used to power most of the internal analog circuitry. It may also be used to drive external components, but in this case the total external current provided by VSM and V3V3 must not exceed 40mA. Use 1µF ceramic capacitance (X7R) to stabilize V3V3.

5.3 Oscillator

The internal oscillator defines the operation frequency of the device, adjustable from 250 to 600kHz by an external resistor at pin RT. Any Frequency in this range can be set by linear interpolation between the values given in the table above (R_{RT}=50kΩ*600kHz/frequency). To use the internal oscillator, solder OSCIN to AGND.

For synchronous operation to an external clock source, a frequency can be applied to OSCIN.
In case of external clock it is necessary to apply a resistor to RT with a value matching the synchronizing frequency. Tolerance between frequency set by R_{RT} and f_{OSCIN} is defined in RRT,OSCIN.

5.4 Digital Dimming Logic

The PWM logic block controls the digital dimming of 0 to 100% at pin PWDIM. When PWM = '0' is applied to pin PWDIM, E522.3x is set to hold state (high impedant) for the regulation signal at CMPx. LGATE outputs are set to match internal synchronization of PWM. Direct control of external dimming transistors is not recommended.
At the falling edge of the PWM signal, dimming circuit is checked for short circuit connections. To verify that the external current is switched off, typ. 16µs after switching LGATE '0', internal control circuitry for short detection in the external dimming circuit is enabled. The threshold for this detection is typ. 50mV $V_{FBH-FBL}$. With the rising edge of V_{PWDIMx} this check is disabled again.
The PWM range of 0 to 100% with 0.1% resolution permits LED brightness control of >1000:1 at a PWM frequency of 400Hz.
Note, that during dimming the current in the external inductor must settle to provide proper regulation. Therefore the minimum dimming pulse width depends on the external circuitry, input voltages and external resonant frequencies, too.
Internal pull-up current to V3V3 makes the PWDIMx pins suitable for open-drain / open-collector control circuits. The voltage capability of V_{VSM} makes this input 5V/3.3V compatible as well.

5.5 Analog Dimming and Highside Sense

The ADIM section provides LED current adjustment, independent of digital dimming feature (e.g. binning or initial current setting).
Voltages below typ. 0.16V are considered an open pin, disabling the converter.
In the range of 0.24V to 2.4V the signal is accepted as reference for regulation, divided by a factor of 6. To use the internal reference voltage of typical 1.2V (= 200mV at $V_{FBH-FBL}$) solder this pin to V3V3.

The high side feedback FBH & FBL provides precise measurement of the load current (e.g. LED current). In any topology FBH must be connected to the positively biased shunt resistor terminal.
Additionally, these pins are monitored for under-voltage to detect open pins or short-to-GND errors, disabling the converter in case of detection. The undervoltage threshold may be superseded by the VSM reset generation.
Note that for SEPIC or Flyback topologies the output must be precharged above the undervoltage threshold at FBx to allow startup. For example the VSM regulator is suitable to drive the output via a rectification device or circuit.

5.6 Inner Current Regulation Loop

The Low side feedback CSxP and CSxN provides inductor current measurement to the inner regulation loop to control the pulse width of the CGATE output. Over-Current protection is provided if the voltage at CSxP pin exceeds 425mV relative to AGND, turning the according CGATE driver off. For over-current limitation please note , that the slope compensation may decrease the actual current limitation for higher dutycycles.
CGATE output is designed to drive the gate of an external true-logic-level N-channel FET with an average gate current of 25mA at switching frequencies up to 660kHz (in OSCIN synchronized operational mode).
The average current can be calculated by multiplication of the operation frequency with the total gate charge of the external FET. For example, for a transistor of 40nC gate-charge the maximum operational frequency is 625kHz. Higher gate-charge leads to lower maximum operational frequency (e.g. 100nC transistors are possible at a maximum frequency of 250kHz).
DRVS should be supplied by VSM (see chapter supply for details). If DRVS is supplied externally, an maximum average current of 40mA in each CGATE is possible. Take additional power generated in E522.3x into account.
E522.3x device provide internal slope compensation ramp generation. The slope can be scaled to match the external circuitry by applying a resistor R_{SLP} between the innerloop shunt R_{SHUNT} and pin CSxP.
For applications designed to work with higher dutycycles than 50%, R_{SLP} should be choosen in the range from typ. 330Ω to 2kΩ. Final resistor value should be defined during prototyping of the complete application.
As a starting value for R_{SLP} in Boost configuration use

$$R_{SLP} = \frac{V_{OUT} \cdot R_{SHUNT}}{5e^{-4} \cdot f_{RT} \cdot L}$$

with f_{RT} = operating frequency set at RT
and L = inductance in Boost circuitry

5.7 Outer Regulation Loop

The outer regulation loop provides control of the converter in combination with the differential high-side feedback amplifier at FBL and FBH. The failure amplifier (named GM) provides the inner regulation loop reference voltage derived from CMP.

A typical compensation network required for optimized operation is a network consisting of a capacitor to reference GND, parallel to a serial connection of a capacitor and a resistor (see typical application diagram). During prototyping the compensation has to be verified for the whole input voltage range, especially for the maximum duty cycle which occurs.

Under-voltage detection at FBL, FBH and CMP are provided to detect external failures like short-connections. A soft-start mechanism is implemented to avoid excessive input current flow. The soft-start startup time is typically 7.5ms with PWDIM='1' to fully release converter output power. A faster setting for softstart length can be ordered, which leads to 3.75ms for a typical implementation. The voltage slopes applied at CMP are either typ. 200mV/ms (standard) or typ. 400mV/ms (fast).

Note that dimming at PWDIMx during softstart stretches this delay (by approximately 1/dutycycle applied).

5.8 Over-Voltage Protection

The OVP (over voltage protection) Pins OVPIN and OVPO provide a GND related output over-voltage protection.

The absolute voltage level of protection is defined by the resistive divider with respect to the maximum voltage at pin OVPIN, connected from converter output voltage to OVPIN and from OVPO to AGND. Recommended resistive range is given in ROVPO.

If E522.3x is turned off or is dimmed, the connection between OVPIN and OVPO is switched off, providing high impedance to reduce current flow in over-voltage protection. This feature also disconnects the DC path between VIN and GND to save energy in sleep mode. Note, that during PWDIM='0' the over-voltage protection is not available.

5.9 ERRB Output

ERRB open-drain output is used to set an error flag for peripheral components, e.g. microcontroller.
The output drives the ERRB flag to AGND, if a failure is detected. The following failure states are handled:

- Over-voltage at OVPIN
- Open-load (detected by over-voltage protection)
- Open feedback connection at FBH or FBL
- Open current feedback at CSP
- FBH or FBL under-voltage detection
- Reversed feedback VFBH - VFBL < typ. -50mV
- Continuous innerloop current limitation for typ. >64ms [1)]
- Open ADIM connection
- Differential feedback FBH-FBL over-voltage [2)]
- PWDIM time-out (e.g. caused by short to GND)
- Short in external dimming transistors [3)]
- VSM or V3V3 under-voltage (e.g. short to GND)
- Junction over-temperature
- Open AGND or PGND connection
- DRVS under-voltage (below reset-threshold)
- ON voltage low (ON logically'0')
- Open RT input or out-of-range OSCIN signal
- Invalid frequency applied to OSCIN

1) Error Flag is set for typ. 1s after detection, restarting the device afterwards.
2) Differential overvoltage at FBH/FBL is detected by CMP undervoltage detection to avoid sensitivity to distortions.
3) Differential voltage across FBH/FBL during dimming is supervised for a typ. threshold of 50mV after a delay of typ. 16µs following the falling edge of the PWDIM signal.

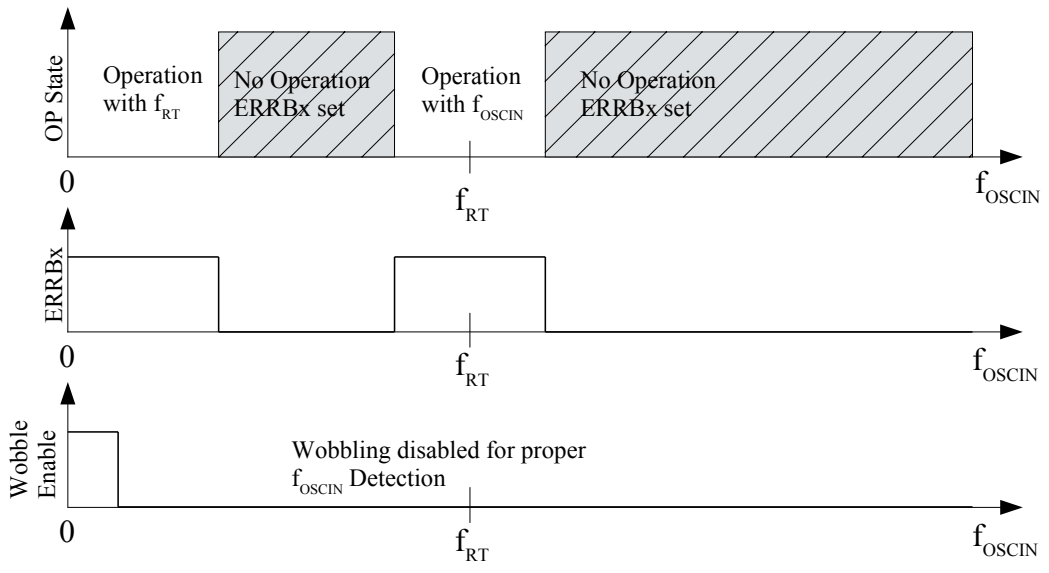


Figure 1. OSCIN Failure Check

5.10 Short Circuit Monitoring for floating LED Loads

The circuitry shown in (Figure 2) can be used to detect LED chain short circuit in floating output topologies (e.g. boost-to-battery). The resistors $R_{SC1,2}$ are used to adapt the threshold for short circuit detection to a threshold of $V_{SC,DETECT}=U(BE)*(1+R_{SC1}/R_{SC2})$, with U(BE) being the base-emitter voltage of the bipolar transistor devices. Choose R_{SC1} value sufficiently high to prevent unintended discharge of the converter output during dimming cycles. The negative thermal coefficient of this topology can be used to partially compensate the temperatur dependent characteristic of the load. With the connection to ERRB of E522.3x, the combined feedback signal includes all failures detected by E522.3x together with the short circuit (or under-voltage) information of the highside load. An additional capacitor parallel to R_{SC2} may be useful to implement debouncing of the feedback signal or to increase of EMI of the circuit.

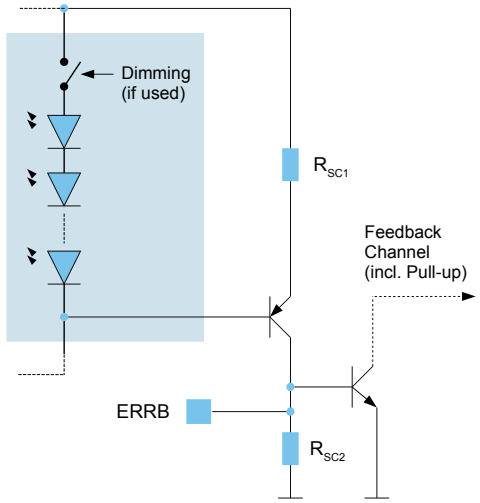


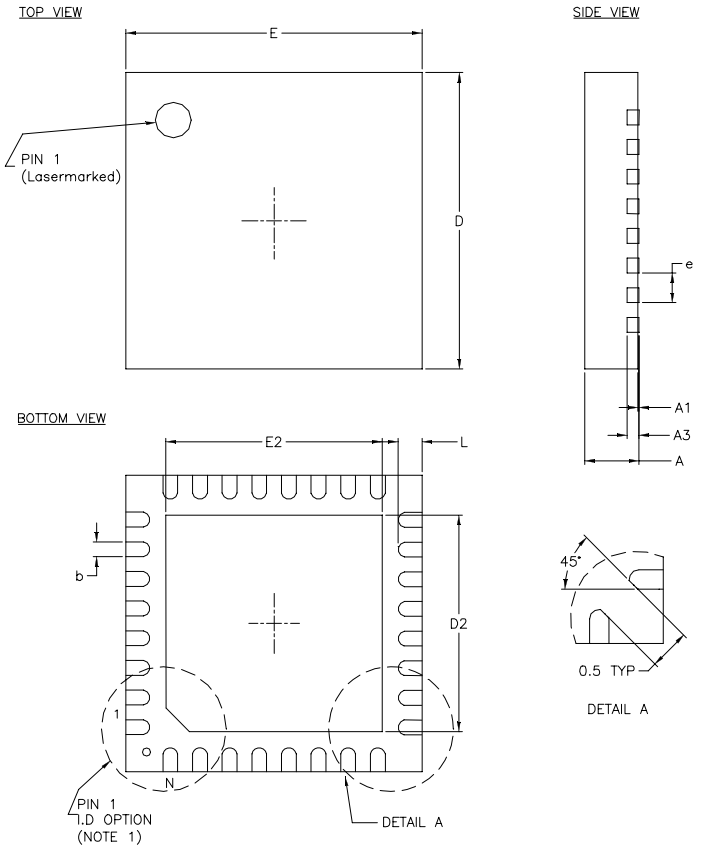
Figure 2. Exemplary shown circuit monitoring in Boost-to-Battery application

6 List of Abbreviations

Term	Explanation
ASSP	Application Specific Standard Product
IC	Integrated Circuit
OVP	Over Voltage Protection
OCP	Over Current Protection
GM	Transconductance
OSC	Oscillator
PWM	Pulse Width Modulation
REF	Reference, usually given as I (current) or V (voltage)
LDO	Low Drop Out Voltage Regulator
CS	Current Sense
FB	Feedback
SMPS	Switched-Mode Power Supply
EMI	Electromagnetic Immunity
EME	Electromagnetic Emission
EMC	Electromagnetic Compatibility

7 Package Information

All devices are available in a Pb free, RoHs compliant QFN32L5 plastic package according to JEDEC MO-220 K, variant VHHD-4. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / width of exposed pad	D2 / E2	3.50	3.65	3.80	0.138	0.144	0.150
Lead pitch	e	--	0.5 BSC	--	--	0.02 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		32			32	

Note: the mm values are valid, the inch values contains rounding errors

8 Marking

8.1 Top Side

- Elmos (Logo)
- 52231A
- XXUYWW

Signature	Explanation
52231	Elmos project number
A	Elmos project revision code
Y	Year of assembly (e.g. 2014)
WW	Week of assembly
XXXX	Production lot number (1 to 4 digits)
U	Assembler Code

9 Functional Safety

The development of this product is based on a process according to an ISO/TS 16949 certified quality management system. Functional safety requirements according to ISO 26262 have not been submitted to Elmos and therefore have not been considered for the development of this product.

10 Record of Revision

Chapter	Revision	Change and Reason for Change	Date	Released Elmos
-	.00	Initial revision	Mar 26, 2015	AMIL/ZOE
-	.01	Page 1 -> new version with new ordering no. added	Jul 21, 2016	DHOE/ZOE
4	.01	Page 9 -> Digital Dimming Logic -> Software parameter added	Jul 21, 2016	DHOE/ZOE
5.7	.01	Revised	Jul 21, 2016	DHOE/ZOE
9	.01	New chapter with Functional Safety Hints	Jul 21, 2016	DHOE/ZOE

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Contact Information

Headquarters
Elmos Semiconductor AG
Heinrich-Hertz-Str. 1 • D-44227 Dortmund (Germany) ☏: +492317549100 ✉: sales-germany@elmos.com : www.elmos.com

Sales and Application Support Office North America
Elmos NA. Inc.
32255 Northwestern Highway • Suite 220 Farmington Hills
MI 48334 (USA) ☏: +12488653200 ✉: sales-usa@elmos.com

Sales and Application Support Office China
Elmos Semiconductor Technology (Shanghai) Co., Ltd.
Unit 16B, 16F Zhao Feng World Trade Building,
No. 369 Jiang Su Road, Chang Ning District,
Shanghai, PR China, 200050 ☏: +86216210 0908 ✉: sales-china@elmos.com

Sales and Application Support Office Korea
Elmos Korea
B-1007, U-Space 2, #670 Daewangpangyo-ro,
Sampyoung-dong, Bunddang-gu, Sungnam-si
Kyounggi-do 463-400 Korea ☏: +82317141131 ✉: sales-korea@elmos.com

Sales and Application Support Office Japan
Elmos Japan K.K.
BR Shibaura N Bldg. 7F
3-20-9 Shibaura, Minato-ku,
Tokyo 108-0023 Japan ☏: +81334517101 ✉: sales-japan@elmos.com

Sales and Application Support Office Singapore
Elmos Semiconductor Singapore Pte Ltd.
3A International Business Park
#09-13 ICON@IBP • 609935 Singapore ☏: +65 6908 1261 ✉: sales-singapore@elmos.com

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