FAIRCHILD
A Schlumberger Company

F68488
General-Purpose Interface Adapter

Microprocessor Product

Description

The F68488 General-Purpose Interface Adapter (GPIA) provides the means to interface between an IEEE-488 standard instrument bus and the F6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

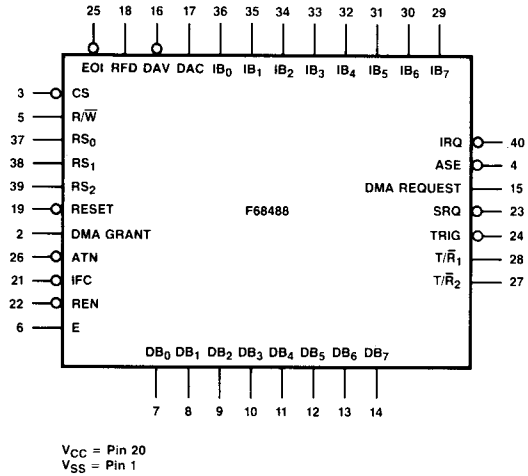
The F68488 will automatically handle all handshake protocol needed on the instrument bus.

- **Single or Dual Primary Address Recognition**
- **Secondary Address Capability**
- **Complete Source and Acceptor Handshakes**
- **Programmable Interrupts**
- **RFD Hold-Off to Prevent Data Overrun**
- **Operates with DMA Controller**
- **Serial and Parallel Polling Capability**
- **Talk-Only or Listen-Only Capability**
- **Selectable Automatic Features to Minimize Software**
- **Synchronization Trigger Output**
- **F6800 Bus Compatible**

Pin Names

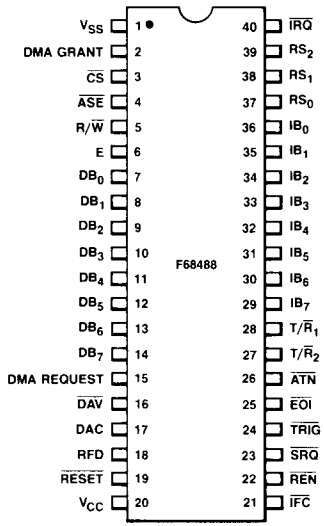
DB_0-DB_7	Bidirectional Data Lines
$\overline{CS}$	Chip Select Input
R/$\overline{W}$	Read/Write Input
RS_0, RS_1, RS_2	Register Select Inputs
$\overline{IRQ}$	Interrupt Request Output
$\overline{RESET}$	Chip Reset Input
DMA GRANT	DMA Transfer in Progress Input
DMA REQUEST	DMA Transfer Ready Output
$\overline{ASE}$	Address Switch Enable Output
IB_0-IB_7	Bidirectional ASCII Bus
DAC	Bidirectional Data Accepted Line
RFD	Bidirectional Ready for Data Line
$\overline{DAV}$	Bidirectional Data Valid Line
$\overline{ATN}$	Attention Input
$\overline{IFC}$	Interface Clear Input
$\overline{SRQ}$	Service Request Output
$\overline{REN}$	Remote Enable Input
$\overline{EOI}$	Bidirectional End or Identify Line
$\overline{TRIG}$	Group Execute Trigger Output
T/$\overline{R}_1$, T/$\overline{R}_2$	Transmit/Receive Control Outputs
E	Enable Clock Input
V_{SS}	Ground
V_{CC}	+5 V Power Supply

Logic Symbol



V_{CC} = Pin 20
V_{SS} = Pin 1

Connection Diagram
40-Pin DIP



(Top View)

5

Functional Description

The IEEE-488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communication to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to or transferred between instruments. A bus controller dictates the role of each device by making the attention ($\overline{ATN}$) line true and sending talk or listen addresses on the instrument bus data lines; those devices that have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a pc board by a microprocessor as a part of the initialization sequence.

When the controller makes the $\overline{ATN}$ line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488-bus driver ICs to meet the complete electrical specifications of the IEEE-488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The F68488 GPIA has been designed to interface the F6800 microprocessor with the complex protocol of the IEEE-488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

Fig. 1. Functional Diagram

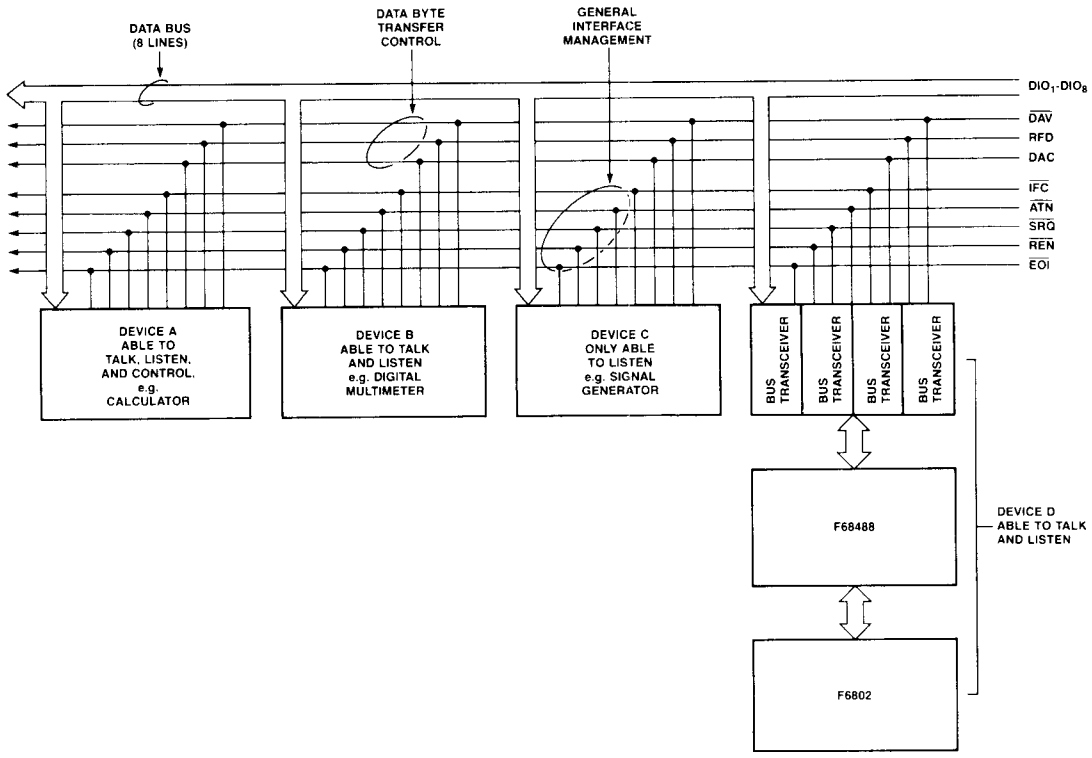
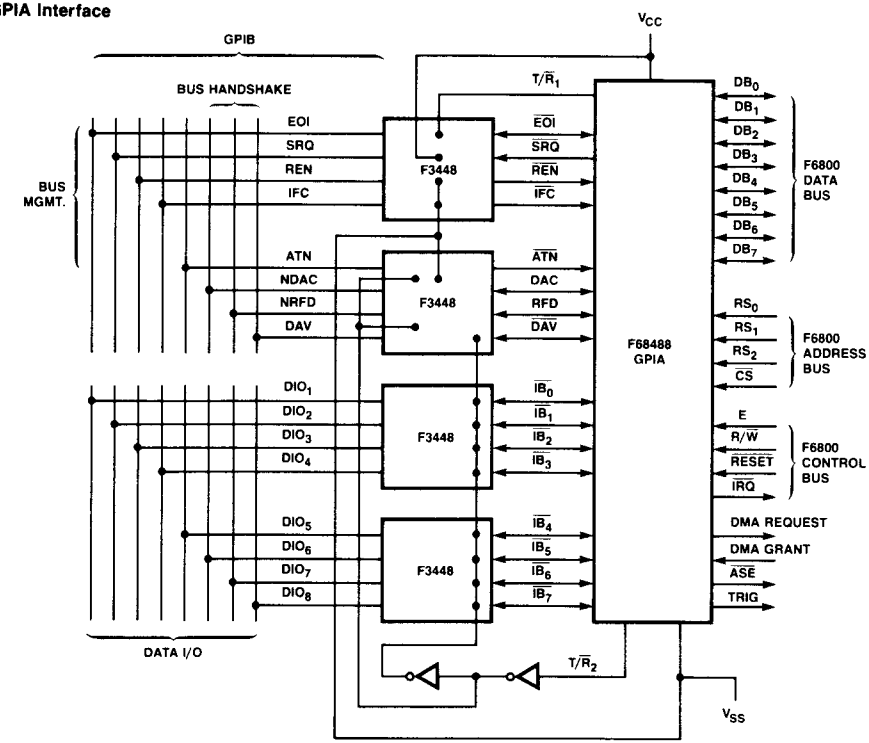


Fig. 2. F68488 GPIA Interface



GPIA/MPU Interface Signals
The F68488 interfaces to the F6800 MPU with an 8-bit bidirectional Data Bus, a Chip Select, Read/Write line, $\overline{\text{RESET}}$ line, three Register Select lines, an Interrupt Request line, two DMA Control lines, and an Address Switch Enable line.

GPIA Bidirectional Data (DB_0-DB_7) – The bidirectional data lines allow the transfer of data between the MPU and the GPIA. The data bus output drivers are 3-state devices that remain in the high-impedance (OFF) state except when the MPU performs a GPIA read operation. The Read/Write line is in the read state when the GPIA is selected for a read operation.

GPIA Chip Select ($\overline{\text{CS}}$) – This input signal is used to select the GPIA. The $\overline{\text{CS}}$ signal must be LOW for selection of the device. Chip select decoding will have to be accomplished with logic external to the chip.

GPIA Read/Write Line (R/$\overline{\text{W}}$) – This signal is generated by the MPU to control register access and direction of data transfer on the data bus. A LOW state on the GPIA Read/Write line allows for the selection of one of seven write-only registers when used in conjunction with the Register Select lines, RS_0, RS_1, RS_2. A HIGH state on the GPIA Read/Write line enables the selection of one of eight read-only registers when used in conjunction with the Register Select lines.

GPIA Register Select (RS_0, RS_1, RS_2) – The three register select lines are used to select the various registers inside the GPIA. These three lines are used in conjunction with the Read/Write line to select a particular register that is to be written to or read from. *Table 1* shows the register select coding.

Interrupt Request ($\overline{\text{IRQ}}$) – The $\overline{\text{IRQ}}$ output goes to the common interrupt bus for the MPU. This is an open drain output which is wire-ORed to the $\overline{\text{IRQ}}$ bus. The $\overline{\text{IRQ}}$ is set false (LOW) when an enabled interrupt occurs and stays false until the MPU reads from the interrupt status register.

$\overline{\text{RESET}}$ – The active-LOW $\overline{\text{RESET}}$ input is used to initialize the device during power-on start-up. The $\overline{\text{RESET}}$ line will be driven by an external power-on reset circuit.

DMA Control Lines (DMA Grant, DMA Request) – The DMA Request line is used to signal waiting data when Byte In (BI) Byte Out (BO) is set HIGH for a DMA controller. The DMA Request line is set HIGH if either the BI or BO interrupt flag is set in the interrupt status register (R0W) and the corresponding bits in the interrupt mask register (R0R) are set true. The DMA Request line is cleared when the DMA Grant is made true. The DMA Grant line is used to signal the GPIA that the DMA controller has control of the MPU data and address lines. The DMA Grant line must be grounded when not in use.

Trigger ($\overline{TRIG}$) – The TRIG pin provides an output corresponding to the GET and fget commands. A hardware or software reset places this output at a LOW level. The trigger output can be programmed HIGH by either of two methods:

1. Setting fget (bit 0 of R3W) by the MPU causes the trigger output to be set. It remains set until the fget bit is programmed LOW or until a reset occurs.
2. The trigger output is set upon reception of a GET command from the controller. It is reset when the GPIA moves out of the device trigger active state (DTAS); i.e., when GET, LADS, or ACDS occur.

Address Switch Enable ($\overline{ASE}$) – The $\overline{ASE}$ output is used to enable the device address switch 3-state buffers to allow the instrument address switches to be read on the MPU bus.

Enable Input (E) – The E input is normally a derivative of the MPU $\phi 2$ clock.

F68488-GPIA/488 Interface Bus Signals
The GPIA provides a set of 18 interface signal lines between the F6800 and the IEEE-488 Standard bus.

Signal Lines ($\overline{IB_0}$-$\overline{IB_7}$) – These bidirectional lines allow for the flow of 7-bit ASCII interface messages and device-dependent messages. Data appears on these lines in a bit-parallel, byte-serial form. These lines are buffered by the transceivers and applied to the 488 bus (DIO_1-DIO_8).

Byte Transfer Lines (DAC, RFD, $\overline{DAV}$) – These lines allow for proper transfer of each data byte on the bus between sources and acceptors. The RFD line goes passively true to indicate that all acceptors are ready for data. A source will indicate the data is valid by pulling $\overline{DAV}$ LOW. Upon the reception of valid data by all acceptors, DAC will go passively true to indicate that the data has been accepted by all acceptors.

Bus Management Lines ($\overline{ATN}$, $\overline{IFC}$, $\overline{SRQ}$, $\overline{REN}$, $\overline{EOI}$) – These lines are used to manage an orderly flow of information across the interface lines.

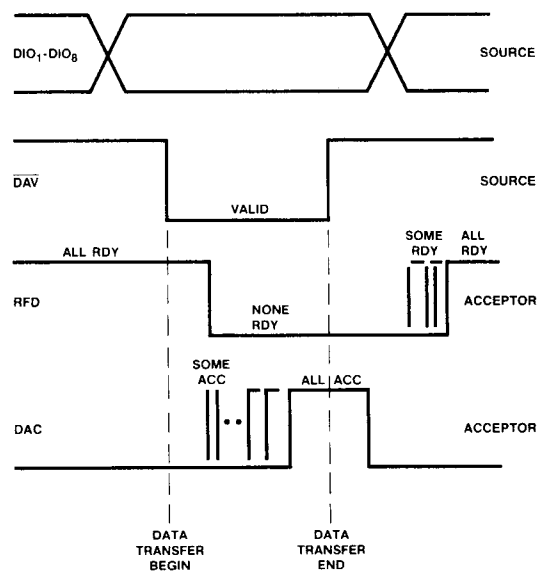
Attention ($\overline{ATN}$) – The $\overline{ATN}$ signal is sent true over the interface to disable current talkers and listeners, freeing the

Table 1 Register Access

RS_2	RS_1	RS_0	R/W	Register Title	Register Symbol
0	0	0	1	Interrupt Status	R0R
0	0	0	0	Interrupt Mask	R0W
0	0	1	1	Command Status	R1R
0	0	1	0	Unused	
0	1	0	1	Address Status	R2R
0	1	0	0	Address Mode	R2W
0	1	1	1	Auxiliary Command	R3R
0	1	1	0	Auxiliary Command	R3W
1	0	0	1	Address Switch*	R4R
1	0	0	0	Address	R4W
1	0	1	1	Serial Poll	R5R
1	0	1	0	Serial Poll	R5W
1	1	0	1	Command Pass-Through	R6R
1	1	0	0	Parallel Poll	R6W
1	1	1	1	Data-In	R7R
1	1	1	0	Data-Out	R7W

*External to F68488

Fig. 3. Source and Acceptor Handshake



signal lines ($\overline{IB}_0$-$\overline{IB}_7$). During the $\overline{ATN}$ active state, devices monitor the DIO_1-DIO_8 lines for addressing or an interface command. Data flows on the DIO_1-DIO_8 when $\overline{ATN}$ is inactive (HIGH).

Interface Clear ($\overline{IFC}$) – The $\overline{IFC}$ signal is used to put the interface system into a known quiescent state.

Service Request ($\overline{SRQ}$) – The $\overline{SRQ}$ signal is used to indicate a need for attention in addition to requesting an interruption in the current sequence of events. This indicates to the controller that a device on the bus is in need of service.

Remote Enable ($\overline{REN}$) – The $\overline{REN}$ signal is used to select one of two alternate sources of devices programming data, local, or remote control.

END or Identify ($\overline{EOI}$) – The $\overline{EOI}$ signal is used to signal the end of a multiple byte transfer sequence and, in conjunction with $\overline{ATN}$, executes a parallel polling sequence.

Transmit/Receive Control Signals ($T/\overline{R}_1$, $T/\overline{R}_2$) – These two signals are used to control the bus transceivers that drive the interface bus. It is assumed that transceivers equivalent to the F3447 or F3448 will be used, where each transceiver has a separate Transmit/Receive control pin. These pins can support one TTL load each. The outputs can then be grouped as shown in *Figure 1* with $\overline{SRQ}$ hardwired HIGH to transmit. The $\overline{REN}$, $\overline{IFC}$, and $\overline{ATN}$ lines are hardwired LOW to receive. The $\overline{EOI}$ line is controlled by $T/\overline{R}_1$ through the bus transceiver, allowing it to transmit or receive. The $T/\overline{R}_1$ line operates exactly as $T/\overline{R}_2$, except during the parallel polling sequence. During parallel poll, $\overline{EOI}$ will be made an input by $T/\overline{R}_1$ while the $\overline{DAV}$ and $\overline{IB}_0$-$\overline{IB}_7$ lines are outputs.

GPIA Internal Controls & Registers

There are 15 locations accessible to the MPU data bus that are used for transferring data to control the various functions of the device and provide current device status. Seven of these registers are write-only and eight are read-only. The various registers are accessed according to the three least significant bits of the MPU address bus and the status of the Read/Write line. One of the 15 registers is external to the device, but an address switch register is provided for reading the address switches. *Table 2* shows actual bit contents of each of the registers.

Data-In Register R7R – The data-in register is an actual 8-bit storage register used to move data from the interface bus when the device is a listener. Reading the register does not destroy information in the data-out register. The DAC (data accepted) line will remain LOW until the MPU removes the byte from the data-in register. The device will automatically finish the handshake by allowing DAC to go HIGH. In RFD (ready for data) hold-off mode, a new handshake is not initiated until a command is sent allowing the device to release hold-off. This will delay a talker until the available information has been processed.

Data-In Register (Read-Only)

DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

DI_0-DI_7 – correspond to DIO_1-DIO_8 of the 488-1975 standard and $\overline{IB}_0$-$\overline{IB}_7$ of the F68488

Data-Out Register R7W – The data-out register is an actual 8-bit storage register used to move data out of the device onto the interface bus. Reading from the data-in register has no effect on the information in the data-out register. Writing to the data-out register has no effect on the information in the data-in register.

Data-Out Register (Write-Only)

DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

DO_0-DO_7 – correspond to DIO_1-DIO_8 of the 488-1975 standard and $\overline{IB}_0$-$\overline{IB}_7$ of the F68488

Interrupt Mask Register R0W – The interrupt mask register is a 7-bit storage register used to select the particular events that will cause an interrupt to be sent to the MPU. The seven control bits may be set independently of each other. If dsel (bit 7 of the address mode register) is set HIGH, CMD (bit 2) will interrupt SPAS or RLC. If dsel is set LOW, CMD will interrupt on UACG, UUCG, and DCAS in addition to RLC and SPAS. The command status register R1R may then be used to determine which command caused the interrupt. Setting GET (bit 5) allows an interrupt to occur on the Group Execute Trigger Command. The END bit (bit 1) allows an interrupt to occur if $\overline{EOI}$ is true (LOW) and $\overline{ATN}$ is false (HIGH). The APT bit (bit 3) allows an interrupt to occur indicating that a secondary address is available to be examined by the MPU if apte (bit 0 of the address mode register) is enabled, listener or talker primary address is received, and a Secondary Command Group is received. A typical response for a valid secondary address would be to set msa (bit 3 of the auxiliary command register) and dacr (bit 4 of the auxiliary command register), releasing the DAC handshake. The BI bit (bit 0) indicates that a data byte is waiting in the data-in register. BI is set HIGH when the data-in register is full. The BO bit (bit 6) indicates that the data-out register is empty. BO is set when the data-out register is empty. The IRQ bit (bit 7) allows any interrupt to be passed to the MPU.

Interrupt Mask Register (Write-Only)

IRQ	BO	GET	X	APT	CMD	END	BI

IRQ – Mask bit for $\overline{IRQ}$ Output

Table 2 Internal Register Contents

Register Name	Mnemonic	Bit 7	6	5	4	3	2	1	0
Interrupt Mask Register	R0W	IRQ	BO	GET		APT	CMD	END	BI
Interrupt Status Register	R0R	INT	BO	GET		APT	CMD	END	BI
Command Status Register	R1R	UACG	REM	LOK		RLC	SPAS	DCAS	UUCG
Unused	R1W								
Address Status Register	R2R	ma	to	lo	ATN	TACS	LACS	LPAS	TPAS
Address Mode Register	R2W	dsel	to	lo		hlde	hlda		apte
Auxiliary Command Register	R3R	Chip	DAC	DAV	RFD	msa	rtl	ulpa	fget
	R3W	RESET	rfdr	feoi	dacr	msa	rtl	dacd	fget
Address Switch Register	R4R	UD_3	UD_2	UD_1	AD_5	AD_4	AD_3	AD_2	AD_1
Address Register	R4W	lsbe	dal	dat	AD_5	AD_4	AD_3	AD_2	AD_1
Serial Poll Register	R5R	S_8	SRQS	S_6	S_5	S_4	S_3	S_2	S_1
	R5W	S_8	rsv	S_6	S_5	S_4	S_3	S_2	S_1
Command Pass-through Register	R6R	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
Parallel Poll Register	R6W	PPR_8	PPR_7	PPR_6	PPR_5	PPR_4	PPR_3	PPR_2	PPR_1
Data-In Register	R7R	DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0
Data-Out Register	R7W	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

BO – Interrupt on Byte Output

GET – Interrupt on Group Execute Trigger

APT – Interrupt on Secondary Address Pass-Through

CMD – Interrupt on SPAS + RLC + $\overline{\text{dsel}}$ (DCAS + UUCG + UACG)

END – Interrupt on $\overline{\text{EOI}}$ and $\overline{\text{ATN}}$

BI – Interrupt on Byte Input

Interrupt Status Register R0R – The interrupt status register is a 7-bit storage register that corresponds to the interrupt mode register with an additional bit, INT (bit 7). Except for the INT bit, the other bits in the status register are set regardless of the state of the interrupt mode register when the corresponding event occurs. The IRQ (MPU Interrupt) is cleared when the MPU reads from the register. The INT bit is the logical OR of the other six bits ANDed with the respective bit of R0W.

Interrupt Status Register (Read-Only)

INT	BO	GET	X	APT	CMD	END	BI

INT – Logical OR of all other bits in this register ANDed with the respective bits in the interrupt mask register

BO – A byte of data has been output.

GET – A Group Execute Trigger has occurred.

APT – An Address Pass-Through has occurred.

CMD – SPAS + RLC + $\overline{\text{dsel}}$ (DCAS + UUCG + UACG) has occurred.

END – An $\overline{\text{EOI}}$ has occurred with $\overline{\text{ATN}}$ = HIGH.

BI – A byte has been input.

Serial Poll Register R5R/W – The serial poll register is an 8-bit storage register that can be both written into and read from by the MPU. It is used for establishing the status byte that the device sends out when it is serial poll enabled. Status may be placed in bits 0 through 5 and bit 7. Bit 6 rsv (request for service) is used to drive the logic that controls the $\overline{\text{SRQ}}$ line on the bus telling the controller that service is needed. This same logic generates the service request state (SRQS) signal that is substituted in the bit 6 position when the status byte is read by the MPU $\overline{IB_0}$-$\overline{IB_7}$. In order to initiate an rsv (request for service), the MPU sets bit 6 true (generating an rsv signal) and this in turn causes the device to pull down the $\overline{\text{SRQ}}$ line. The SRQS signal is the same as rsv when SPAS is false. Bit 6, as read by the MPU, will be the SRQS.

Serial Poll Register (Read)

S_8	SRQS	S_6	S_5	S_4	S_3	S_2	S_1

S_1-S_8 – Status bits

SRQS – Bus is in service request status state

Serial Poll Register (Write)

S_8	rsv	S_6	S_5	S_4	S_3	S_2	S_1

S_1-S_8 – Status bits

rsv – Generate a service request

Parallel Poll Register R6W – This register will be loaded by the MPU, and the complement of the bits in this register will be delivered to the instrument bus (IB_0-IB_7) during PPAS (Parallel Poll Active State). This register powers up in the PP0 (Parallel Poll No Capability) state. The reset bit (auxiliary command register bit 7) will clear this register to the PP0 state.

The parallel poll interface function is executed by this device using the PP2 subset (Omit Controller Configuration Capability). The controller cannot directly configure the parallel poll output of this device. This must be done by the MPU. The controller will be able to configure the parallel poll indirectly by issuing an addressed command that has been defined in the MPU software.

Parallel Poll Register (Write-Only)

PP_8	PP_7	PP_6	PP_5	PP_4	PP_3	PP_2	PP_1

Bits delivered to bus during Parallel Poll Active State (PPAS)

Register powers-up in the PP0 state.

Parallel Poll is executed using the PP2 subset.

Address Mode Register R2W – The address mode register is a storage register with six bits for control: to, lo, hlde, hlda, dsel, and apte. The to bit (bit 6) selects the talker/listener and addresses the device to talk only. The lo bit (bit 5) selects the talker/listener and sets the device to listen only. The apte bit (bit 0) is used to enable the extended addressing mode. If apte is set LOW, the device goes from the TPAS (Talker Primary Address State) directly to the TADS (Talker Addressed State). If apte is set HIGH and the secondary address is valid, set msa true. The hlda bit (bit 2) holds off RFD (Ready for Data) on all data until rfdr is set true. The hlde bit (bit 3) holds off RFD on $\overline{EOI}$ enabled (LOW) and $\overline{ATN}$ not enabled (HIGH). This allows the last byte in a block of data to be continually read as needed. Writing rfdr true (HIGH) will release the handshake.

Address Mode Register (Write-Only)

dsel	to	lo	X	hdle	hdla	X	apte

dsel – Configure for automatic completion of handshake sequence on occurrence of GET, UACG, UUCG, SDC, or DCL commands

to – Set to talk-only mode

lo – Set to listen-only mode

hdle – Hold-off RFD on end

hdla – Hold-off RFD on all data

apte – Enable the address pass-through feature

Address Status Register R2R – The address status register is not a storage register, but is simply an 8-bit port used to couple internal signal modes to the MPU bus. The status flags represented here are stored internally in the logic of the device. These status bits indicate the addressed state of the talker/listener as well as flags that specify whether the device is in the talk-only or listen-only mode. The ma signal is true when the device is in:

TACS – Talker Active State

TADS – Talker Addressed State

LACS – Listener Active State

LADS – Listener Addressed State

SPAS – Serial Poll Active State

ATN – Bit 4 contains the condition of the attention line

Address Status Register (Read-Only)

ma	to	lo	ATN	TACS	LACS	LPAS	TPAS

ma – My address has occurred.

to – The talk-only mode is enabled.

lo – The listen-only mode is enabled.

ATN – The Attention command is asserted.

TACS – GPIA is in the Talker Active State.

LACS – GPIA is in the Listener Active State.

LPAS – GPIA is in the Listener Primary Addressed State.

TPAS – GPIA is in the Talker Primary Addressed State.

Address Switch Register R4R – The address switch register is external to the device. There is an enable line ($\overline{ASE}$) to be used to enable 3-state drivers connected between the address switches and the MPU. When the MPU addresses the address switch register, the enable line directs the switch information to

5

be sent to the MPU. The five least significant bits of this 8-bit register are used to specify the bus address of the device, and the remaining three bits may be used at the discretion of the user. The most probable use of one or two of the bits is for controlling the listen-only or talk-only functions.

Address Switch Register (Read-Only)

UD_3	UD_2	UD_1	AD_5	AD_4	AD_3	AD_2	AD_1

AD_1-AD_5 – Device Address

UD_1-UD_3 – User Definable Bits

When this register is addressed, the $\overline{ASE}$ pin is set to allow external address switch information to be read from a bus device.

Address Register R4W – The address register is an 8-bit storage register. The purpose of this register is to carry the primary address of the device. The primary address is placed in the five least significant bits of the register. If external switches are used for device addressing, these are normally read from the address switch register and then placed in the address register by the MPU.

The AD_1-AD_5 bits (0 - 5) are for the device address. The lsbe bit (bit 7) is set to enable the dual primary addressing mode. During this mode, the device will respond to two consecutive addresses; one address with AD_1 equal to 0 and the other address with AD_1 equal to 1. For example, if the device address is $0F, the dual primary addressing mode would allow the device to be addressed at both $0F and $0E. The dal bit (bit 6) is set to disable the listener and the dat bit (bit 5) is set to disable the talker.

This register is cleared by the $\overline{RESET}$ input only (not by the reset bit of the auxiliary command register, bit 7). When $\overline{ATN}$ is enabled and the primary address is received on the $\overline{IB}_0$-$\overline{IB}_7$ lines, the F68488 will set bit 7 of the address status register (MA). This places the F68488 in the TPAS or LPAS.

When $\overline{ATN}$ is disabled, the GPIA may go to one of three states: TACS, LACS or SPAS.

Address Register (Write-Only)

lsbe	dal	dat	AD_5	AD_4	AD_3	AD_2	AD_1

lsbe – Enable dual primary addressing mode

dal – Disable the listener

dat – Disable the talker

AD_1-AD_5 – Primary device address, usually read from address switch register

Register is cleared by $\overline{RESET}$ input pin only.

Auxiliary Command Register R3R/W – Bit 7, reset, initializes the device to the following states (reset is set true by external $\overline{RESET}$ input pin and by writing into the register from the MPU):

SIDS – Source Idle State

AIDS – Acceptor Idle State

TIDS – Talker Idle State

LIDS – Listener Idle State

LACS – Listener Active State

PPIS – Parallel Poll Idle State

PUCS – Parallel Poll Unaddressed to Configure State

PP0 – Parallel Poll No Capability

The rfdr (release RFD handshake) bit (bit 6) allows for completion of the handshake that was stopped by RFD (Ready For Data) hold-off commands hlda and hlde.

The fget (force group execute trigger) bit (bit 0) has the same effect as the GET (Group Execute Trigger) command from the controller. (IEEE STD 488 p. 39.)

The rtl (return to local) bit (bit 2) allows the device to respond to local controls and the associated device functions are operative.

The dacr (release DAC handshake) bit (bit 4) is set HIGH to allow DAC to go passively true. This bit is set to indicate that the MPU has examined a secondary address or an undefined command.

The ulpa (upper/lower primary address) bit (bit 1) will indicate the state of bit 0 on the DIO_1-DIO_8 bus lines at the time the last primary address was received. This bit can be read but not written by the MPU.

The msa (valid secondary address) bit (bit 3) is set true (HIGH) when TPAS (Talker Primary Addressed State) or LPAS (Listener Primary Addressed State) is true. The device will become addressed to listen or talk.

The primary address must have been previously received.

The RFD, DAV, and DAC (Ready for Data, Data Valid, and Data Accepted) bits assume the same state as the corresponding signal on the F68488 package pins. The MPU may only read these bits. These signals are not synchronized with the MPU clock.

The dacd (data accept disable) bit (bit 1) set HIGH by the MPU will prevent automatic handshake on addresses or commands. The dacr bit is used to release the handshake.

The feoi (forced end or identify) bit (bit 5) tells the device to send $\overline{EOI}$ LOW with the next data byte transmitted. The $\overline{EOI}$ line is then returned HIGH after the next byte is transmitted. NOTE: The following signals are not stored but revert to a false (LOW) level one clock cycle (MPU $\phi 2$) after they are set true (HIGH):

1. rfdr
2. feoi
3. dacr

These signals can be written but not read by the MPU.

Auxiliary Command Register

reset	rfdr	feoi	dacr	msa	rtl	dacd	fget	W
reset	DAC	DAV	RFD	msa	rtl	ulpa	fget	R

reset – Initialize the chip to the following status:

1. All interrupts cleared
2. Following bus states are in effect: SIDS, AIDS, TIDS, LIDS, LOCS, PPIS, PUCS, and PP0
3. Bit is set by $\overline{RESET}$ input pin.

DAC – Corresponds to Data Accepted signal on F68488 package pins

DAV – Corresponds to Data Valid signal on F68488 package pins

RFD – Corresponds to Ready For Data signal on F68488 package pins

msa – If GPIA is in LPAS or TDAS, setting msa will force GPIA to LADS or TADS.

rtl – Return to local if local lockout is disabled

ulpa – State of LSB of the address received on the DIO_{1-8} bus lines

fget – Force Group Execute Trigger Command from controller has occurred.

rfdr – Complete handshake stopped by RFD hold-off

feoi – Set $\overline{EOI}$ true, clears after next byte transmitted

dacr – MPU has examined an undefined command or secondary address.

dacd – Prevents automatic handshake on addresses or commands

Command Status Register R1R – The command status register flags commands or states as they occur. These flags or states are simply coupled onto the MPU bus from internal storage nodes.

These are five major address commands. REM shows the remote/local state of the talker/listener.

The RLC bit (bit 3) is set whenever a change of state of the remote/local flip-flop occurs and reset when the command status register is read.

The DCAS bit (bit 1) indicates that either the device clear or selected device clear has been received, activating the device clear function.

The SPAS bit (bit 2) indicates that the SPE command has been received, activating the device serial poll function.

The UACG bit (bit 7) indicates that an undefined address command has been received and, depending on programming, the MPU decides whether to execute or ignore it.

The UUCG bit (bit 0) indicates that an undefined universal command has been received.

Command Status Register (Read)

UACG	REM	LOK	X	RLC	SPAS	DCAS	UUCG

UACG – Undefined Address Command

REM – Remote Enabled

LOK – Local Lockout Enabled

RLC – Remote Local State Changed

SPAS – Serial Poll Active State is in effect.

DCAS – Device Clear Active State is in effect.

UUCG – Undefined Universal Command

Command Pass-Through Register R6R – The command pass-through register is an 8-bit port with no storage. When this port is addressed by MPU, it connects the instrument data bus ($\overline{IB_0}$-$\overline{IB_7}$) to the MPU data bus DB_0-DB_7. This port can be used to pass commands and secondary addresses, that are not automatically interpreted, through to the MPU for inspection.

Command Pass-Through Register (Read Only)

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

An 8-bit port used to pass commands and secondary addresses to the MPU that are not automatically interpreted by the GPIA.

Absolute Maximum Ratings

Voltage of any pin relative to ground	−0.3 V, +7.0 V
Operating Temperature (Ambient)	0°C, +70°C
Storage Temperature (Ambient)	−55°C, +150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to +70°C, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	
I_{IN}	Input Leakage Current		1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	3-State (OFF State) Input Current D_0-D_7		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
V_{OH}	Output HIGH Voltage D_0-D_7 Other Outputs	 2.4 2.4			V	 I_{Load} = −205 μA I_{Load} = −200 μA
V_{OL}	Output LOW Voltage D_0-D_7 IRQ			 0.4 0.4	V	 I_{Load} = 1.6 mA I_{Load} = 3.2 mA
I_{LOH}	Output Leakage Current (OFF State) $\overline{IRQ}$		 1.0	 10	μA	 V_{OH} = 2.4 V
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D_0-D_7 All Other Inputs			 12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0 MHz
C_{OUT}	Output Capacitance IRQ			5.0	pF	V_{IN} = 0, T_A = 25°C, f = 1.0 MHz

Bus Timing Characteristics

Read *(Figure 4)*

Symbol	Characteristic	Min	Typ	Max	Unit
$t_{cyc}E$	Enable Cycle Time	1.0		25	μs
PW_{EH}	Enable Pulse Width, HIGH	0.45			μs
PW_{EL}	Enable Pulse Width, LOW	0.43			μs
t_{AS}	Set-up Time, Address and R/W Valid to Enable Positive Transistion	160			ns
t_{DDR}	Data Delay Time			320	ns
t_H	Data Hold Time	10			ns
t_{AH}	Address Hold Time	10			ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input			25	ns
Write *(Figure 5)*					
$t_{cyc}E$	Enable Cycle Time	1.0			μs
PW_{EH}	Enable Pulse Width, HIGH	0.45		25	μs
PW_{EL}	Enable Pulse Width, LOW	0.43			μs
t_{AS}	Set-up Time, Address and R/W Valid to Enable Positive Transistion	160			ns
t_{DSW}	Data Set-up Time	195			ns
t_H	Data Hold Time	10			ns
t_{AH}	Address Hold Time	10			ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input			25	ns

5

Fig. 4 Bus Read Timing Characteristics
(Read Information from GPIA)

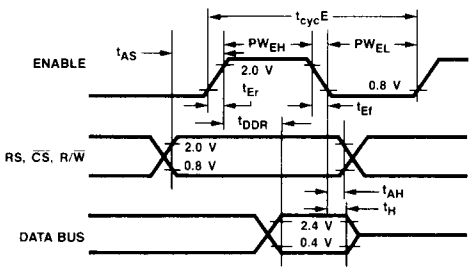
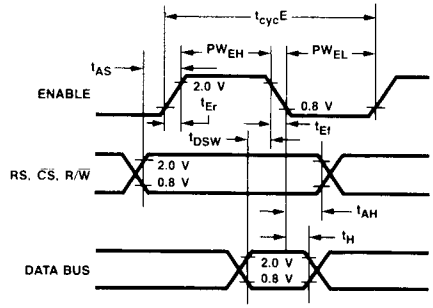


Fig. 5 Bus Write Timing Characteristics
(Write Information into GPIA)



Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F68488P,S	0°C to +70°C
	F68488CP,CS	−40°C to +85°C
	F68488DL	−55°C to +85°C
	F68488DM	−55°C to +125°C
1.5 MHz	F68A488P,S	0°C to +70°C
	F68488CP,CS	−40°C to +85°C
2.0 MHz	F68B488P,S	0°C to +70°C

P = Plastic package, S = CER-DIP package