Product Preview

VSC8144

2.488 Gbit/sec 4:1 SONET/SDH
Transceiver with Integrated Clock Generator

Features

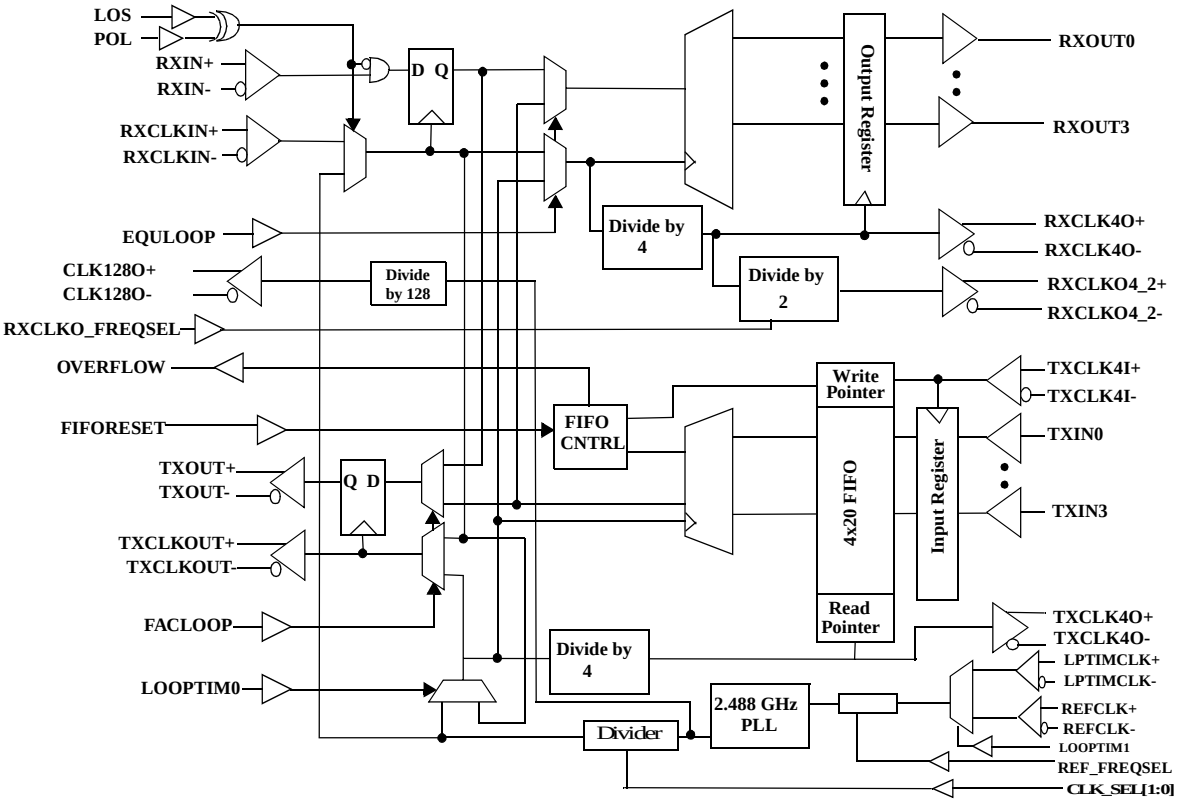
- Multi-rate 4 Bit Transceiver Targeted for SONET OC-48, OC-24, OC-12,. OC-3, and Gigabit Ethernet Rates.
- 4-bit LVDS Low Speed Interface
- On-chip PLL Based Clock Generator
- High-Speed Clock Output with Power Down Option
- Provides Equipment, Facility and Split Loopback Modes as well as Loop Timing Modes.
- Loss of Signal (LOS) Detect Input
- Meets Bellcore Jitter Performance Specifications
- Single 2.5V Power Supply (add 3.3V Supply for TTL)
- 1.5 Watts Max Power Dissipation
- 100-pin PQFP Package 14x14x2mm

General Description

The VSC8144 is a SONET/SDH compatible multi-rate transceiver with integrated clock generator for use in SONET/SDH systems operating at OC-48, OC-24, OC-12, OC-3, or Gigabit Ethernet data rates. The internal clock generator uses a phase locked loop to multiply either a 77.76MHz or 155.52MHz reference clock (SONET/SDH applications) in order to provide the 155Mhz, 622Mhz, 1.244Ghz or 2.488GHz clock for internal logic and output retiming. The 4 bit parallel LVDS interface incorporates an on-board FIFO eliminating loop timing design issues by providing a flexible parallel timing architecture. In addition, the device provides both facility and equipment loopback modes and two loop timing modes. The LVTTL outputs operate at 2.5V. If TTL outputs are necessary, the LVTTL are converted to a TTL output by setting the LVTTL power pin to 3.3V. The VSC8144 operates using a 2.5V power supply, and is packaged in a thermally enhanced 100-pin PQFP. If TTL outputs are used, a 3.3V supply is also necessary.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

VSC8144 Block Diagram



Functional Description

Multirate Internal Clock

A Clock select bus input (CLKSEL[1:0]) allows selection of the internal clock to operate at OC-3,OC-12,OC-48 or Gigabit ethernet rates. The bus consists of two bits and are LVTTL inputs.

Table 1: Reference Frequency

Internal Frequency	*CLKSEL0*	*CLKSEL1*
155.52MHz	0	0
622 MHz	0	1
1244 Mhz	1	0
2488 MHz	1	1

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

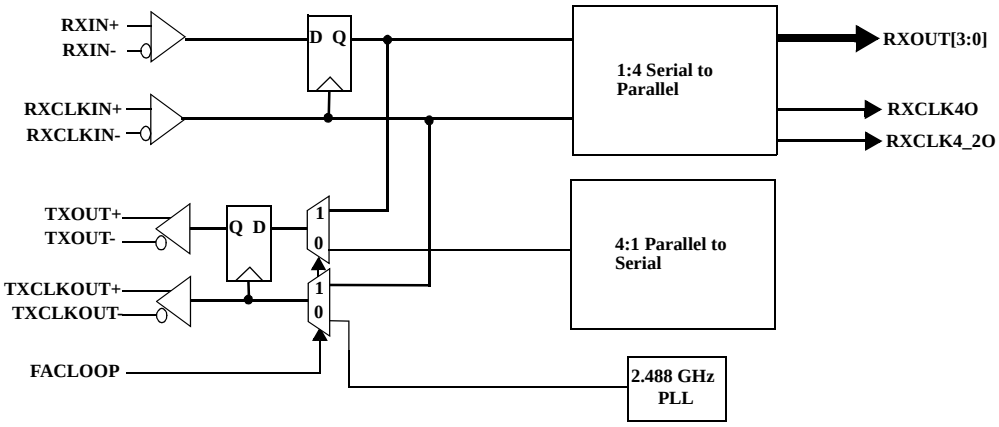
Loss of Signal

The VSC8144 has a LVTTL input LOS to force the part into a Loss of Signal state. Most optics have a TTL output usually called “SD”, (Signal Detect), based on the optical power of the incoming light stream. Depending on the optics manufacturer, this signal is either active high or low. To accommodate polarity differences, the internal Loss of Signal is generated when the POL and LOS inputs are of opposite states. Once active, all zeroes “0” will be propagated downstream using the transmit clock until the optical signal is regained and LOS and POL are in the same logic state.

Loss of Lock

The VSC8144 has a LVTTL output that indicates PLL loss of lock.

Figure 1: Facility Loopback Data Path



Facility Loopback

The facility loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high-speed serial receive data (RXIN) is presented at the high-speed transmit output (TXOUT), as depicted in Figure 1. In addition, the high-speed receive clock input (RXCLKI) is selected and presented at the high-speed transmit clock output (TXCLKOUT). In Facility Loopback mode, the high-speed receive data (RXIN) is also converted to parallel data and presented at the low speed receive output pins (RXOUT[3:0]). The receive clock (RXCLKIN) is also divided down and presented at the low speed clock output (RXCLK4O).

Equipment Loopback Data Path

The Equipment Loopback function is controlled by the EQULOOP signal, which is active high. When the Equipment Loopback mode is activated, the high-speed transmit data generated from the parallel to serial conversion of the low speed data (TXIN[3:0]) is selected and converted back to parallel data in the receiver section and presented at the low speed parallel data outputs (RXOUT[3:0]), as shown in Figure 2. The internally generated 2.488 GHz clock is used to generate the low speed receive output clocks (RXCLK4O and RXCLK4_2O).

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

In Equipment Loopback mode the transmit data (TXIN[3:0]) is serialized and presented at the high-speed output (TXOUT) along with the high-speed transmit clock (TXCLKOUT) which is generated by the on chip PLL.

Figure 2: Equipment Loopback Data Path

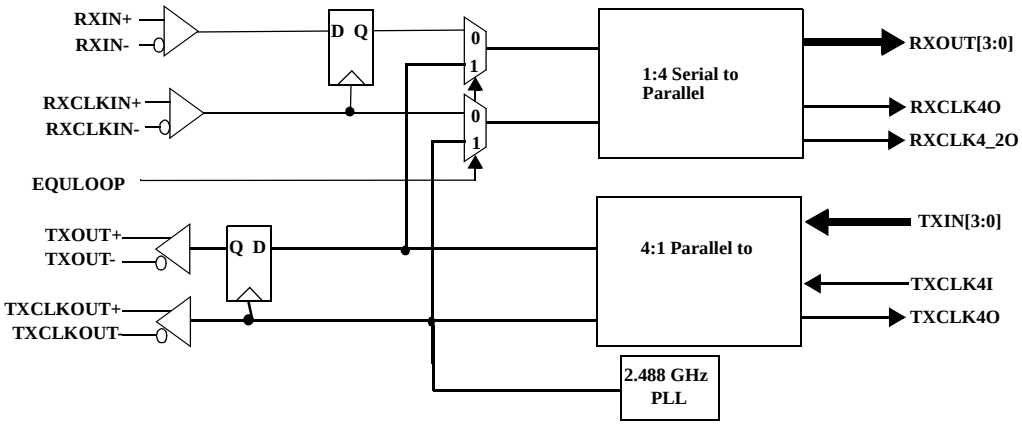
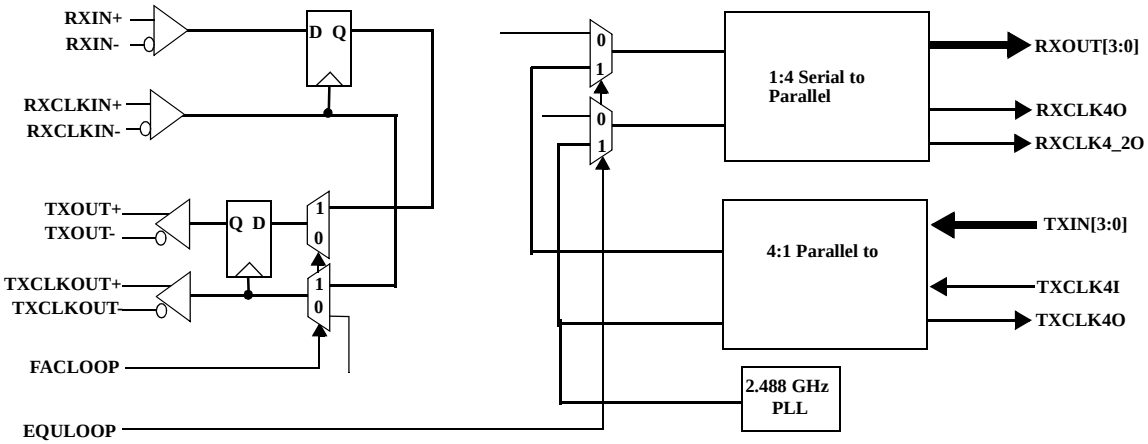


Figure 3: Split Loopback Datapaths



Split Loopback

Equipment and Facility Loopback modes can be enabled simultaneously. In this case, high-speed serial data received (RXIN) and clock (RXCLKIN) are muxed through to the high-speed serial outputs (TXOUT and TXCLKOUT). The low speed 4-bit transmit stream (TXIN[3:0]) is muxed into the low speed 4-bit receive output stream (RXOUT[3:0]). (See figure 3).

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Looptiming

LOOPTIM0 mode bypasses the PLL when LOOPTIM0 is asserted high. In this mode the PLL is bypassed using the receive high-speed clock (RXCLKIN), and the entire part is synchronously clocked from a single external source.

LOOPTIM1 bypasses the reference clock (REFCLK) and uses an external clock as input to the PLL. When LOOPTIM1 is asserted high, The RXCLK4_2O output can be tied to the LPTIMCLK input. In order to meet jitter transfer, the RXCLK4_2O needs to be filtered by a 1X PLL circuit with a narrow pass characteristic. The part is forced out of this mode in Equipment Loopback to prevent the PLL from feeding its own clock back.

Clock Generator

An on-chip Phase Locked Loop (PLL) generates the high speed transmit clock from the externally provided REFCLK input. The on-chip PLL uses a low phase noise reactance based Voltage Controlled Oscillator (VCO) with an on-chip loop filter. The loop bandwidth of the PLL is within the SONET specified limit of 2MHz.

Table 2: Reference Frequency

Reference Frequency	*REF_SEL1*
77.76MHz	0
155.52MHz	1

The customer can select to provide either a 77.76MHz or 155.52MHz reference clock frequency. REF_FREQSEL is used to select the input reference frequency.

The REFCLK should be of high quality since noise on the REFCLK below the loop band width of the PLL will pass through the PLL and appear as jitter on the output. Preconditioning of the REFCLK signal with a VCXO may be required to avoid passing REFCLK noise with greater than 4ps RMS of jitter to the output. The VSC8144 will output the REFCLK noise in addition to the intrinsic jitter from the VSC8144 itself during such conditions.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +2.5V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{CC} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to +5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{CC} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+150^{o}$C

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +2.5V$\pm$5%

Operating Temperature Range ..... 0^{o}C Ambient to $+110^{o}$C Case Temperature

Notes:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8144 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

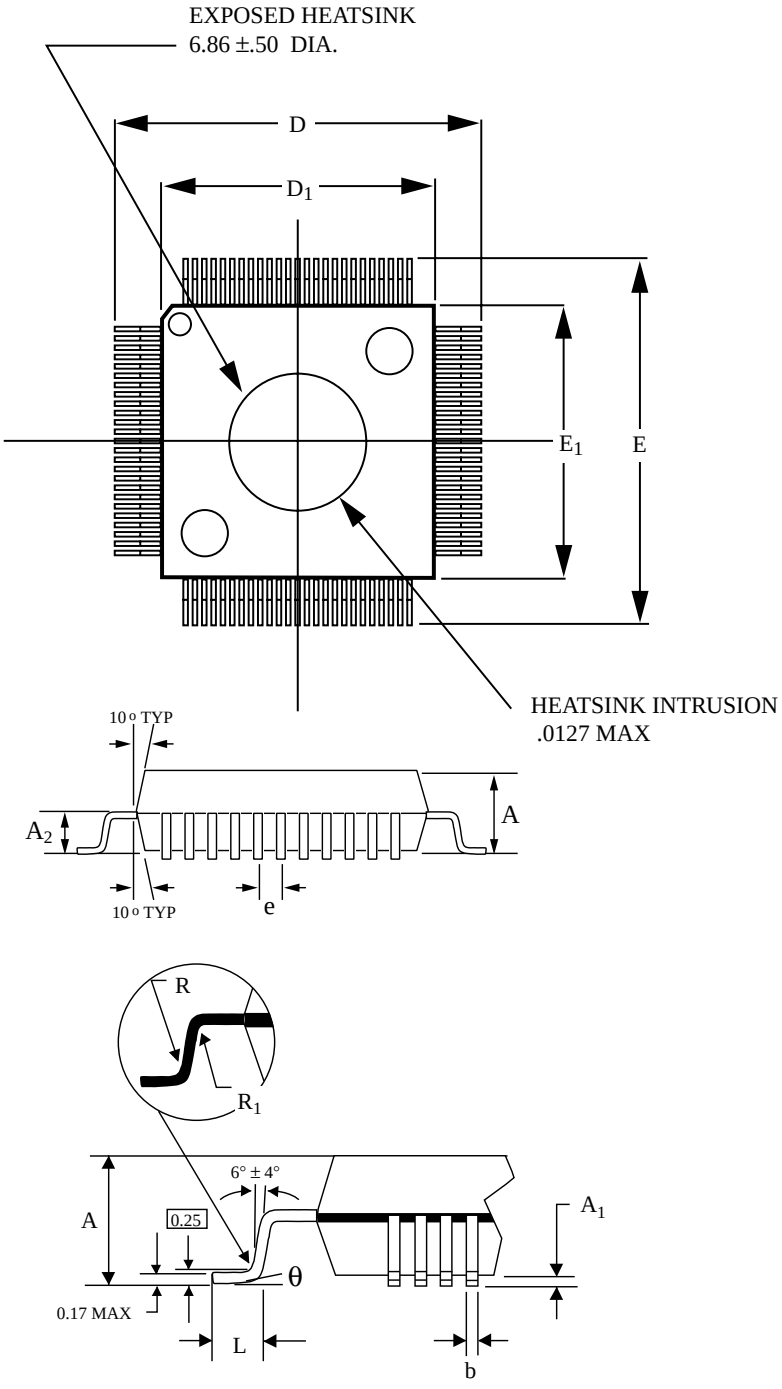
Package Pin Descriptions

Table 3: TBD

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896

Package Information

100 PQFP Package Drawings



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10/-.05
D	17.20	±.25
D1	14.00	±.10
E	17.20	±.25
E1	14.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP

NOTES:
(1) Drawings not to scale.
(2) All units in millimeters unless otherwise noted

Package #: 101-318-3
Issue #: 1

Notice

This document contains information about a proposed product during it's concept phase of development and is subject to change without notice at any time. All features and specification are design goals only. Please contact Vitesse Semiconductor to obtain the latest product status and most recent versions of this specification.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896