APPLIED MICRO CIRCUITS CORPORATION

Part Number S3390

Revision B - November 20, 2002

S3390

DATA SHEET

12.5 Gbps 3.3 V Transimpedance Amplifier

FEATURES

- 12.5 Gbps NRZ Operation
- 9.5 GHz Typical Bandwidth
- 5.5 kΩ Typical Differential Transimpedance
- 3.3 V Power Supply
- 10 pA/rt Hz Typical Noise Current Density
- High Max Input Current
- Low Pulse Width Distortion
- Non-Inverting Single-Ended Output Capability
- 119 mW Typical Power Dissipation
- Wire Bond Die

APPLICATIONS

- SONET OC-192
- Fiber Optic Data Links
- HDTV/CATV Fiber Links
- Fiber Optics Access Boxes
- 10G Ethernet Fiber Links

GENERAL DESCRIPTION

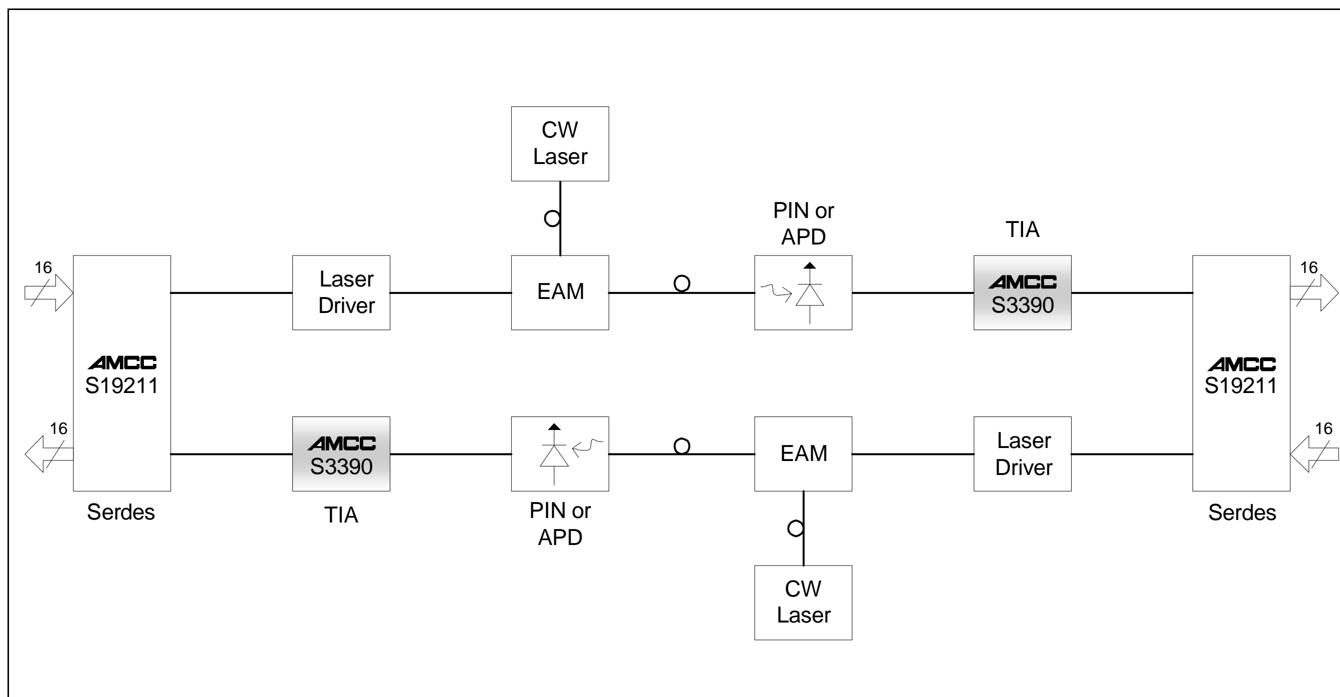
The S3390 is a high-speed transimpedance amplifier for 12.5 Gbps applications. The S3390 provides a high performance solution for amplifying a photodetector output current into a differential or single-ended voltage swing. This output voltage may then be used as an input to clock recovery unit with or without a post amplifier.

Input currents as high as 2.0 mA can be amplified with low duty cycle distortion. The low input noise allows signals down to 13 µA (peak) to be detected with a signal to noise ratio of 22 dB (allows for BER < 1E-10).

The outputs are voltage limited to 600 mV, differential, in order to allow a wide input dynamic range without exceeding the input voltage range of the transceiver device.

Figure 1 contains a typical system block diagram for the S3390 device.

Figure 1. Typical System Application



DETAILED DESCRIPTION

Figure 2 depicts the block diagram of the S3390 transimpedance amplifier. The amplifier circuitry consists of a transimpedance stage with a gain of 370 Ω, a gain stage with a gain of six and an output stage with a gain of 2.5, providing a total gain of approximately 5.5 kΩ.

A DC cancellation loop is used to ensure that the signal into the transimpedance stage is always at the same common mode level irrespective of the amplitude of the input signal. This optimizes the dynamic range by preventing the transimpedance stage from becoming saturated.

Figure 2. S3390 Detailed Block Diagram

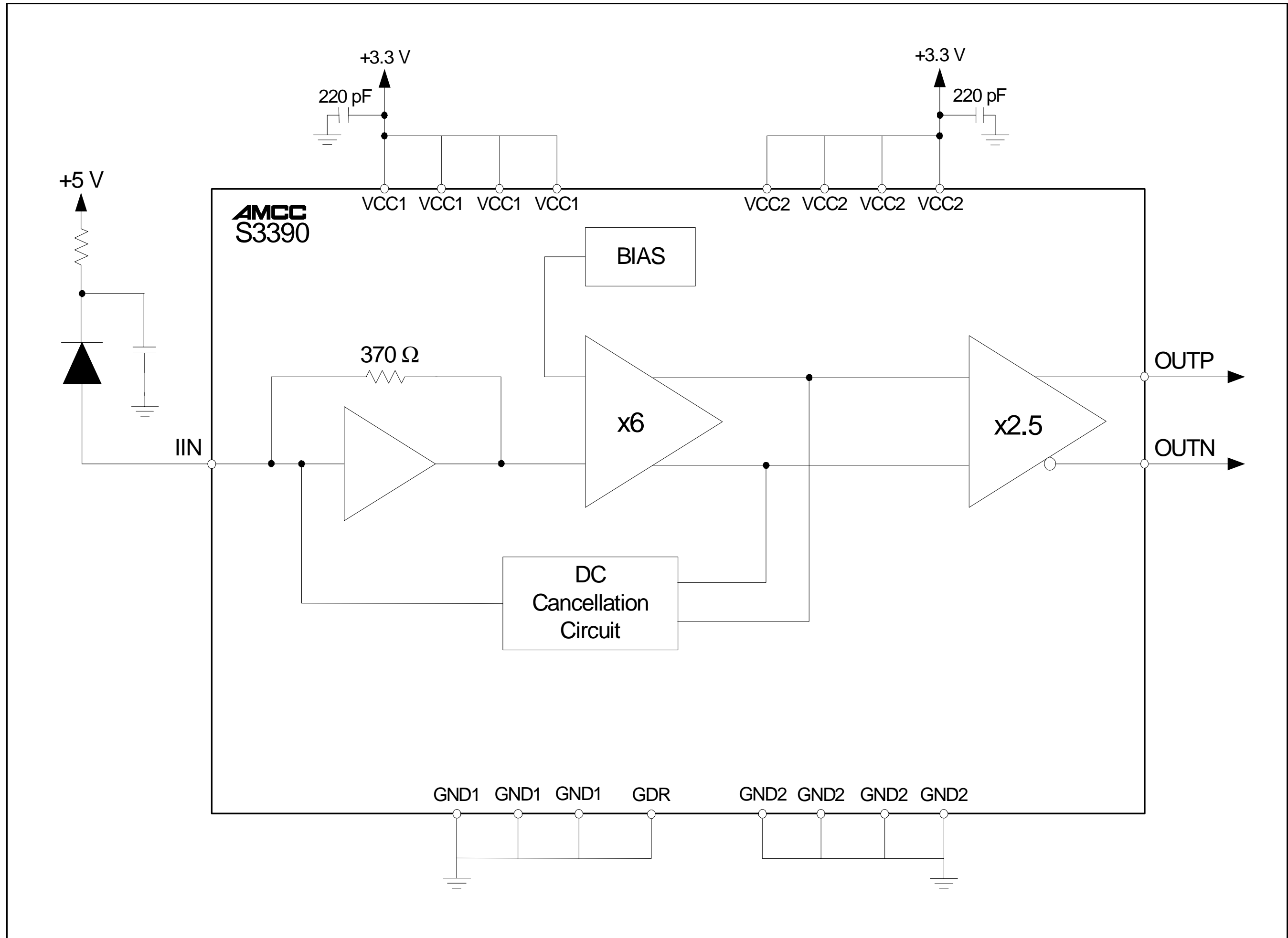


Table 1. Pad Assignment and Description

Pin Name	I/O[1]	Pad #	Coordinate [X,Y][2]	Description
GND1	GND	1 2 20	[295.2, 97.5] [447.6, 97.5] [97.5, 295.2]	Ground
GND2	GND	4 5 6 7	[752.4, 97.5] [904.8, 97.5] [1057.2, 97.5] [1102.5, 295.2]	Ground
GDR	GND	3	[600, 97.5]	This pad is an internal shield and should be connected to Ground.
VCC1	PWR	14 15 16 17	[523.8, 1102.5] [371.4, 1102.5] [219, 1102.5] [97.5, 950.1]	Positive 3.3 V supply
VCC2	PWR	10 11 12 13	[1102.5, 950.1] [981, 1102.5] [828.6, 1102.5] [676.2, 1102.5]	Positive 3.3 V supply
IIN	I	18	[97.5, 600]	PIN diode input
NC	I	19	[97.5, 447.6]	No connect
OUTP	O	9	[1102.5, 675.68]	Positive output. The output must be terminated 50 Ω (AC coupled) to GND or 100 Ω line-to-line. An unused output must be terminated 50 Ω (AC coupled) to GND.
OUTN	O	8	[1102.5, 523.28]	Negative output. The output must be terminated 50 Ω (AC coupled) to GND or 100 Ω line-to-line. An unused output must be terminated 50 Ω (AC coupled) to GND.

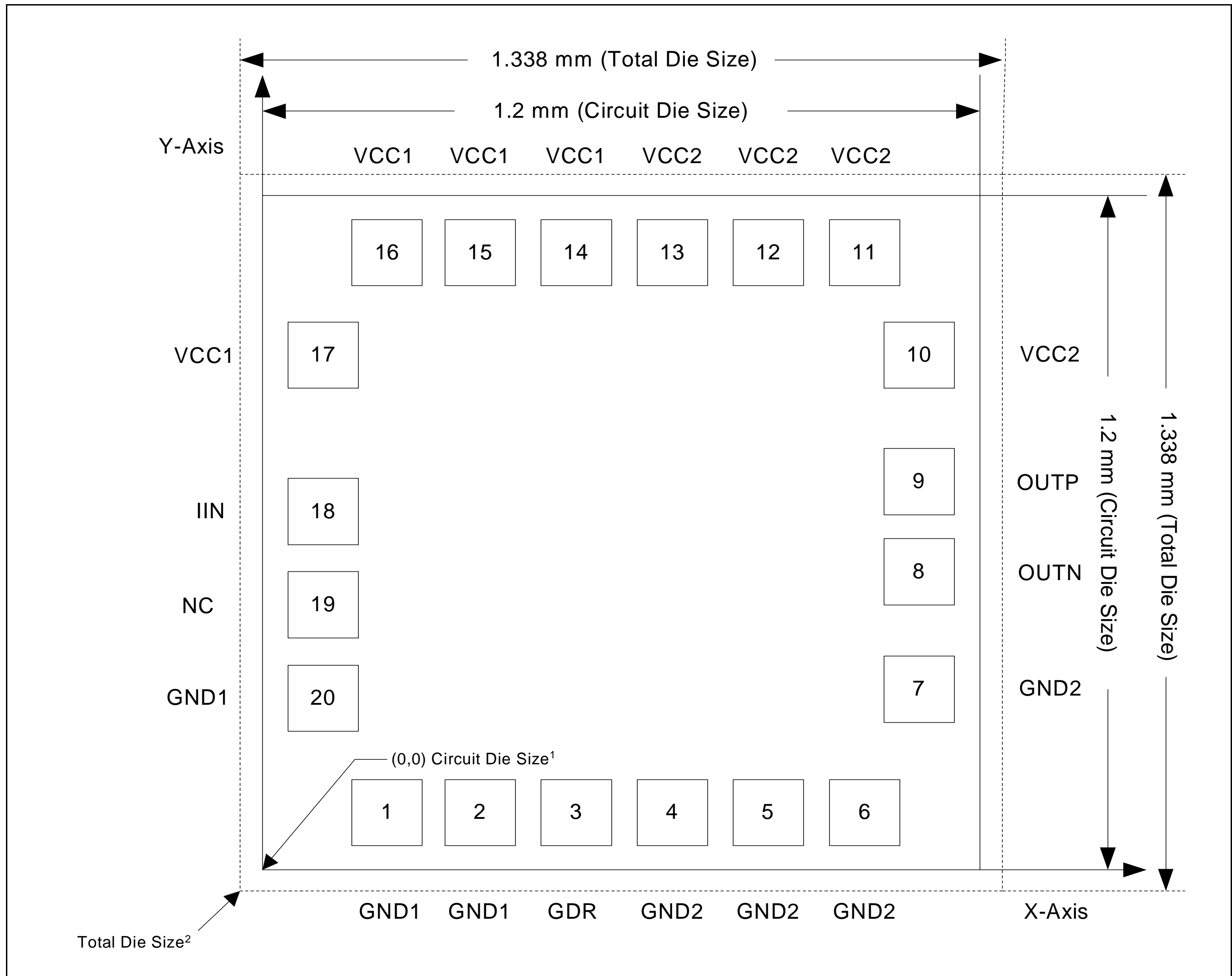
1. I = Input Pin, O = Output Pin, PWR = Power Pin, GND = Ground Pin.
2. The coordinates are in µm from the lower left corner of the circuit die to the center of the pad.

Notes:
a. Total pad size is 114 µm x 114 µm. The size of the exposed area is 100 µm x 100 µm.
b. The back of the die is not metallized and should be connected to GND using conductive epoxy.
c. All Supply and Ground pads should be connected.

Die Issues

Die level test only. Tests include transimpedance gain, transimpedance bandwidth, output ripple, output reflection coefficient, differential output swing, parametric test on I/O and power pins, and visual inspection.

Figure 3. Bonding Pad Location

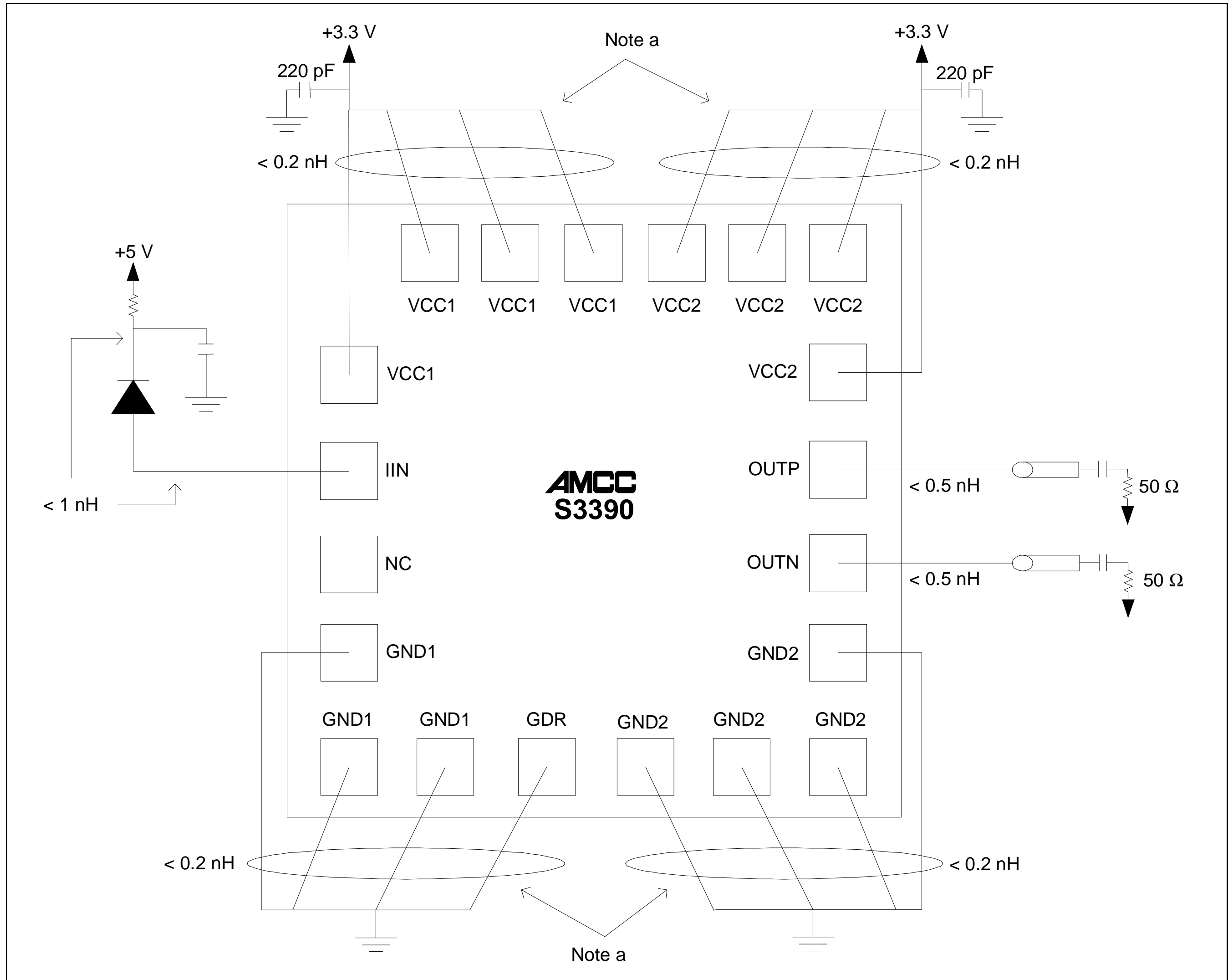


1. The circuit die size is the smallest possible size of the die. The lower left-hand corner of the circuit die is the origin of the xy-coordinate system. Pad coordinates indicated in Table 1 are measured from this origin to the pad's center.
2. The total die size is the largest possible size of the die. It includes a splicing area around the circuit die. The actual size of any given die may vary in size from the minimum (circuit die) size to the maximum (total die) size.
3. The tested dies do not have probe marks at the following pad location: 7, 13, 14, 19.

Note:

a. Die thickness is 0.254 mm (10 mil).

Figure 4. Recommended Bond Wire Inductance



Note:

a. Maximize bondwire separations between VCC1 & VCC2 and GND1/GDR & GND2.

Table 2. Typical Gold Bond Wire Inductance

Bond Wire Diameter (μm)	Inductance (nH/mm)
25	0.81
30	0.77
32	0.76

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S3390 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated or at any other conditions beyond those indicated in the *Recommended Operating Conditions* of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-55	150	°C
Operating Junction Temperature	T_J		120	°C
Power Supply Voltage	VCC1, VCC2	-0.5	4.0	V
Input Current	IIN		6	mA_{rms}
			12	mA_p
ESD Voltage Rating[1], (High Speed I/O)	V_{ESD1}	100		V
ESD Voltage Rating[1], (All Other I/O)	V_{ESD2}	400		V

1. The S3390 ESD voltage ratings are based on the human body model.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Junction temperature under bias	T_J	0		100	°C
Ambient temperature under bias	T_A	0		85	°C
Power Supply Voltage	VCC1, VCC2	3.13	3.3	3.47	V

Table 5. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Current	I_{CC}		36	49	mA	
Input Bias Voltage	V_{INBIAS}	0.8	0.9	1	V	
Common Mode Output Voltage	V_{OCM}	V_{CC} - 0.2	V_{CC} - 0.25	V_{CC} - 0.3	V	100 Ω line-to-line termination, or 50 Ω (AC coupled) termination to Ground.

Table 6. AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
AC Transimpedance	Z_T	2375	2750	4000	V/A	Single-ended, 50 Ω load (AC coupled)
		4750	5500	8000	V/A	Differential, 100 Ω load, line to line

Table 6. AC Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
-3 dB Bandwidth	BW_{-3dB}	8	9.5	14.5	GHz	See Note 1.
Low Frequency -3dB Cutoff	BW_{LF}		25	40	kHz	
Peak Input Current	I_{PK}	2.0	2.2		mA	10.7 Gbps
		1.8	2.0			12.5 Gbps
Input Noise Current Density	I_n		10	12.5	pA/rt Hz	0 – 10 GHz
Input Noise Current	I_{NOISE}		1	1.25	µArms	0 – 10 GHz
Differential Output Swing	V_{OD}	375	500	600	mV	Peak-to-peak differential. 100 Ω line-to-line termination.
Single-Ended Output Swing	V_{OS}	187	250	300	mV	Single-ended, 50 Ω (AC coupled) line termination to GND.
Output Resistance	R_{OUT}	42	50	58	Ω	
Output Reflection Coefficient[1]	S_{22}		-13	-10	dB	1 – 8 GHz. Differential output
			-8	-6		1 – 8 GHz. Single-Ended output
			-5	-4		8 – 15 GHz Single-Ended output
Output Ripple[1]	Ripple	-0.5	0	0.5	dB	1 – 8 GHz.
Group Delay Deviation[1] (100 MHz to 8 GHz)	Group Delay		15	20	ps	Input Current = 10 µA.
Group Delay Deviation[1] (8 GHz to F_{-3dB})	Group Delay		30	40	ps	Input Current = 10 µA.
Peaking[1,2]	Peak		1	2	dB	25 kHz to 10 GHz.
Total Jitter (Pk to Pk) (At 1E-12 BER)	J_T		0.05	0.10	UI	I_{IN} = 1.8 mA_{p-p}, 10.7 Gbps, PRBS 2^31-1
			0.05	0.11		I_{IN} = 2.0 mA_{p-p}, 10.7 Gbps, PRBS 2^31-1
			0.08	0.15		I_{IN} = 2.5 mA_{p-p}, 11.1 Gbps, PRBS 2^31-1
			0.05	0.12		I_{IN} = 1.8 mA_{p-p}, 12.5 Gbps, PRBS 2^31-1

1. Assuming a total input bond wire inductance (between the photodiode and IIN pin) of 1 nH and photodiode capacitance of 0.2 pF and photodiode series resistance of 10 Ω.
2. Electrical domain only. The value does not take into account the optical roll-off. The actual value with optical roll-off should be better.

TYPICAL OPERATING CHARACTERISTICS

Figure 5. Gain Compression (Differential)

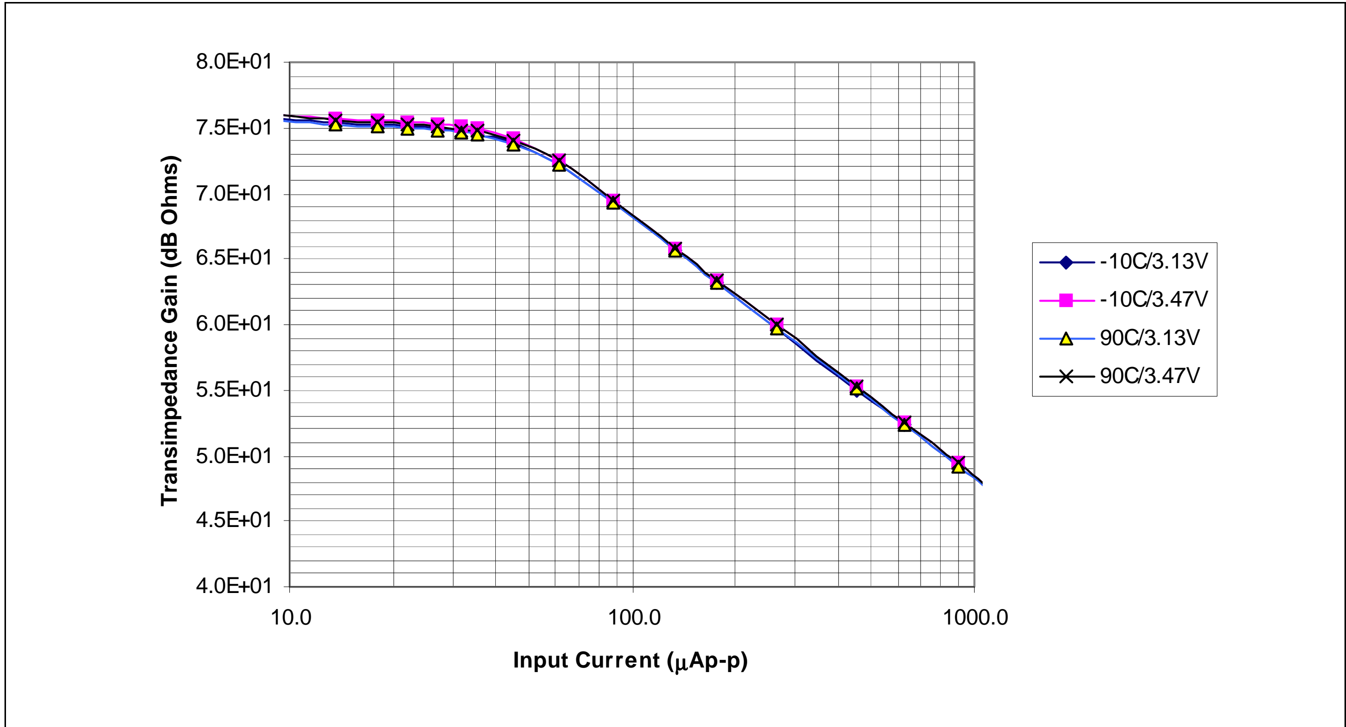


Figure 6. Eye Diagram (10.7 Gbps, PRBS 2^{23}-1, I_{IN} = 1.8 mA_{p-p}, 25°C, 3.3 V)

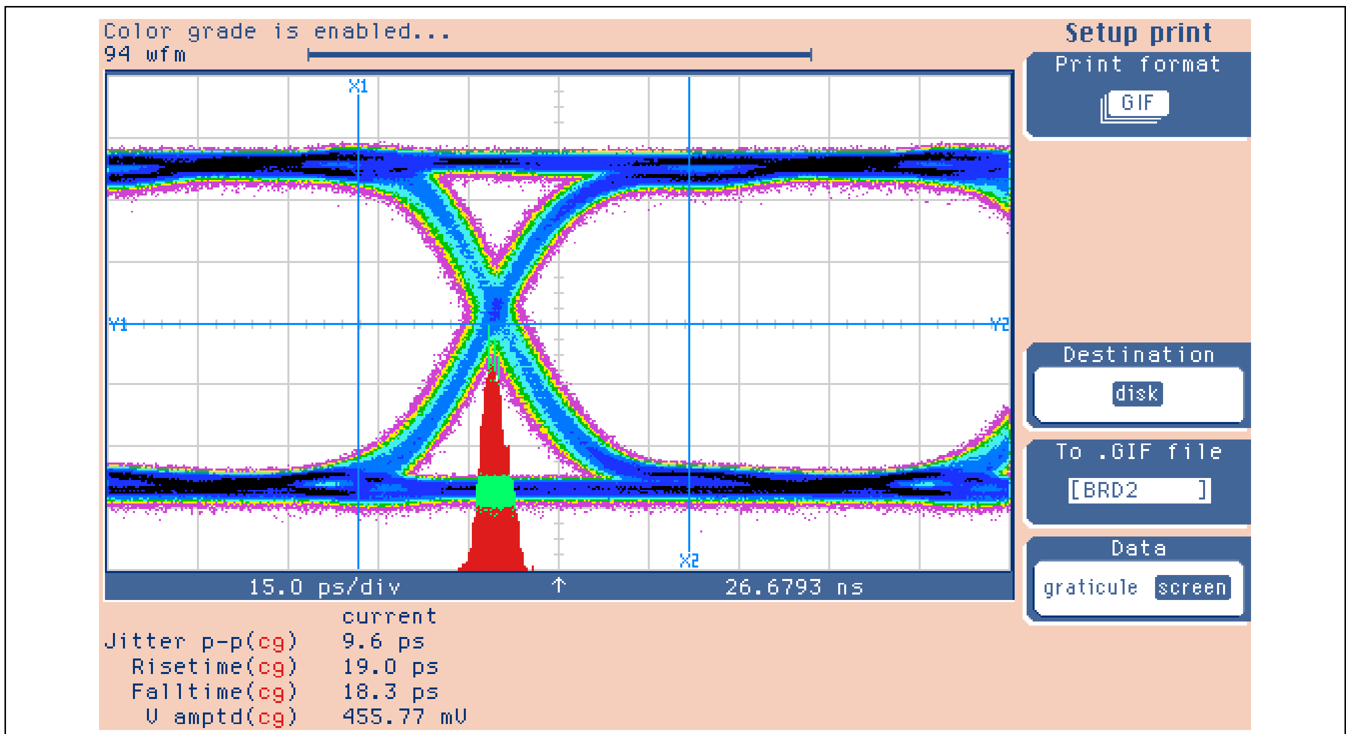


Figure 7. Eye Diagram (12.5 Gbps, PRBS 2^{23}-1, I_{IN} = 1.8 mA_{p-p}, 25°C, 3.3 V)

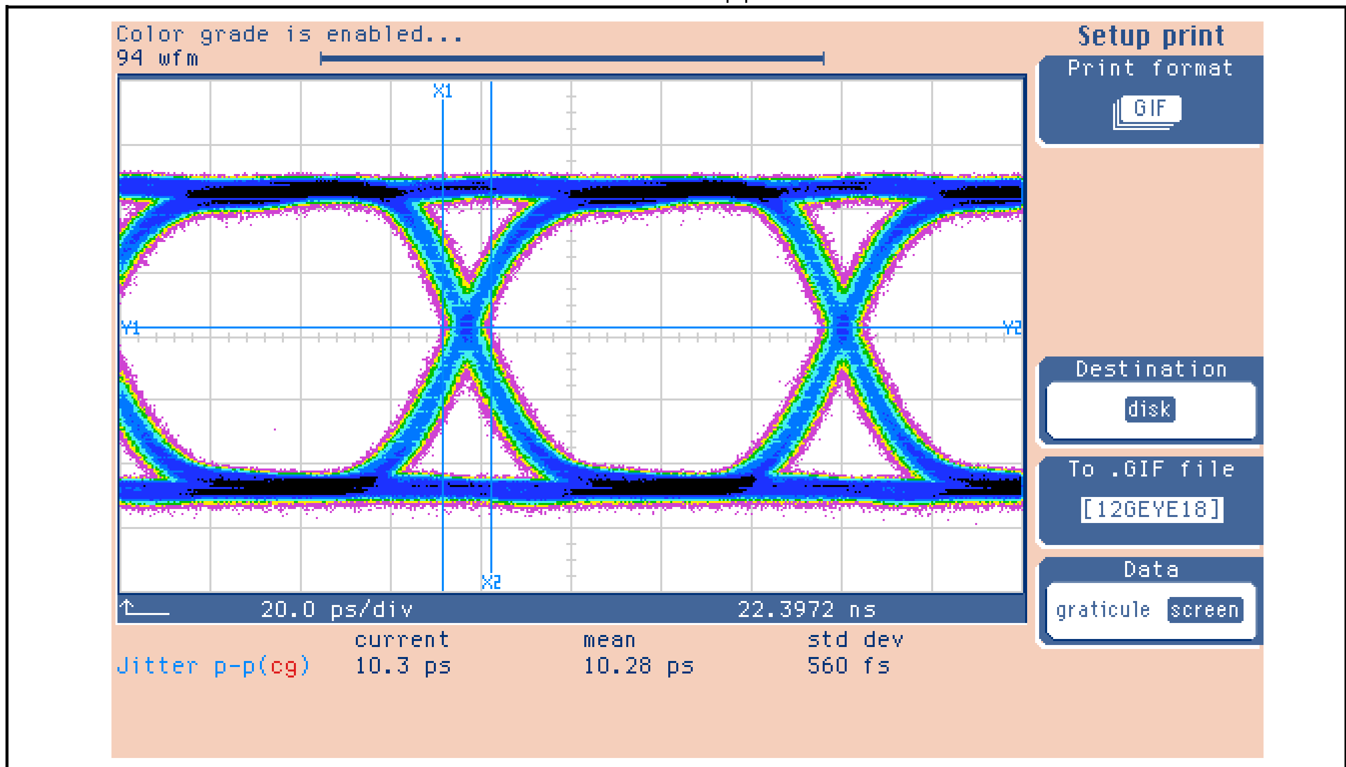


Figure 8. Eye Diagram (12.5 Gbps, PRBS 2^{23}-1, I_{IN} = 2.5 mA_{p-p}, 25°C, 3.3 V)

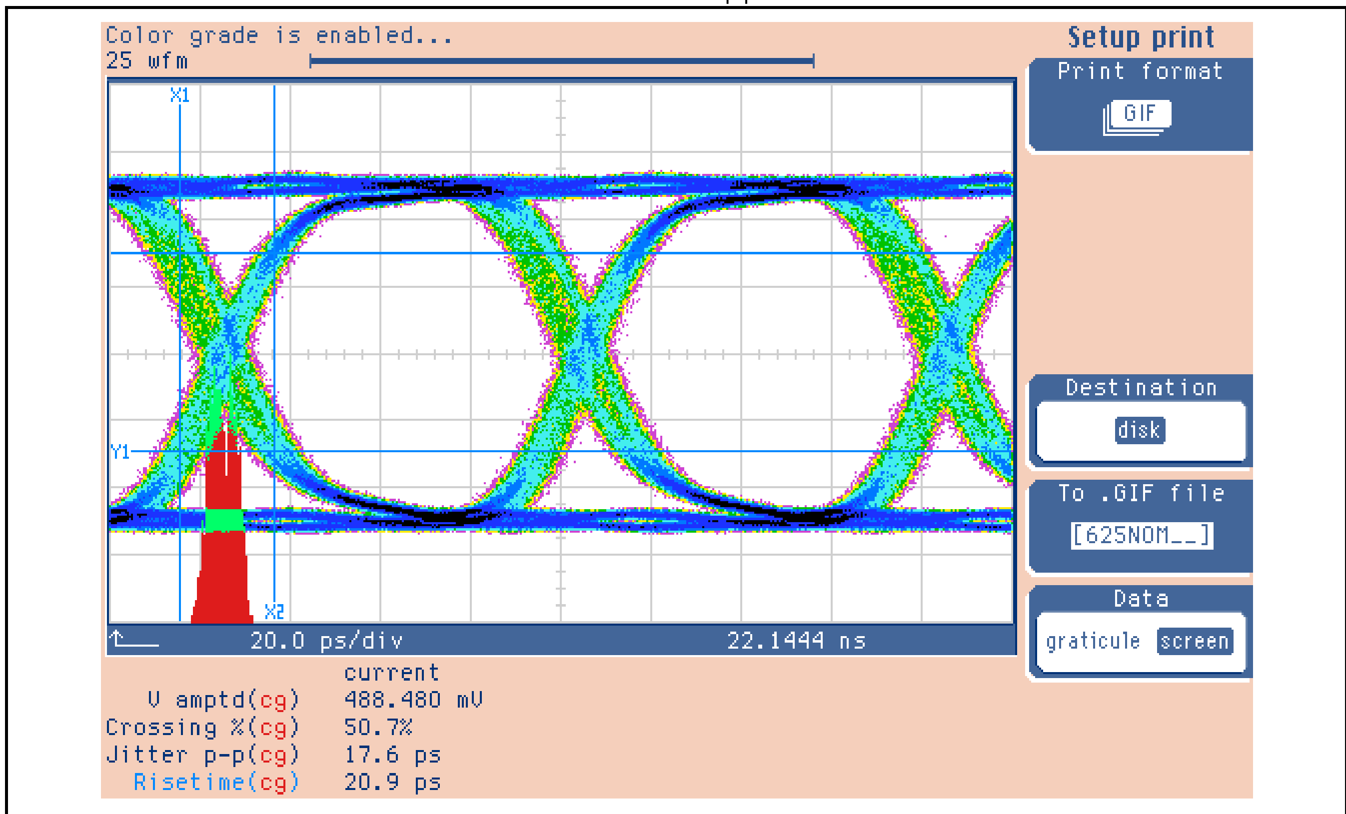


Figure 9. Eye Diagram (10.7 Gbps, PRBS 2^{23}-1, I_{IN} = 20 µA_{p-p}, 25°C, 3.3 V)

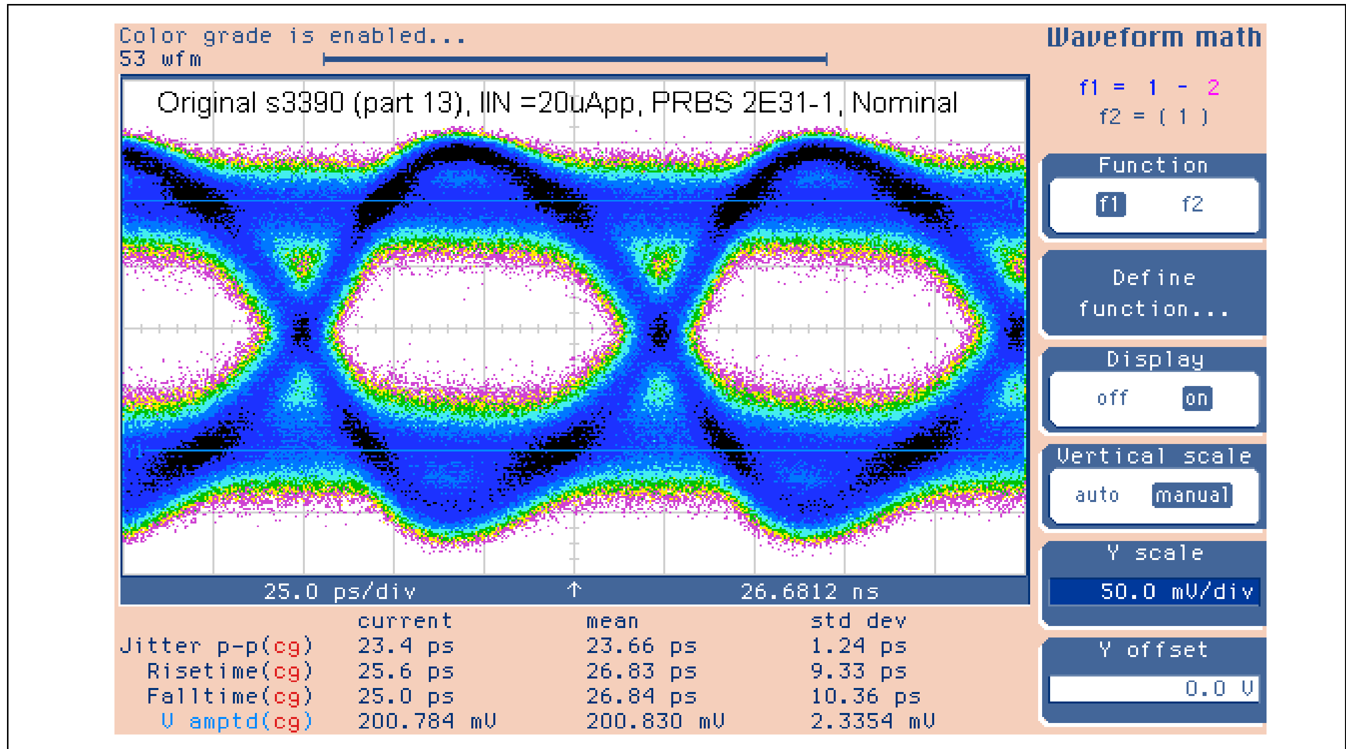


Figure 10. Measured S_{21} (25°C, 3.3 V, 8 samples)

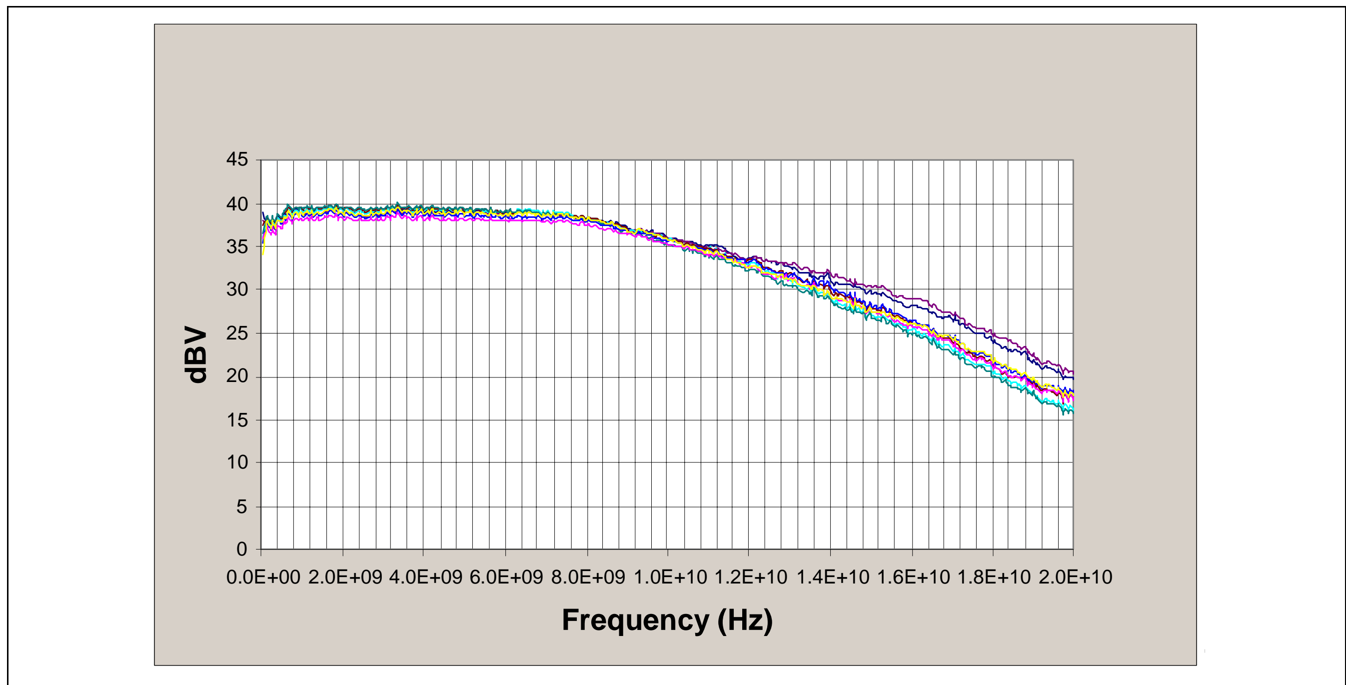
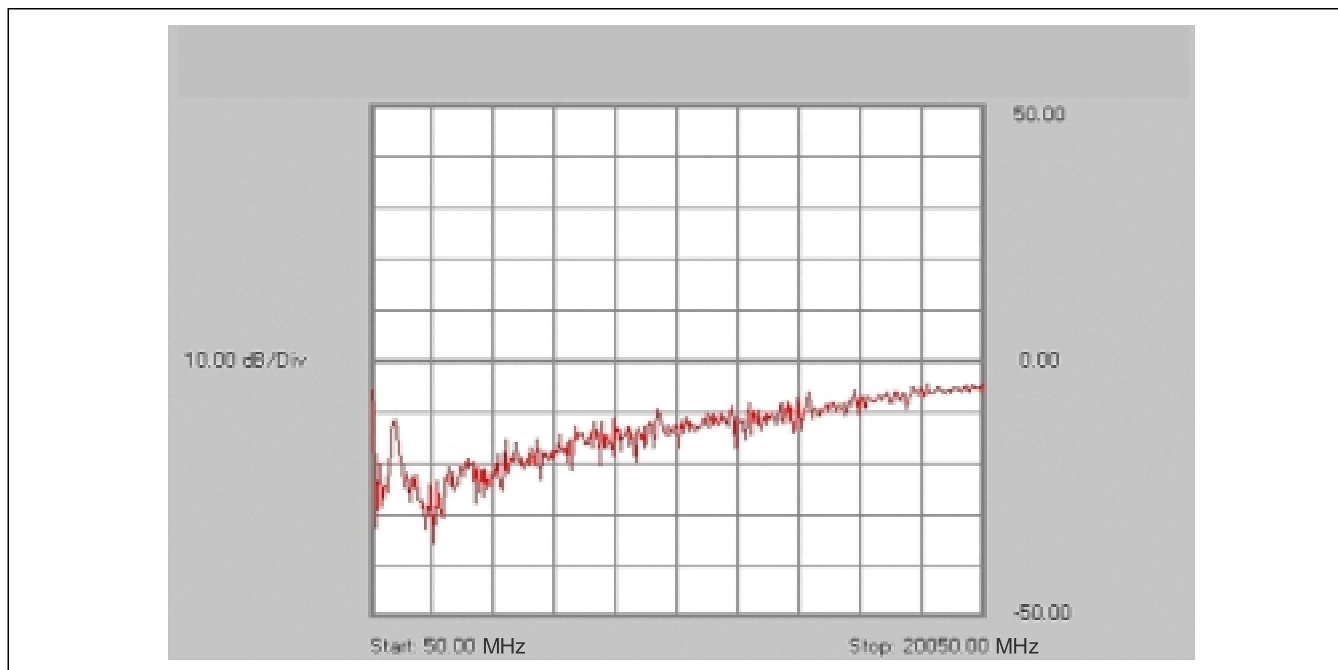


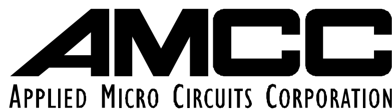
Figure 11. Measured Differential S_{22} (25°C, 3.3 V)



Ordering Information

Prefix	Device	Package
S – Integrated Circuit	3390	DI – Die

X Prefix **XXXX** Device **XX** Package



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