LM363

LM363 Precision Instrumentation Amplifier

Literature Number: SNOSBG8A

National Semiconductor

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LM363 Precision Instrumentation Amplifier

General Description

The LM363 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1000. High precision is attained by on-chip trimming of offset voltage and gain. A super-beta bipolar input stage gives very low input bias current and voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains. The LM363 operates with supply voltages from ±5V to ±18V with only 1.5 mA current drain.

The LM363's low voltage noise, low offset voltage and offset voltage drift make it ideal for amplifying low-level, low-impedance transducers. At the same time, its low bias current and high input impedance (both common-mode and differential) provide excellent performance at high impedance levels. These features, along with its ultra-high common-mode rejection, allow the LM363 to be used in the most demanding instrumentation amplifier applications, replacing expensive hybrid, module or multi-chip designs. Because the LM363 is internally trimmed, precision external resistors and their associated errors are eliminated.

The 16-pin dual-in-line package provides pin-strappable gains of 10, 100 or 1000. Its twin differential shield drivers eliminate bandwidth loss due to cable capacitance. Compensation pins allow overcompensation to reduce bandwidth and output noise, or to provide greater stability with capacitive loads. Separate output force, sense and reference pins permit gains between 10 and 10,000 to be programmed using external resistors.

On the 8-pin metal can package, gain is internally set at 10, 100 or 500 but may be increased with external resistors. The shield driver and offset adjust pins are omitted on the 8-pin versions.

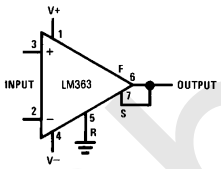
The LM363 is rated for 0°C to 70°C.

Features

- Offset and gain pretrimmed
- 12 nV/√Hz input noise (G = 500/1000)
- 130 dB CMRR typical (G = 500/1000)
- 2 nA bias current typical
- No external parts required
- Dual shield drivers
- Can be used as a high performance op amp
- Low supply current (1.5 mA typ)

Typical Connections

8-Pin Package



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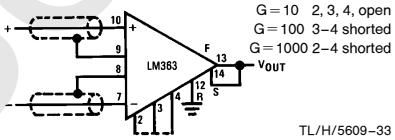
16-Pin Package



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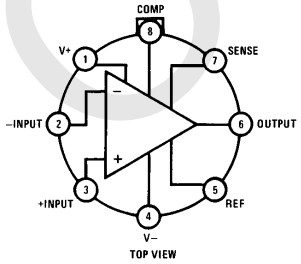
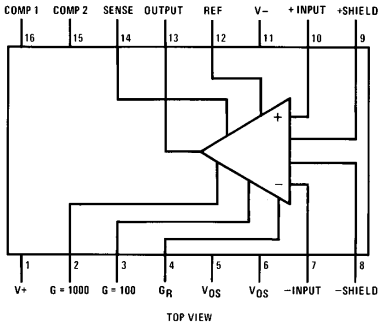
Connection Diagrams

Metal Can Package



Order Number LM363H-10, LM363H-100 or LM363H-500
See NS Package Number H08C

16-Pin Dual-In-Line Package



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Order Number 363D
See NS Package Number D16C

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±10V
Input Current	±20 mA
Input Voltage	Equal to Supply Voltage
Reference and Sense Voltage	±25V
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

LM363 Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	LM363			Units
		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
FIXED GAIN (8-PIN)					
Input Offset Voltage	G = 500	30	150	**400**	µV
	G = 100	50	250	**700**	µV
	G = 10	0.5	2.5	**6**	mV
Input Offset Voltage Drift	G = 500	1		**4**	µV/°C
	G = 100	2		**8**	µV/°C
	G = 10	20		**75**	µV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G = 500	0.1	0.8	**0.9**	%
	G = 100	0.07	0.7	**0.8**	%
	G = 10	0.05	0.6	**0.7**	%
PROGRAMMABLE GAIN (16-PIN)					
Input Offset Voltage	G = 1000	50	250	**500**	µV
	G = 100	100	450	**900**	µV
	G = 10	1	3.5	**8**	mV
Input Offset Voltage Drift	G = 1000	1		**5**	µV/°C
	G = 100	2		**10**	µV/°C
	G = 10	10		**100**	µV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G = 1000	2.0	3.0	**3.5**	%
	G = 100	0.1	0.7	**0.8**	%
	G = 10	0.6	2.0	**2.3**	%
FIXED GAIN AND PROGRAMMABLE					
Gain Temperature Coefficient	G = 1000	40			ppm/°C
	G = 500	20			ppm/°C
	G = 100, 10	10			ppm/°C
Gain Non-Linearity (±10V Swing, 2 kΩ Load)	G = 10, 100	0.01	0.03	**0.04**	%
	G = 500, 1000	0.01	0.05	**0.06**	%

LM363 Electrical Characteristics (Continued) (Notes 1 and 2)

Parameter	Conditions	LM363			Units
		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Common-Mode Rejection Ratio ($-10V \le V_{CM} \le 10V$)	G = 1000, 500	130	114	**104**	dB
	G = 100	120	94	**84**	dB
	G = 10	105	90	**80**	dB
Positive Supply Rejection Ratio (5V to 15V)	G = 1000, 500	130	110	**100**	dB
	G = 100	120	100	**95**	dB
	G = 10	100	85	**78**	dB
Negative Supply Rejection Ratio (−5V to −15V)	G = 1000, 500	120	100	**90**	dB
	G = 100	106	85	**75**	dB
	G = 10	86	70	**60**	dB
Input Bias Current		2	10	**20**	nA
Input Offset Current		1	3	**5**	nA
Common-Mode Input Resistance		100	8		GΩ
Differential Mode Input Resistance	G = 1000, 500	0.2			GΩ
	G = 100	2			GΩ
	G = 10	20			GΩ
Input Offset Current Change	$-11V \le V_{CM} \le 13V$	20	100	**300**	pa/V
Reference and Sense Resistance		50			kΩ
	Min		30	**27**	kΩ
	Max		80	**83**	kΩ
Open Loop Gain	G_{CL} = 1000, 500	10	1		V/μV
Supply Current	Positive	1.2	2.4	**3.0**	mA
	Negative	1.6	2.8	**3.4**	mA

Note 1: These conditions apply unless otherwise noted; $V^+ = 15V$, $V^- = -15V$, $V_{CM} = 0V$, $R_L = 2\ k\Omega$, reference pin grounded, sense pin connected to output and $T_j = 25°C$.

Note 2: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range is 0°C to 70°C for the LM363.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% tested. These limits are not used in determining outgoing quality levels.

Note 5: Maximum rated junction temperature is 100°C for the LM363. Thermal resistance, junction to ambient, is 150°C/W for the TO-99(H) package and 100°C/W for the ceramic DIP (D).

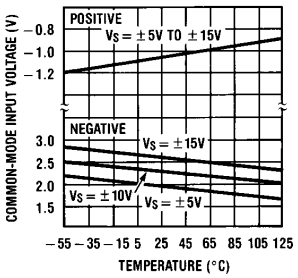
Typical Performance Characteristics $T_A = 25°C$

Parameter	Fixed Gain and Programmable			Units
	1000/500	100	10	
Input Voltage Noise, rms, 1 kHz	12	18	90	nV/√ Hz
Input Voltage Noise (Note 6)	0.4	1.5	10	μVp-p
Input Current Noise, rms, 1 kHz	0.2	0.2	0.2	pA/√ Hz
Input Current Noise (Note 6)	40	40	40	pAp-p
Bandwidth	30	100	200	kHz
Slew Rate	1	0.36	0.24	V/μs
Settling Time, 0.1% of 10V	70	25	20	μs
Offset Voltage Warm-Up Drift (Note 7)	5	15	50	μV
Offset Voltage Stability (Note 8)	5	10	100	μV
Gain Stability (Note 8)	0.01	0.005	0.05	%

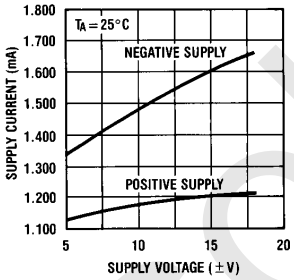
Note 6: Measured for 100 seconds in a 0.01 Hz to 10 Hz bandwidth.

Note 7: Measured for 5 minutes in still air, $V^+ = 15V$, $V^- = -15V$. Warm-up drift is proportionally reduced at lower supply voltages.

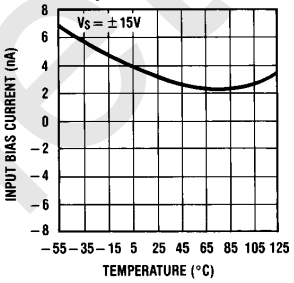
Common-Mode Input Voltage Limit



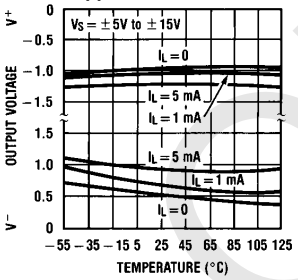
Supply Current vs Supply Voltage



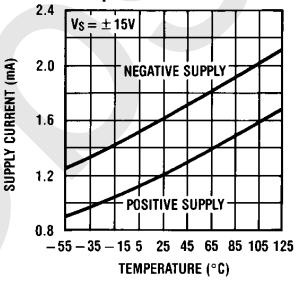
Input Bias Current vs Temperature



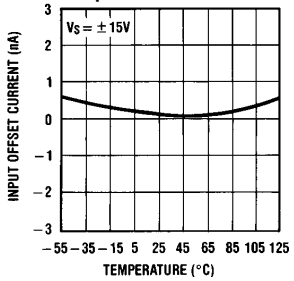
Output Swing Referred to Supplies



Supply Current vs Temperature



Input Offset Current vs Temperature



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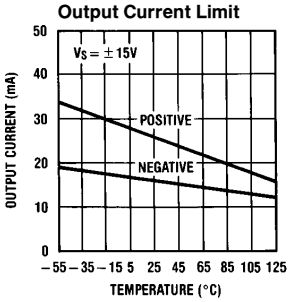
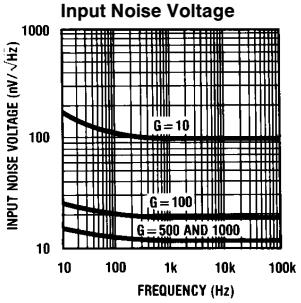
Typical Performance Characteristics (Continued)

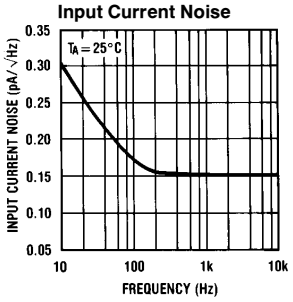
Output Current Limit



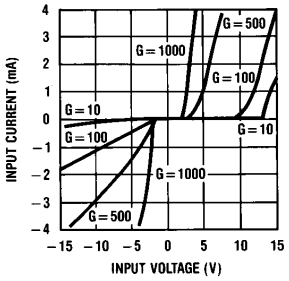
Input Noise Voltage



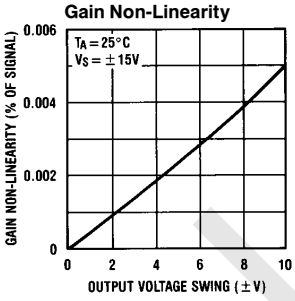
Input Current Noise



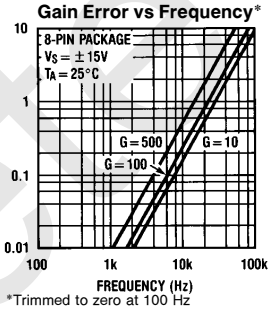
Input Current vs Voltage Overdrive



Gain Non-Linearity

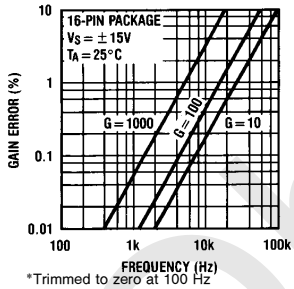


Gain Error vs Frequency*



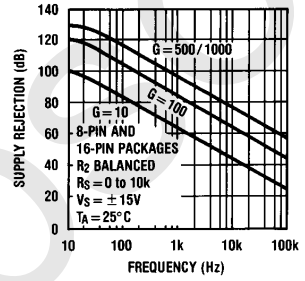
*Trimmed to zero at 100 Hz

Gain Error vs Frequency*

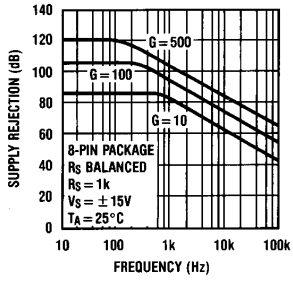


*Trimmed to zero at 100 Hz

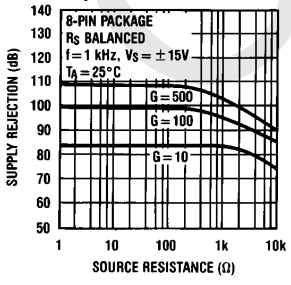
Positive Power Supply Rejection



Negative Power Supply Rejection



Negative Power Supply Rejection



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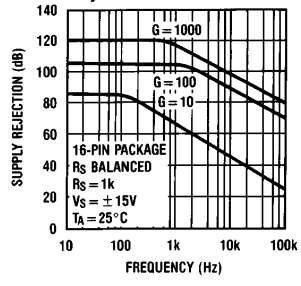
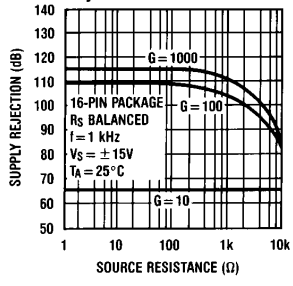


Negative Power Supply Rejection



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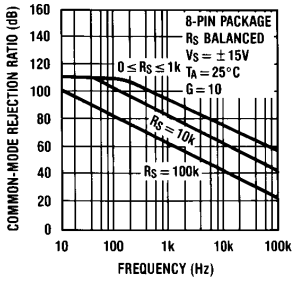
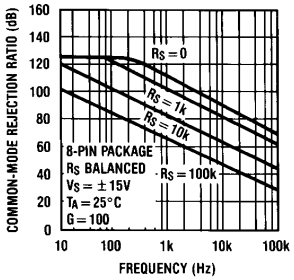
Typical Performance Characteristics (Continued)

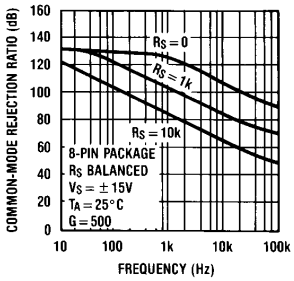
CMRR with Balanced Source Resistance



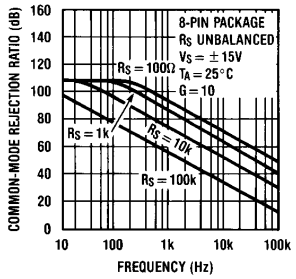
CMRR with Balanced Source Resistance



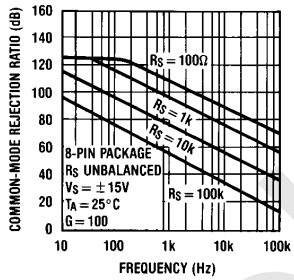
CMRR with Balanced Source Resistance



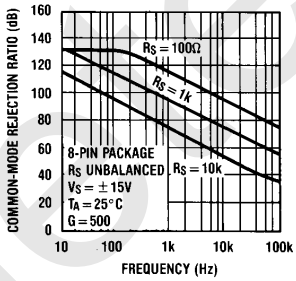
CMRR with Unbalanced Source Resistance



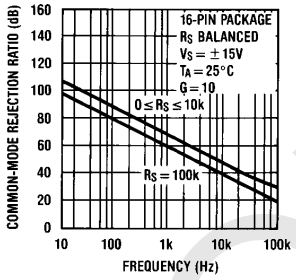
CMRR with Unbalanced Source Resistance



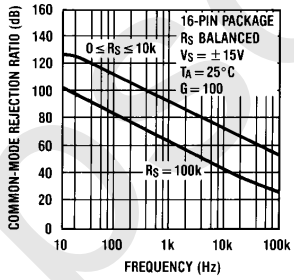
CMRR with Unbalanced Source Resistance



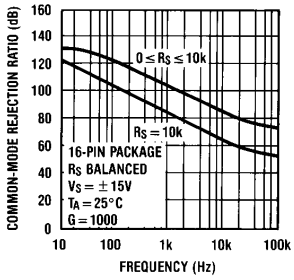
CMRR with Balanced Source Resistance



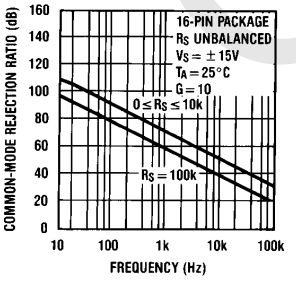
CMRR with Balanced Source Resistance



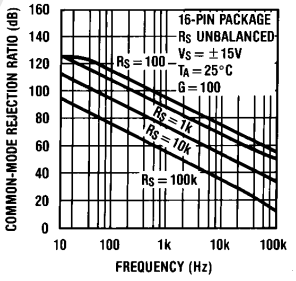
CMRR with Balanced Source Resistance



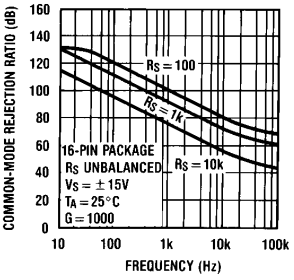
CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



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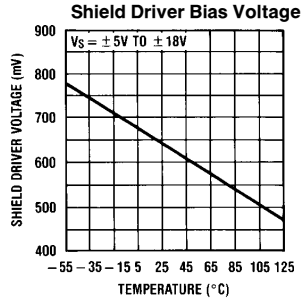
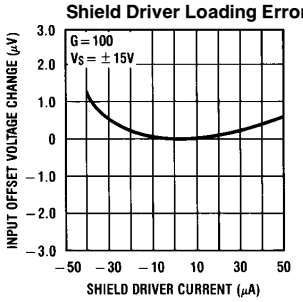
Typical Performance Characteristics (Continued)

Shield Driver Bias Voltage



Shield Driver Loading Error



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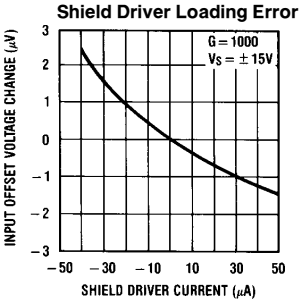
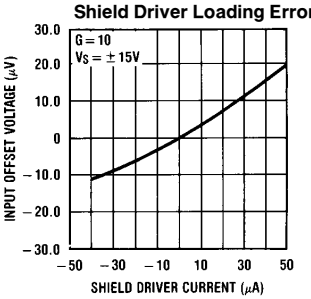
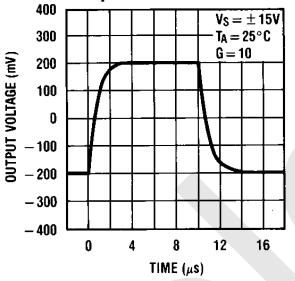


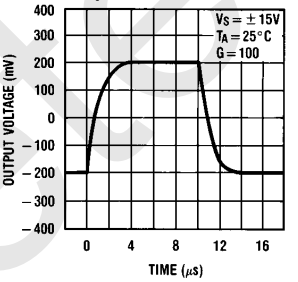
Shield Driver Loading Error



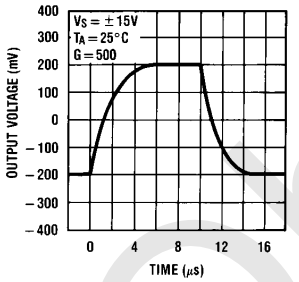
Small Signal Transient Response



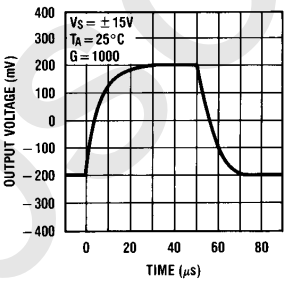
Small Signal Transient Response



Small Signal Transient Response



Small Signal Transient Response



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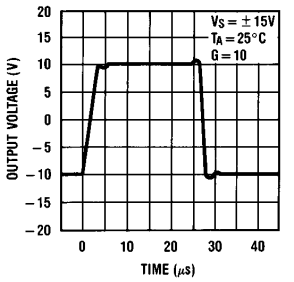
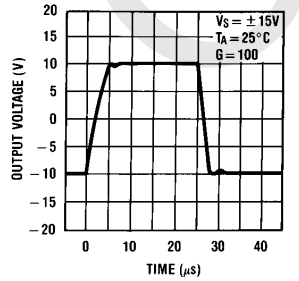
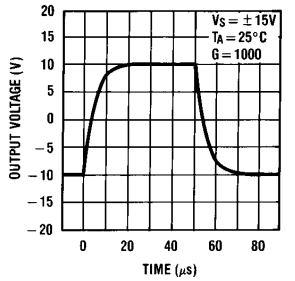


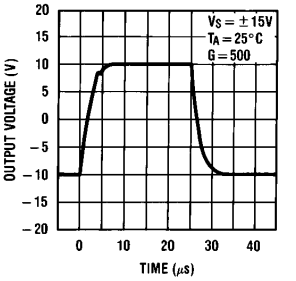
Large Signal Transient Response



Large Signal Transient Response



Large Signal Transient Response



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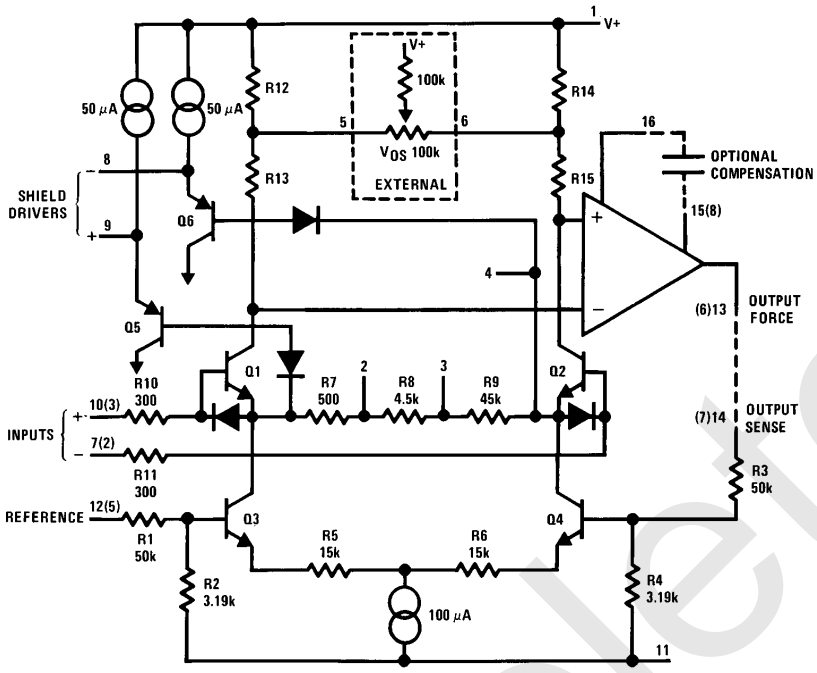
Simplified Schematic (pin numbers in parentheses are for 8-pin package)



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Theory of Operation

Referring to the Simplified Schematic, it can be seen that the input voltage is applied across the bases of Q1 and Q2 and appears between their emitters. If R_{E1-2} is the resistance across these emitters, a differential current equal to V_{IN}/R_{E1-2} flows from Q1's emitter to Q2's. The second stage amplifier shown maintains Q1 and Q2 at equal collector currents by negative feedback to Q4. The emitter currents of Q3 and Q4 must therefore be unbalanced by an amount equal to the current flow across R_{E1-2}. Defining $R_{E3-4} = R5 + R6$, the differential voltage across the emitters of Q4 to Q3 is equal to

$$\frac{V_{IN}}{R_{E\,1-2}} \times R_{E3-4}.$$

This voltage divided by the attenuation factor

$$\frac{R4}{R3+R4} = \frac{R2}{R1+R2}$$

is equal to the output-to-reference voltage. Hence, the overall gain is given by

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{R3+R4}{R4} \times \frac{R_{E3-4}}{R_{E1-2}}.$$

Application Hints

The LM363 was designed to be as simple to use as possible, but several general precautions must be taken. The differential inputs are directly coupled and need a return path to power supply common. Worst-case bias currents are only 10 nA for the LM363, so the return impedance can be as high as 100 MΩ. Ground drops between signal return and IC supply common should not be ignored. While the LM363 has excellent common-mode rejection, signals must remain within the proper common-mode range for this specification to apply. Operating common-mode range is guaranteed from −10V to +10V with ±15V supplies.

The high-gain (500 or 1000) versions have large gain-bandwidth products (15 MHz or 30 MHz) so board layout is fairly critical. The differential input leads should be kept away from output force and sense leads, especially at high impedances. Only 1 pF from output to positive input at 100 kΩ source impedance can cause oscillations. The gain adjust leads on the 16-pin package should be treated as inputs and kept away from the output wiring.

POWER SUPPLY

The LM363 may be powered from split supplies from ±5V to ±18V (or single-ended supplies from 10V to 36V). Positive supply current is typically 1.2 mA independent of supply voltage. The negative supply current is higher than the positive by the current drawn through the voltage dividers for the reference and sense inputs (typ 600 μA total). The LM363's excellent PSRR often makes regulated supplies unnecessary. Actually, supply voltage can be as low as 7V total but PSRR is severely degraded, so that well-regulated supplies are recommended below 10V total. Split supplies need not be balanced; output swing and input common-mode range will simply not be symmetrical with unbalanced supplies. For example, at +12V and −5V supplies, input common-mode range is typically +10.5V to −2V and output swing is +11V to −4V.

When using ultra-low offset versions, best results are obtained at ±15V supplies. For example, the LM363-500's offset voltage is guaranteed within 150 μV at ±15V at 25°C. Running at ±5V results in a worst-case negative PSRR error of 10V (−15V to −5V) multiplied by 3.2×10^{-6} (110 dB) or 32 μV, increasing the worst-case offset. Positive PSRR results in another 10 μV worst-case change.

INPUTS

The LM363 input circuitry is depicted in the Simplified Schematic. The input stage is run relatively rich (50 μA) for low voltage noise and wide bandwidth; super-beta transistors and bias-current cancellation (not shown) keep bias currents low. Due to the bias-current cancellation circuitry, bias current may be either polarity at either input. While input current noise is high relative to bias current, it is not significant until source resistance approaches 100 kΩ.

Input common-mode range is typically from 3V above V^- to 1.5V below V^+, so that a large potential drop between the input signal and output reference can be accommodated. However, a return path for the input bias current must be provided; the differential input stage is not isolated from the supplies. Differential input swing in the linear region is equal to output swing divided by gain, and typically ranges from 1.3V at G = 10 to 13 mV at G = 1000.

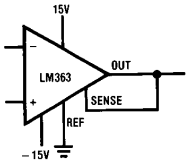
Clamp diodes are provided to prevent zener breakdown and resulting degradation of the input transistors. At large input overdrives these diodes conduct, greatly increasing input currents. This behavior is illustrated in the I_{IN} vs V_{IN} plot in the Typical Performance Characteristics. (The graph is not symmetrical because at large input currents a portion of the current into the device flows out the V^- terminal.)

The input protection resistors allow a full 10V differential input voltage without degradation even at G = 1000. At input voltages more than one diode drop below V^- or two diode drops above V^+ input, current increases rapidly. Diode clamps to the supplies, or external resistors to limit current to 20 mA, will prevent damage to the device.

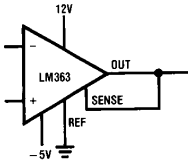
REFERENCE AND SENSE INPUTS

The equivalent circuit is shown in the schematic diagram. Limitations for correct operation are as follows. Maximum *differential* swing between reference and sense pins is typically ±15V (±10V guaranteed). If this limit is exceeded, the sense pin no longer controls the output, which then pegs high or low. The *negative* common-mode limit is 1.5V below V^-. (This is permissible because R2 and R4 are returned to a node biased higher than V^-.) If large *positive* voltages are applied to the reference and sense pins, the common-mode range of the signal inputs begins to suffer as the drop across R13 and R16 increases. For example, at ±15V supplies, $V_{REF} = V_{SENSE} = 0V$, signal input range is typically −12V to + 13.5V. At $V_{REF} = V_{SENSE} = 15V$, signal input range drops to −11V to +13.5V. The reference and sense pins can be as much as 10V above V^+ as long as a restricted signal common-mode range (−10V min) can be tolerated.

For maximum bipolar output swing at ±15V supplies, the reference pin should be returned to a voltage close to ground. At lower supply voltages, the reference pin need not be halfway between the supplies for maximum output swing. For example, at $V^+ = +12V$ and $V^- = -5V$, grounding the reference pin still allows a +11V to −4V swing. For single-supply systems, the reference pin can be tied to either supply if a single output polarity is all that is required. For a bipolar input and output, create a low impedance reference with an op amp and voltage divider or a regulator (e.g., LM336, LM385, LM317L). This forms the reference for all succeeding signal-processing stages. (Don't connect the reference terminal directly to a voltage divider; this degrades gain error.) See *Figure 1*.



a. Usual configuration maximizes bipolar output swing.



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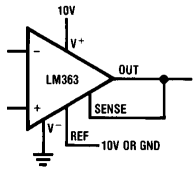
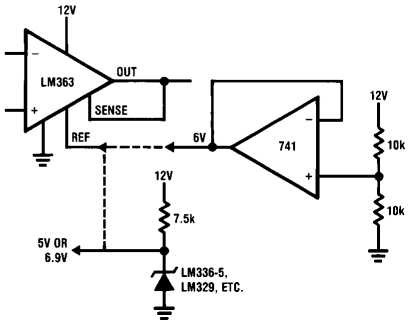
b. Unequal supplies, output ground referred. Full output swing preserved referred to supplies.

FIGURE 1. Reference Connections

Application Hints (Continued)



c. Single Supply, Unipolar Output



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d. Single Supply, Bipolar Output

FIGURE 1. Reference Connections (Continued)

OUTPUTS

The LM363's output can typically swing within 1V of the supplies at light loads. While specified to drive a 2 kΩ load to ±10V, current limit is typically 15 mA at room temperature. The output can stably drive capacitive loads up to 400 pF. For higher load capacitance, the amplifier may be overcompensated (see COMPENSATION section, following). The output may be continuously shorted to ground without damaging the device.

OFFSET VOLTAGE

The LM363's offset voltage is internally trimmed to a very low value. Note that data sheet values are given at $T_j = 25°C$, $V_{CM} = 0V$ and $V^+ = V^- = 15V$. For other conditions, warm-up drift, temperature drift, common-mode rejection and power supply rejection must be taken into account. Warm-up drift, due to chip and package thermal gradients, is an effect separate from temperature drift. Typical warm-up drift is tabulated in the Electrical Characteristics; settling time is approximately 5 minutes in still air. At load currents up to 5 mA, thermal feedback effects are negligible ($\Delta V_{OS} \leq 2\mu V$ at G = 1000).

Care must be taken in measuring the extremely low offset voltages of the high gain amplifiers. Input leads must be held isothermal to eliminate thermocouple effects. Oscillations, due to either heavy capacitive loading or stray capacitance from input to output, can cause erroneous readings. In either case, overcompensation will help. High frequency noise fed into the inputs may be rectified internally, and produce an offset shift. A simple low-pass RC filter will usually cure this problem (*Figure 2*). Use film type resistors for their low thermal EMF. In highly noisy environments, LC filters can be substituted for increased RF attenuation.

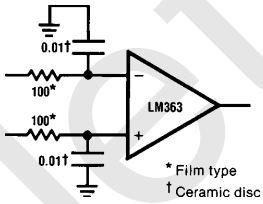

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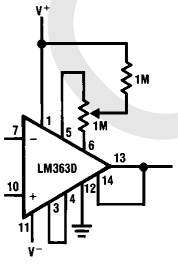
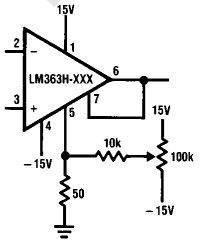
FIGURE 2. Low Pass Filter Prevents RF Rectification

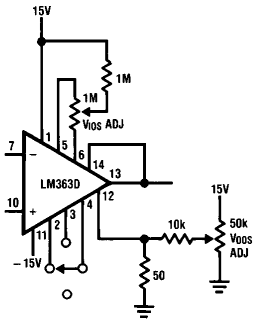
Instrumentation amplifiers have both an input offset voltage (V_{IOS}) and an output offset voltage (V_{OOS}). The total input-referred offset voltage (V_{OSRTI}) is related to the instrumentation amplifier gain (G) as follows: $V_{OSRTI} = V_{IOS} + V_{OOS}/G$. The offset voltage given in the LM363 specifications is the total input-referred offset. As long as only one gain is used, offset voltage can be nulled at either input or output as shown in *Figures 3a* and *3b*. When the 16-pin device is used at multiple gain settings, both V_{IOS} and V_{OOS} should be nulled to get minimum offset at all gains, as shown in *Figure 3c*. The correct procedure is to trim V_{OOS} for zero output at G = 10, then trim V_{IOS} at G = 1000.



a. Input Offset Adj. for 16-Pin Package



b. Output Offset Adj. for 8-Pin Package



c. Input and Output Offset Adjustment for 16-Pin Package

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FIGURE 3. Offset Voltage Trimming

Application Hints (Continued)

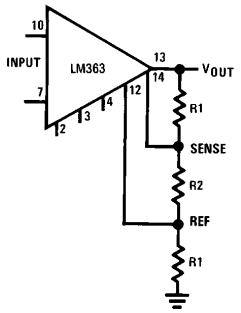
Because the LM363's offset voltage is so low to begin with, offset nulling has a negligible effect on offset temperature drift. For example, zeroing a 100 μV offset, assuming external resistor TC of 200 ppm/°C and worst-case internal resistor TC, results in an additional drift component of 0.08 μV/°C. For this reason, drift specifications are guaranteed, with or without external offset nulling.

GAIN ADJUSTMENT

Gain may be increased by adding an external voltage divider between output force and sense and reference; the preferred connection is shown in *Figure 4*. Since both the sense and reference pins look like 50 kΩ ($\pm$20 kΩ) to V$^-$, impedances presented to both pins must be equal to avoid offset error. For example, a 100Ω imbalance can create a worst-case output offset of 50 mV, creating an input-referred error of 5 mV at G = 10 or 50 μV at G = 1000.

Increasing gain this way increases output offset error. An LM363H-100 may have an output offset of 5 mV, resulting in input referred offset component of 50 μV. Raising the gain to 200 yields a 10 mV error at the output and changes input referred error by an additional 50 μV.

External resistors connected to the reference and sense pins can only *increase* the gain. If ultra-low output impedance is not critical, the technique in *Figure 5* can be used to trim the gain to nominal value. Alternatively, the V_{OS} adjustment terminals on the 16-pin package may be used to trim the gain (*Figure 10b*).



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R1 and R2 should be as low as possible to avoid errors due to 50 kΩ input impedance of reference and sense pins. Total resistance (R2 + 2R1) should be above 4 kΩ, however, to prevent excessive load on the LM363 output. The exact formula for calculating gain (G) is:

$$G = G_O\left(1 + \frac{2R1}{R2} + \frac{R1}{50k}\right)$$

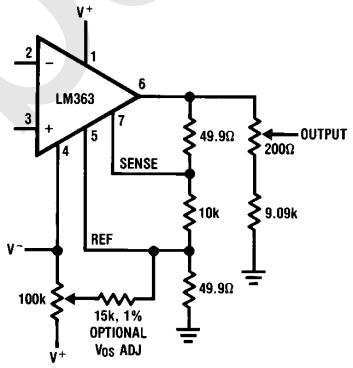
G_O = preset gain

The last term may be ignored in applications where gain accuracy is not critical. The table below gives suggested values for R1 and R2 along with the calculated error due to "closest value" standard 1% resistors. Total gain error tolerance includes contributions from LM363 G_O error and resistor tolerance ($\pm$1%) and works out to approximately 2.5% in every case.

Pinout shown is for 16-pin package. This same technique can also be used with 8-pin versions.

Gain Increase	1.5	2	2.5	3	4	5	6	7	8	9	10
R1	1.21k	1.21k	2k	2k	1.78k	2k	2.49k	2.94k	3.48k	3.92k	4.42k
R2	5k	2.49k	2.74k	2.05k	1.21k	1k	1k	1k	1k	1k	1k
Error (typ)	+0.6%	−0.2%	0	−0.3%	−0.6%	+0.8%	+0.5%	−0.9%	+0.4%	−0.9%	−0.7%

FIGURE 4. Increasing Gain



Pinout shown is for 8-pin versions. This same technique can also be used with 16-pin version.

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FIGURE 5. Adjusting Gain, Alternate Technique

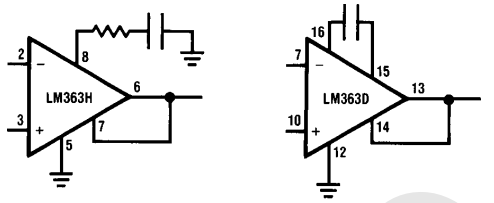
Application Hints (Continued)

COMPENSATION AND OUTPUT CLAMPING

The LM363 is internally compensated for unity feedback from output to sense. Increasing gain with external dividers will decrease the bandwidth and increase stability margin. Without external compensation, the amplifier can stably drive capacitive loads up to 400 pF. When used as an op amp (sense and reference pins grounded, feedback to inverting input), the LM363 is stable for gains of 100 or more. For greater stability, the device may be over-compensated as in *Figure 6*. Tables I and II depict suggested compensation components along with the resulting changes in large and small signal bandwidth for the 8-pin and 16-pin packages, respectively.

Note that the RC network from pin 8 of the 8-pin device to ground has a large effect on power bandwidth, especially at low gains. The Miller capacitance utilized for overcompensating the 16-pin device permits higher slew rate and larger load capacitance for the same bandwidth, and is preferred when bandwidth must be greatly reduced (e.g., to reduce output noise).

Heavy Miller overcompensation on the 16-pin package can degrade AC PSRR. A large capacitor between pins 15 and 16 couples transients on the positive supply to the output buffer. Since the amplifier bandwidth is severely rolled off it cannot keep the output at the correct state at moderate frequencies. Hence, for good PSRR, either keep the Miller capacitance under 1000 pF or use the pin 15-to-ground compensation shown in Table I.



a. 8-Pin Package b. 16-Pin Package

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FIGURE 6. Overcompensation

TABLE I. Overcompensation on 8-Pin Package

Gain	Compensation Network (Pin 8 to Ground)†	Small Signal 3 dB Bandwidth (kHz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
500	—	125	100k	400
	100 pF, 15k	95	15k	600
	1000 pF, 5k	45	1.8k	800
	0.01 μF,500Ω	10	200	1000*
	0.1 μF	1	20	1000*
100	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	80	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*
10	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	90	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*

*Also stable for $C_L \geq 0.05\ \mu F$
†Pin 15 to ground on 16-pin package

TABLE II. Overcompensation on 16-Pin Package

Gain	Compensation Capacitor (Pin 15 to 16)	Small Signal 3 dB Bandwidth (Hz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
1000	—	45k	45k	1000*
	10 pF	16k	16k	2000*
	100 pF	2.5k	2.5k	2500*
	1000 pF	250	250	3000*
	0.01 μF	25	25	3000*
100	—	140k	100k	900
	10 pF	50k	50k	1600
	100 pF	7.5k	7.5k	2000*
	1000 pF	750	750	2000*
	0.01 μF	75	75	2000*
10	—	180k	90k	600
	10 pF	60k	50k	1100
	100 pF	9k	9k	1600
	1000 pF	900	900	2000*
	0.01 μF	90	90	2000*

*Also stable for $C_L \geq 0.05\ \mu F$

Application Hints (Continued)

Because the LM363's output voltage is approximately one diode drop below the voltage at pin 15 (pin 8 for the 8-pin device), this point may be used to limit output swing as seen in *Figure 7a*. Current available from this pin is only 50 μA, so that zeners must have a sharp breakdown to clamp accurately. Alternatively, a diode tied to a voltage source could be used as in *Figure 7b*.

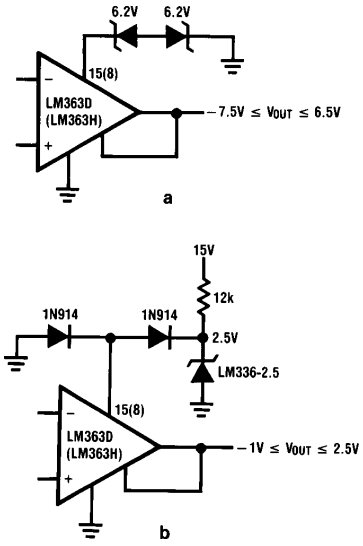

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FIGURE 7. Output Clamp

SHIELD DRIVERS

When differential signals are sent through long cables, three problems occur. First, noise, both common-mode and differential, is picked up. Second, signal bandwidth is reduced by the RC low-pass filter formed by the source impedance and the cable capacitance. Finally, when these RC time constants are not identical (unbalanced source impedance and/or unbalanced capacitance), AC common-mode rejection is degraded, amplifying both induced noise and ''ground'' noise. Either filtering at the amplifier inputs or slowing down the amplifier by overcompensating will indeed reduce the noise, but the price is slower response. The LM363D's dual shield drivers can actually increase bandwidth while reducing noise.

The way this is done is by bootstrapping out shield capacitance. The shield drivers follow the input signal. Since both sides of the shield capacitance swing the same amount, it is effectively out of the circuit at frequencies of interest. Hence, the input signal is not rolled off and AC CMRR is not degraded (*Figure 8*). The LM363D's shield drivers can handle capacitances (shield to center conductor) as high as 1000 pF with source resistances up to 100 kΩ.

For best results, identical shielded cables should be used for both signal inputs, although small mismatches in shield driver to ground capacitance ($\leq$500 pF) do not cause problems. At certain low values of cable capacitance (50 pF–200 pF), high frequency oscillations can occur at high source resistance ($\geq$ 10 kΩ). This is alleviated by adding 50 pF to ground at both shield driver outputs. Do not use only one shield driver for a single-ended signal as oscillations can result; shield driver to input capacitance must be roughly balanced ($\pm$30%). To further reduce noise pickup, the shielded signal lines may be enclosed together in a grounded shield. If a large amount of RF noise is the problem, the only sure cure is a filter capacitor at both inputs; otherwise the RFI may be internally rectified, producing an offset.

DC loading on the shield drivers should be minimized. The drivers can only source approximately 40 μA; above this value the input stage bias voltages change, degrading V_{OS} and CMRR. While the shield drivers can sink several mA, V_{OS} may degrade severely at loads above 100 μA (see Shield Driver Loading Error curve in Typical Performance Characteristics). Because the shield drivers are one diode drop above the input levels, unbalanced leakage paths from shield to input can produce an input offset at high source impedances. Buffering with emitter-followers (*Figure 8b*) reduces this leakage current by reducing the voltage differential and eliminates any loading on the amplifier.

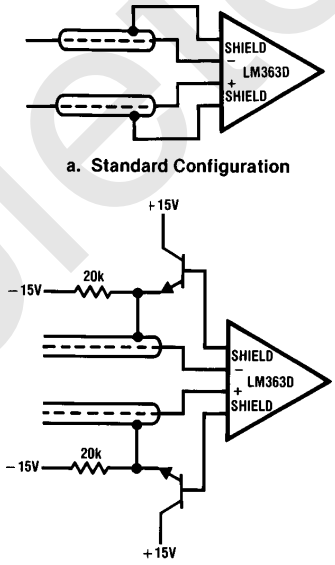

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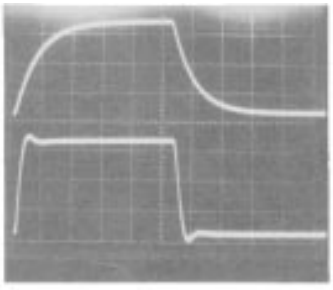
FIGURE 8. Driving Shielded Cables

MISCELLANEOUS TRIMMING

The V_{OS} adjust and shield driver pins available on the 16-pin package may be used to trim the other parameters besides offset voltage, as illustrated in *Figure 10*. The bias-current trim relies on the fact that the voltage on the shield driver and gain setting pins is one diode drop respectively above and below the input voltage. Input bias current can be held to within 100 pA over the entire common-mode range, and input offset current always stays under 30 pA. The CMRR trims use the shield driver pins to drive the V_{OS} adjust pins, thus maintaining the LM363's ultra-high input impedance.

Application Hints (Continued)

If power supply rejection is critical, frequently only the negative PSRR need be adjusted, since the positive PSRR is more tightly specified. Any or all of the trim schemes of *Figure 10* can be combined as desired. As long as the center tap of the 100k trimpot is returned to a voltage 200 mV below V^+, the trim schemes shown will not greatly affect V_{OS}. Both the gain and DC CMRR trims can degrade positive PSRR; the positive PSRR can then be nulled out if desired. The correct order of trimming from first to last is bias current, gain, CMRR, negative PSRR, positive PSRR and V_{OS}.



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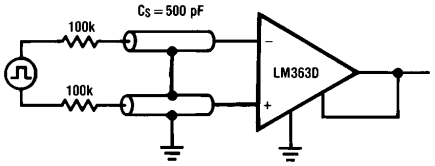
Top Trace: Cable Shield Grounded



Bottom Trace: Cable Shield Bootstrapped

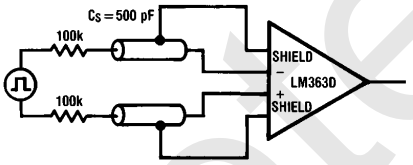


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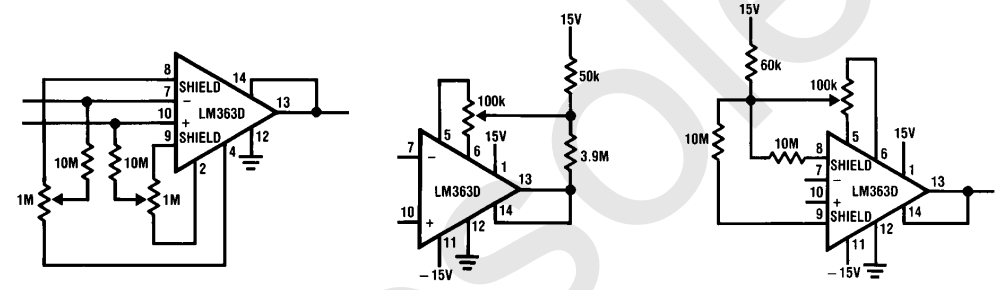
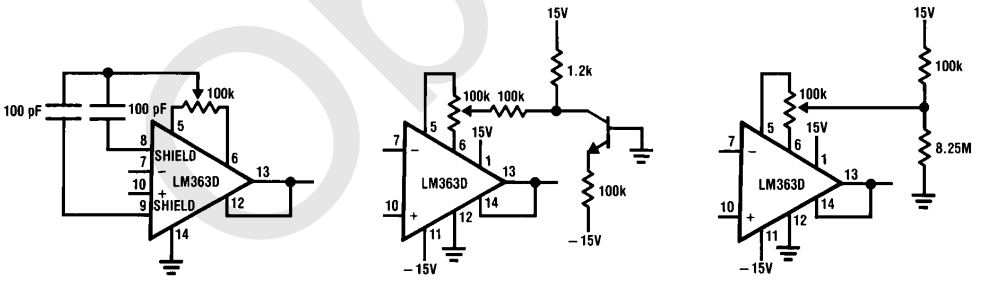
FIGURE 9. Improved Response using Shield Drivers



a. Bias Current b. Gain c. DC CMRR



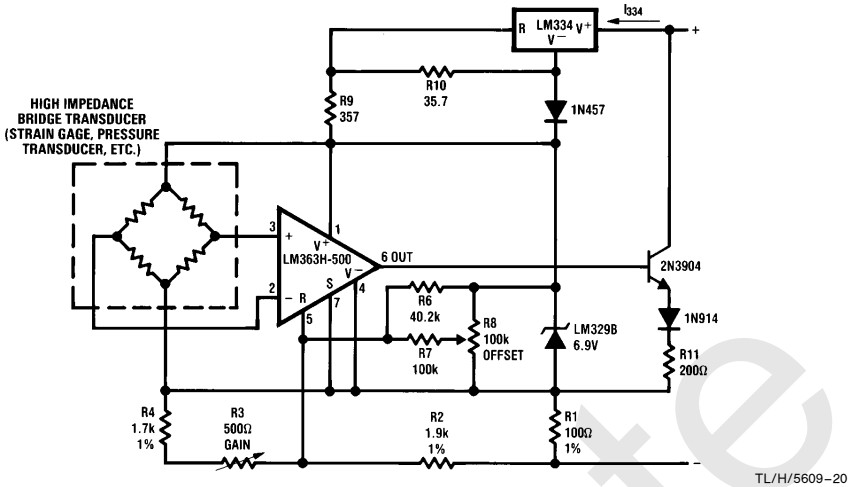
d. AC CMRR e. Negative PSRR f. Positive PSRR

TL/H/5609–19

FIGURE 10. Other Trims for 16-Pin Package

Typical Applications

4 mA-20 mA Two Wire Current Transmitter



TL/H/5609–20

The LM329 reference provides excellent line regulation and gain stability. When bridge is balanced ($I_{OUT} = 4$ mA), there's no drop across R3 and R4, so that gain and offset adjustments are non-interactive. The LM334 configured as a zero-TC current source supplies quiescent current to circuit. R11 provides current limiting.

Design Equations

$$I_{OS} = (I_{R6} + I_{R7}) \left(1 + \frac{R2}{R1}\right) = 4 \text{ mA}$$

$$\text{Gain} = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \cong \frac{A_V}{R1} \times \frac{R2 + R3 + R4}{R3 + R4} \cong \frac{10 \text{ mA}}{\text{mV}}$$

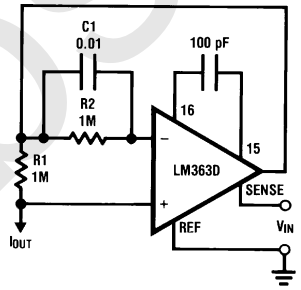
when A_V = LM363 voltage gain

$$\text{Pick } I_{334} = \frac{0.68V}{R9} + \frac{68 \text{ mV}}{R10} \cong 3.8 \text{ mA}$$

$$I_{MAX} = I_{334} + \frac{V_Z - 2.4V}{R11} = 26 \text{ mA}$$

$$I_{BRIDGE(MAX)} \cong I_{334} - I_{363} - I_Z \cong 1.5\text{mA}$$

Precision Current Source (Low Output Current)

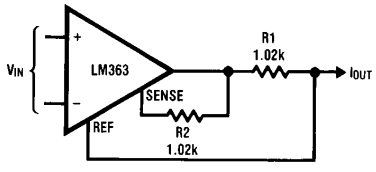


$R1 = R2$

$$I_{OUT} = \frac{V_{IN}}{GR1}, \ |V_{IN}| \leq 10V$$

TL/H/5609–21

Precision Voltage to Current Converter (Low Input Voltage)



$R1 = R2$

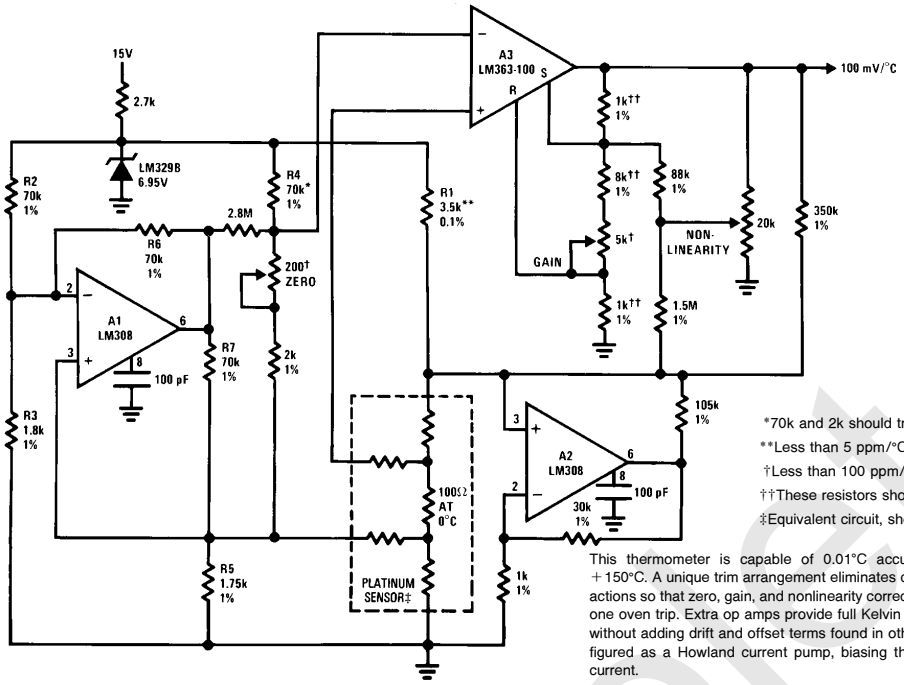
$Req = R1 \| 50 \text{ k}\Omega$

$$I_{OUT} = \frac{G \, V_{IN}}{Req} = \frac{G \, V_{IN}}{1 \text{ k}\Omega}$$

TL/H/5609–22

Typical Applications (Continued)

Curvature Corrected Platinum RTD Thermometer



TL/H/5609–23

*70k and 2k should track to 5 ppm/°C

**Less than 5 ppm/°C drift

†Less than 100 ppm/°C drift

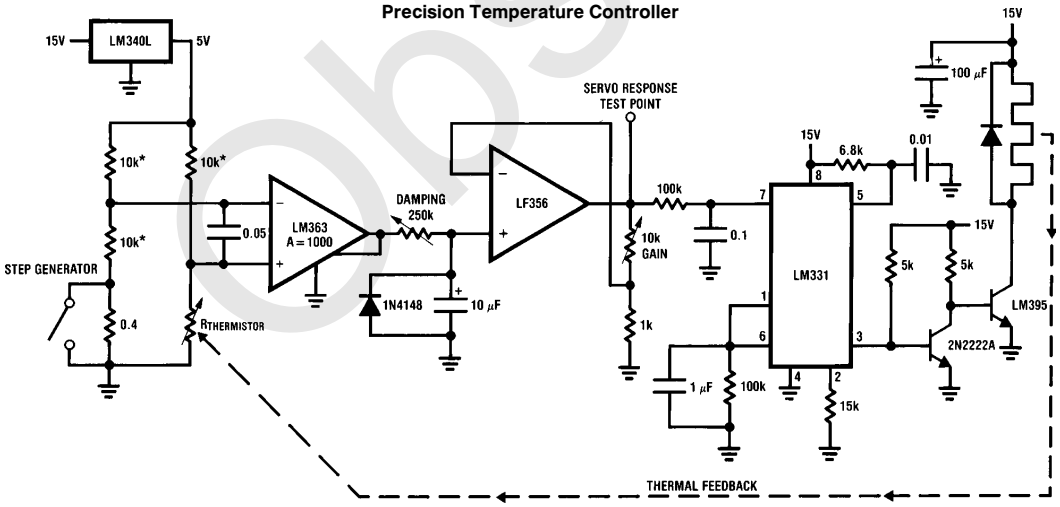
††These resistors should track to 20 ppm/°C

‡Equivalent circuit, showing lead resistance

This thermometer is capable of 0.01°C accuracy over −50°C to +150°C. A unique trim arrangement eliminates cumbersome trim interactions so that zero, gain, and nonlinearity correction can be trimmed in one oven trip. Extra op amps provide full Kelvin sensing on the sensor without adding drift and offset terms found in other designs. A2 is configured as a Howland current pump, biasing the sensor with a fixed current.

Resistors R2, R3, R4 and R5 from a bridge driven into balance by A1. In balance, both inputs of A1 are at the same voltage. Since R6 = R7, A1 draws equal currents from both legs of the bridge. Any loading of the R4/R5 leg by the sensor would unbalance the bridge; therefore, both bridge taps are given to the sensor open circuit voltage and no current is drawn.

Precision Temperature Controller

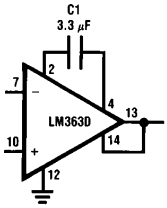


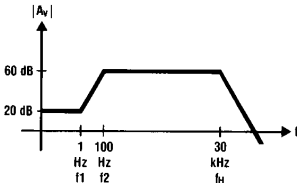
TL/H/5609–24

*Ultronix 105A wirewound
Thermistor = Yellow Springs #44032
Setpoint stability = 2.5X10⁻⁴°C/Hr

Typical Applications (Continued)

Low Frequency Rolloff (AC Coupling)



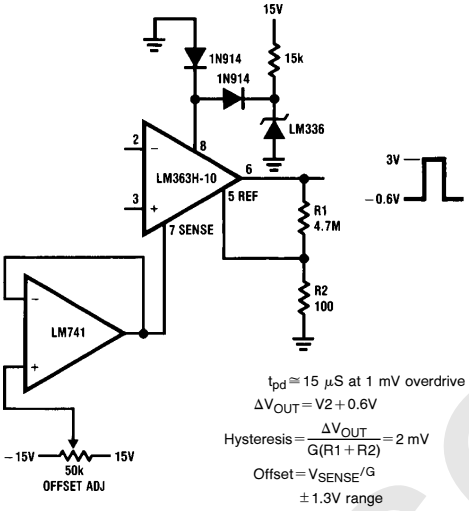


$$f1 = \frac{1}{2\pi C1(50\ k\Omega)} = 1\ Hz$$

f2 = 100 f1 = 100Hz
Reduced DC voltage gain attenuates offset error and 1/f noise by a factor of 100.

TL/H/5609–25

Precision Comparator with Balanced Inputs and Variable Offset



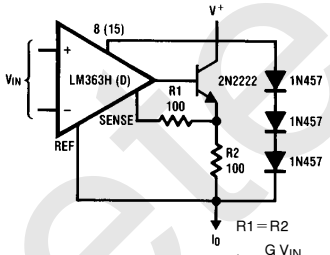
$t_{pd} \cong 15\ \mu S$ at 1 mV overdrive

$\Delta V_{OUT} = V2 + 0.6V$

$$\text{Hysteresis} = \frac{\Delta V_{OUT}}{G(R1 + R2)} = 2\ mV$$

$\text{Offset} = V_{SENSE}/G$
±1.3V range

Boosted Current Source with Limiting



R1 = R2

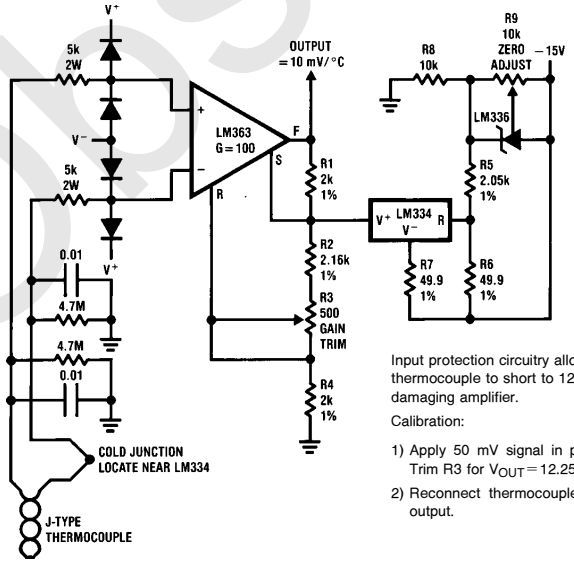
$$I_O = \frac{G\ V_{IN}}{R2}$$

$$I_{MAX} = \frac{V_{BE}}{R2}$$

≅60 mA

TL/H/5609–26

Thermocouple Amplifier with Cold Junction Compensation



Input protection circuitry allows thermocouple to short to 120 V_{AC} without damaging amplifier.

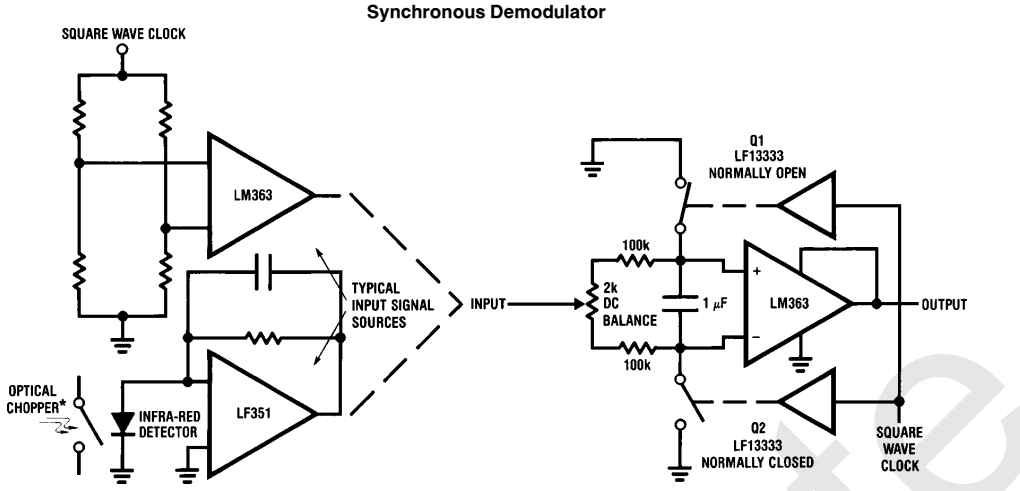
Calibration:

1) Apply 50 mV signal in place of thermocouple. Trim R3 for $V_{OUT} = 12.25V$.
2) Reconnect thermocouple. Trim R9 for correct output.

TL/H/5609–27

Typical Applications (Continued)

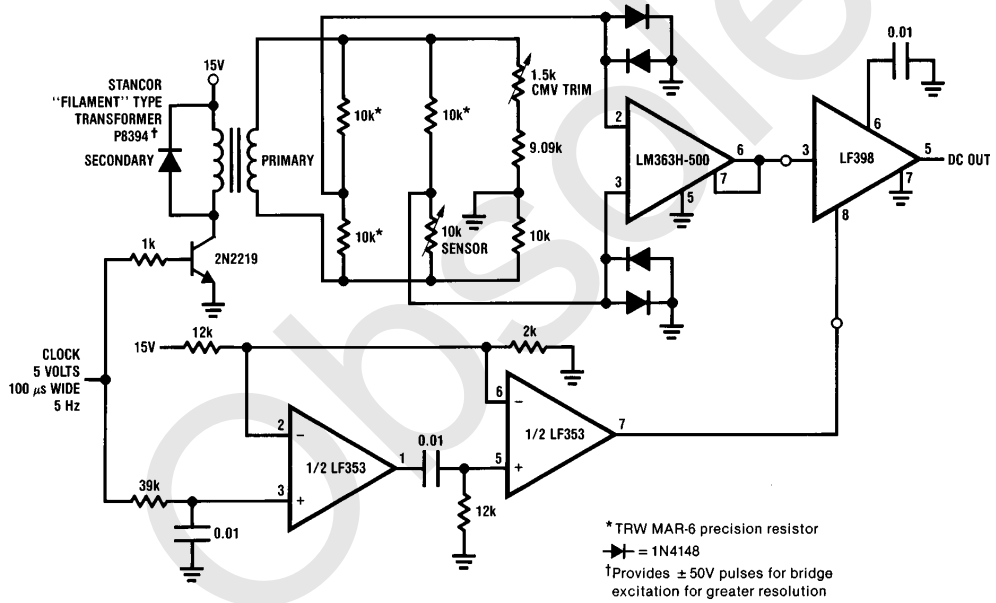
Synchronous Demodulator



TL/H/5609–28

*Use square wave drive produced by optical chopper to run LF13333 switch inputs.

Pulsed Bridge Driver/Amplifier



*TRW MAR-6 precision resistor

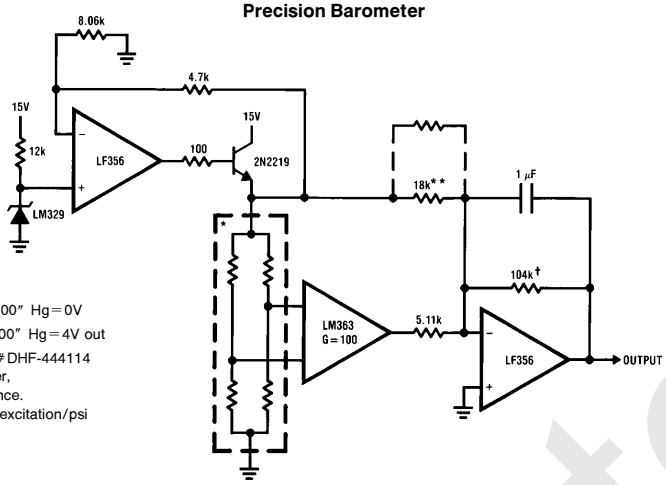
= 1N4148

†Provides ±50V pulses for bridge excitation for greater resolution without overdissipation

TL/H/5609–29

Typical Applications (Continued)

Precision Barometer



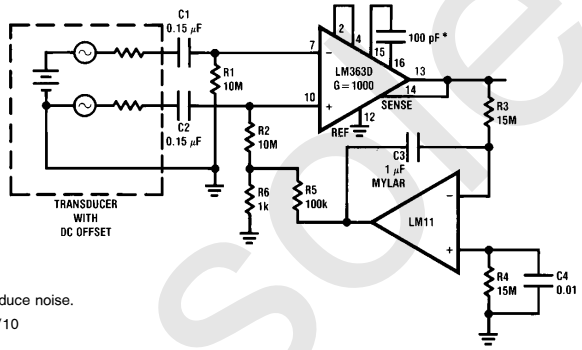
**Parallel trim for 28.00″ Hg = 0V

†Parallel trim for 32.00″ Hg = 4V out

*B.L.H. Electronics #DHF-444114
Pressure Transducer,
350Ω input impedance.
Output = 1 mV/volt excitation/psi

TL/H/5609–30

Removing Large DC Offsets



*Optional bandlimiting to reduce noise.

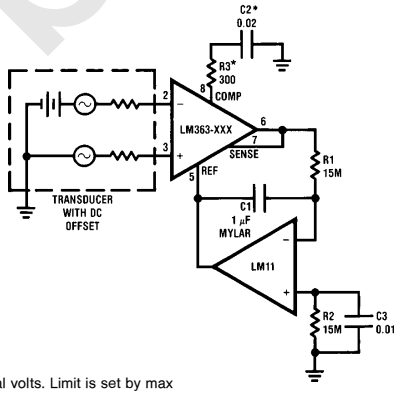
Pick R1C1 = R2C2 = R3C3/10

$$= \frac{1}{2\pi f_l}$$

f_l = 0.1 Hz for values shown. Integrator nulls out offset error to LM363 bias currents flowing into R1 and R2.

TL/H/5609–31

Removing Small DC Offsets



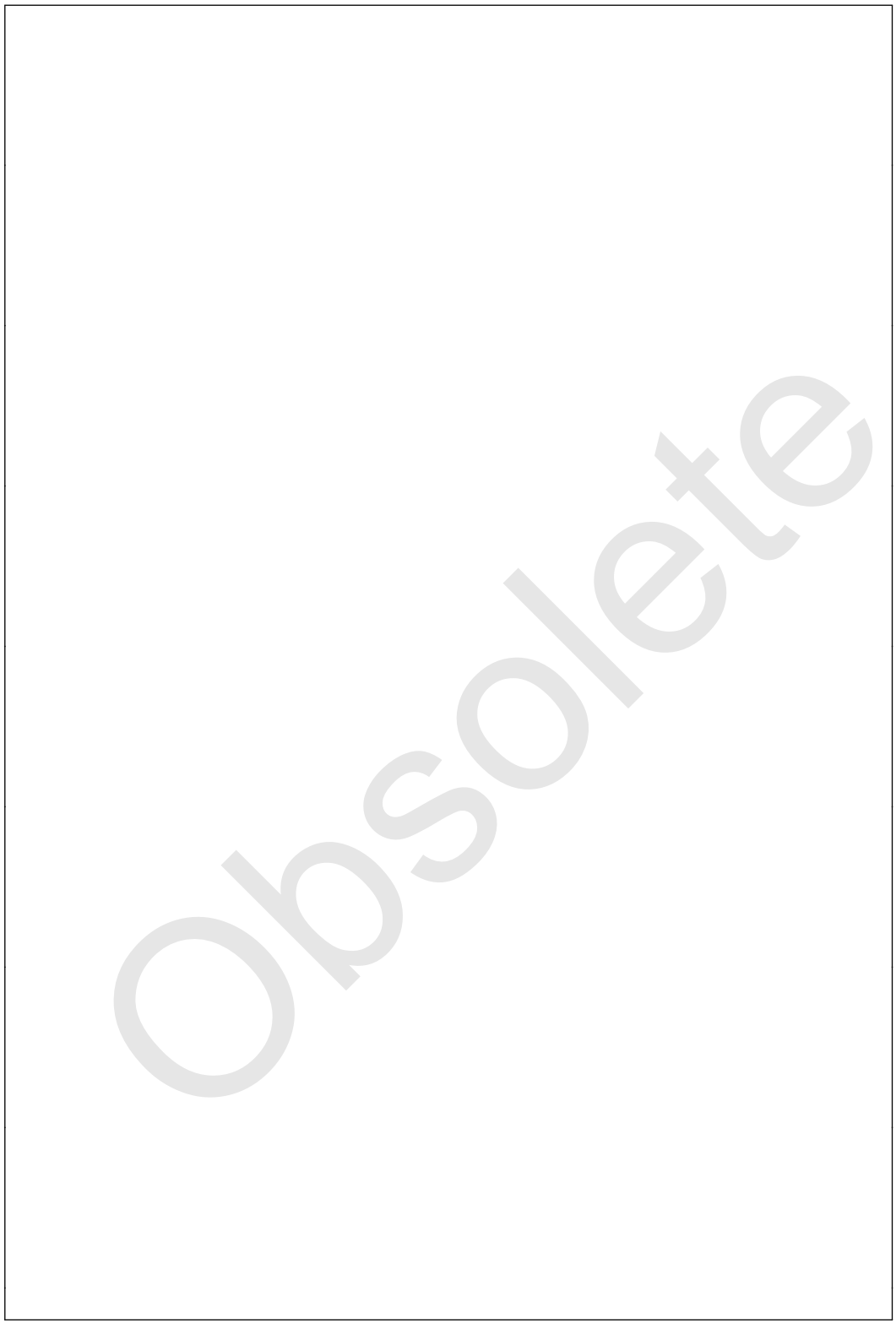
*Optional bandlimiting to reduce noise.

Low frequency break

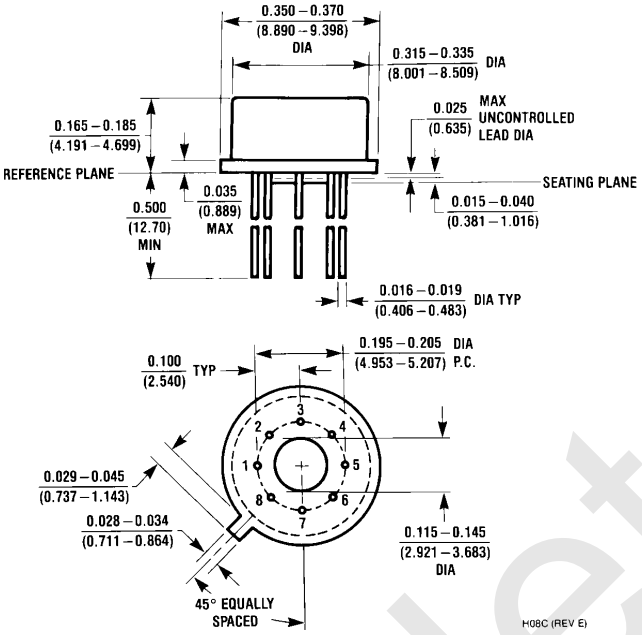
$$\text{frequency } f_l = \frac{1}{2\pi R1C1} = 0.01 \text{ Hz}$$

Accommodates out referred offset of several volts. Limit is set by max differential between reference and sense terminals.

TL/H/5609–32

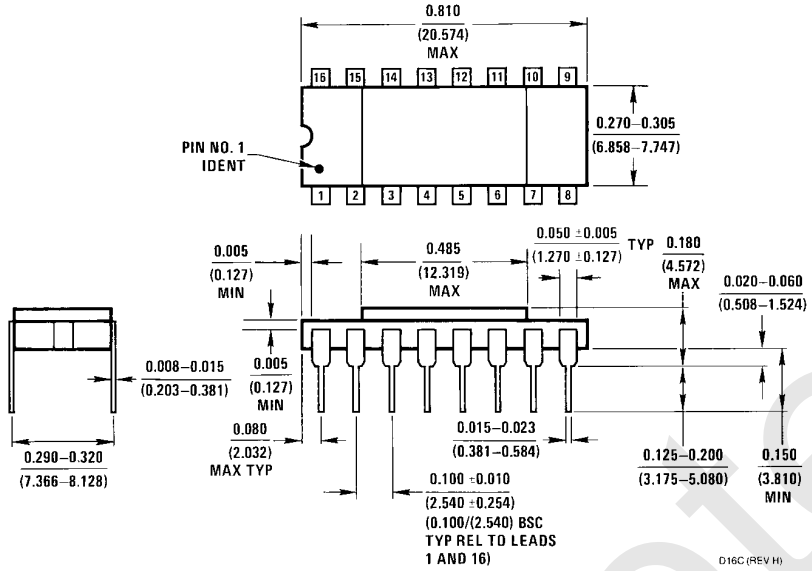

Obsolete

Physical Dimensions inches (millimeters)



Metal Can Package (H)
Order Number LM363H-10, LM363H-100 or LM363H-500
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)



Hermetic Dual-In-Line Package (D)
Order Number LM363D
NS Package Number D16C

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
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