T6A15

TENTATIVE DATA

TFT-LCD GATE DRIVER

T6A15 is a Gate Driver LSI for driving TFT-LCD Panel, which achieves high voltage operation.
T6A15 enables to correspond to various driving types, since the voltage for driving TFT-LCD panel can be input from external and a threshold level of a control signal can be changed.
T6A15 realized high integration by using C-MOS technology.

- TFT-LCD Gate Driver LSI.
- TFT-LCD driving pins: 240 Outputs (pins).
- High Voltage Operation : 30V (Max.)
- It incorporates bidirectional Shift-Resistor.
- It is easy to change panel drive voltage.
- It is possible to change the threshold level of the control signal.
- **Two or more T6A15 can be cascaded.**
- TFT-LCD data driver (T6A14) can be used with T6A15.

Tape Carrier Package

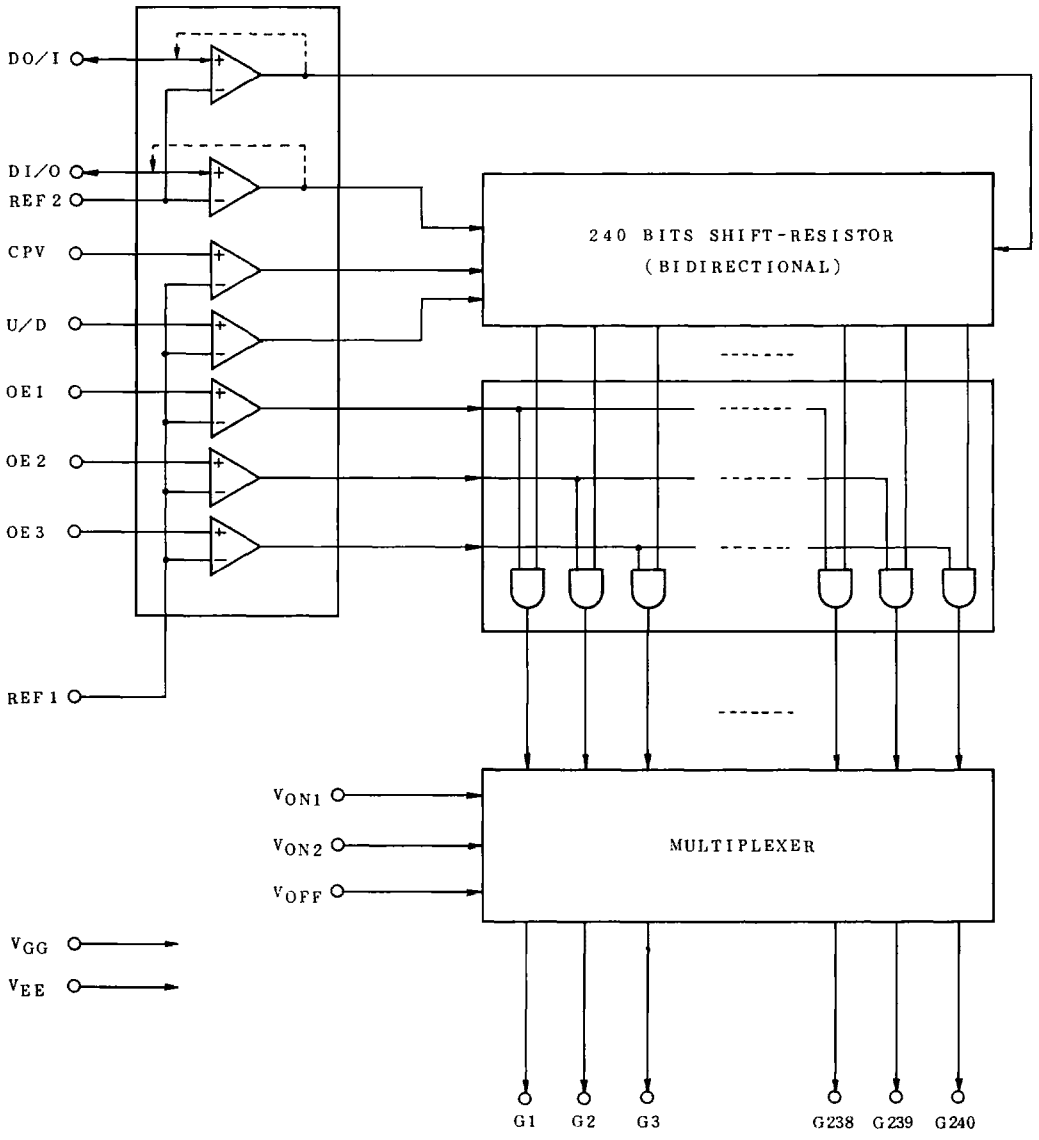
Unit : mm

T6A15	LEAD PITCH		
	IN, I/O	OUT	
(UB)	0.70	0.20	*

* Refer to Packaging Outline Dimensions.

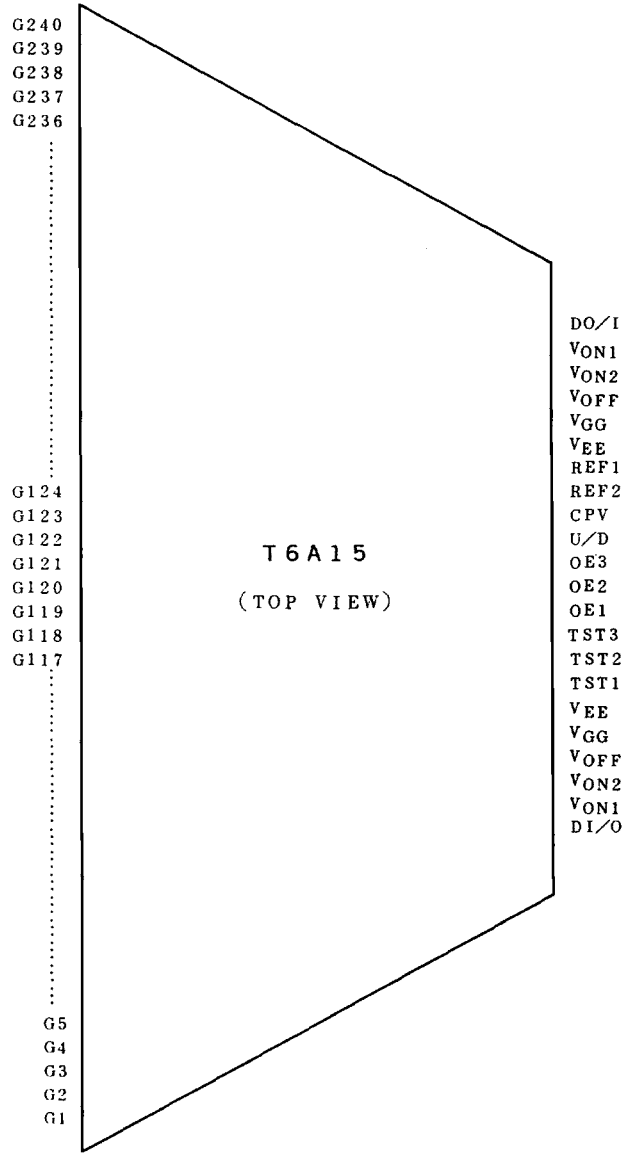
- Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

BLOCK DIAGRAM



PIN FUNCTION

PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical Shift Data Input and Output Pin
These pins are used to input and output a shift data.
DI/O or DO/I changes as follows according to U/D pin.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
Input Pin
It is a data to input into LSI synchronously to the rise of CPV and it is input in the first Shift-Resistor.
Output Pin
It outputs the data of the last Shift-Resistor synchronously to the fall of CPV. It is the input data of the next LSI in case of cascade connection.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer Direction Select Pin
It defines a shift direction of Shift-Resistor. Data shift as shown below synchronously to the rise of CPV.
U/D="H" : G1→G2→G3→G4→G5 ..... → G240
U/D="L" : G240→G239→G238→G237 ... → G1
This pin must be used "H" or "L" level in DC level.</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical Shift Clcok
It is a shift clock of Shift-Resistor. Data of Shift-Resistor shift synchronously to the rise of CPV.</td></tr>
<tr><td>OE1
OE2
OE3</td><td>I</td><td>Output Enable Pin
These pins control the output data of Output Pin (G1~G240)
OE1~3="H" level : Outputs the voltage correspond to data of Shift-Resistor.
OE1~3="L" level : Outputs the voltage of V_{OFF} regardless of Shift-Resistor data.
Output pins are controlled by these pins as shown.
Pins controlled by OE1 : G1,G4,G7,G10,~G235,G238
Pins controlled by OE2 : G2,G5,G8,G11,~G236,G239
Pins controlled by OE3 : G3,G6,G9,G12,~G237,G240</td></tr>
</table>

PIN NAME	I/O	FUNCTION
REF1 REF2	I	Reference Level Input Pin These pins set up various threshold voltage of Input Signals. Input pins defined by REF1 ... CPV, U/D, OE1~3 Input pins defined by REF2 ... DI/O, DO/I (case of input) These pins must be force "H" or "L" level in DC level.
V_{ON1} V_{ON2}	I	Analog Input Pin The voltage of these pins outputs to the Output Pins(G1~G240) as follows when a data of Shift-Resistor is "H" level. V_{ON1} : G1,G3,G5,G7, ~ G237,G239 (odd number) V_{ON2} : G2,G4,G6,G8, ~ G238,G240 (even number) There are two pins for each of V_{ON1} and V_{ON2}, and same voltage must be input to same type pins.
V_{OFF}	I	Analog Input Pin It outputs a voltage to output pin corrspond to Shift-Resistor when a data of Shift-Resistor is "L" level, and it outputs the voltage regardless of shift-resistor data when OE1~3 are "L" level.
G1~G240	O	TFT-LCD Panel Driving Pins
TST1 TST2 TST3	I	Test Pin These pins must be open.
V_{GG}		Power Supply Voltage It is a power supply pin of LSI. There are two V_{GG} pins, and same voltage must be input.
V_{EE}		Power Supply Voltage It is a power supply pin of LSI. There are two V_{EE} pins, and same voltage must be input.

FUNCTIONAL DESCRIPTION

. DEFINING A THRESHOLD VOLTAGE

(1) Input mode

REF1 can define threshold voltages of CPV, U/D and OE1~3, and REF2 can define threshold voltages of DI/O and DO/I.

Therefore, the voltage of REF1 and REF2 must be in center of voltage from "H" level to "L" level.

(2) Output mode

DI/O or DO/I outputs a voltage of V_{EE} or V_{GG} regardless of REF1 and REF2. In case of cascade connection, REF2(excepted for first LSI) must be input the threshold voltage from V_{EE} to V_{GG}.

cf.) Input Signals(excepted for REF1, REF2)

"H" level=5V "L" level=0V

Power supply voltages

V_{GG}=20V V_{EE}=-10V

In these condition, the threshold of REF are as follows.

REF1	REF2	CONDITION
2.5V	2.5V	1. First LSI cascaded 2. Single LSI (Using a single of LSI)
2.5V	5.0V	From the Second LSI to the last one cascaded

. OPERATION METHOD

(1) Input mode

DI/O or DO/I (case of input data) is input into LSI synchronously to the rise of CPV and it is input in the first Shift-Resistor. The data decides analog voltages (V_{ON} or V_{OFF}) which are output to TFT-LCD Panel driving pins(G1~G240).

(2) Output mode

DI/O or DO/I(case of output data) outputs the data of the last Shift-Resistor synchronously to the fall of CPV.

When the data is "H" level, it outputs the voltage of V_{GG}. When it is "L" level, it outputs the voltage of V_{EE}.

The data of the Shift-Resistor is as follows:

U/D="H" level

DI/O → G1 → G2 → G3 → G4 → G5 → G6 → G7 → G8 → ... G240 → DO/I

U/D="L" level

DI/I → G240 → G239 → G238 → G237 → G236 → G235 → ... G1 → DI/O

. TFT-LCD PANEL DRIVING PINS (G1~G240)

These pins are output analog voltages of V_{ON1} or V_{ON2} when the data of the Shift-Resistor are "H" level. These pins are output analog voltages of V_{OFF} when the data are "L" level or OE1~3 is "L" level.

These pins is controlled by OE1~3 as shown.

OE1="L" level " G1,G4,G7,G10,...G238 These pins output the voltage of V_{OFF}.

OE2="L" level " G2,G5,G8,G11,...G239 These pins output the voltage of V_{OFF}.

OE3="L" level " G3,G6,G9,G12,...G240 These pins output the voltage of V_{OFF}.

TIMING CHART

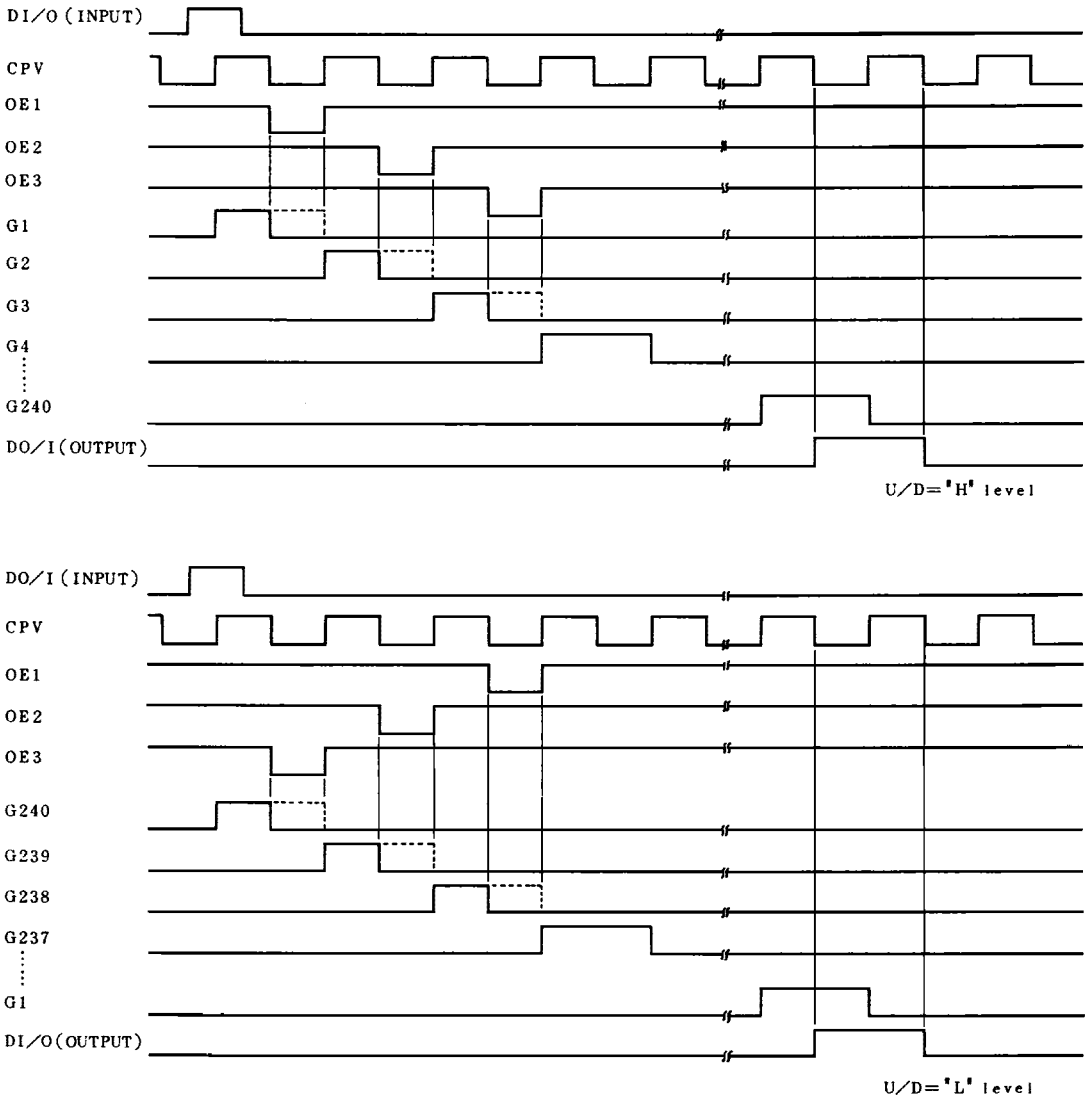


Fig. 1

MAXIMUM RATINGS (V_{EE}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Supply Voltage	V_{GG}		-0.3~35	V	
Reference Voltage	V_R		-0.3~V_{GG}+0.3	V	
Input Voltage	V_{IN}		-0.3~V_{GG}+0.3	V	
Analog Input Voltage	V_{IY}		-0.3~V_{GG}+0.3	V	
Storage Temperature	T_{stg}		-55~125	°C	

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS (V_{EE}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Operating Voltage	V_{GG}		20~30	V	
Operating Temperature	T_{op}		-20~75	°C	
Operating Frequency	f_{CPV}	V_{GG}=30V	DC~100	kHz	
Output Load Capacitance	C_L		500(MAX)	PF/PIN	
Analog Input Voltage	V_{IY}		0~V_{GG}	V	V_{ON1},V_{ON2},V_{OFF}

DC CHARACTERISTICS

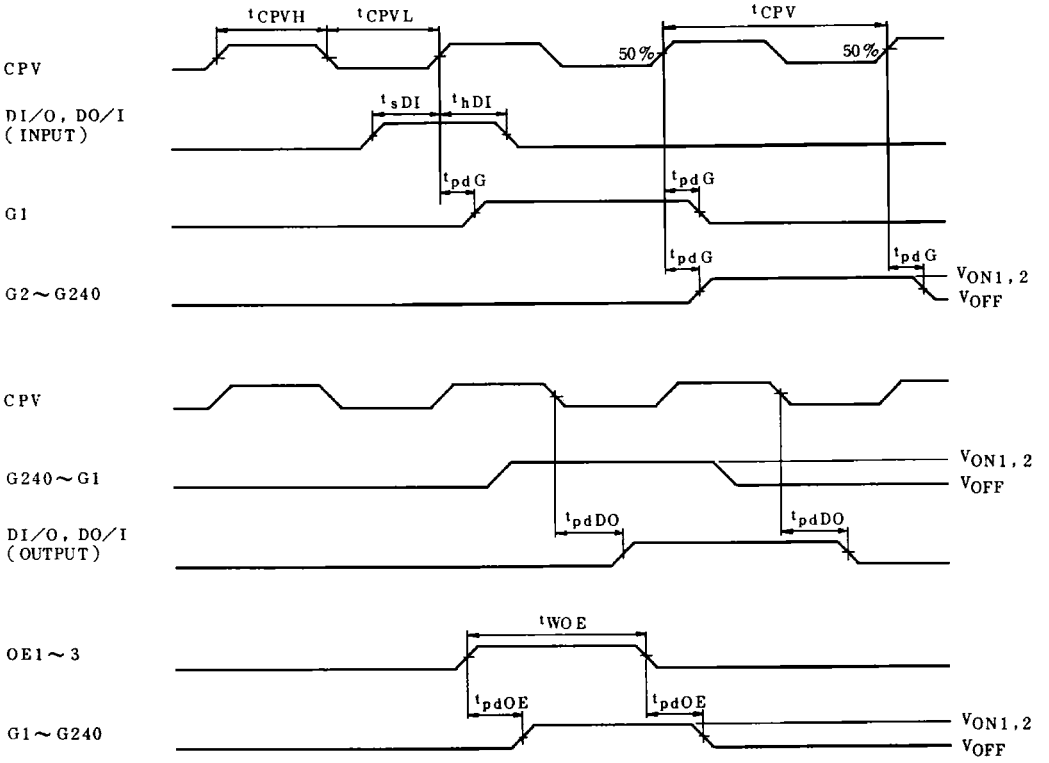
(Unless otherwise specified, V_{GG}=30V, V_{EE}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	APPLY PIN
Input "L" Level	V_{IL}		0	VR-1.5	V	Logic Input
Input "H" Level	V_{IH}		VR+1.5	V_{GG}	V	Logic Input
Output "L" Level	V_{OL}	I_{OL}=0.6mA	0	0.3	V	DI/O, DO/I
Output "H" Level	V_{OH}	I_{OH}=-0.6mA	29.7	30	V	DI/O, DO/I
Reference Voltage	VR		2.5	22	V	REF1, REF2
Output Resistance	R_{OG}		-	1.0	kΩ	G1~G240
	ΔR_{OG}	*1	-	±250	Ω	G1~G240
Input Leak Current	I_{IN}		-1.0	1.0	μA	Logic Input
	I_{OZ}		-5.0	5.0	μA	DI/O, DO/I
Current Consumption	I_{GG}	f_{CPV}=100kHz	-	4.0	mA	V_{GG}

Directions

*1 In case of selecting same power supply (V_{ON1} or V_{ON2} or V_{OFF}), it is the difference of Resistance in a chip.

AC CHARACTERISTICS



(Unless otherwis specified, V_{GG}=30V, V_{EE}=0V, Rising and falling time=10ns)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Operating Frequency	t_{CPV}		10	-	μs
CPV Pulse Width "H"	t_{CPVH}		4	-	μs
CPV Pulse Width "L"	t_{CPVL}		4	-	μs
Data Set Up Time	t_{sDI}		1	-	μs
Data Hold Time	t_{hDI}		1	-	μs
OE Enable Time	t_{WOE}		1	-	μs
Output Delay Time 1	t_{pdDO}		-	1	μs
Output Delay Time 2	t_{pdG}		-	1	μs
Output Delay Time 3	t_{pdOE}		-	1	μs