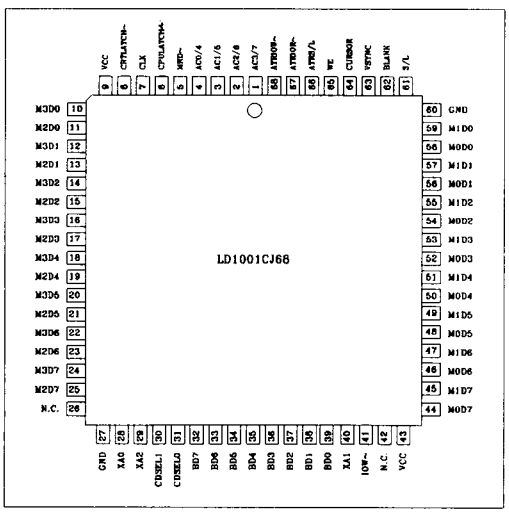
# EGA CHIP SET

## DESCRIPTION

The LD1001/1002 are EGA chip set IC's, designed to meet MDA, CGA, EGA requirements. The LD1001 is a data controller which contains the Graphics Controller 1, Graphics Controller 2, serialization, and attribute control positions of the EGA video controller. The Graphics Controller 1 and 2 control the data path and bit-level processing for video planes 0, 1, 2, 3 respectively. The LD1002 is a timing Controller which contains the CRT Controller, Light pen interface, Sequencer, Video Palette RAM and output drivers, and some Attribute Controller logic.The LD1001/LD1002 are fabricated in an advanced 2u CMOS process to achieve low drain power and high speed requirements.




## FEATURES

* IBM EGA, CGA, MDA compatible
* Onboard RGB drivers
* Light pen interface
* Low power CMOS design
* 256K DRAM support
* Surface mount fabrication

## APPLICATIONS

* EGA board
* High resolution Workstations

## ORDERING INFORMATION

| Part number | Package | Operating temperature |
|---|---|---|
| LD1001CJ68 | PLCC | 0° C to +70° C |
| LD1002CJ84 | PLCC | 0° C to +70° C |

## GENERAL DESCRIPTION

The LD1001 is a 68 pin PLCC data controller which supports the following functions: read masking, write data rotating, internal read data latches and Boolean logic unit for read/modify/write operations on the video memory. The Attribute serializer fetches pixel data serializes it, and sends out 4-bit color Palette address to the Timing Controller Chip. The LD1002 is an 84 pin PLCC and provides video outputs, screen refresh addresses, and arbitration between the CPU and CRT memory cycles so the screen can be redrawn without any flashing or "snow".

## LD1001 SYMBOL DESCRIPTION

| Symbol | Pin | Signal type | Pin description |
|---|---|---|---|
| AC0/4 - AC3/7 | 1-4 | O | Color palette address outputs (active high). To represent all video attributes, except for final color value. |
| MRD~ | 5 | I | Memory read (avtive low). Used by CPU to read display memory in conjunction with the high going edge of the CPULATCH~ input. |
| CPULATCH~ | 6 | I | CPU latch (active low). It is generated by the LD1002. The display memory data will be read into the LD1001. The low to high going edge of this signal, along with MRD~ active, will output data onto BD0-7 for a CPU memory read operation. |
| CLK | 7 | I | Clock input. This clock is used to clock the video data outputs (AC0/4 - AC3/7). |
| CRTLATCH~ | 8 | I | CRT latch (active low). It is generated by the LD1002, the display memory graphics data is loaded into the LD1001 on the low to high going edge. The data in the display memory must meet set up and hold requirements. The data loaded is transferred into the Shifter Register when S/L is low. |
| M0D0-7 | | I/O | Memory data buses (three state). To send and receive data to and from the display memory. |
| M1D0-7 | | I/O | Memory data buses (three state). To send and receive data to and from the display memory. |
| M2D0-7 | | I/O | Memory data buses (three state). To send and receive data to and from the display memory. |
| M3D0-7 | | I/O | Memory data buses (three state). To send and receive data to and from the display memory. |
| XA0-2 | | I | Address lines (active high). Used to access the graphics controller register. |
| CDSEL0-1 | 30-31 | O | Screen memory map controls. |
| BD0-7 | 32-37 | I/O | Data bus (three state). Data is transfers from or to the LD1001 via this bus. |
| IOW~ | 41 | I | Write signal (active low). Data present on BD0-7 is latched internally on the rising edge of this signal. |
| S/L | 61 | I | Shift or load. Generated by LD1002 and serves two functions. When low, the display memory is loaded into the Shifter. When high, it is shifted by one bit per clock. |

## LD1001 SYMBOL DESCRIPTION

| Symbol | Pin | Signal type | Pin description |
|---|---|---|---|
| BLANK | 62 | I | Composite blanking input. (active high). If CURSOR is high during the falling edge of BLANK , the following line will have an underline attribute. |
| VSYNC | 63 | I | Vertical sync input (active high). Increments the video blank and cursor blank counters. |
| CURSOR | 64 | I | Cursor. It indicates a valid cursor position when the display is active, and if CURSOR is high during the falling edge of BLAK, it indicates that the next line is to be underlined. |
| WE | 65 | I | Write enable (active high). When it is active, the display memory data is output on the M0D0-7, M1D0-7, M2D0-7, and M3D0-7 data buses. When WE is low, these data buses are three stated. |
| ATRS/L | 66 | I | Attribute Shift/Load. Used by the attribute controller section to load new pixel data during alphanumeric modes. When low, new pixel data is loaded; when high the data is shifted out. |
| ATRIOR~ | 67 | I | Attribute controller I/O Read strobe (active low). It is used to read the STATUS 1 Register. This input also resets the attribute controller input to address (index) mode. |
| ATRIOW~ | 67 | I | Attribute controller I/O Write strobe (active low). It is used to write to the attribute controller registers. |
| VCC | 9,43 | I | Most positive supply voltage. |
| GND | 27,60 | O | Signal ground. |

## LD1002 SYMBOL DESCRIPTION

| Symbol | Pin | Signal type | Pin description |
|---|---|---|---|
| A0-7 | 78-1 | I | Address lines. Used to address control registers and screen RAM. |
| CRTINT~ | 8 | O | CRT interrupt (open drain). If it is enabled, will go low when Vertical sync occurs |
| HSYNC | 9 | O | Horizontal retrace (active high). |
| VSYNC | 10 | O | Vertical retrace (active high). |
| BLANK | 12 | O | Composite blanking output (active high). Is used to blank the screen. |
| CURSOR | 13 | O | Cursor. It indicates a valid cursor position when the display is active, and if CURSOR is high during the falling edge of BLANK, it indicates that the next line is to be underlined. |
| BD0-7 | 14-21 | I/O | Data buses (three state). |
| B, G, R | 22-24 | O | Color outputs (active high). Are the primary Red, Green, and Blue color outputs. |
| B', G', R' | 25-27 | O | Secondary color outputs (active high). In 4 bit color mode, G~ is the only one used. In monochrome mode, B~ is the video output, and G~ is the Intensity control. |
| RAS0-3~ | | O | Row address strobes (active low). To enable the screen memory planes. |
| IOCHRDY~ | 33 | O | I/O ready(open drain, active low). Inserts the "wait states" to synchronize the CPU cycle to the screen RAM cycle. This single is only active during screen memory read or write cycles. |
| WE | 34 | O | Write enable (active high). Indicates that the current memory cycle will be a write cycle. |
| CPULATCH~ | 35 | O | CPU latch (active low). Is used to latch screen memory for a pending CPU read cycle. |
| CAS~ | 36 | O | Column address strobe (active low). To enable screen memory planes. |
| CLK | 37 | O | Video clock output. Used to clock video data through the LD1001. Depending on register initialization, this output will either follow DOTCLK, or DOTCLK divide by two. |
| AC0/4 - AC3/7 | 38-41 | I | Palatte address inputs (active high). |
| DOTCLK | 42 | I | Clock input. This clock input is used internally as a master clock. |

## LD1002 SYMBOL DESCRIPTION

| Symbol | Pin | Signal type | Pin description |
|---|---|---|---|
| ATRS/L | 43 | O | Pixel load. Used by LD1001 to load new pixel data during alpha-numeric modes. |
| S/L | 44 | O | Shift load. Used by the LD1001 to load pixel data from the screen RAM during graphics modes. |
| VMEMR~ | 45 | I | Video memory read request (active low). Requests a screen RAM read cycle. |
| VMEMW~ | 46 | I | Video memory write request (active low). Initiates a write cycle to screen RAM. |
| M1D3 | 49 | I | Plane 2 RAM select. This line selects which of the banks of RAM in plane 2 is currently in used as the font plane. |
| OEMX1~ | 50 | O | Multiplexer 1 output enable (active low). To enable the external latch to drive the address bus for planes 2 and 3 during alphanu-meric modes. |
| OEMX2~ | 51 | O | Multiplexer 2 output enable (active low). To enable the external latch to drive the address bus for planes 2 and 3 during alphanu-meric modes. |
| CRTLATCH~ | 53 | O | CRT latch (active low). Is used to latch memory LD1001 for CRT display cycles. |
| BA0-7 | 61-54 | O | Address bus for memory planes 2 and 3. |
| AA0-7 | 69-62 | O | Address bus for memory planes 0 and 1. |
| A000 | 70 | I | Memory address control input. It is used to select different ad-dress sources for screen address bit-0 during CPU cycle. |
| LPEN~ | 72 | I | Light pen input strobe(Active on the falling edge). This signal is used to latch the current screen refresh address into the light pen registers of the CRTC section of the LD1002. |
| IOG | 73 | I | I/O enable (active high). Provides external decoding of address bits higher than A7. When low the internal I/O mapped registers are deactivated. |
| IOR~ | 75 | I | I/O read strobe (active low). Is used to enable the data bus (BD0-7) drivers. |
| IOW~ | 76 | I | I/O write strobe (active low). Data present on the BD0-7 is latched internally on the rising edge of this signal. |
| RESET | 77 | I | Reset input (active high). |

## LD1002 SYMBOL DESCRIPTION

| Symbol | Pin | Signal type | Pin description |
|---|---|---|---|
| A0-7 | 78-1 | I | Address lines. Used to address control registers and screen RAM. |
| A8-16 | | I | Address lines. Used only for screen RAM accesses. Are ignored during control register accesses. |
| VCC | 11,52 | I | Most positive supply voltage. |
| GND | 31,74 | O | Signal ground. |

## LD1001/1002 PROGRAMMING TABLE

| Description | Port Address | Index | Conditions |
|---|---|---|---|
| **ATTRIBUTE CONTROL REGISTER** | | | |
| Index Register | $C0, C1 | | IOG = high |
| Palette color 0 | $C0, C1 | $00 | |
| Palette color 1 | $C0, C1 | $01 | |
| Palette color 2 | $C0, C1 | $02 | |
| Palette color 3 | $C0, C1 | $03 | |
| Palette color 4 | $C0, C1 | $04 | |
| Palette color 5 | $C0, C1 | $05 | |
| Palette color 6 | $C0, C1 | $06 | |
| Palette color 7 | $C0, C1 | $07 | |
| Palette color 8 | $C0, C1 | $08 | |
| Palette color 9 | $C0, C1 | $09 | |
| Palette color 10 | $C0, C1 | $0A | |
| Palette color 11 | $C0, C1 | $0B | |
| Palette color 12 | $C0, C1 | $0C | |
| Palette color 13 | $C0, C1 | $0D | |
| Palette color 14 | $C0, C1 | $0E | |
| Palette color 15 | $C0, C1 | $0F | |
| Mode control | $C0, C1 | $10 or $30 | |
| Overscan (border) color | $C0, C1 | $11 or $31 | |
| Color plane enable | $C0, C1 | $12 or $32 | |
| Horizontal pixel panning | $C0, C1 | $13 or $33 | |

## LD1001/1002 PROGRAMMING TABLE

| Description | Port Address | Index | Conditions |
|---|---|---|---|
| **MISCELLANEOUS OUTPUT REGISTER** | | | |
| Misc. output register | $C2, C3 | | |
| **SEQUENCER INDEX REGISTER** | | | |
| Sequencer index register | $C4 | | |
| Reset control | $C5 | $00 | |
| Clocking mode | $C5 | $01 | |
| Plane enable | $C5 | $02 | |
| Character blank select | $C5 | $03 | |
| Memory mode | $C5 | $04 | |
| **GRAPHICS CONTROLLER** | | | |
| Gra. cont. 2 shadow | $CA | | |
| Gra. cont. 1 and 2 index | $CE | | |
| Mode register shadow | $CF | $05 | |
| Misc. shadow | $CF | $06 | |
| **LIGHT PEN** | | | |
| Light pen clear | $DB | | |
| Light pen set | $DC | | |
| **CRT CONTROL REGISTERS** | | | |
| Index Register | $3x0, 2, 4, 6 | | x=B Monochrome |
| Horizontal total | $3x1, 3, 5, 7 | $00 | x=D Color |
| Horizontal display end | $3x1, 3, 5, 7 | $01 | |
| Start horizontal blank | $3x1, 3, 5, 7 | $02 | |
| End horizontal blank | $3x1, 3, 5, 7 | $03 | |
| Start horizontal retrace | $3x1, 3, 5, 7 | $04 | |
| End horizontal retrace | $3x1, 3, 5, 7 | $05 | |
| Vertical total | $3x1, 3, 5, 7 | $06 | |
| Overflow | $3x1, 3, 5, 7 | $07 | |
| Preset row scan | $3x1, 3, 5, 7 | $08 | |
| Max scan line | $3x1, 3, 5, 7 | $09 | |
| Cursor start | $3x1, 3, 5, 7 | $0A | |
| Cursor end | $3x1, 3, 5, 7 | $0B | |
| Start address high | $3x1, 3, 5, 7 | $0C | |
| Start address low | $3x1, 3, 5, 7 | $0D | |
| Cursor location high | $3x1, 3, 5, 7 | $0E | |
| Vertical retrace start | $3x1, 3, 5, 7 | $0F | |
| Light pen high | $3x1, 3, 5, 7 | $10 | |
| Vertical retrace end | $3x1, 3, 5, 7 | $11 | |
| Light pen low | $3x1, 3, 5, 7 | $11 | |
| Vertical display end | $3x1, 3, 5, 7 | $12 | |

## LD1001/1002 PROGRAMMING TABLE

| Description | Port Address | Index | Conditions |
|---|---|---|---|
| Offset | $3x1, 3, 5, 7 | $13 | |
| Underline location | $3x1, 3, 5, 7 | $14 | |
| Start vertical blank | $3x1, 3, 5, 7 | $15 | |
| End vertical blank | $3x1, 3, 5, 7 | $16 | |
| Mode control | $3x1, 3, 5, 7 | $17 | |
| Line compare | $3x1, 3, 5, 7 | $18 | |

## REGISTER FUNCTIONAL DESCRIPTIONS

### ATTRIBUTE INDEX REGISTER (AIR)

**AIR BIT0-4:**
Attribute address bits.
The address register is a pointer register located at 3C0 Hex. This register is loaded with a binary value that points to the attribute data register where data is to be written. The attribute controller does not have an address input to control selection of the index and data registers. Instead, the input mode toggles between the index and data registers on alternate accesses. To reset the mode to index register, read from port 3DA Hex when in the color modes, or read from port 3BA Hex when in monochrome mode.

**AIR BIT 5:**
Palette Address Source.
0 = To load the Color Palette Register
1 = To enable the screen data to access the color palette

**AIR BIT 6-7:** Not used.

### PALETTE REGISTERS 00 - 0F Hex (PR)

**PR BIT0-5:**
Palettes.
These 6-bit registers allow dynamic mapping between the text attribute or graphics color input value and the displayed color on the CRT screen. A logical 1 selects the appropriate color. The Color Palette Register should be modified only during the vertical retrace interval to avoid glitches in the displayed image. Note that some color monitors do not have an intensity input and are only capable of displaying 8 colors. Monitors with 4 color inputs are capable of displaying 16 colors, and monitors with 6 color inputs are capable of displaying 64 colors.

**PR BIT 0** = Blue Video
**PR BIT 1** = Green Video
**PR BIT 2** = Red Video
**PR BIT 3** = Sec. Blue/Monochrome Video
**PR BIT 4** = Sec. Green/Intensity
**PR BIT 5** = Sec. Red
**PR BIT 6-7** = Not used.

### MODE CONTROL REGISTER (MCR)

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 10 or 30 Hex before writing can take place.

**MCR BIT 0:**
Graphics/Alpha
0 = Alphanumeric operation
1 = Bit mapped graphics operation

**MCR BIT 1:**
Display type.
0 = Monochrome display attributes
1 = Color display attributes

**MCR BIT 2:**
Line graphics (character codes C0 - DF Hex).
For character fonts that do not use the line graphics character codes in the range of C0 - DF Hex, bit -2 of this register should be set to "0".

0 = Set ninth column to the same color as the background
1 = Enables the special line graphics character codes for the IBM Monochrome Display Adapter. Forces the ninth column dot of a line graphic character to be the same color as the eighth column dot of the character.

**MCR BIT 3:**
Blink enable.
0= Select the background intensity of the attribute input. This mode is available for compatibility with the MDA and CGA.
1 = Enable the blink attribute in graphic/alphanumeric modes

**MCR BIT 4-7:** Not used.

## ATTRIBUTE OVERSCAN COLOR REGISTER (AOCR)

This is a write only register pointed to by the value in the Attribute Index Register. This value must be either 11 or 31 Hex before writing can take place. The processor output port address for this register is 3C0 Hex.

**AOCR BIT 0-5:**
Overscan color.
This 6 bit register determines the overscan (border) color displayed on the CRT screen.
0= Monochrome displays
1= Select the appropriate color for each location

**AOCR BIT 6-7:** Not used.

## ATTRIBUTE COLOR PLANE REGISTER (ACPR)

This is a write only register pointed to by the value in the Attribute Index Register. This value must be either 12 or 32 Hex before writing can take place.

**ACPR BIT 0-3:**
Color plane assignments.
0= Disable the respective display memory
1= Enable the respective display memory

**ACPR BIT 4-5:**
Video Status Mux.
Selects two of the six color outputs to be available on the status port. the following table illustrates the combinations available and the color output wiring. Bit-4 of this register is also used to clear the blink control counters for both the cursor and attribute blink functions. When bit-4 is "1", the counters are cleared and the 6 color outputs are three stated.

| ACPR | | ISR1 | |
|---|---|---|---|
| bit-5 | bit-4 | bit-5 | bit-4 |
| 0 | 0 | red | blue |
| 0 | 1 | sec. blue | green |
| 1 | 0 | sec. red | sec. green |

## ATTRIBUTE HORIZONTAL PEL PANNING REGISTER (AHPPR)

This is a write only register pointed to by the value in the Attribute index Register. This value must be either 13 or 33 Hex before writing can take place.

**AHPPR BIT 0-3:**
Horizontal Pel Panning.
This 4 bit register selects the number of picture elements (pel) to shift the video data to the left. Pel panning is available in both Alphanumeric and bit-mapped modes. In Monochrome Alphanumeric mode, the image can be shifted a maximum of 9 pels. In all other Alphanumeric modes and bit-mapped modes, the image can be shifted a maximum of 8 pels. The sequence for shifting the image is:

Monochrome Alphanumeric only
9 pels/char: 8,0,1,2,3,4,5,6,7

All other modes
8 pel/char: 0,1,2,3,4,5,6,7

**AHPPR BIT 4-7:** Not used.

## MISCELLANEOUS OUTPUT REGISTER (MOR)

This is a write only register. To access this register, IOG must be high and A0-A7 must have a Hex value of C2. The IOW input is the write strobe. A high on reset will cause all bits to reset.

**MOR BIT 0:**
I/O address select.
This bit maps the CRTC I/O addresses 3Bx or 3Dx Hex for the IBM Monochrome or Color Graphics Monitor Adapter emulation.
0= Sets CRTC address to 3B0-7 Hex and Input Status Register 1's address to 3BA Hex for monochrome emulation.
1= Sets CRTC address to 3D0-7 Hex and Input Status Register 1's address to 3DA Hex for Color/Graphics Monitor Adapter emulation.

**MOR BIT 1-4:** Not used.

**MOR BIT 5:**
Page bit.
Selects between two 64K pages of memory when in the Odd/Even modes (0, 1, 2, 3, 7).
0 = Selects the low page of memory
1 = Selects the high page of memory

**MOR BIT 6-7:** Not used.

**SEQUENCER REGISTER**

| Description | Port Address | Index |
|---|---|---|
| Index reg. | C4 | |
| Reset control | C5 | 0 |
| Clocking mode | C5 | 1 |
| Plane enable | C5 | 2 |
| Character bank sel. | C5 | 3 |
| Memory mode | C5 | 4 |

Note: Access to all registers is write only, and IOG must be high while IOW is used as a data strobe.

**SEQUENCER INDEX REGISTER (SIR)**

The Index register is a write only register. It points to the control register to be modified.

**SIR BIT 0-4:** Control register index value.

**SIR BIT 5-7:** Not used.

**SEQUENCER RESET CONTROL REGISTER (SRCR)**

The Reset Control Register is a write only register that is a accessed when an index value of 00 Hex is loaded into the Index Register.

**SRCR BIT 0:**
Async reset.
0 = Forces the sequencer to halt asynchronously and causes the following outputs to these state:

| | |
|---|---|
| CRTLATCH | high |
| CLK | three state |
| ATRS/L | three state |
| S/L | three state |
| RAS 0-3 | three state |
| WE | three state |
| CPULATCH | three state |
| CAS | three state |

Note: Using this bit to halt the sequencer will result in corrupted screen memory.

1 = Start the sequencer (SRCR BIT 1 = 1)

**SRCR BIT 1:**
Sync reset.
This bit should be cleared before changing the clocking mode register to keep from corrupting screen memory.

0 = Forces the sequencer to halt synchronously
1 = Start the sequencer (SRCR BIT 0 = 1)

**SRCR BIT 2-7:** Not used.

**SEQUENCER CLOCKING MODE REGISTER (SCMR)**

The Clocking Mode Register is a write only register accessed by writing an Index Value of 01 Hex to the Index Register. Before modifying the contents of this register, the Sync Reset bit in the reset Control Register should be cleared. Then modification may take place, followed by resetting the Sync Reset bit.

**SCMR BIT 0:**
8/9 pixels.
0 = Select 9 pixel clocks for every character fetch
1 = Select 8 pixel clocks for every character fetch

**SCMR BIT 1:**
Bandwidth.
0 = Forces the sequencer to allow only one video memory cycle out of five for CPU access, while the remainder go for refreshing the screen.
1 = Sets the sequencer to allow 3 out of 5 accesses for the CPU. All high resolution modes (640 pixels or greater) uses the 20% Bandwidth mode (low) as the screen must have more data sent to it in a given amount of time.

**SCMR BIT 2:**
Shift load.
This mode can be used to chain 16 bits together in the shift register.
0 = Load video serialization logic with every character cycle
1 = Reload shifters every other character cycle

**SCMR BIT 3:**
Dot Clock Select.
0 = CLK signal will follow the DOTCLOCK pin
1 = CLK will be DOTCLOCK devided by 2. The divide by 2 mode is used for low resolution modes (320 x 200 and 40 character modes).

**SCMR BIT 4-7:** Not used.

**SEQUENCER PLANE ENABLE REGISTER (SPER)**

This is a write only register accessed with an Index Value of 02 Hex. It provides a write mask function on a plane by plane basis. By enabling all planes (writing a value of 0F Hex to the register), 32 bits at a time may be written by the CPU into the screen memory.

**SPER BIT 0-3:**
0 = Mask the plane
1 = Enable (in any bit location) the particular plane for modification

**SPER BIT 4-7:** Not used.

**SEQUENCER CHARACTER BANK SELECT (SCBS)**

This register is write only and is accessed with an Index Value of 03 Hex. This register is used in alphanumeric modes to provide a means of using more than 256 character types at a time.

**SCBS BIT 0:**
Character Bank select B.
Selects the bank of RAM used when the character attribute bit (M1D3 input) is low according to the following table:

| D1 | D0 | Bank Selected |
|---|---|---|
| 0 | 0 | 1st 8K of plane 2, Bank 0 |
| 0 | 1 | 1st 8K of plane 2, Bank 1 |
| 1 | 0 | 1st 8K of plane 2, Bank 2 |
| 1 | 1 | 1st 8K of plane 2, Bank 3 |

**SCBS BIT 1:**
Character Bank select A.
Selects the Bank of RAM used when the character attribute bit (M1D3 input) is low according to the following table:

| D3 | D2 | Bank Selected |
|---|---|---|
| 0 | 0 | 1st 8K of plane 2, Bank 0 |
| 0 | 1 | 1st 8K of plane 2, Bank 1 |
| 1 | 0 | 1st 8K of plane 2, Bank 2 |
| 1 | 1 | 1st 8K of plane 2, Bank 3 |

In alphanumeric modes, the M1D3 signal (bit 3 of the attribute byte) normally controls the foreground intensity on/off function. This bit, however, may be redefined as a switch between character sets. This function is enabled when there is a difference between the value in Char Bank Select A and Char Bank Select B. Whenever these two modes are the same, the character select function is disabled. The memory mode register bit 1 must be set high (indicating a full 256K of screen RAM), otherwise Bank 0 will be the only Bank selected, even if non-zero values are in this register.
The Async Reset clears this register. async Reset should only be done during a system reset.

**SCBS BIT 4-7:** Not used.

**SEQUENCER MEMORY MODE REGISTER (SMMR)**

This is a write only register accessed with an Index Value of 04 Hex.

**SMMR BIT 0:** Not used.

**SMMR BIT 1:**
Extended Memory.
0 = Expansion memory card is not installed
1 = Expansion memory card is installed and enables access to memory through address bits 14 and 15.

**SMMR BIT 2:**
Odd/Even.
0 = Directs Even processor addresses to access maps 0 and 2, while Odd CPU addresses access maps 1 and 3.
1 = access data sequentially within a bit map. The maps are accessed according to the value in the map mask register.

**SMMR BIT 3-7:** Not used.

**GRAPHICS CONTROLLER REGISTER (GCR)**

This is a write only register, and IOG must be high to allow further address decoding externally. IOW is the data strobe.

| Description | Port Address | Index |
|---|---|---|
| Graphics 1 pos. | CC | |
| Graphics 1 pos. | CE | |
| Mode Register | CF | 05 |
| Miscellaneous | CF | 06* |

* Position dependent register, data written to this register will be invalid if wrong values are written to the Graphics 1 position register.

### GRAPHICS 1 POSITION REGISTER (G1PR)

**G1PR BIT 0-1:**
Position Address.
These 2 bits are binary encoded hierarchy bits for the graphics controller 1 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 00 Hex for correct EGA operation.

**G1PR BIT 2-7:** Not used.

### GRAPHICS 1 INDEX REGISTER (G1IR)

The processor port address for this register is 3CF Hex.

**G1IR BIT 0-3:**
Register Index.
The value written into this register is used to access the remaining registers in the Graphics 1 section.

**G1IR BIT 4-7:** Not used.

### GRAPHICS CONTROLLER MODE REGISTER (GCMDR)

This is a write only register and is accessible when the value in the Graphics 1 Index Register is 05 Hex. The processor port address for this register is 3CF Hex.

**GCMDR BIT 0-1:** Not used.

**GCMDR BIT 2:**
Test Condition.
0 = Normal.
1 = Forces the Graphics and Chain internal signal to a logic "1".

**GCMDR BIT 3-7:** Not used.

### GRAPHICS CONTROLLER MISCELLANEOUS REGISTER (GCMSR)

This is a write only register and is accessible when the value in the Graphics 1 Index Register is 06 Hex.

**GCMSR BIT 0:**
Graphics Mode.This bit controls alpha mode addressing.
0 = Normal.
1 = Selects Graphics mode addressing, which disables the character address latches, and sends identical addressing to both AA0-7 and BA0-7 Hex busses.

**GCMSR BIT 1:**
Chain Odd to Even.
0 = Normal.
1 = Directs the processor address bit 0 to be replaced by higher order bit. Odd/Even planes will be selected by the value of the processor A0 bit.

**GCMSR BIT 2-7:** Not used.

### LIGHT PEN CLEAR (LPC)

This is a write only register that is used to clear the light pen input latch. Data written is ignored, so anything can be written. This register is accessed when IOG is High, DB Hex is on the A0-7 bus, and IOW is strobed.

### LIGHT PEN SET (LPS)

This write only register is used to set the light pen input latch. Data written is ignored, so anything can be written. This register is accessed when IOG is high, DC Hex is on the A0-7 bus, and IOW is strobed.

### CRT CONTROLLER INDEX REGISTER (CCIR)

The CRT Controller Index Register is a pointer register at the addresses 3B0, 3B2, 3B4 and 3B6 Hex in Monochrome modes, and 3D0, 3D2, 3D4 and 3D6 Hex in Color modes. This is a write only register.

**CCIR BIT 0-4:**
Index.
The binary coded value written to this register defines the address of the actual control register to be accessed.

**CCIR BIT 5-7:** Not used.

### CRT CONT. HORIZ. TOTAL REGISTER (CCHTR)

This write only register is accessed when the value written to the CRT Controller Index Register is 00 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5 and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCHTR BIT 0-7:**
Horizontal total.
This register sets the total number of character fetches in a horizontal scan period, including both active and blanked times. This register directly controls the horizontal scan frequency that is set to the CRT display. The value loaded in this register should be the total number of fetches desired less 2.

### CRT CONT. HORIZ. DISPLAY ENABLE END REGISTER (CCHDER)

This is a write only register accessed when the value written to the CRT Controller Index Register is 01 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCHDER BIT 0-7:**
Horizontal enable end.
This register defines the length of the the horizontal display enable function, which determines the number of characters (or pels) that are displayed horizontally. The value written here should be one less that the desired number of characters to be displayed.

### CRT CONT. START HORIZ. BLANKING REGISTER (CCSHR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 02 Hex. The addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCSHR BIT 0-7:**
Start horizontal blanking register.
This register controls when the Horizontal Blanking signal goes active. The Horizontal Blanking signal goes active when the Horizontal character count is equal to the value in this register. The underline scan line output is multiplexed on the CURSOR output pin, and will be active for one character clock cycle beyond the end of the blanking signal.

### CRT CONT. END HORIZ. BLANKING REGISTER (CCEHR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 03 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCEHR BIT 0-4:**
End horizontal blanking.
These 5 bits control the length of the Horizontal Blanking signal in character clock increments. The value to be loaded into this register should be equal to the number of clock cycles to be blanked added to the value of the five least significant bits of the Start Horizontal Blanking register.

**CCEHR BIT 5-6:**
Display enable skew control.
These bits determine the amount of the skew in the Display Enable signal. Skew control is required to provide enough time for the CRT Controller to access the Display Buffer for a character and attribute code, access the font plane, and go through the Horizontal Panning register (in Attribute Controller section) to the character shift registers in the Attribute Controller section. Each alpha mode access requires that the Display Enable signal be skewed by one character cycle so that the video is properly aligned with the horizontal and vertical sync signals. Skew Control encoding is a follows:

| BIT-6 | BIT-5 | |
|---|---|---|
| 0 | 0 | Zero character clock skew |
| 0 | 1 | One character clock skew |
| 1 | 0 | Two character clock skew |
| 1 | 1 | Three character clock skew |

**CCEHR BIT 7:** Not used.

### CRT CONT. START HORIZ. RETRACE REGISTER (CCSRR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 04 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCSRR BIT 0-7:**
Start horizontal retrace.
This register controls the time that the horizontal sync signal goes active. Varying this value can be used to center the image on the screen. The value loaded to this register must be equal to the character clock value at which the signal should go active.

## END HORIZ. RETRACE REGISTER (EHRR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 05 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**EHRR BIT 0-4:**
End horizontal retrace.
These 5 bits control the duration of the HSYNC signal. The value written to this register should be equal to the desired length of the HSYNC pulse (in character clock cycles) added to the 5 least significant bits of the Start Horizontal Retrace Register.

**EHRR BIT 5-6:**
Horizontal retrace delay.
These bits control the skew of the horizontal sync signal (HSYNC) in character clock cycle increments. The 2 bit value is binary encoded, and writing a 00 Hex will cause the CRT Controller to produce an HSYNC with a skew of zero character clock cycle.

**HERR BIT 7:**
Start Odd memory address.
This bit controls whether the first screen memory fetch after a horizontal retrace is from an Even or an Odd address. This bit can be useful in horizontal panning applications. Normally it should be set to "0".
0 = Even address
1 = Odd address

## CRT CONT. VERTICAL TOTAL REGISTER (CCVTR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 06 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCVTR BIT 0-7:**
Vertical total.
This register is used to control the total number of horizontal lines that are scanned during a vertical frame, including both active and blanked times. The value used is a 9 bit value. The 8 LSB's are written to this register, and the MSB is written to bit 0 of the CRT Controller Overflow Register. This register determines the Vertical Scan Frequency sent to the Crt display.

## CRT CONTROLLER OVERFLOW REGISTER (CCOR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 07 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCOR BIT 0-5:**
Overflow.
This register contains the 9th bit (MSB's) for the listed control registers. The bits are used in conjunction with the registers to control their functions using 9 bits.

**CCOR BIT 0:** Vertical Total Bit 8.
**CCOR BIT 1:** Vertical Display Enable End Bit 8.
**CCOR BIT 2:** Vertical Retrace Start Bit 8.
**CCOR BIT 3:** Start Vertical Blank Bit 8.
**CCOR BIT 4:** Line Compare Bit 8.
**CCOR BIT 5:** Cursor Location Bit 8.

**CCOR BIT 6-7:** Not used.

## CRT CONT. PRESET ROW SCAN REGISTER (CCPSR)

This is a write only register accessed when the value written to the CRT Controller Index Register is 08 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCPSR BIT 0-4:**
Preset row scan.
This register is used to control the starting row scan count after a vertical retrace. The row scan counter is incremented each horizontal retrace time, until a maximum row scan occurs. This register is useful for doing smooth scrolling in alphanumeric modes.

**CCPSR BIT 5-7:** Not used.

**CRT CONT. MAXIMUM SCAN LINE REGISTER (CCMSR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 09 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCMSR BIT 0-4:**
Maximum scan line.
This register controls the number of scan lines per character row. The value to be written must be the character cell height (in lines) minus one.

**CCMSR BIT 5-7:** Not used.

**CRT CONT. CURSOR START REGISTER (CCCSR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 0A Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCCSR BIT 0-4:**
Cursor start.
This register controls which row within the character cell is where the cursor is to begin. The value to be written must be one less than the desired row number.

**CCCSR BIT 5-7:** Not used.

**CRT CONT. CURSOR END REGISTER (CCER)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 0B Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCER BIT 0-4:**
Row scan cursor end.
These bits are used to control the location within the character cell where the cursor goes inactive. The value written here should be equal to the character cell row number desired.

**CCER BIT 4-6:**
Cursor skew.
These 2 bits control the amount of skew (in character clock cycles) in the cursor signal. This values affects only the cursor and not the underline function, which is multiplexed on the same CURSOR line. Encoding for these bits is as follows:

| BIT-6 | BIT-5 | |
|---|---|---|
| 0 | 0 | Zero character clock cycle |
| 0 | 1 | One character clock cycle |
| 1 | 0 | Two character clock cycle |
| 1 | 1 | Three character clock cycle |

**CCER BIT 7:** Not used.

**CRT CONT. START ADDRESS HIGH REGISTER (CSHR)**

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0C Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CSHR BIT 0-7:**
Start address high
This register contains the 8 high-order bits of a 16 bit value indicating the first address fetched from screen memory after a vertical retrace.

**CRT CONT. START ADDRESS LOW REGISTER (CCSLR)**

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0D Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCSLR BIT 0-7:**
Start address low.
This register contains the 8 low-order bits of a 16 bit value indicating the first address fetched from screen memory after a vertical retrace.

**CRT CONT. CURSOR LOC. HIGH REGISTER (CCLHR)**

This is a read/write register accessed when the value

written to the CRT Controller Index Register is 0E Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCLHR BIT 0-7:**
Cursor location high.
This register contains the 8 high-order bits of a 16 bit value indicating the cursor location as referenced to the screen memory address. This allows hardware panning and scrolling through the screen memory while the cursor remains in the same location.

**CRT CONT. CURSOR LOC. LOW REGISTER (CCLLR)**

This is a read/write register accessed when the value written to the CRT Controller Index Register is 0F Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCLLR BIT 0-7:**
Cursor location low.
This register contains the 8 low-order bits of a 16 bit value indicating the cursor location as referenced to the screen memory address. This is used together with the CRT Controller Cursor Location Low Register.

**CRT CONT. VERTICAL RETRACE START REGISTER (CCVRR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 10 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCVRR BIT 0-7:**
Vertical retrace start.
This register is the lower 8 bits of the 9 bit value controlling the start of the Vertical Sync (VSYNC signal). This value is in horizontal scan lines. The 9th bit (MSB) of this value is written to bit 2 of the CRT Controller Overflow Register.

**CRT CONT. LIGHT PEN HIGH REGISTER (CLHR)**

This is a read only register accessed when the value written to the CRT Controller Index Register is 10 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CLHR BIT 0-7:**
Light pen high.
This register contains the 8 MSB's of the screen memory address being fetched when the LPEN input is triggered.

**CRT CONT. VERTICAL RETRACE END REG. (CVRER)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 11 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CVRER BIT 0-3:**
Vertical retrace end.
These 4 bits determine the duration of the vertical sync signal (VSYNC output). The value written must equal the duration of the sync (in number of horizontal lines) added to the 4 LSB's of the Start Vertical Retrace Register.

**CVRER BIT 4:**
Vertical interrupt.
0 = Disable the vertical interrupt
1 = Enable the vertical interrupt

**CVRER BIT 5:**
Enable vertical interrupt output.
0 = Enable the vertical interrupt output
1 = Disable the vertical interrupt output

**CVRER BIT 6:**
Functional test mode.
0 = Normal operation
1 = Test mode

**CVRER BIT 7:** Not used.

**CRT CONT. LIGHT PEN LOW (CCLPL)**

This is a read only register accessed when the value written to the CRT Controller Index Register is 11 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCLPL BIT 0-7:**
Light pen.
This register contains the 8 LSB's of the screen memory address being fetched when the LPEN input is triggered.

**CRT CONT. VERT. DISPLAY ENABLE END REG. (CVDEG)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 12 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CVDEG BIT 0-7:**
This register has the lower 8 bits of the 9 bit value defining the location (in number of horizontal screen lines) where the vertical display enable goes inactive. The MSB of this value is in bit 1 of the CRT Controller Overflow Register.

**CRT CONTROLLER OFFSET REGISTER (COR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 13 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**COR BIT 0-7:**
This register controls the logical line width of the display memory. The value written to this register controls the address offset of the character or pel directly beneath any other pixel. Depending on the clocking method selected, the address may be either a word or double word address.

**CRT CONT. UNDERLINE LOC. REGISTER (CCULR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 14 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CCULR BIT 0-4:**
This register controls the line within the character cell where an underline will appear. The value in this register must be one less than the screen line desired.

**CCULR BIT 5-7:** Not used.

**CRT CONT. START VERT. BLANKING REG. (CSVBR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 15 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CSVBR BIT 0-7:**
This register contains the 8 LSB's of a 9 bit value describing the horizontal screen line count at which the vertical blanking function goes active. The MSB is in bit-3 of the CRT Controller Overflow Register.

**CRT CONT. END VERT. BLANKING REG. (CEVBR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 16 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CEVBR BIT 0-4:**
This register controls the vertical blanking duration by setting the screen count value for when the vertical blank output becomes inactive. The value to be written here should be the desired blanking width (in horizontal lines) added to the bottom 5 bits of the value in the Start Vertical Blanking Register.

**CRT CONT. MODE CONTROL REGISTER (CMCR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 17 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CMCR BIT 0:**
Compatibility mode support .
0 = Row scan counter bit-0 is substituted for memory address bit 13, allowing compatibility with CGA's method of addressing screen memory.
1 = Normal.

**CMCR BIT 1:**
Select row scan count.
0 = Selects row scan counter bit-1 as address bit 14 for

the screen referesh address bus.
1 = Select address counter bit-14.

**CMCR BIT 2:**
Horizontal retrace select.
This selects either horizontal retrace or horizontal retrace divided by two as the clock that increaments the vertical resolution of the CRTC, since the 9 bit vertical timing counter can only operate up to 512 counts. By selecting the count by two option, the vertical displayed resolution can be doubled to 1024 lines.
0 = Selects horizontal retrace.
1 = Selects horizontal retrace divided by two.

**CMCR BIT 3:**
Count by two.
This bit controls the incrementing of the address counter.
0 = Increment address counter with every character clock cycle.
1 = Increment address counter with every second character cycle.
This is used to generate either a byte or word address for the screen memory.

**CMCR BIT 4:**
Output control.
0 = Enable HSYNC, VSYNC, CURSOR, and BLANK outputs.
1 = Set HSYNC, VSYNC, CURSOR, and BLANK outputs to three state.

**CMCR BIT 5:**
Address wrap.
This bit selects the memory address counter bit 13 or 15 to appear on the memory address bus as the LSB (A0) during Word Mode. If not in Word Mode, the state of this bit has no effect.
0 = Set for 64K configuration.
1 = Set for 256K configuration.

**CMCR BIT 6:**
Word/Byte mode.
0 = Word mode. This causes the memory address conter bits to be shifted down one bit on the memory address bus, With the MSB of the counter appearing on the new LSB of that address bus.
1 = Byte mode.

**CMCR BIT 7:**
Hi-resolution.
0 = Clear the horizontal and vertical traces.
1 = Enable the horizontal and vertical timing counters.

**CRT CONT. LINE COMPARE REGISTER (CLCR)**

This is a write only register accessed when the value written to the CRT Controller Index Register is 18 Hex. the addresses that may be used to access this register are 3B1, 3B3, 3B5, and 3B7 Hex in Monochrome modes, and 3D1, 3D3, 3D5, and 3D7 Hex in Color modes.

**CLCR BIT 0-7:**
This register is used to implement a split-screen function. When the vertical counter reaches this value, the address counters are cleared. Thus allowing a section of the screen to be immune to scrolling. The value loaded to this register is the 8 LSB's of a 9 bit value. The MSB is bit-4 of the CRT Controller Overflow register.

**ATTRIBUTE CONTROL REGISTERS**

| Description | Decode Pin | Index |
|---|---|---|
| Index reg. | ATRIOW | |
| Mode Cont. | ATRIOW | 10 or 30 Hex |
| Color Plane Enable | ARRIOW | 12 or 32 Hex |

**ATTRIBUTE CONTROL INDEX REGISTER (ACIR)**

This is a write only register

**ACIR BIT 0-4:**
Attribute register index value.
This address register is a pointer register accessed when ATRIOW is low. This register is loaded with a binary value that points to the attribute data register where data is to be written. The Attribute Controller does not have an address bit input to control selection of the Index and Data registers. Instead, the input mode toggles between Index Register and Data Register access modes on alternate accesses. To reset the Input mode to the Index Register, the STRIOR pin should be strobed active (low).

**ACIR BIT 5:**
Palette address source.
0 = To load color palette register.
1 = To enable the screen data to access the color palette.

**ACIR BIT 6-7:** Not used.

**ATTRIBUTE CONT. MODE CONTROL REG. (ACMCR)**

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 10 or 30 Hex before writing can take place. The processor output port for this register is 3C0 Hex.

**ACMCR BIT 0:**
Graphics/Alpha mode.
0 = Alphanumeric mode.
1 = Graphics mode.

**ACMCR BIT 1:** Not used.

**ACMCR BIT 2:**
Line graphics.
0 = The 9th column dot will be the same color as the background.
1 = Enables the special line graphics character codes for IBM Monochrome Display Adapter. Sets the 9th column dot of a line graphics character code to the same color as the 8th column dot of the character. The line graphics character codes are C0 through DF Hex.

**ACMCR BIT 3:**
Blank enable.
0 = Selects the background intensity of the attribute input. This mode was available on the MDA and CGA.
1 = Enable the blink attribute in alphanumeric or graphics modes.

**ACMCR BIT 4-7:** Not used.

**ATTRIBUTE CONT. COLOR PLANE ENABLE REG. (ACPER)**

This is a write only register pointed to by the value in the Attribute Index Register. The value must be either 12 or 32 Hex before writing can take place. The processor output port for this register is 3C0 Hex.

**ACPER BIT 0-3:** Not used.

**ACPER BIT 4:**
Video status mux 0.
0 = Resume counting operation. This does not enable the blinking function it only enables the blinking counters.
1 = Clear the blink counter and stop counting.

**ACPER BIT 5-7:** Not used.

**GRAPHICS CONT. GRAPHICS 1 POSITION REG. (GC1PR)**

This is a write only register. The processor output port address for this register is 3CC Hex.

**GC1PR BIT 0-1:**
These 2 bits are binary encoded hierarchy bits for the graphics controller 1 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 00 Hex for correct EGA operation.

**GC1PR BIT 2-7:** Not used.

**GRAPHICS CONT. GRAPHICS 2 POSITION REG. (GC2PR)**

This is a write only register. The processor output port address for this register is 3CA Hex.

**GC2PR BIT 0-1:**
These 2 bits are binary encoded hierarchy bits for the graphics controller 2 section. The position register controls which 2 bits of the processor data bus the section responds to. This register must be programmed with a value of 01 Hex for correct EGA operation.

**GC2PR BIT 2-7:** Not used.

**GRAPHICS CONT. GRAPHICS 1 & 2 INDEX REGISTER (GC12R)**

This is a write only register.

**GC12R BIT 0-3:**
The value written into this register is used to access the remaining registers in the graphics 1 & 2 section.

**GC12R BIT 4-7:** Not used.

**GRAPHICS CONT. SET/RESET REGISTER (GSRR)**

This is a write only register pointed to by the value in the Graphics Controller 1 and 2 Index Register. The value must be 00 Hex before writing can take place.

**GSRR BIT 0-3:**
These bits represent the value written to the respective memory planes when the processor does a memory write with write mode "0" selected and set/reset enabled. Set/Reset can be enabled on a plane by

plane basis by using the Enable Set/Reset Register.
0 = Reset
1 = Set

**GSRR BIT 4-7:** Not used.

**GRAPHICS CONT. ENABLE SET/RESET REG. (GSERR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 01 Hex.

**GSERR BIT 0-3:**
These bits enable the Set/Reset function for the respective memory planes. When high, the data in the respective Set/Reset bits are written into the memory. When low, processor data is written directly to memory for those bit locations. The Set/Reset function only works in write mode 00 Hex.

**GSERR BIT 4-7:** Not used.

**GRAPHICS CONT. COLOR COMPARE REG. (GCCR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 02 Hex.

**GCCR BIT 0-3:**
These bits represent a 4 bit (one per plane) color to be compared. If read mode "1" is selected, the data returned from a memory read operation will contain a "1" in each bit position where the memory data in each plane is equal to the value in this register.

**GCCR BIT 4-7:** Not used.

**GRAPHICS CONTROLLER DATA ROTATE REG. (GCDRR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 03 Hex.

**GCDRR BIT 0-3:**
Rotate count.
The value written to these locations will determine the number of bit data will be shifted left during write mode "0" memory write operations.

**GCDRR BIT 3-4:**
Function select.
Data written to memory can operate logically with data already in the processor latches. Data may be any of the choices selected by the Write Mode Register except processor latches. If rotated data is selected, the rotate applies before the logical function. The function codes are defined as follows:

| BIT-4 | BIT-3 | |
|---|---|---|
| 0 | 0 | Data unmodified |
| 0 | 1 | Data AND'ed with latched data |
| 1 | 0 | Data OR'ed with latched data |
| 1 | 1 | Data XOR'ed with latched data |

**GCDRR BIT 5-7:** Not used.

**GRAPHICS CONT. READ MAP SELECT REG. (GRMSR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 04 Hex.

**GRMSR BIT 0-2:**
Map select 0-2.
These bits represent an encoded value of the memory plane number from which the processor will read data. This register has no effect on the color compare read mode operation.

**GRMSR BIT 3-7:** Not used.

**GRAPHICS CONTROLLER MODE REGISTER (GCMR)**

**GCMR BIT 1-0:**
Write Mode.
00 = Write Mode "0", each of the 4 planes is written with the CPU date rotated left by the value in the Rotate Register. This is always true, except when the Set/Reset Register in enabled, in which case that plane would be written by the nono-rotate value in the Set/Reset Register.
01 = Write Mode "1", each plane is written with the data read from the planes by the previous memory read operation.
10 = Write Mode "2", memory planes 0-3 are filled with the values of data bits 0-3 respectively.
11 = Non valid condition.

**GCMR BIT 2:**
Test condition.
0 = Normal.
1 = Set internal signals of C0-3, Graphics, and Chain to logic "1".

**GCMR BIT 3:**
Read Mode.
0 = Normal memory read.
1 = Results of color compare operation (memory read cycles).

**GCMR BIT 4:**
Odd/Even.
0 = Normal
1 = Select the Odd/Even addressing mode, used for CGA emulation modes.

**GCMR BIT 5:**
Shift register mode.
0 = Normal.
1 = Direct the shift registers in each graphics section to format the serial stream with even numberd bits to the even numbered maps and odd numbered bits to the odd numbered maps.

**GCMR BIT 6-7:** Not used.

**GRAPHICS CONT. MISCELLANEOUS REG. (GCMSR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 06 Hex.

**GCMSR BIT 0:**
Graphics Mode.
0 = Alphanumeric mode.
1 = Graphics mode addressing, which disables the character address latches, and sends identical addressing to both AA0-7 and BA0-7 busses.

**GCMSR BIT 1:**
Chain Odd/Even.
0 = Normal.
1 = Direct the processor address bit-0 to be replaced by a higher order bit. Odd/Even planes will be selected by the value of the processor A0 bit.

**GCMSR BIT 2:**
Memory Map "0". Controls CDSEL0 output.

**GCMSR BIT 3:**
Memory Map "1". Controls CDSEL1 output.

**GCMSR BIT 4-7:** Not used.

**GRAPHICS CONT. COLOR DON'T CARE REG. (GCCDR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 07 Hex.

**GCCDR BIT 0-3:**
Plane 0-3 don't care.
0 = Normal.
1 = A color compare read operation will yield a "1" regardless of the actual comparison result.

**GCCDR BIT 4-7:** Not used.

**GRAPHICS CONT. BIT MASK REGISTER (GCBMR)**

This is a write only register and is accessible when the value in the Graphics 1 & 2 Index Register is 08 Hex.

**GCBMR BIT 0-7:**
0 = Corresponding bit in each bit plane to be immune to change provided that the location being written was the last location read by the processor.
1 = Unimpeded modification to the appropriate bits in all planes.

## LD1002 PINOUT