

HD64570 (SCA)

Serial Communications Adapter

Description

The HD64570 Serial Communications Adapter (hereinafter referred to as SCA) is a high-speed, high-performance data communication controller providing efficient, high-performance communication protocol processing at low cost.

The SCA incorporates powerful key functions such as a two-channel multiprotocol serial communications interface (MSCI), a four-channel direct memory access controller (DMA controller) with chained-block transfer function, and a four-channel timer. The built-in MSCI, supporting various communication protocol modes such as asynchronous, byte synchronous, and bit synchronous modes, allows serial communications using protocols such as HDLC. In addition, the SCA supports four types of 8/16-bit bus interfaces, allowing a direct interface with the host MPU. This bus interface capability combined with 32-byte deep receive and transmit FIFOs in the MSCI can provide high throughput for many communication systems. Accordingly, the SCA can be widely adopted to a computer communication controller that requires multi-channel serial communications, PBXs, and office automation equipment such as personal computers and facsimiles.

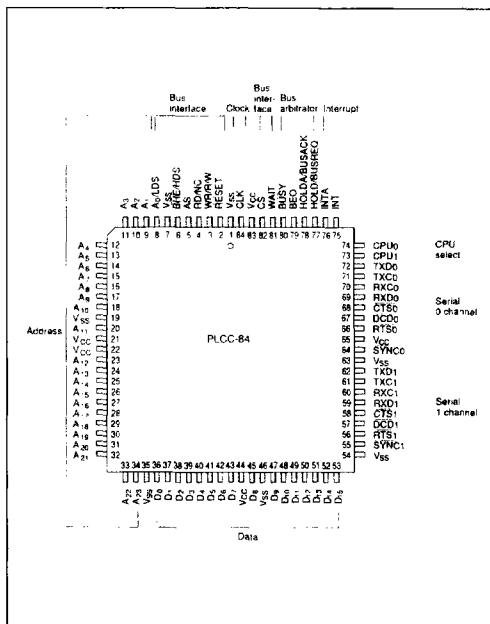
*For details about HD64570 specifications, please refer to "HD64570 SCA User's Manual" (Order Number M50T007).

SCA Features

- Multiprotocol Serial Communications Interface (MSCI)
 - Two full duplex channels
 - Asynchronous, byte synchronous (mono-sync, bi-sync, or external synchronous), or bit synchronous (HDLC or loop) modes
 - 32-byte deep for both receive and transmit buffers
 - Transmission and reception control using modem control signals (RTS, CTS, and DCD)
 - Advanced digital PLL (ADPLL) function
 - Clock extraction
 - Noise suppression for receive data and receive clock
 - Baud rate generator
 - Interrupt request
 - Maximum transfer rate: 7.1 Mbps ($f = 10 \text{ MHz}$)
- Direct Memory Access Controller (DMA Controller)
 - Four channels
 - DMA transfer between memory and built-in MSCI
 - Chained block transfer in bit synchronous mode
 - Programmable channel priority
 - Programmable bus release and channel switch conditions

- Timer
 - Four channels
 - 16-bit reloadable upcounter timer
 - Interrupt request
- Wait State Controller
 - Wait state control using an external pin or software
- Interrupt Controller
 - Interrupt request to the MPU
 - 20 interrupt sources
 - Programmable acknowledge cycle
- Bus Arbitrator
 - Bus arbitrator between the built-in DMA controller and external bus masters
 - Multiple serial channels realized by daisy chain structure
- Bus Interface
 - HD641016, HD64180, and other two other types of 16-bit bus interfaces available by mode switching through external pins
 - 8-bit or 16-bit programmable bus width
 - Byte swap function
 - 16 Mbytes of address space
- Maximum operation frequency
 - 10 MHz
- Package
 - CP-84 (84-pin PLCC)

SCA Pin Arrangement



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



Table 2-1 CP-84 Pin Configuration

Pin No.	Pin Name				Pin No.	Pin Name			
	CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3		CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3
1	V _{SS}				43	D ₇			
2	RESET				44	V _{CC}			
3	WR	WR	R/W	R/W	45	D ₈			
4	RD	RD	N.C.	N.C.	46	V _{SS}			
5	AS				47	D ₉			
6	BHE	N.C.	HDS	HDS	48	D ₁₀			
7	V _{SS}				49	D ₁₁			
8	A ₀	A ₀	LDS	LDS	50	D ₁₂			
9	A ₁				51	D ₁₃			
10	A ₂				52	D ₁₄			
11	A ₃				53	D ₁₅			
12	A ₄				54	V _{SS}			
13	A ₅				55	SYNC1			
14	A ₆				56	RTS1			
15	A ₇				57	DCD1			
16	A ₈				58	CTS1			
17	A ₉				59	RxD1			
18	A ₁₀				60	RxC1			
19	V _{SS}				61	TxC1			
20	A ₁₁				62	TxD1			
21	V _{CC}				63	V _{SS}			
22	V _{CC}				64	SYNC0			
23	A ₁₂				65	V _{CC}			
24	A ₁₃				66	RTS0			
25	A ₁₄				67	DCD0			
26	A ₁₅				68	CTS0			
27	A ₁₆				69	RxD0			
28	A ₁₇				70	RxC0			
29	A ₁₈				71	TxC0			
30	A ₁₉				72	TxD0			
31	A ₂₀				73	CPU1			
32	A ₂₁				74	CPU0			
33	A ₂₂				75	INT			
34	A ₂₃				76	INTA			
35	V _{SS}				77	HOLD	BUSREQ	BUSREQ	BUSREQ
36	D ₀				78	HOLDA			
37	D ₁				79	BEO			
38	D ₂				80	BUSY			
39	D ₃				81	WAIT			
40	D ₄				82	CS			
41	D ₅				83	V _{CC}			
42	D ₆				84	CLK			

Note: Refer to section 2.2, Pin Functions, for details on CPU modes.

2.2 Pin Functions

The SCA pin functions are summarized in table 2-2.

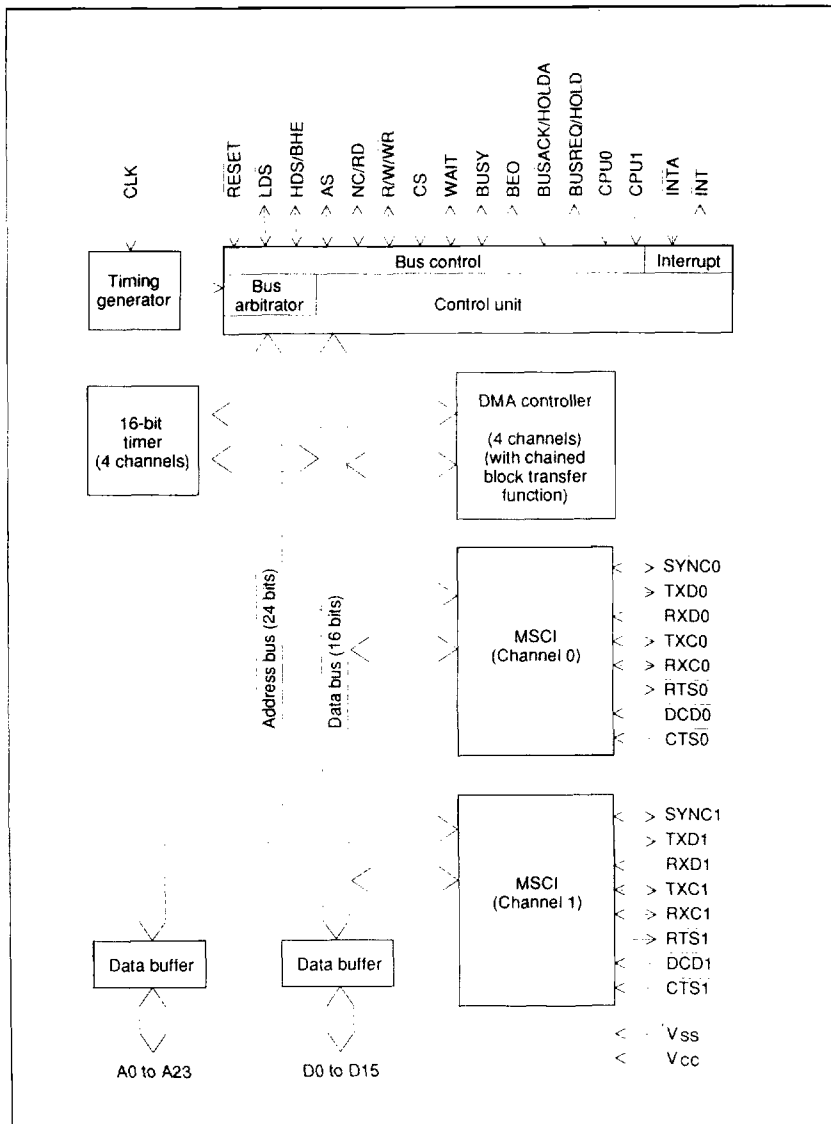
Table 2-2 SCA Pin Functions

Type	Symbol	I/O	Function
Power supply	V _{CC}	I	Power supply
	V _{SS}	I	Ground
Clock	CLK	I	System clock
Reset	RESET	I	Reset
Address bus	A ₀ to A ₇	I/O	Address bus
	A ₈ to A ₂₃	O	Address bus
Address bus	D ₀ to D ₁₅	I/O	Data bus
Bus interface	\overline{RD}	I/O	Read
	\overline{WR}	I/O	Write
	$\overline{R/W}$	I/O	Read/write
	\overline{HDS}	I/O	Higher data strobe
	\overline{LDS}	I/O	Lower data strobe
	\overline{BHE}	I/O	Higher byte access strobe
	WAIT	I/O	Wait request
	CS	I	Chip select
	AS	I/O	Address strobe
System control	BUSREQ	O	Bus request
	BUSACK	I	Bus request acknowledge
	HOLD	O	Hold request
	HOLDA	I	Hold request acknowledge
	BEO	O	Bus enable
	BUSY	I/O	Bus busy
	CPU0, CPU1	I	Bus interface mode selection (Refer to table 2-3.)
Interrupt	INT	O	Interrupt request
	INTA	I	Interrupt request acknowledge
MSCI	TXD0, TXD1	O	Transmit data
	RXD0, RXD1	I	Receive data
	TXC0, TXC1	I/O	Transmit clock
	RXC0, RXC1	I/O	Receive clock
	RTS0, RTS1	O	Modem control (\overline{RTS})
	DCD0, DCD1	I	Modem control (\overline{DCD})
	CTS0, CTS1	I	Modem control (\overline{CTS})
SYNC0, SYNC1	I/O	Synchronization	

Table 2-3 CPU Mode (Bus Interface Mode) Selection by CPU0 and CPU1

CPU0	CPU1	CPU Mode
0	0	Mode 0 (80 series 16-bit CPU)
0	1	Mode 1 (HD64180)
1	0	Mode 2 (HD641016)
1	1	Mode 3 (68 series 16-bit CPU)

SCA Block Diagram



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