

# TC9807P, TC9807FW

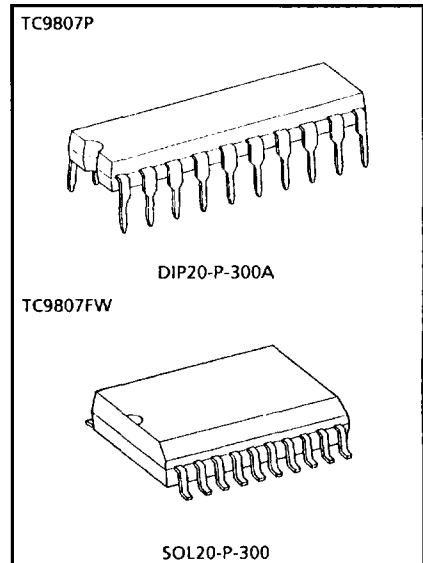
## TENTATIVE DATA

TC9807 is a 20-pin CMOS programmable logic device (PLD) based on EEPROM cells. It has a zero-standby function. Designed using Toshiba's original technology, this device features low power dissipation and inputs that are compatible with TTL, NMOS, and CMOS output voltage levels.

The device functions as a dedicated address coder, based on an AND array structure.

### FEATURES

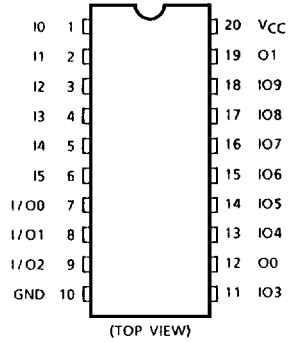
- Architecture ..... 12 AND terms  
12 exclusive OR terms
- Security cell ..... Protection of proprietary information
- Signature word ..... 12 bits for user ID code or inventory control
- High speed operation .....  $t_{pd}$  (input-output) = 11ns (Typ.)
- Low power dissipation .....  $I_{CC}$  (standby) = 4 $\mu$ A (max. @25°C)
- Wide operating voltage range ....  $V_{CC}$  = 5  $\pm$  0.25V
- Package ..... 20-pin plastic DIP (TC9807P)  
20-pin plastic SOL (TC9807FW)



Weight DIP20-P-300A : 1.30g (Typ.)  
SOL20-P-300 : 0.46g (Typ.)

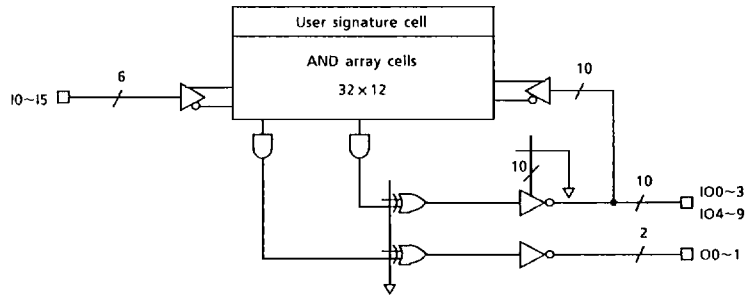
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## PIN NAMES & FUNCTIONS

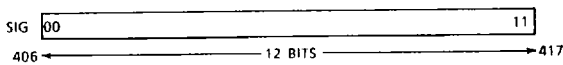
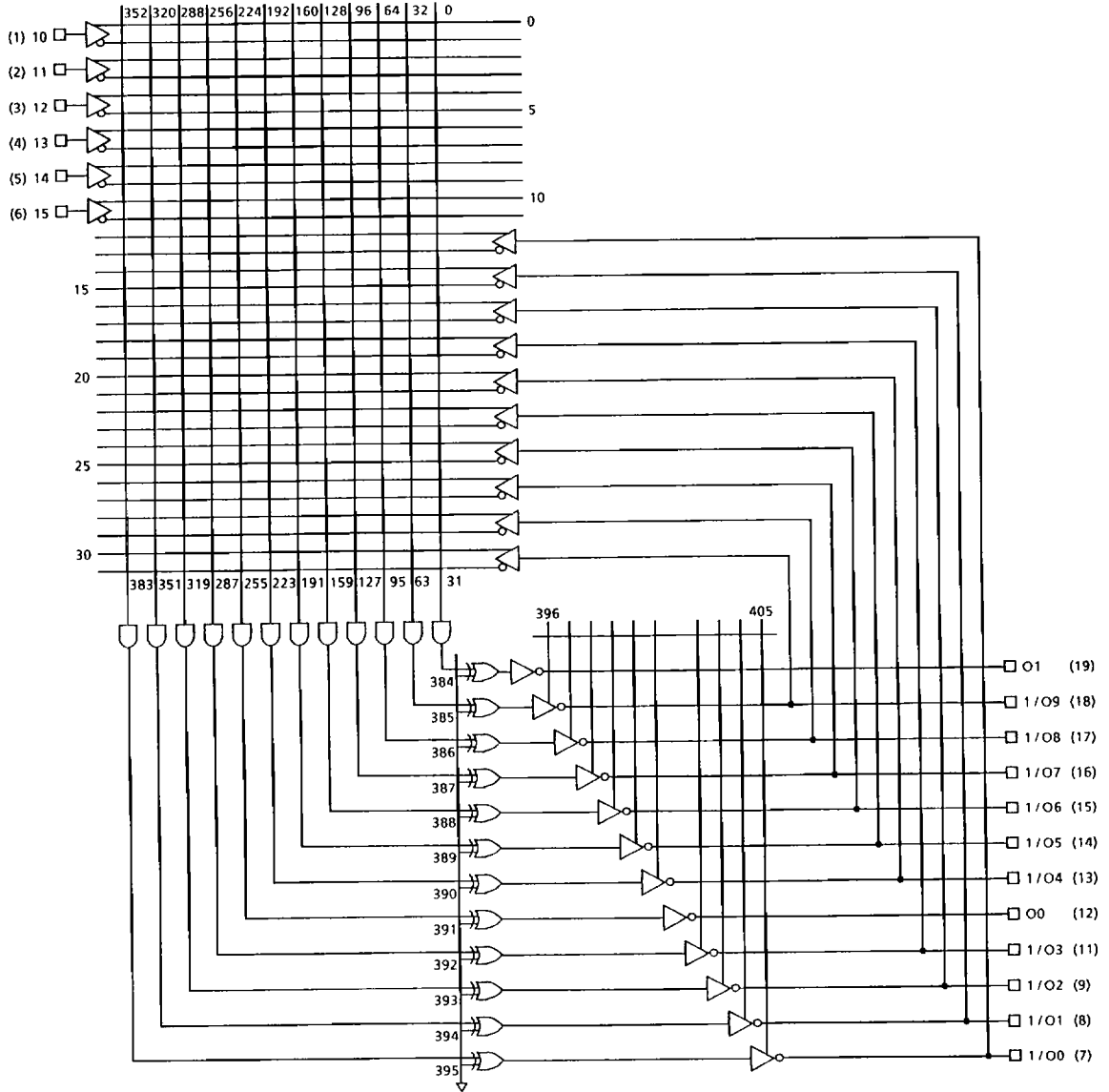


- IO~15 ..... Input only
- O0, O1 ..... Output only
- I/O0~I/O9 ..... Input/output

## FUNCTION DIAGRAM



LOGIC DIAGRAM



## ARCHITECTURE

### 1. MEMORY CELLS

Programmable memory cells are divided into the following four types : AND array, input/output control array, flag, and user signature.

Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects.

(1) AND array (32 × 12)

Programs signals used to control 10 input/outputs. Setting the program data to 1 sets input/output pins to output ; to 0 sets input/output pins to input.

(2) Input/Output control array (10)

Setting program data to 1 disconnects signals to an AND array : setting to 0 connects. Output from this array enables CMOS output (I/O0~I/O9).

(3) Flag cell

A. Output polarity selection cell .... 12 bits

B. Security cell ..... 1 bit

(4) User signature cell

User can program a 12-bit memory array for a variety of uses including ID codes, inventory control, and revision number. Programming the security bit (security cell) disables access of cells other than the signature cell.

### 2. Macro cells

(1) Output polarity of AND array

Twelve exclusive OR gates control the output polarity of the AND array. These gates are user programmable : setting program data to 1 inputs the output signal from the AND array as inverted ; setting program data to 0, as non-inverted.

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 70$	mA
Power Dissipation	$P_D$	500 (DIP) * / 300 (SOL)	mW
Storage Temperature	$T_{stg}$	-65~150	°C
Lead Temperature (10s)	$T_L$	300	°C

- \* 500mW in the range of  $T_a = -40\sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  should be applied up to 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.75~5.25	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~500 ( $V_{CC} = 5.0\text{V} \pm 0.25\text{V}$ )	ns

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## DC ELECTRICAL CHARACTERISTICS

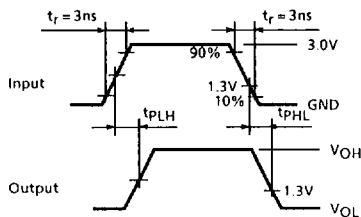
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C			Ta = -40 ~85°C		UNIT		
				V <sub>CC</sub>	MIN.	TYP.	MAX.	MIN.		MAX.	
High-level input voltage	V <sub>IH</sub>	—		5 ± 0.25	2.0	—	—	2.0	—	V	
Low-level input voltage	V <sub>IL</sub>	—		5 ± 0.25	—	—	0.8	—	0.8	V	
High-level output voltage	V <sub>OH</sub>	—	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.75	4.65	4.75	—	4.65	—	V
				I <sub>OH</sub> = -6mA	4.75	4.43	4.56	—	4.38	—	
Low-level output voltage	V <sub>OL</sub>	—	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.75	—	0.0	0.1	—	0.1	V
				I <sub>OL</sub> = 6mA	4.75	—	0.18	0.26	—	0.33	
Input leakage current	I <sub>IN</sub>	—	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.25	—	—	± 0.1	—	± 1.0	μA	
Quiescent current	I <sub>CCSB</sub>	—	V <sub>IN</sub> = V <sub>CC</sub> or GND Standby	5.25	—	—	4.0	—	40.0	μA	
Operating current	I <sub>CCOP</sub>	—	f <sub>IN</sub> = 1MHz Operating	5.25	—	—	—	—	12.0	mA	

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 25pF, Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

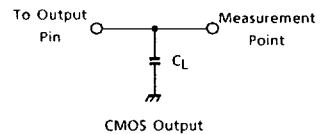
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C			Ta = -40 ~85°C		UNIT	
				V <sub>CC</sub>	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (Input, I/O-Output)	t <sub>PLH</sub> t <sub>PHL</sub>	—		5 ± 0.25	—	12.0	18.0	—	21.0	ns

### Switching Characteristic Test Waveform

1) t<sub>PD</sub> (t<sub>PLH</sub>, t<sub>PHL</sub>)



### Output Test Connection Diagram



Note)  $C_L$  includes the capacitance of probe.