

HN624316N Series

1,048,576-word × 16-bit / 2,097,152-word × 8-bit CMOS
Programmable Mask ROM

HITACHI

The HN624316N is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or as 2,097,152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8,086 and 68,000, etc.

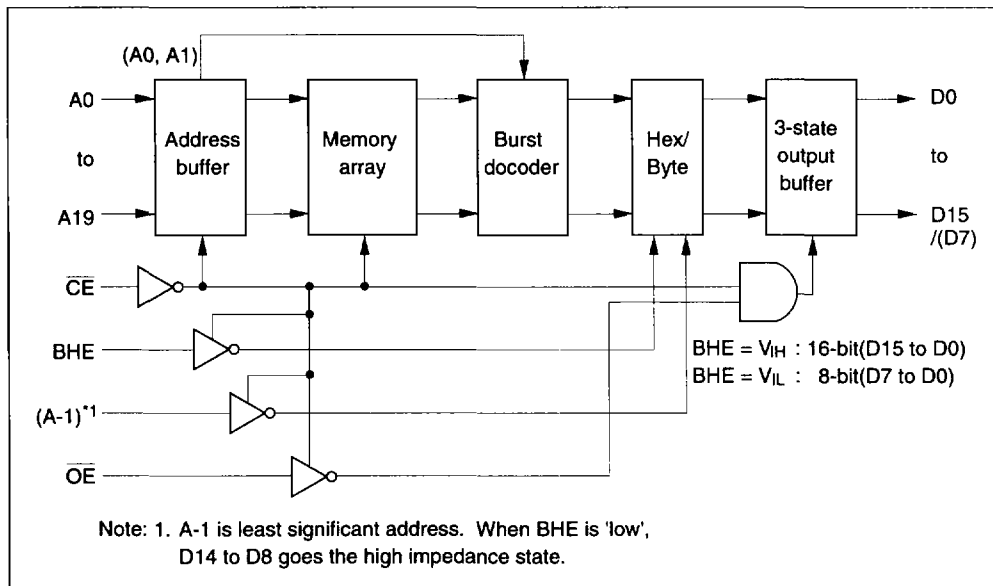
Features

- Single +5 V power supply
- Normal access time: 120 ns/150 ns (max)
- Burst access time: 60 ns/70 ns (max)
- Low power consumption: 300 mW (typ) active
5 μ W (typ) standby
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN624316NP-12	120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624316NP-15	150 ns	
HN624316NFB-12	120 ns	44-pin plastic SOP
HN624316NFB-15	150 ns	(FP-44D)
HN624316NTA-12	120 ns	48-pin plastic TSOP-II
HN624316NTA-15	150 ns	(TTP-48D)

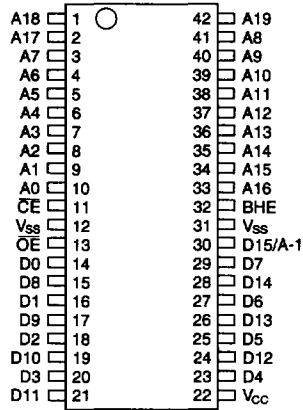
Block Diagram



HN624316N Series

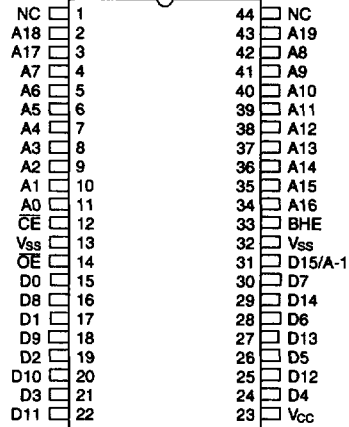
Pin Arrangement

HN624316NP



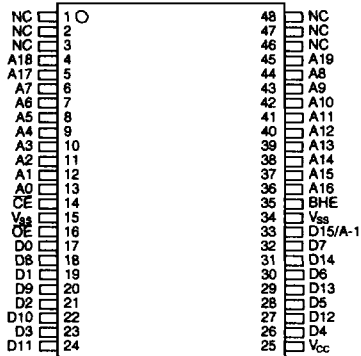
(Top view)

HN624316NFB



(Top view)

HN624316NTA



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
All input and output voltage	V_{in}, V_{out}	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature range	T_{opr}	0 to +70	°C	
Storage temperature range	T_{stg}	-55 to +125	°C	
Temperature under bias	T_{bias}	-20 to +85	°C	

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Electrical Characteristics ($V_{CC} = 5$ V \pm 10%, $V_{SS} = 0$ V, $T_a = 0$ to +70 °C)

Item	Symbol	Min	Max	Unit	Test conditions	
Supply current	Active	I_{CC}	—	120/ 110	mA	$V_{CC} = 5.5$ V, $I_{DOUT} = 0$ mA, $t_{RC} = 120$ ns/150 ns
	Standby	I_{SB1}	—	30	μ A	$V_{CC} = 5.5$ V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	$V_{CC} = 5.5$ V, $\overline{CE} \geq 2.2$ V
Input leakage current	$ I_{IL} $	—	10	μ A	$V_{IN} = 0$ to V_{CC}	
Output leakage current	$ I_{OL} $	—	10	μ A	$\overline{CE} = 2.2$ V, $V_{OUT} = 0$ to V_{CC}	
Output voltage	V_{OH}	2.4	—	V	$I_{OH} = -205$ μ A	
	V_{OL}	—	0.4	V	$I_{OL} = 1.6$ mA	

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Capacitance ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{IN} = 0\text{ V}$, $f = 1\text{ MHz}$)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

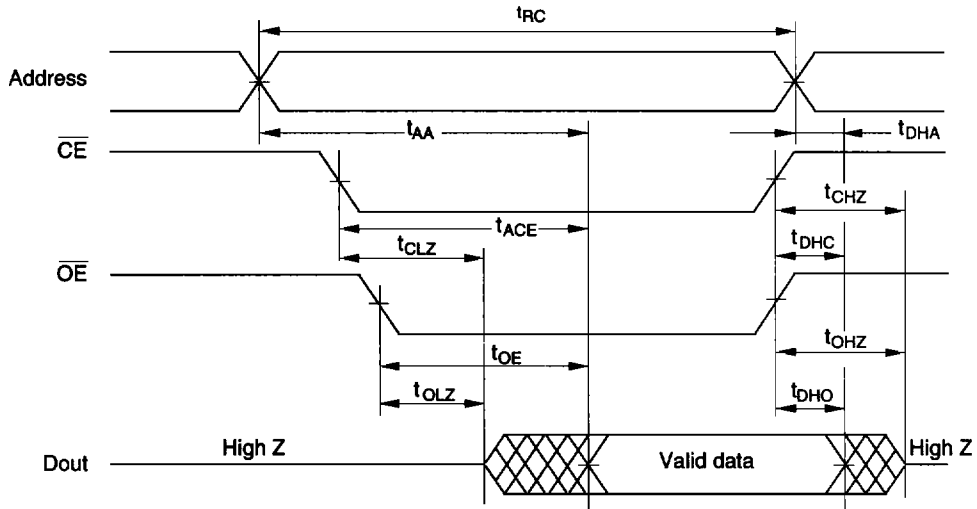
- Output load: 1TTLgate + $C_L = 100\text{ pF}$ (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

Item	Symbol	HN624316N-12		HN624316N-15		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	120	—	150	—	ns
Burst read cycle time	t_{BC}	60	—	70	—	ns
Address access time	t_{AA}	—	120	—	150	ns
Burst address access time	t_{BA}	—	55	—	70	ns
\overline{CE} access time	t_{ACE}	—	120	—	150	ns
\overline{OE} access time	t_{OE}	—	55	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from \overline{CE}	t_{DHC}	0	—	0	—	ns
Output hold time from \overline{OE}	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
\overline{CE} to output in high Z	t_{CHZ}^{*1}	—	40	—	70	ns
\overline{OE} to output in high Z	t_{OHZ}^{*1}	—	40	—	70	ns
BHE to output in high Z	t_{BHZ}^{*1}	—	40	—	70	ns
\overline{CE} to output in low Z	t_{CLZ}	5	—	5	—	ns
\overline{OE} to output in low Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

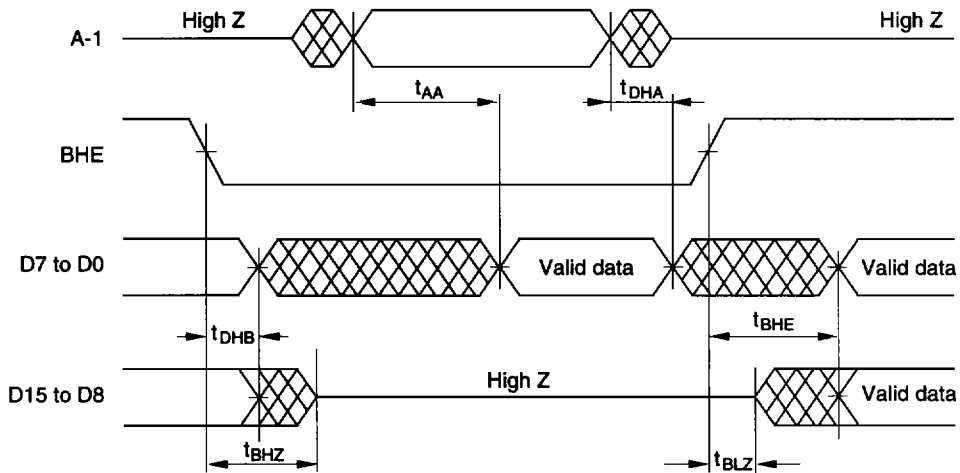
Timing Diagram

(1) Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



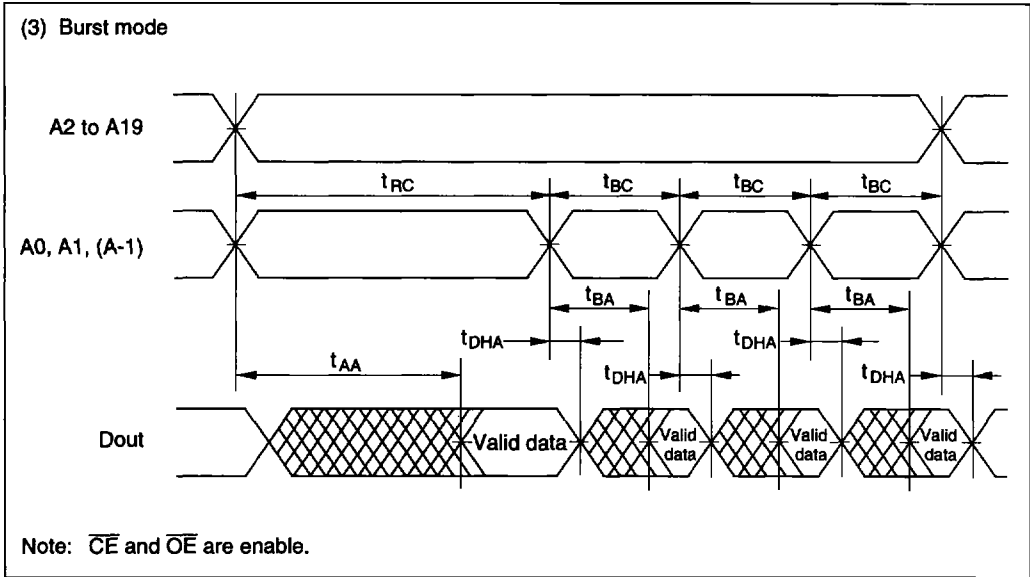
- Notes: 1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
- 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
- 3. t_{CLZ} , t_{OLZ} : Determined by slower.

(2) Word mode, Byte mode switch

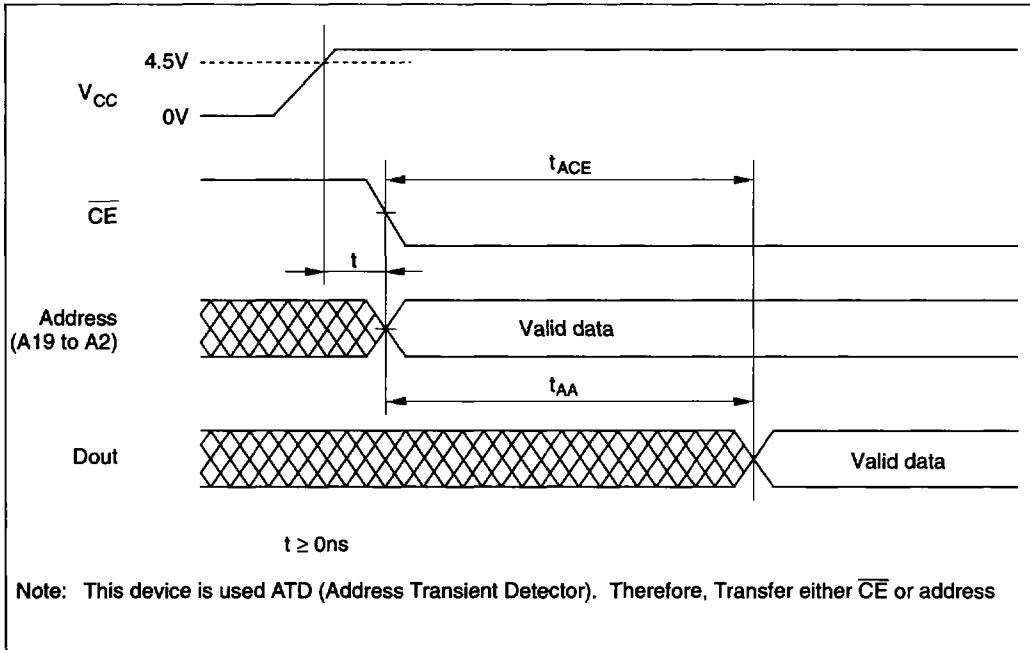


- Notes: 1. \overline{CE} and \overline{OE} are enable A19 to A0 are valid.
- 2. D15/A-1 pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

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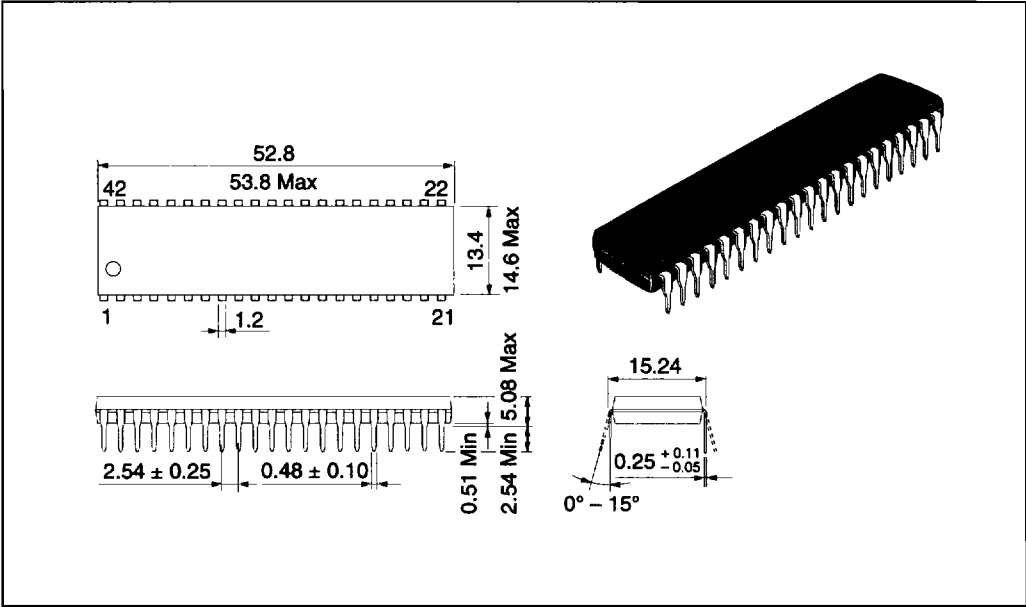
Power Up Sequence



Package Dimensions

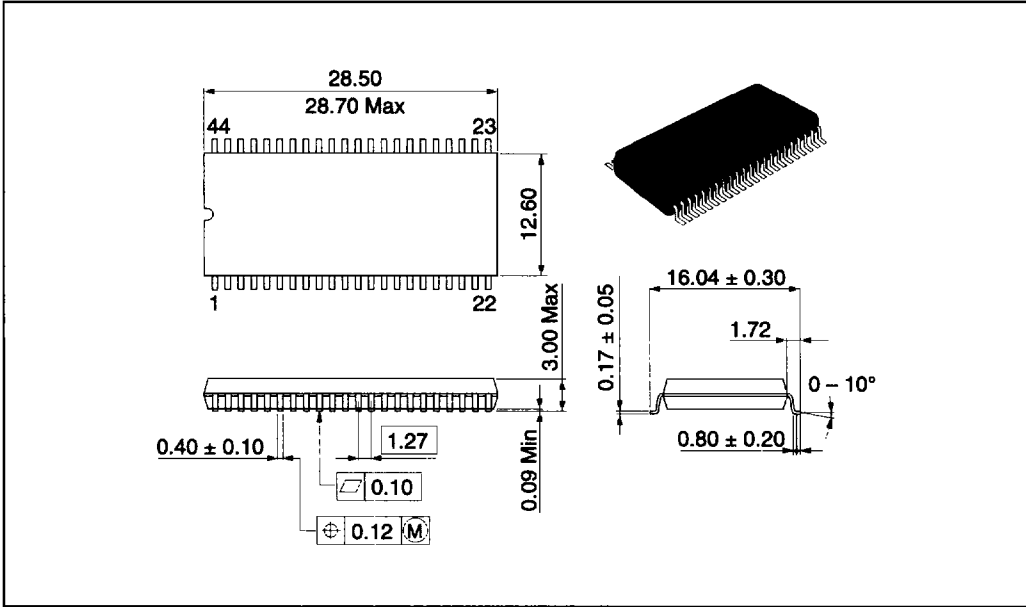
HN624316NP Series (DP-42)

Unit : mm



HN624316NFB Series (FP-44D)

Unit : mm



HN624316N Series

Package Dimensions (cont)

HN624316NTA Series (TTP-48D)

Unit : mm

