Presettable Counters

General Description

These high-speed counters consist of four dc-coupled, master-slave flip-flops which are internally interconnected to provide divide-by-two, divide-by-four, divide-by-five, divide-by-six, divide-by-eight, divide-by-ten, divide-by-twelve, or divide-by-sixteen operations. The counters are fully programmable; that is, the outputs may be preset to any number by placing a low logic level on the count/load input and entering the desired number at the data inputs. Transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters also feature a direct clear which, when placed at a low logic level, sets all outputs low regardless of the conditions on the clocks.

Typical Count Configurations

DM7280/DM8280, DM7290/DM8290

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

DM7281/DM8281, DM7291/DM8291

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table for the DM7281/8281, DM7291/8291.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

DM7288/DM8288

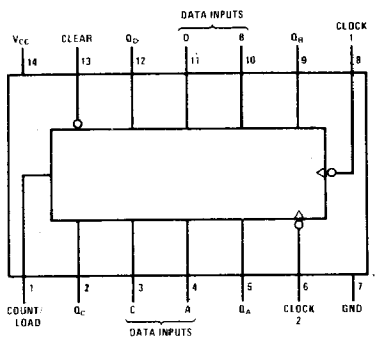
The 8288 divide-by-twelve counter is a four-bit subsystem consisting of divide-by-two and divide-by-six counters in a 14-pin package. For divide-by-twelve operation, output A is connected externally to the clock-2 input.

Features

- Direct replacements Signetics 8280, 8281, 8288, 8290, 8291
- Pin-for-pin with popular Series 54 counters:
  8280, 8290–54176, 54196
  8281, 8291–54177, 54197
- Fully programmable
- Independent clear input
- Performs BCD, bi-quinary, or quinary counting
- Output Q_A maintains full fan-out while driving clock 2

TYPE	TYPICAL CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	CLOCK 1	CLOCK 2	
7280/8280 7281/8281 7288/8288	50 MHz	25 MHz	150 mW
7290/8290 7291/8291	50 MHz	25 MHz	150 mW

Connection Diagram



7280(J), (W); 8280(J), (N), (W); 7281(J), (W); 8281(J), (N), (W); 7288(J), (W); 8288(J), (N), (W); 7290/8290(J), (N), (W); 7291/8291(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM72/82									UNITS
				80, 81			88			90, 91			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			−1.5			−1.5	V
I_{OH}	High Level Output Current					−800			−800			−800	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −800μA		2.6			2.6			2.6			V
I_{OL}	Low Level Output Current					16			16			16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16 mA				0.4			0.4			0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1			1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 4.5V	Count/Load, Data			40			40			40	μA
			Clear, Clock 1			80			80			80	
			Clock 2 (8281, 8291)			40			N/A			80	
			Clock 2 (Others)			80			80			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Count/Load			−1.6			−1.6			−1.6	mA
			Data			−1.2			−1.2			−1.2	
			Clear			−3.2			−3.2			−2.8	
			Clk 1, Clk 2 (8280, 8290)			−3.2			−3.2			−4.8	
			Clock 2 (Others)			−1.6			−1.6			−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		−18		−57	−18		−57	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max			30	45		30	45		30	48	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM	TO	CONDITIONS		DM72/82 80, 81 MIN	DM72/82 80, 81 TYP	DM72/82 80, 81 MAX	DM72/82 88 MIN	DM72/82 88 TYP	DM72/82 88 MAX	DM72/82 90, 91 MIN	DM72/82 90, 91 TYP	DM72/82 90, 91 MAX	UNITS
f_{MAX}	Maximum Clock Frequency	Clock 1	Q_A			35	50		35	50		40	50		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 1	Q_A				9	13		9	13		9	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 1	Q_A				11	17		11	17		11	17	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_B				12	18		12	18		12	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_B				14	21		14	21		14	21	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_C				27	41		27	41		24	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_C				34	51		34	51		28	42	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock 2	Q_D	8280, 8288, 8290	C_L = 15 pF, R_L = 400Ω		13	20		13	20		14	21	ns
				8281, 8291			44	66		N/A			36	54	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clock 2	Q_D	8280, 8288, 8290			17	26		17	26		16	23	ns
				8281, 8291			50	75		N/A			42	63	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any Data Input	Any Output				19	29		19	29		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Any Data Input	Any Output				31	46		31	46		25	38	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Any Output				29	43		29	43		22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Load	Any Output				32	48		32	48		24	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Any Output				32	48		32	48		25	37	ns
t_W	Pulse Width				Clock 1	14			14			14			ns
					Clock 2	28			28			28			
					Clear	25			25			25			
					Load	20			20			20			
t_{HOLD}	Input Hold Time				High-Level Data	$t_{W(LOAD)}$			$t_{W(LOAD)}$			$t_{W(LOAD)}$			ns
					Low-Level Data	$t_{W(LOAD)}$			$t_{W(LOAD)}$			$t_{W(LOAD)}$			
t_{SETUP}	Input Setup Time				High-Level Data	15			15			10			ns
					Low-Level Data	20			20			15			
t_{ENABLE}	Count Enable Time					25			25			30			ns

Truth Tables

80, 90
DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

80, 90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

81, 91
TRUTH TABLE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

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TRUTH TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H

H = High Level, L = Low Level

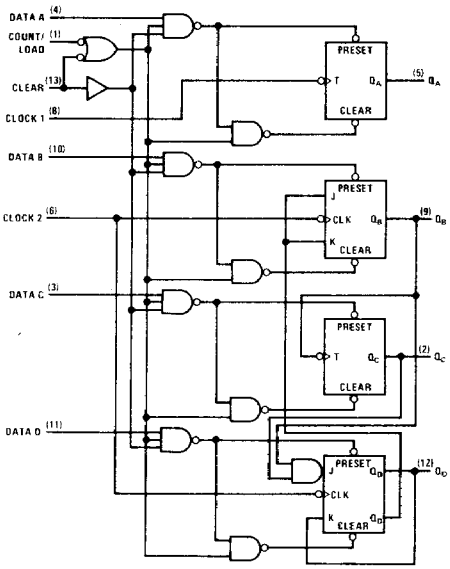
Notes:

(A) Output Q_A connected to clock 2 input.

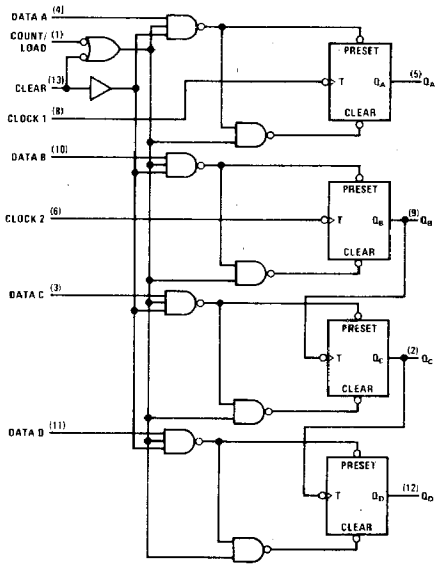
(B) Output Q_D connected to clock 1 input.

Logic Diagrams

80, 90



81, 91



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