NEC

MOS INTEGRATED CIRCUIT

μPD16332

40-BIT EL-PANEL DRIVER

The μPD16332 is an EL panel row driver using a high breakdown voltage CMOS process. It consists of 40-bit bidirectional shift registers, and a high breakdown voltage CMOS driver block. The logic block operates on a 5-V power supply, designed to be connected directly to a microcontroller (CMOS level input). The driver block has a 250 V, 100 mA high breakdown voltage output, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

FEATURES

- High breakdown voltage CMOS structure
- High breakdown voltage, high current output (250 V, 100 mA MAX.)
- 40-bit directional shift registers on chip
- Data control by transfer clock (external)
- 80-pin plastic QFP (3-Direction Lead)
- Wide operating temperature range (T_A = –40 to +85°C)
- /PC pin allows polarity of all driver outputs to be inverted.

ORDERING INFORMATION

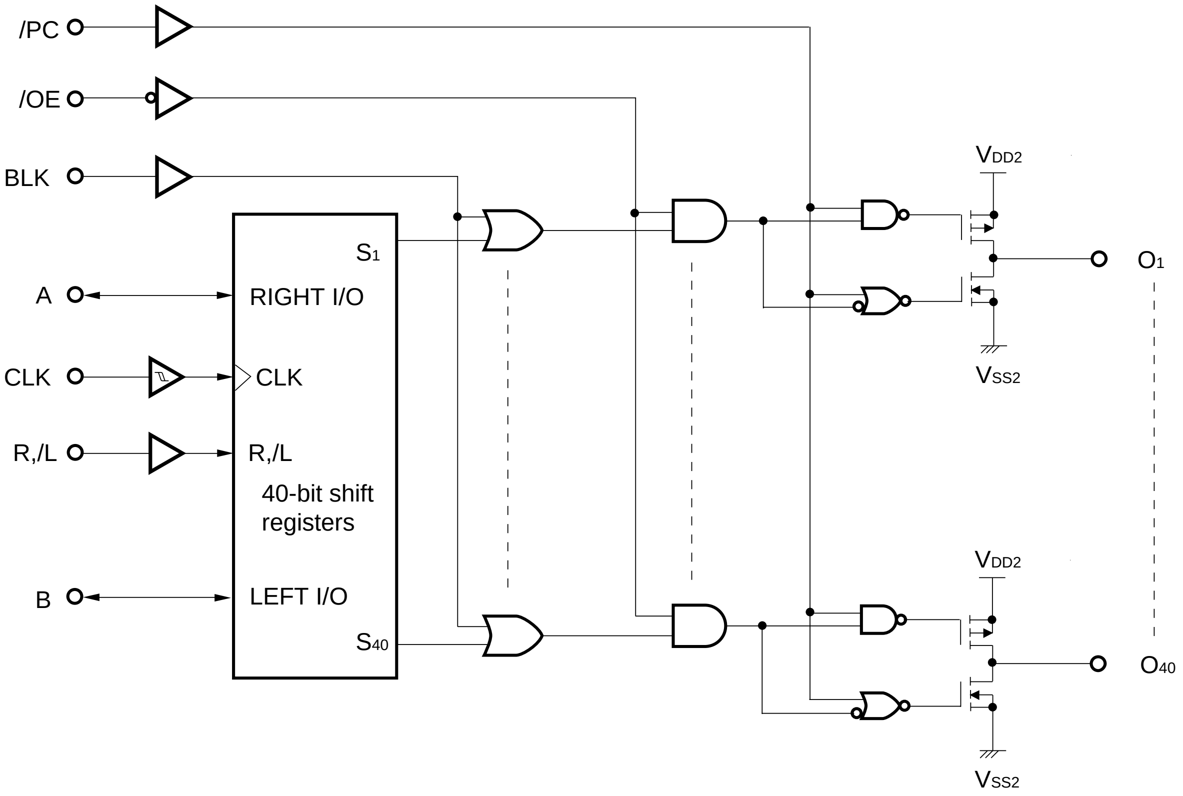
Part Number	Package
μPD16332GF-3L9	80-pin plastic QFP

Remark /xxx indicates active low signal.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

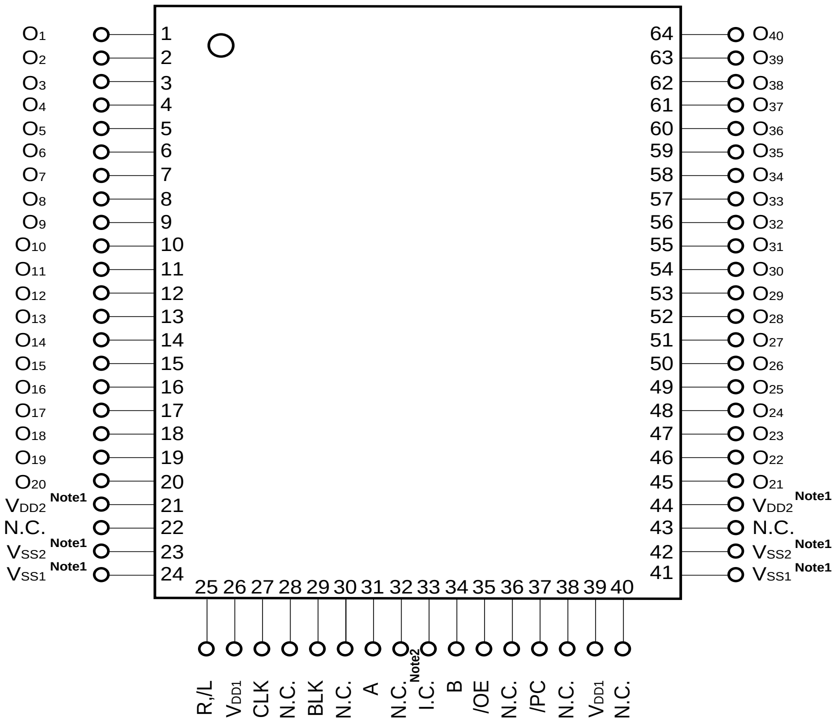
Document No. S13014EJ3V1PM00 (3rd edition)
Date Published November 1998 NS CP(K)
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

μPD16332GF-3L9



Notes 1. Be sure to use all pins V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2}. Use V_{SS1} and V_{SS2} at the same potential.

2. Pin 33 is connected to the lead frame internally, and therefore be sure to leave it open.

Caution **Be sure to enter the power to V_{DD1}, logic signal, and V_{DD2}, in that order, and turn off the power in the reverse order.**

PIN CONFINGRATION

Pin Symbol	Pin Name	Pin Number	Description
BLK	Blanking input	29	Please refer to the TRUTH TABLE 2.
/OE	Output enable input	35	Please refer to the TRUTH TABLE 2.
/PC	Polarity change input	37	/PC = L : Polarity of all outputs inverted
A	RIGHT data input	31	When R,/L = H, A: Input B: Output
B	LEFT data input	34	When R,/L = L, A: Output B: Input
CLK	Clock input	27	Shift is executed on a rising edge.
R,/L	Shift control input	25	H: Right shift mode $A \rightarrow O_1 \cdots O_{40} \rightarrow B$ L: Left shift mode $B \rightarrow O_{40} \cdots O_1 \rightarrow A$
O_1 to O_{40}	High breakdown voltage output	1 to 20, 45 to 64	250 V, 100 mA MAX.
V_{DD1}	Logic block power supply	26, 39	5 V ± 10 %
V_{DD2}	Driver block power supply	21, 44	30 to 240 V
V_{SS1}	Logic ground	24, 41	Connected to system GND
V_{SS2}	Driver ground	23, 42	Connected to system GND
I.C.	Internal-connection	33	Connected to the lead frame internally Be sure to leave it open.
N.C.	Free pins	22, 28, 30, 32, 36, 38, 40, 43	Non-connection

TRUTH TABLE 1 (SHIFT REGISTER BLOCK)

Input		Output		Shift register
R,/L	CLK	A	B	
H	↑	S_1 Input	S_{40} Output	Execution of right shift
H	H or L			Retained
L	↑	S_1 Output	S_{40} Input	Execution of left shift
L	H or L			Retained

TRUTH TABLE 2 (DRIVER BLOCK)

DATA	BLK	/OE	/PC	On	Reference
×	H	L	H	H	All driver outputs are H.
×	H	L	L	L	All driver outputs are L.
×	×	H	×	Z	All driver outputs are Z.
L	L	L	×	Z	
H	L	L	H	H	
H	L	L	L	L	

Remark H : High Level , L : Low Level , ×: H or L , Z : High Inpedance ,
DATA : Contence of the Shift Register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Rating	Unit
Logic supply voltage	V_{DD1}	–0.5 to +6.0	V
Driver supply voltage	V_{DD2}	–0.5 to +250	V
Logic input voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Logic output voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver output voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Driver output current	I_{O2}	±100	mA
Power dissipation	P_D	1000$^{\text{Note}}$	mW
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	$T_{stg.}$	–65 to +150	°C

Note When $T_A \geq$ +25 °C, load should be alleviated at a rate of –8.0 mW/°C.

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

RECOMMENDED OPERATING RANGE (T_A = –40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver supply voltage	V_{DD2}	30		240	V
Input voltage high	V_{IH}	0.7·V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}	0		0.2·V_{DD1}	V
Driver output current	I_{OH}			–70	mA
	I_{OL}			+70	mA

ELECTRICAL CHARACTERISTICS
(T_A = + 25 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 240 V, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level output voltage	V_{OH1}	Logic, I_{OH} = –1.0 mA	0.9·V_{DD1}		V_{DD1}	V
Low level output voltage	V_{OL1}	Logic, I_{OL} = 1.0 mA	0		0.1·V_{DD1}	V
High level output voltage	V_{OH21}	O_1 to O_{40}, I_{OH} = –10 mA	220			V
	V_{OH22}	O_1 to O_{40}, I_{OH} = –70 mA	190			V
Low level output voltage	V_{OL21}	O_1 to O_{40}, I_{OL} = 10 mA			20	V
	V_{OL22}	O_1 to O_{40}, I_{OL} = 70 mA			35	V
3-state output current	I_{TL}	V_{O2} = V_{DD2} or V_{SS2}			±10.0	μA
Input leakage current	I_{IL}	V_I = V_{DD1} or V_{SS1}			±1.0	μA
High level input voltage	V_{IH}		0.7·V_{DD1}			V
Low level input voltage	V_{IL}				0.2·V_{DD1}	V
Static consumption current	I_{DD11}	Logic, T_A = +25 °C			100	μA
	I_{DD12}	Logic, T_A = –40 to +85 °C			1000	μA
	I_{DD21}	Driver, T_A = +25 °C			100	μA
	I_{DD22}	Driver, T_A = –40 to +85 °C			1000	μA

SWITCHING CHARACTERISTICS (T_A = + 25 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 240 V, Logic C_L = 15 pF, Driver C_L = 330 pF, Driver R_L = 10 kΩ)

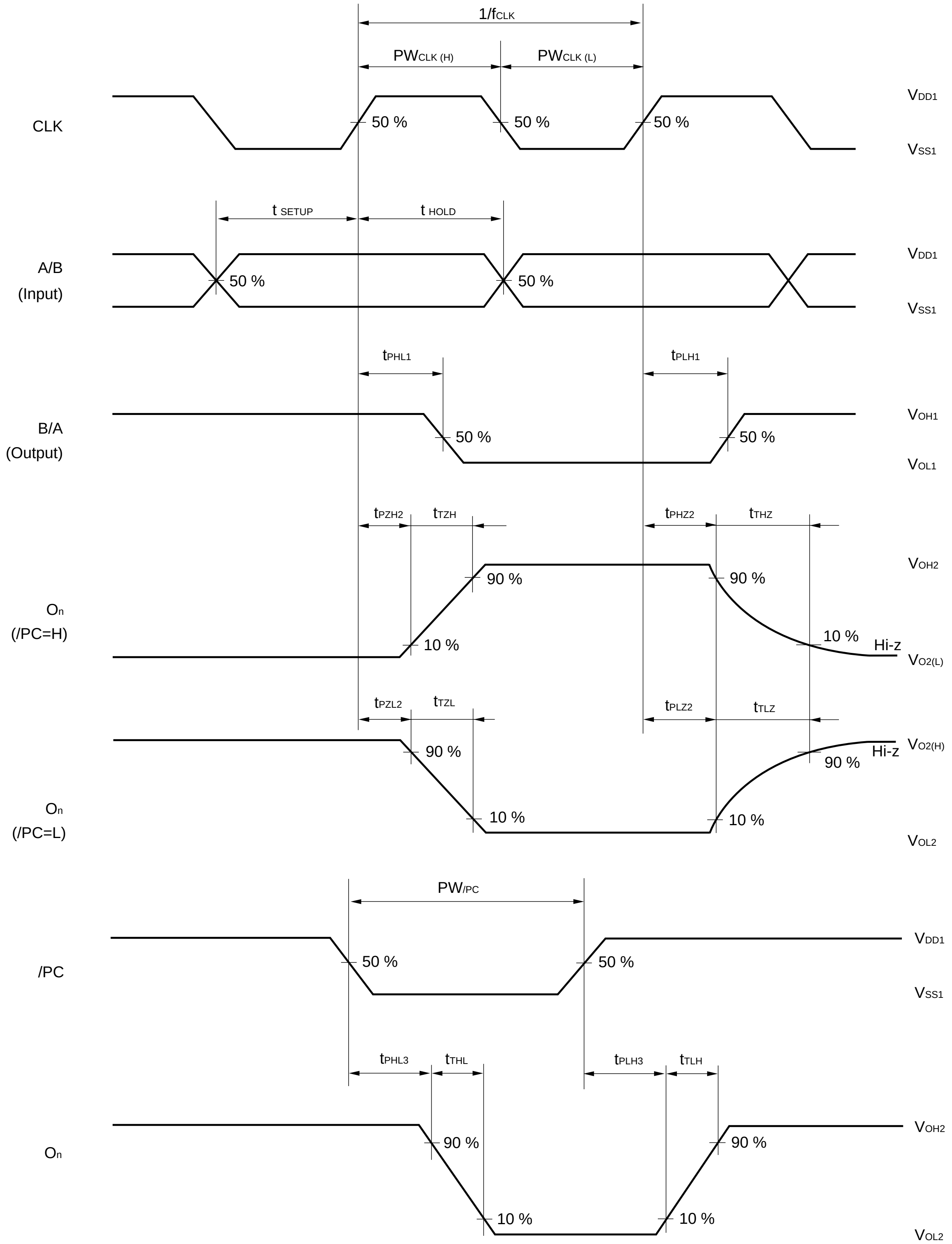
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission delay time	t_{PHL1}	CLK → A/B			100	ns
	t_{PLH1}				100	ns
	t_{PZH2}	CLK → O_1 to O_{40}			500	ns
	t_{PZL2}				500	ns
	t_{PHZ2}				1.0	μs
	t_{PLZ2}				1.0	μs
	t_{PHL3}	/PC → O_1 to O_{40}			1.0	μs
	t_{PLH3}				1.0	μs
	t_{PZH4}	/OE → O_1 to O_{40}			500	ns
	t_{PZL4}				500	ns
	t_{PHZ4}				1.0	μs
	t_{PLZ4}				1.0	μs
	t_{PZH5}	BLK → O_1 to O_{40}			500	ns
	t_{PZL5}				500	ns
	t_{PHZ5}				1.0	μs
	t_{PLZ5}				1.0	μs
Rise time	t_{TZH}	O_1 to O_{40}			2.0	μs
	t_{TLH}				2.0	μs
	t_{TLZ}				15	μs
Fall time	t_{TZL}	O_1 to O_{40}			2.0	μs
	t_{THL}				2.0	μs
	t_{THZ}				15	μs
Maximum clock frequency	$f_{max.}$	Data fetch, Duty = 50 %	10			MHz
		With cascading, Duty = 50 %	6.6			MHz
Input capacitance	C_I				15	pF

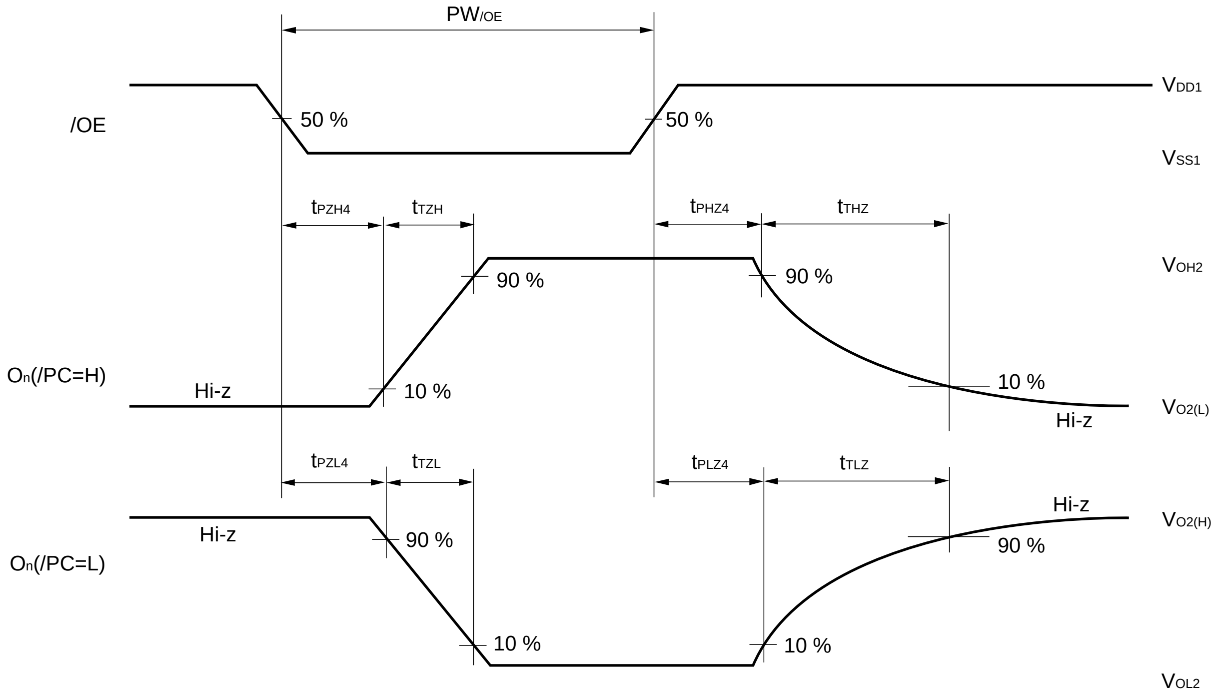
TIMING REQUIREMENTS (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

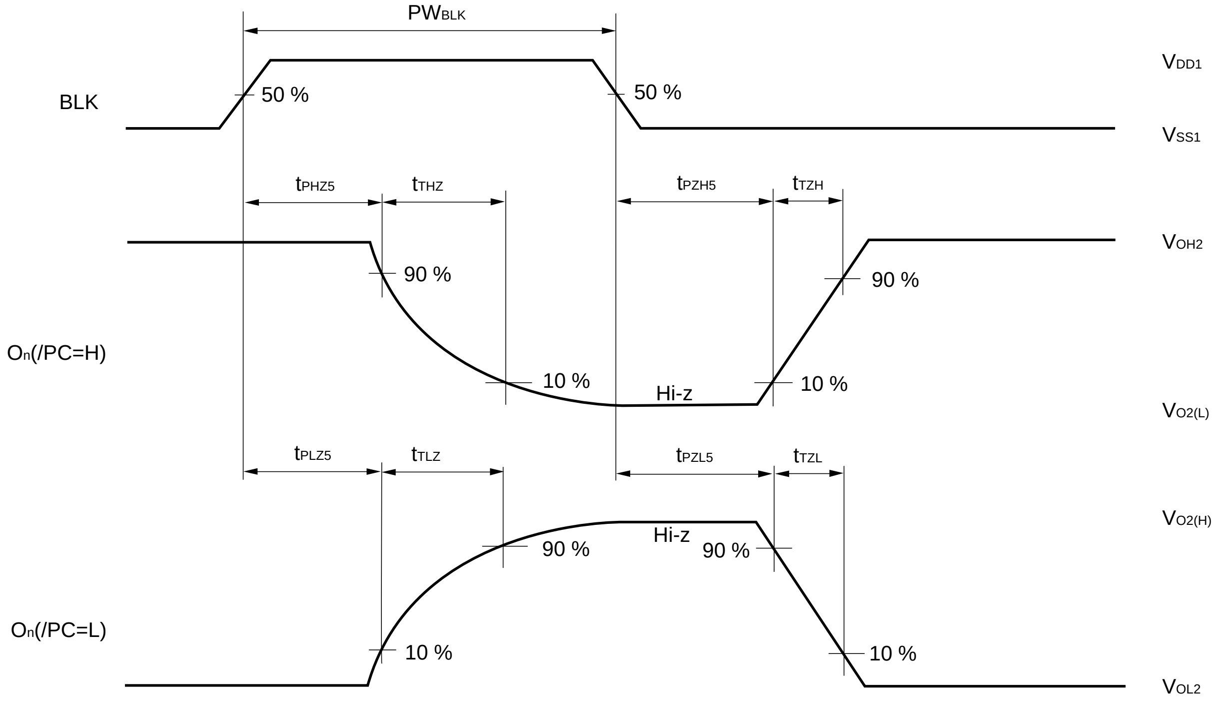
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		50			ns
Blank pulse width	PW_{BLK}		3			μs
/PC pulse width	$PW_{/PC}$		3			μs
Enable pulse width	$PW_{/OE}$		3			μs
Data setup time	t_{SETUUP}		50			ns
Data hold time	t_{HOLD}		50			ns

SWITCHING CHARACTERISTIC WAVEFORM (R,/L = H) ( ) : For Left Shift

$V_{IH} = V_{IL} = 0.5V_{DD1}$

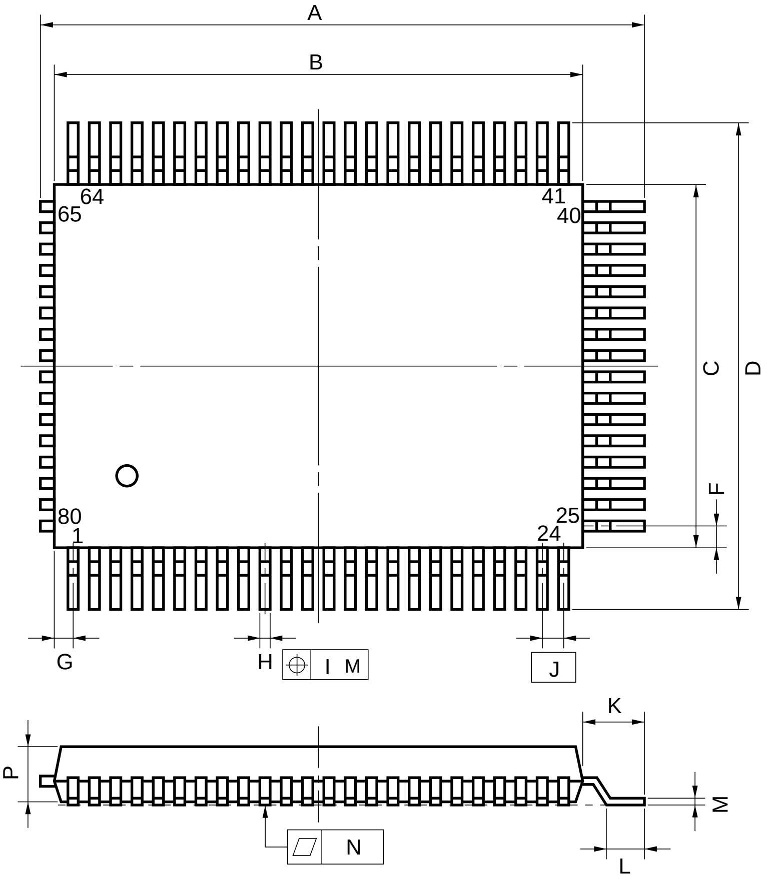



PW/OE
/OE
50 %
50 %
VDD1
VSS1
tPZH4
tTZH
tPHZ4
tTHZ
VOH2
90 %
90 %
On(/PC=H)
Hi-z
10 %
10 %
VO2(L)
Hi-z
tPZL4
tTZL
tPLZ4
tTLZ
Hi-z
VO2(H)
Hi-z
90 %
90 %
On(/PC=L)
10 %
10 %
VOL2

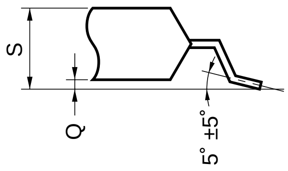

PWBLK
VDD1
BLK
50 %
50 %
VSS1
tPHZ5
tTHZ
tPZH5
tTZH
VOH2
90 %
90 %
On(/PC=H)
10 %
Hi-z
10 %
VO2(L)
tPLZ5
tTLZ
tPZL5
tTZL
VO2(H)
90 %
Hi-z
90 %
On(/PC=L)
10 %
10 %
VOL2

PACKAGE DRAWING

80 PIN PLASTIC QFP (THREE DIRECTIONS) (14X20)



detail of lead end



P80GF-80-3L9-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.3±0.4	0.878±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16332.

For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case he soldering is done under different conditions.

Type of Surface Mount Device

μPD16332GF-3L9 : 80-pin plastic QFP

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	T.B.D.	—
VPS	T.B.D.	—
Pin partial heating	Pin partial temperature: 300°C MAX., Duration: 3 sec. MAX., Time limit: None[Note]	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25°C and relative humidity at 65% or less.

Caution **Do you apply more than one soldering method t any one time, except for the partial heating method.**

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

References

Semiconductor Device Moounting Technology Manual(C10535E)
Quality Grade on NEC Semiconductor Devices (C11531E)

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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