

ML2517**Preliminary****Recording/Playback LSI with On-Chip 4-Mbit Cell Analog-Storage Flash Memory****GENERAL DESCRIPTION**

OKI ML2517 is a single-chip recording/playback LSI featuring an innovative Analog Multi-Level Storage technology that enables you to store non-compressed analog signals directly into the on-chip 4-Mbit Cell Flash memory. The LSI boasts superb sound quality and unsurpassed recording/playback time as long as 17 minutes. A unique cell design allows you to store digital data as well as analog signals into a single Flash memory. The low operating voltage (2.7 to 3.3 V) and small foot-print enable the ML2517 to have a perfect choice for a recording/playback subsystem of size-critical handy and portable terminals.

FEATURES

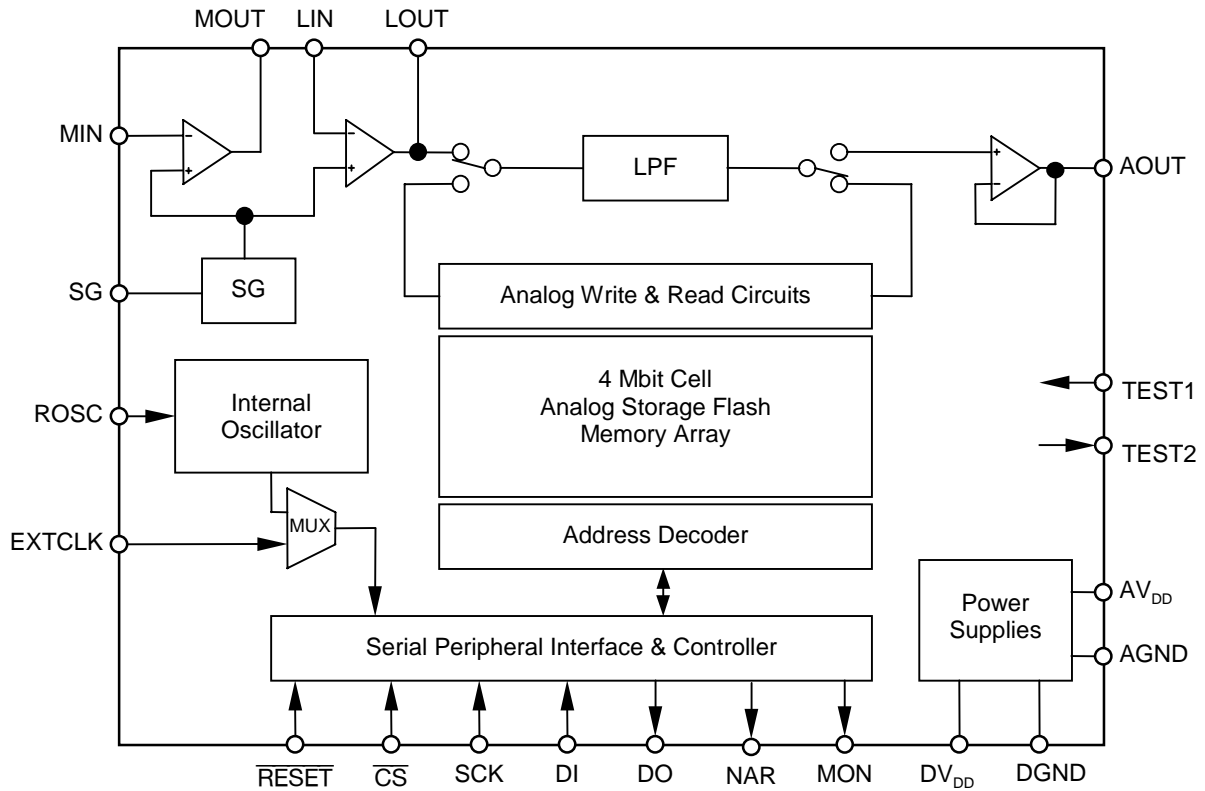
- On-chip 4-Mbit Cell Analog Flash Memory
 - Programming/Erasing Cycles : 10,000 cycles
 - Data Retention Period : 10 years
- MCU Interface
 - Serial Peripheral Interface (SPI; Mode 0 and Mode 1)
- Recording/Playback Time (With internal oscillator)
 - Approx. 640 sec (At $f_{SAM} = 6.4$ kHz)
 - Approx. 723 sec (At $f_{SAM} = 5.3$ kHz)
 - Approx. 1,024 sec (At $f_{SAM} = 4.0$ kHz)
- Sampling Frequencies
 - 4.0 kHz, 5.3 kHz and 6.4 kHz
- Two Recording/Playback Modes
 - Sequential Recording/Playback Mode where you can specify Start and Stop addresses.
 - Random Block Recording/Playback Mode where you can make addressing in Blocks.
- Capability to store data in both analog and digital formats
 - Size-variable digital data storage area (2 Kbit to 4 Mbit)
 - 2-Kbit data write time : Approx. 406 msec (with WRDT1 command)
 - 4-Kbit data write time : Approx. 531 msec (with WRDT2 command)
 - 2-Kbit data read time : Approx. 380 msec
- Built-in Microphone Amplifier
- Built-in LPF/Smoothing Filter (LPF attenuation: -40 dB/oct)
- Built-in Oscillation Circuit, No oscillator required
 - Supports external clock input (Clock Frequency: 1.0 to 8.192 MHz)
- Power Supply Voltage : 2.7 to 3.3 V
- Package : 32-pin Plastic SOP (SOP32-P-525-1.27K)
- Operating Temperature : -10 to +70°C

CONTENTS

GENERAL DESCRIPTION	1
FEATURES	1
BLOCK DIAGRAM	4
PIN LAYOUT (TOP VIEW)	4
PIN DESCRIPTION.....	5
ABSOLUTE MAXIMUM RATINGS	6
RECOMMENDED OPERATING CONDITIONS	6
ELECTRICAL CHARACTERISTICS	6
DC Characteristics.....	6
Analog Block Characteristics	7
AC Characteristics.....	7
TIMING DIAGRAMS	10
Timings for Serial Peripheral Interface (SPI).....	10
Operational Timings at Power-On.....	10
Timings for Powering Up and Powering Down	11
Timings for Recording Operation.....	11
Timings for Playing Operation	12
Timings for Erasing Operation	12
Timings for Pause of Recording Operation.....	13
Timings for Pause of Playing Operation.....	14
Timings for Pause of Erasing Operation.....	15
Timings for Addressing in Random Block Recording/Playback Mode.....	16
Timings for Writing Digital Data	16
Timings for Transferring Digital Data.....	17
FUNCTIONAL DESCRIPTION.....	18
Two Recording/Playback Modes.....	18
1. Sequential Recording/Playback Mode	18
2. Random Block Recording/Playback Mode	19
Addressable Memory Space and Addressing Unit	20
1. Addressing in Sequential Recording/Playback Mode	20
2. Addressing in Random Block Recording/Playback Mode	21
Operational Timings at Power-On.....	22
Control Commands.....	23
1. MODE Command (1H).....	23
2. REC Command (2H).....	24
3. PLAY Command (3H).....	24
4. STOP Command (4H).....	25
5. PAUSE Command (5H)	25
6. ERASE Command (6H)	25
7. STADR Command (7H).....	26
8. SPADR Command (8H)	27
9. RDADR Command (9H).....	27
10. RDSTAT Command (AH).....	28
11. WRDT1 Command (BH)	29
12. WRDT2 Command (CH)	30
13. SETRD Command (DH)	31
14. RDDT Command (EH)	31
15. PDWN Command (FH).....	31
16. Command List.....	32
Serial Peripheral Interface (SPI).....	33
1. Timings for Writing a Command and Data	34
2. Timings for READ Commands	36

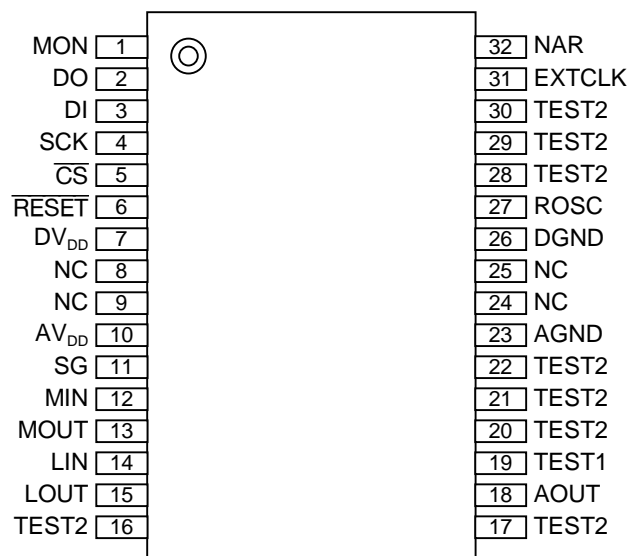
Operations in Sequential Recording/Playback Mode	38
1. Recording	38
2. Playing	42
3. Erasing	45
4. Controlling Phrase Addresses	46
Operations in Random Block Recording/Playback Mode	49
1. Recording	49
2. Playing	55
3. Erasing	59
4. Controlling Phrase Addresses	60
Writing Digital Data	64
1. Write Operation with the WRDT1 Command	64
2. Write Operation with the WRDT2 Command	66
Reading Digital Data	68
1. Data Transfer Operation with the SETRD Command	68
2. Read Data Operation with the RDDT Command	69
Power Up and Power Down Operations	69
Designing Analog Input/Output Amplifying Circuit	70
SG Pin Wiring	71
LPF Characteristics	71
Power Supply Circuit	72
APPLICATION CIRCUIT EXAMPLE	73

BLOCK DIAGRAM



PIN LAYOUT (TOP VIEW)

32-pin Plastic SOP
(SOP32-P-525-1.27-K)



NC: No Connection
Keep these pins open.

PIN DESCRIPTION

Pin	Symbol	Type	Description
6	$\overline{\text{RESET}}$	I	"L" level input to this pin causes the LSI to initialize itself and enter power-down state. You need to input a "L" pulse whenever you turns the LSI on.
5	$\overline{\text{CS}}$	I	The Chip Select pin. "L" level input enables data input/output through the serial interface.
4	SCK	I	The Shift Clock input pin for the DI and the DO pins.
3	DI	I	The Command & Data input pin in serial format.
2	DO	O	The Status, Address & Digital data output pin in serial format.
1	MON	O	Outputs "H" level during recording, play and erase operations. Also outputs "H" level during digital data read/write operation.
32	NAR	O	Outputs "H" level when the LSI is ready to accept the next address input in Random Block Recording/Playback mode.
31	EXTCLK	I	The External Clock input pin. Clock frequency ranging from 1.0 to 8.192 MHz is allowed to input. When the internal oscillation clock is used, be sure to connect this pin to the DGND.
27	ROSC	I	Insert a 33 k Ω resistor ($\pm 1\%$ tolerance) between this pin and the DGND pin. The value of this resistor determines the frequency of the internal oscillation circuit. Be sure to insert a 33 k Ω resistor even if you use an external timing source.
11	SG	O	The analog reference voltage (Signal Ground Voltage) output pin. Inserting a 0.1 μF or close value capacitor between this pin and the AGND pin is recommended.
12	MIN	I	The inverting input pin to the internal OP amplifier. The non-inverting input pin is internally connected to SG.
13	MOUT	O	The output pin from the internal OP amplifier.
14	LIN	I	The inverting input pin to the internal OP amplifier. The non-inverting input pin is internally connected to SG.
15	LOUT	O	The output pin from the internal OP amplifier. Output from this pin is source signal for recording.
18	AOUT	O	The Analog Output pin. Connect to an amplifier to drive an external speaker.
19	TEST1	I	The LSI testing pin. Be sure to connect to GND.
16,17,20, 21,22,28 29,30	TEST2	O	The LSI testing pins. Keep these pins open.
7	DV _{DD}	—	The Digital power supply pin. Insert a 0.1 μF or larger by-pass capacitor between this pin and the DGND pin.
26	DGND	—	The Digital Ground pin.
10	AV _{DD}	—	The Analog power supply pin. Insert a 0.1 μF or larger by-pass capacitor between this pin and the AGND pin.
23	AGND	—	The Analog Ground pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +5.0	V
Input Voltage	V_{IN}	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD}+0.3$	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$	960	mW
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 3.3	V
Operating Temperature	T_{OP}	—	-10 to +70	$^\circ\text{C}$
External Clock Frequency *1	f_{EXTCLK}	—	1.0 to 8.192	MHz

Note *1: Applicable with external clock only. Select an external clock frequency and dividing factor so that you can get a frequency of 1.024 MHz \pm 3% after dividing the external clock frequency.

ELECTRICAL CHARACTERISTICS**DC Characteristics**

$DV_{DD} = AV_{DD} = 2.7$ to 3.3 V, DGND = AGND = 0 V, $T_a = -10$ to $+70^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1	V_{IH}	DGND = AGND = 0 V	$0.8 \times V_{DD}$	—	—	V
"L" Input Voltage *1	V_{IL}	—	—	—	$0.2 \times V_{DD}$	V
"H" Output Voltage *2	V_{OH}	$I_{OH} = -400 \mu\text{A}$	$V_{DD}-0.3$	—	—	V
"L" Output Voltage *2	V_{OL}	$I_{OL} = 2 \text{ mA}$	—	—	0.45	V
"H" Input Current *1	I_{IH}	$V_{IH} = V_{DD}$	—	—	10	μA
"L" Input Current *1	I_{IL}	$V_{IL} = 0 \text{ V}$	-10	—	—	μA
Operating Current 1	I_{DD1}	In Recording Operation	—	30	45	mA
Operating Current 2	I_{DD2}	In Playback Operation	—	20	30	mA
Operating Current 3	I_{DD3}	In Ready state for a command	—	5	10	mA
Power Down Current Consumption	I_{DDS}	—	—	—	10	μA

*1: Applicable to logic input pins (DI, SCK, $\overline{\text{CS}}$, $\overline{\text{RESET}}$ and EXTCLK) except ROsc and TEST1 pins.

*2: Applicable to logic output pins (DO, NAR and MON) except TEST2 pin.

Analog Block Characteristics

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = -10 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
OP Amp. Input Impedance *1	R _{INA}	—	1	—	—	MΩ
OP Amp. Open Loop Gain *2	G _{OP}	f _{IN} = 0 to 4 kHz	40	—	—	dB
OP Amp. Load Resistance *3	R _{OUTA}	—	200	—	—	kΩ
AOUT Load Resistance *4	R _{AOUT}	—	50	—	—	kΩ
SG Pin Output Voltage	V _{SG}	—	1.25	1.35	1.45	V
LOUT Output Voltage Range *5	Voice	—	0.5	—	2.2	V
	Beep	At center, SG Voltage	-0.5	—	+0.5	V

*1: Applicable to MIN and LIN pins.

*2: Applicable to MIN, MOUT, LIN and LOUT pins.

*3: Applicable to MOUT and LOUT pins.

*4: Applicable to AOUT pin.

*5: See “Designing Analog Input/Output Amplifying Circuit” later in this document.

AC Characteristics

DV_{DD} = AV_{DD} = 2.7 to 3.3 V, DGND = AGND = 0 V, Ta = -10 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External Clock Duty Ratio	R _{DUTY}	—	40	50	60	%
RESET Pulse Width	t _{RST}	—	1	—	—	μs
CS↓ – SCK↑ Setup Time	t _{CSS}	—	200	—	—	ns
SCK↓ – CS↑ Hold Time	t _{CSH}	—	200	—	—	ns
SCK “H” Level Pulse Width	t _{WH}	—	200	—	—	ns
SCK “L” Level Pulse Width	t _{WL}	—	200	—	—	ns
DI Setup Time	t _{DIS}	—	20	—	—	ns
DI Hold Time	t _{DIH}	—	20	—	—	ns
DO Output Delay	t _{DOD}	—	—	—	200	ns
DO Output Enabled Transit Time	t _{DOE}	—	—	—	200	ns
DO Output Hi-Z Transit Time	t _{DOZ}	—	—	—	200	ns
Interval between Commands	t _{CS}	After MODE, STADR, SPADR, RDADR, RDSTAT, RDDT, PDWN commands only	5	—	—	μs
		Applicable to any other commands than the above. At 6.4 kHz sampling frequency	345	—	—	μs
MON Pulse Width at Power-On	t _{INIT}	—	—	—	110	ms
Powering Up Time	t _{PWUP}	With the SG pin open	—	—	1	ms
Power-down Transit Time after PDWN Command Input	t _{PDWN}	—	—	—	100	μs
Power-down Transit Time after “L” Input to RESET Pin	t _{PDWNR}	—	—	—	100	μs
“L” Pulse Width Input to CS pin to Exit from Power-down	t _{CSWL}	—	1	—	—	μs
MON Rise Time after REC Command Input *1	t _{RECM}	At 6.4 kHz sampling frequency	—	—	180	μs
REC Bit Setup Time after REC Command Input	t _{RECR}	—	—	—	324	ms

$DV_{DD} = AV_{DD} = 2.7 \text{ to } 3.3 \text{ V}, DGND = AGND = 0 \text{ V}, Ta = -10 \text{ to } +70^\circ\text{C}$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MON Rise Time after PLAY Command Input *1	t_{PLYM}	At 6.4 kHz sampling frequency	—	—	180	μs
PLAY Bit Setup Time after PLAY Command Input	t_{PLYR}	—	—	—	36	ms
MON Rise Time after ERASE Command Input *1	t_{ERSM}	At 6.4 kHz sampling frequency	—	—	180	μs
ERASE Bit Setup Time after ERASE Command Input	t_{ERSR}	—	—	—	324	ms
MON Fall Time after STOP Command Input while Recording/Erasing	t_{SPCM}	At 4.0 kHz sampling frequency	—	—	360	ms
		At 5.3 kHz sampling frequency	—	—	342	ms
		At 6.4 kHz sampling frequency	—	—	333	ms
MON Fall Time after STOP Command Input while Playing	t_{SPCM}	At 4.0 kHz sampling frequency	—	—	108	ms
		At 5.3 kHz sampling frequency	—	—	91	ms
		At 6.4 kHz sampling frequency	—	—	81	ms
REC/ERASE Bit Reset Time after STOP Command Input while Recording/Erasing *1	t_{SPCR}	At 6.4 kHz sampling frequency	—	—	45	ms
PLAY Bit Reset Time after STOP Command Input while Playing *1	t_{SPCR}	At 6.4 kHz sampling frequency	—	—	180	μs
PAUSE Bit Setup Time after PAUSE Command Input *1	t_{PSCP}	At 6.4 kHz sampling frequency	—	—	180	μs
PAUSE Bit Reset Time after PAUSE Command Input while Pausing *1	t_{SPCP1}	At 6.4 kHz sampling frequency	—	—	180	μs
PAUSE Bit Reset Time after STOP Command Input while Pausing *1	t_{SPCP2}	At 6.4 kHz sampling frequency	—	—	180	μs
NAR "H" Level Output Time while in Random Block Recording/Playback Mode *1	t_{NARH}	Block Size = 2 Sectors At 6.4 kHz sampling frequency	265	—	360	ms
NAR "L" Level Output Time while in Random Block Recording/Playback Mode *1	t_{NARL}	Block Size = 2 Sectors At 6.4 kHz sampling frequency	265	—	—	ms
NAR Falling Time after STADR Command Input while in Random Block Recording/Playback Mode	t_{STNAR}	—	—	—	5	μs

$DV_{DD} = AV_{DD} = 2.7 \text{ to } 3.3 \text{ V}, DGND = AGND = 0 \text{ V}, Ta = -10 \text{ to } +70^\circ\text{C}$

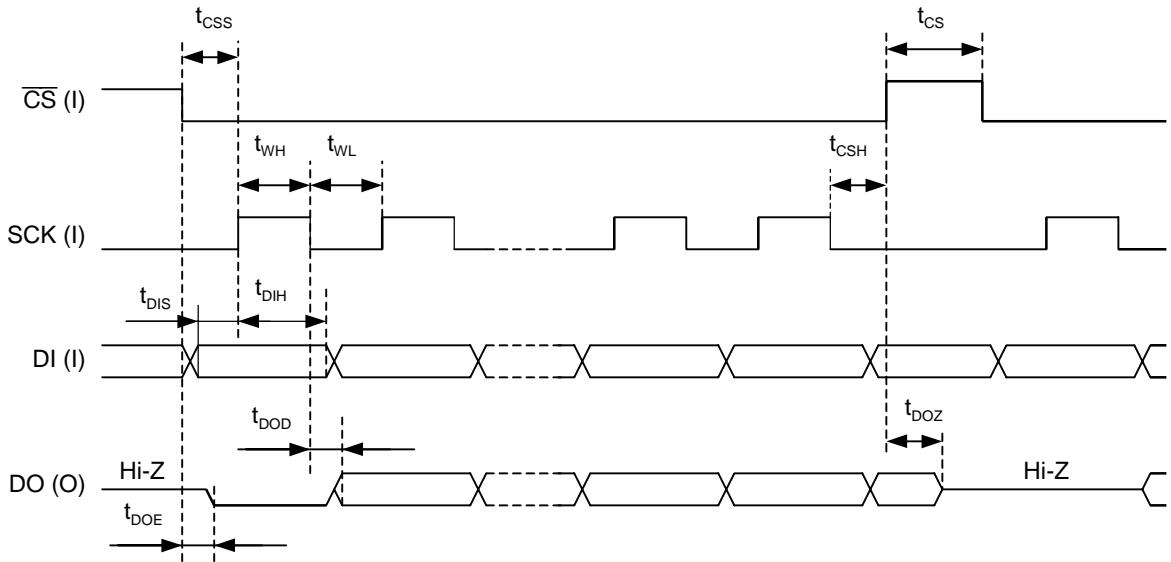
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
MON Rise Time after WRDT1/WRDT2 Command Input	t_{WRM}	—	—	—	288	μs	
PGM Bit Setup Time after WRDT1/WRDT2 Command Input	t_{WRR}	1st-time command input	—	—	324	ms	
		2nd-time and thereafter	—	—	288	μs	
MON "H" Level Output Duration while Executing WRDT1/WRDT2 Command	t_{WMON1}	1st-time command input	—	—	342	ms	
		2nd-time and thereafter	—	—	18	ms	
PGM Bit Setting Duration while Executing WRDT1/WRDT2 Command	t_{WPGM}	—	—	—	18	ms	
MON Rising Time after SETRD Command Input	t_{RDM}	—	—	—	288	μs	
READ Bit Setup Time after SETRD Command Input	t_{RDR}	—	—	—	36	ms	
MON "H" Level Output Duration while Executing SETRD Command	t_{WMON2}	—	—	—	54	ms	
READ Bit Setting Duration while Executing SETRD Command	t_{WRD}	—	—	—	18	ms	
Error in Sampling Frequency Generated by Internal Clock Oscillation *2	Absolute Error	Δf_{SAM1}	$Ta = 25^\circ\text{C}$ $DV_{DD} = AV_{DD} = 3.0 \text{ V}$	-3.0	—	+3.0	%
	Error from Voltage Fluctuation	Δf_{SAM2}	Error = 0% at $Ta = 25^\circ\text{C}$ $DV_{DD} = AV_{DD} = 3.0 \text{ V}$	-6.0	—	+6.0	%
	Error from Temperature Fluctuation	Δf_{SAM3}	Error = 0% at $DV_{DD} = AV_{DD} = 3.0 \text{ V}$ $Ta = 25^\circ\text{C}$	-6.0	—	+6.0	%

Note *1: The value changes in proportion to the sampling period.

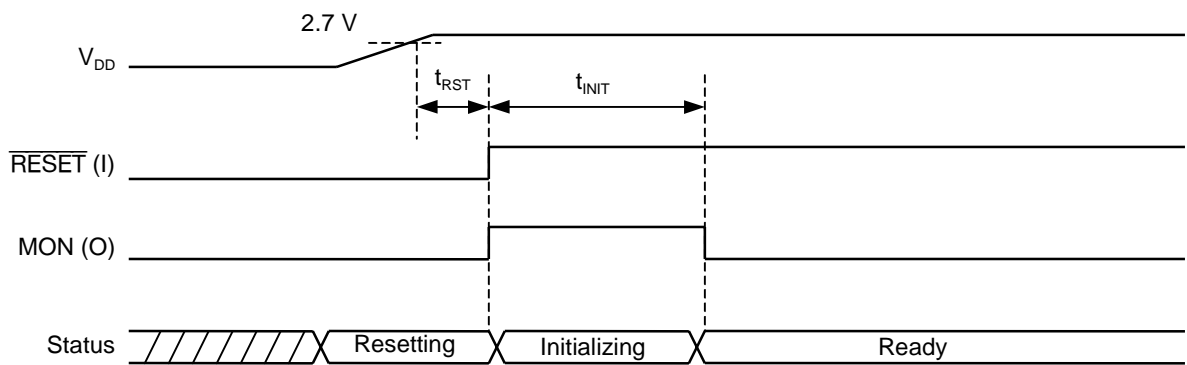
Note *2: When a 33 k Ω resistor is inserted between ROSC and DGND pins.

TIMING DIAGRAMS

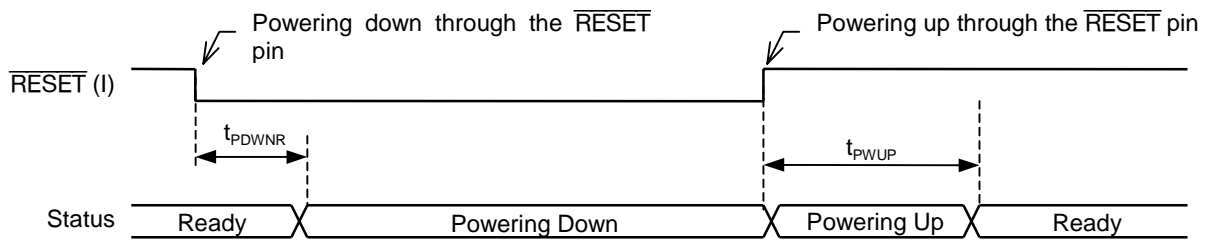
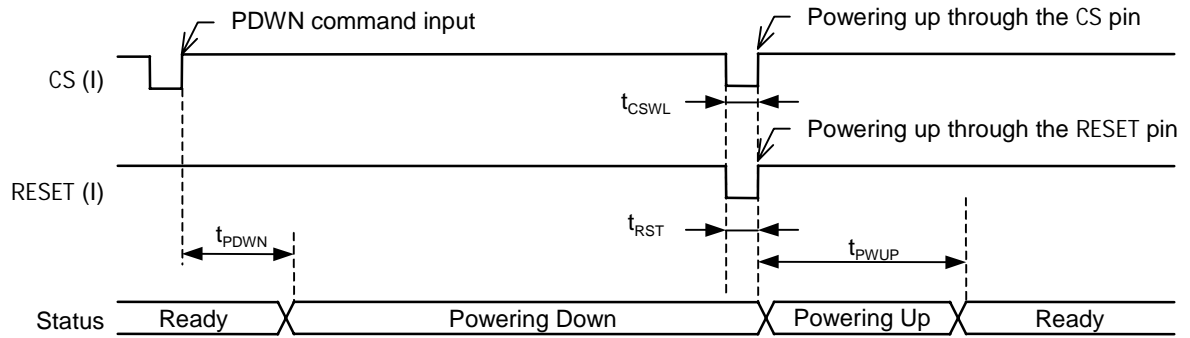
Timings for Serial Peripheral Interface (SPI)



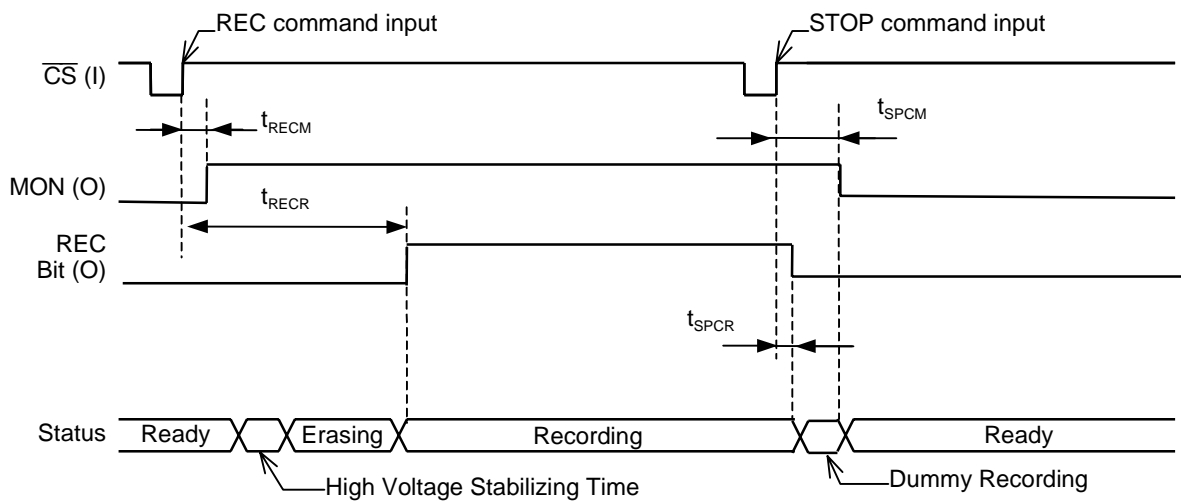
Operational Timings at Power-On



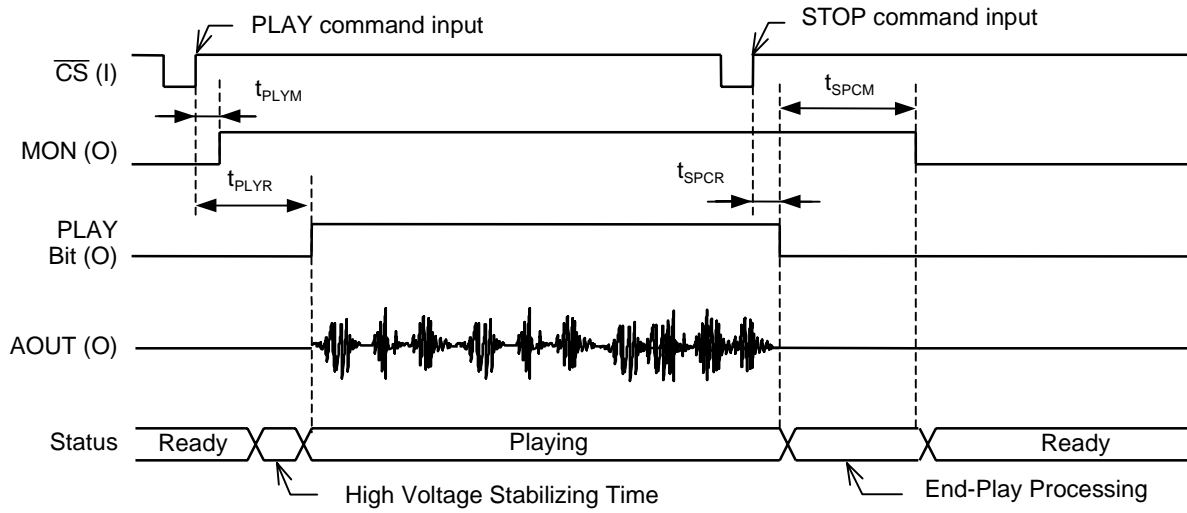
Timings for Powering Up and Powering Down



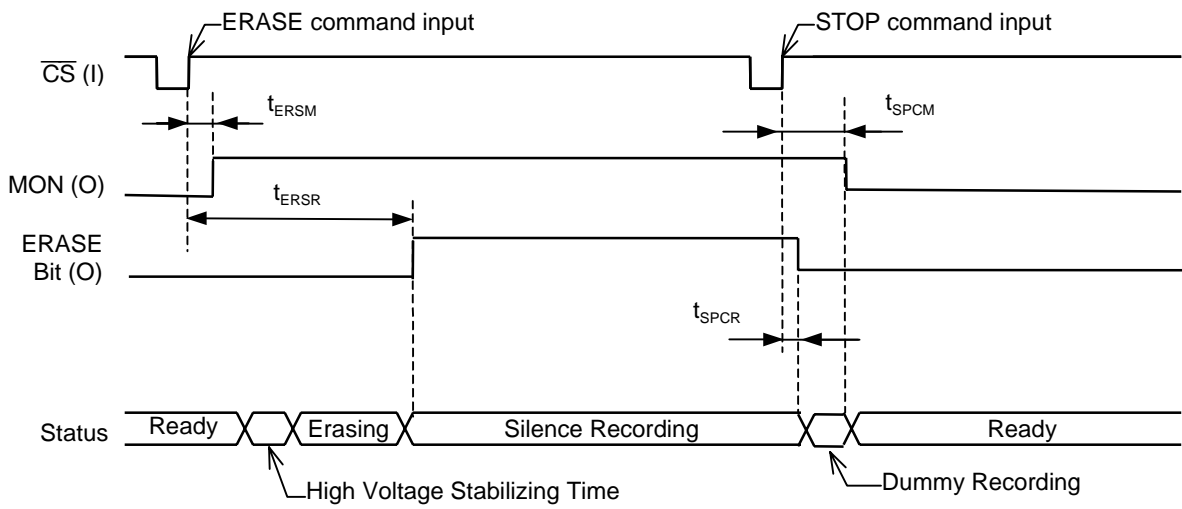
Timings for Recording Operation



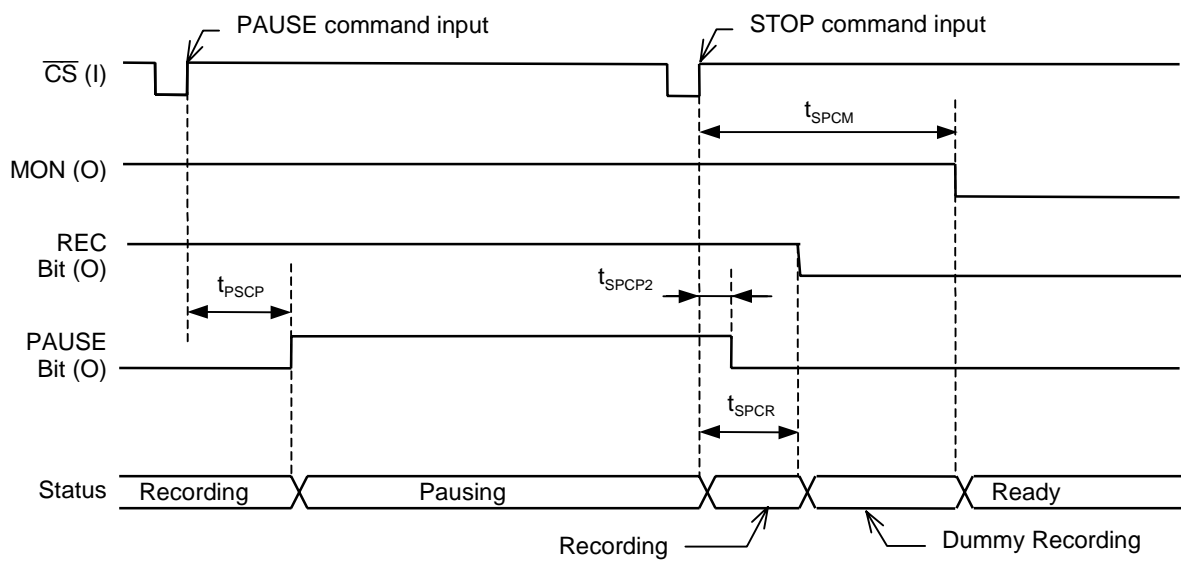
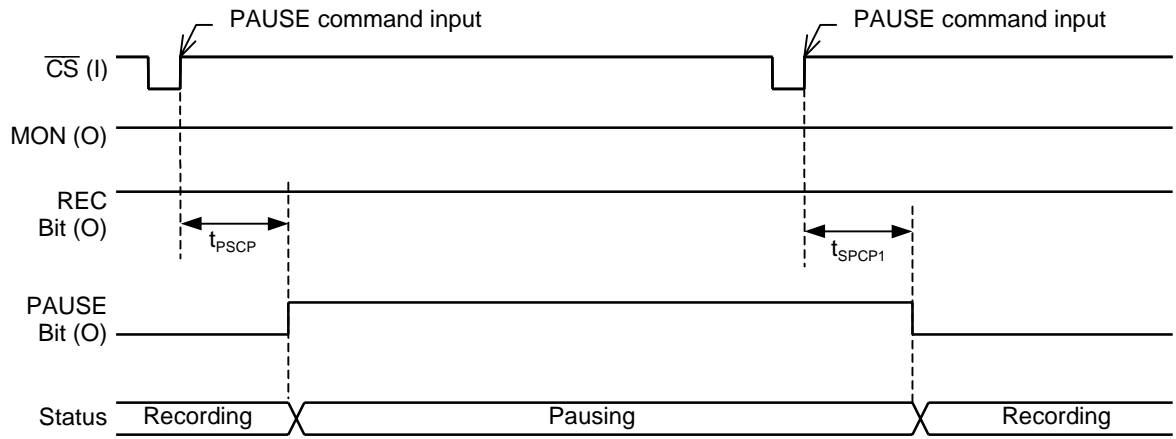
Timings for Playing Operation



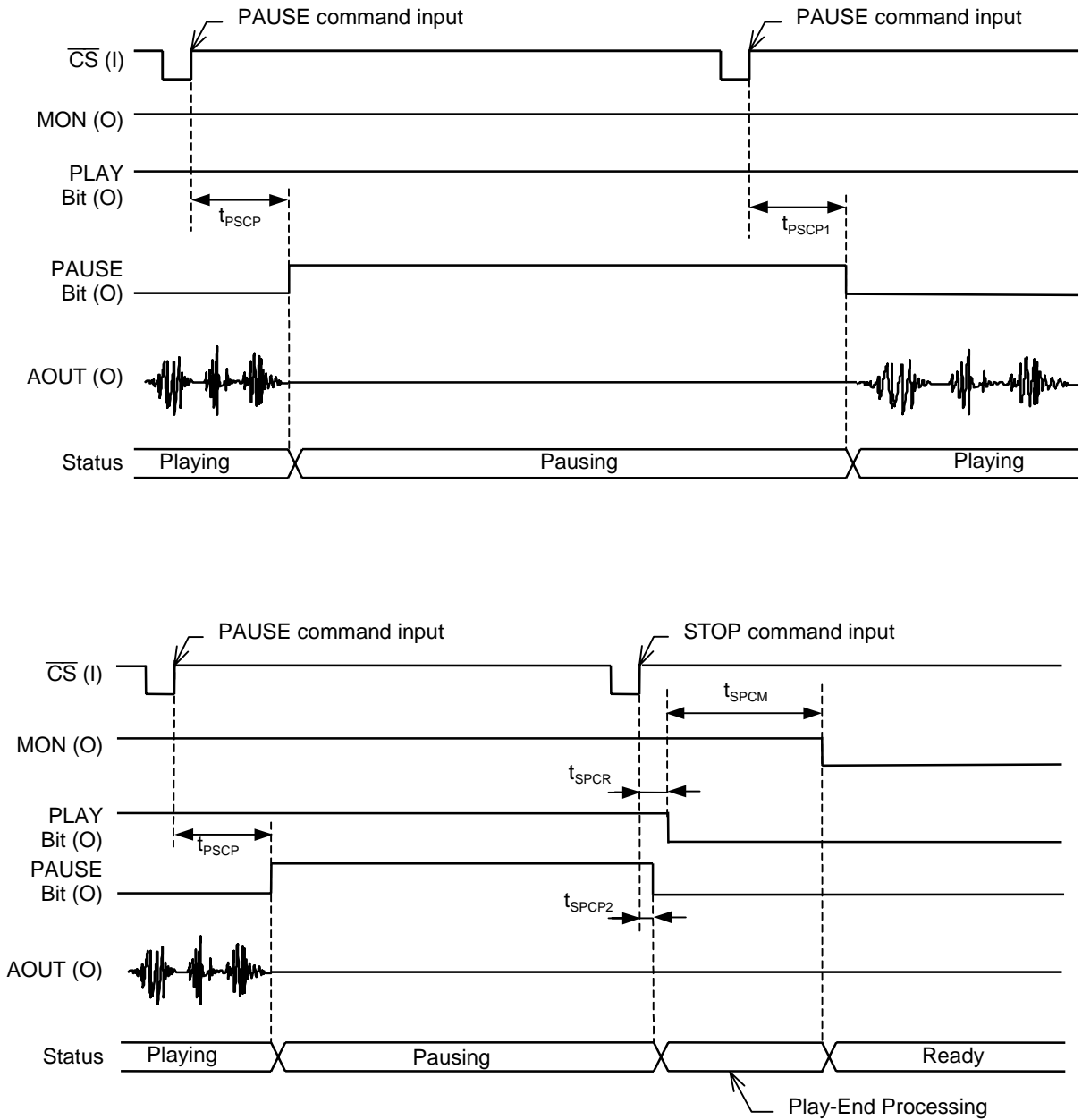
Timings for Erasing Operation



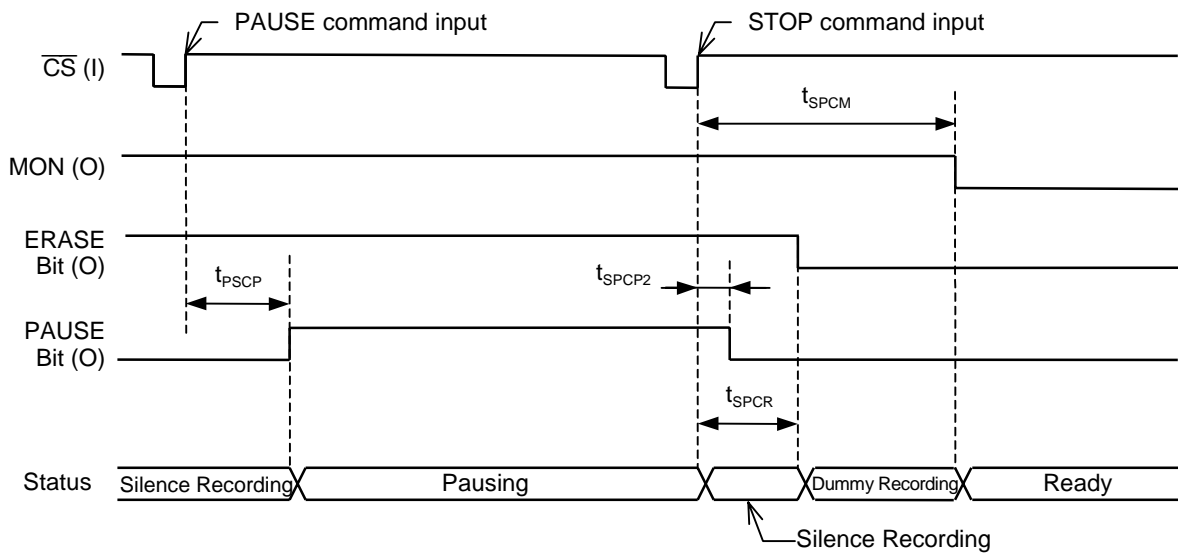
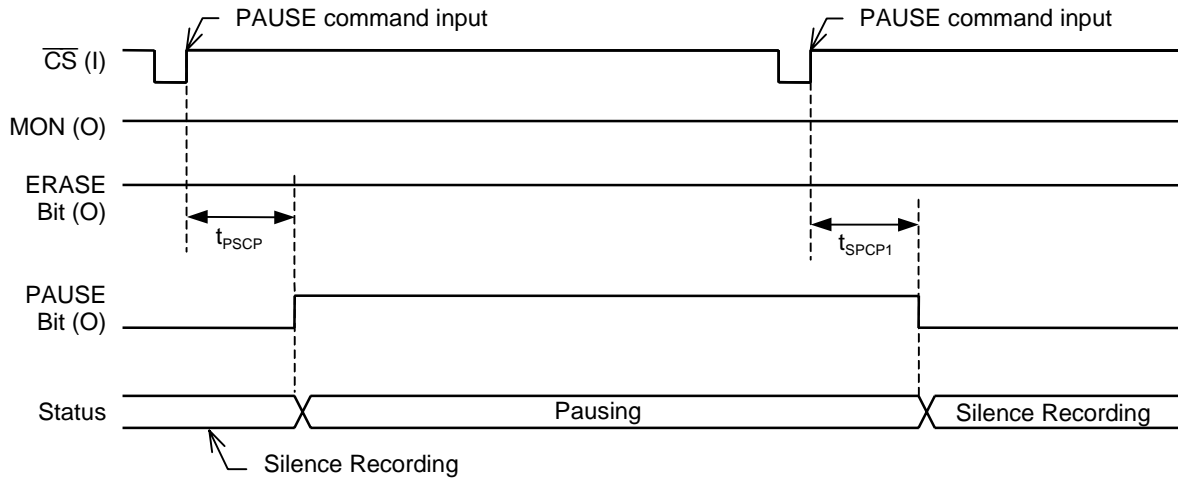
Timings for Pause of Recording Operation



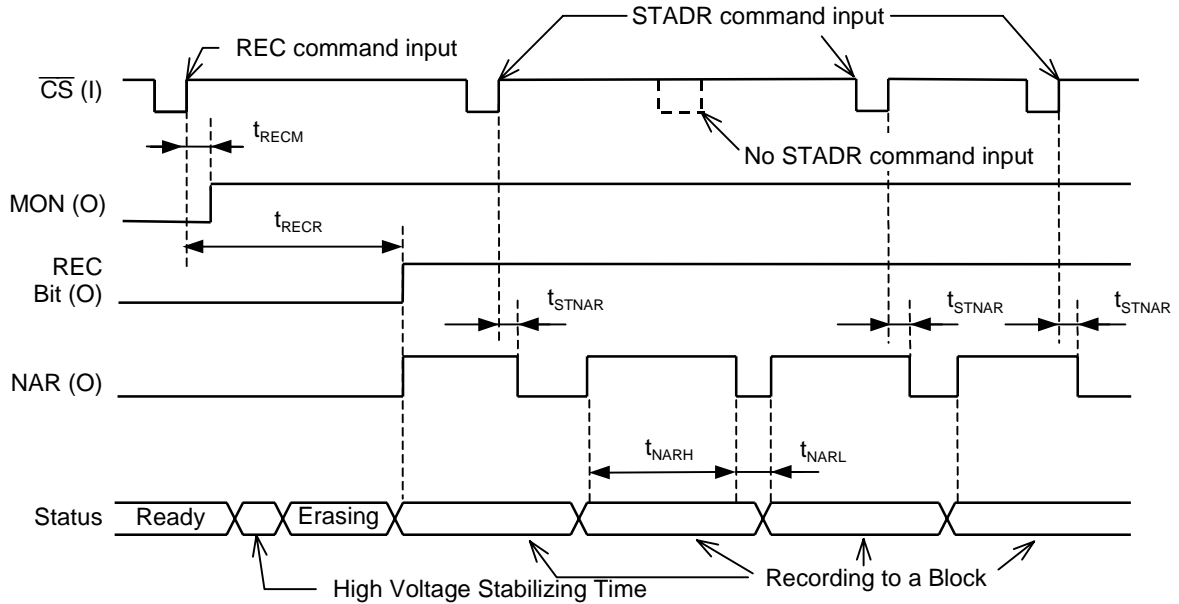
Timings for Pause of Playing Operation



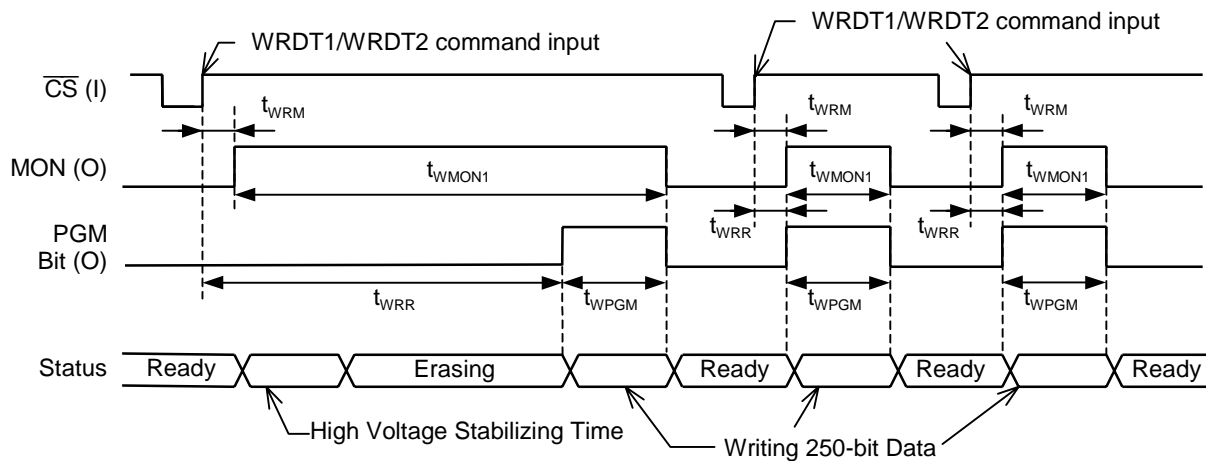
Timings for Pause of Erasing Operation



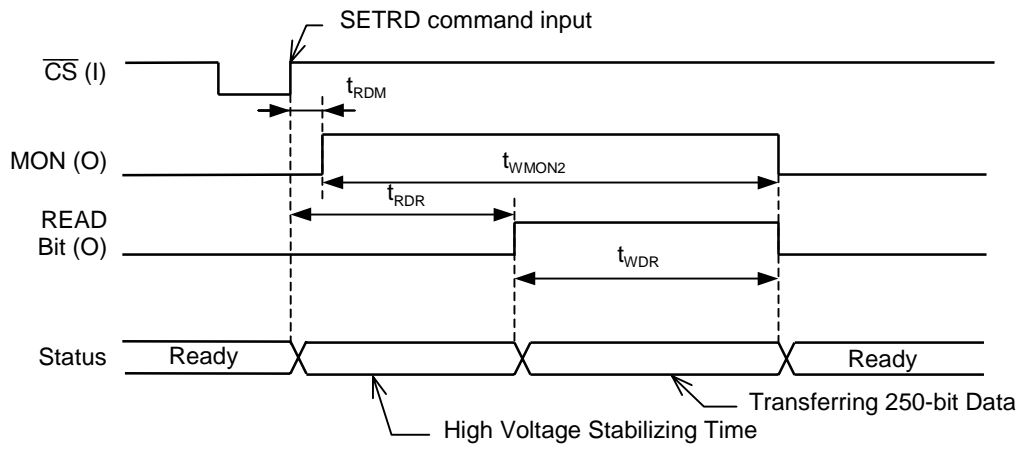
Timings for Addressing in Random Block Recording/Playback Mode



Timings for Writing Digital Data



Timings for Transferring Digital Data



FUNCTIONAL DESCRIPTION

Two Recording/Playback Modes

ML2517 provides two Recording/Playback modes:

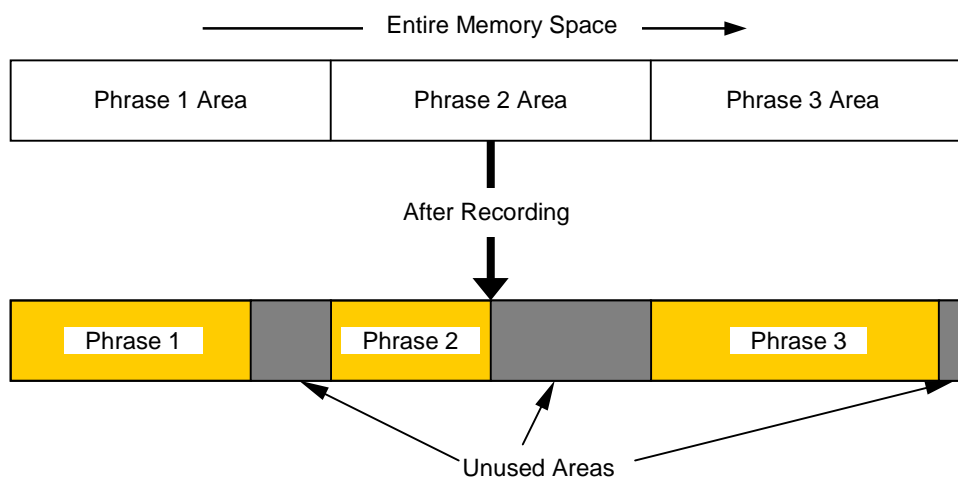
1. Sequential Recording/Playback Mode
2. Random Block Recording/Playback Mode

1. Sequential Recording/Playback Mode

Sequential Recording/Playback Mode lets you specify the Start Address and the Stop Address and record/play to/from the continuous memory area defined by two addresses. Therefore, the value for the Stop Address must be larger than that for the Start Address.

Sequential Mode provides you with more simplified controls over recording and playing operations.

The following section describes a sample memory space usage in Sequential Recording/Playback Mode. As shown in the figure below, each phrase has its own memory area defined by the Start and Stop addresses. Since the Start Address for each phrase points to a specific memory address location, you can control a phrase simply by re-defining the Stop address only even after you have redone the phrase. In case that the recording time is shorter and a part of the assigned memory space is left un-recorded, such space remains unused.



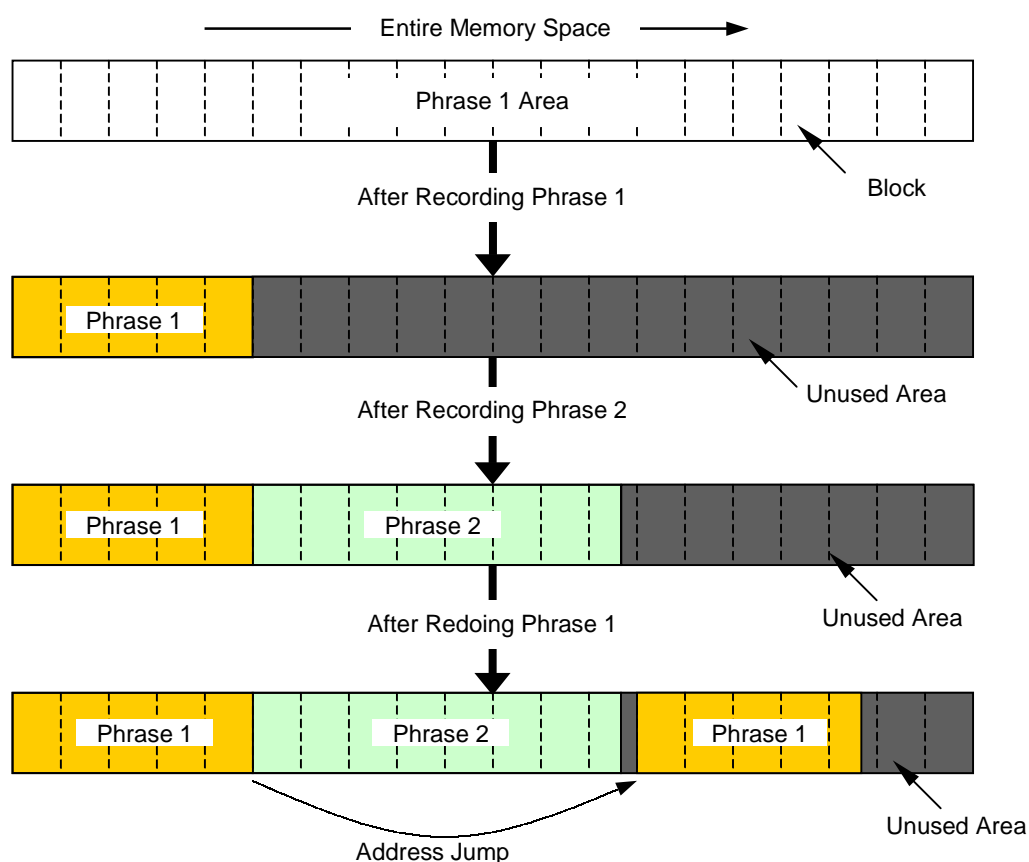
By storing the Start and Stop addresses of each recorded phrase in the digital data area of the on-chip Flash memory with the WRDT1 or WRDT2 command, you can retain phrase address data even after turning the power off. To read the Stop address of a recorded phrase, use the RDADR command after each recording session.

2. Random Block Recording/Playback Mode

In Random Block Recording/Playback Mode, the entire memory space is divided into multiple Blocks, enabling you to randomly specify non-contiguous memory areas for a recording or playing session. This allows you to minimize unused memory space. You can also define a phrase of variable length.

Each block size can be selected out of four different sizes so that you can control recording/playback operations more flexibly according to the external MCU's load status.

The following section describes a sample memory space usage in Random Block Recording/Playback Mode. The figure below shows a case in which you redo Phrase 1 after recording Phrase 1 and Phrase 2. Even if Phrase 1 goes longer than the earlier one, recording goes on using the blocks next to the blocks used by Phrase 2. This means that a memory area assigned to each phrase is not pre-defined and you can always assign any unused blocks to any phrase.

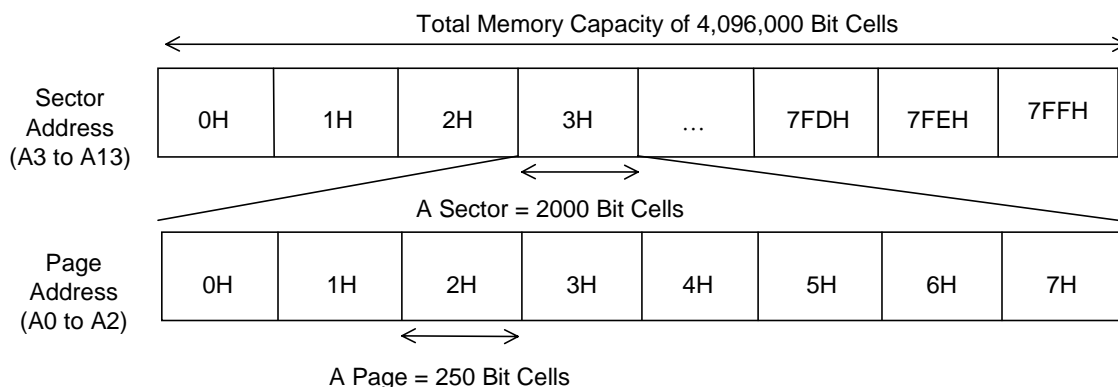


By storing the Start and Stop addresses of each recorded phrase and the Block addresses used for the phrase into the digital data area of the on-chip Flash memory with the WRDT1 or WRDT2 command, you can retain phrase address data even after turning the power off. To read the Stop address of a recorded phrase, use the RDADR command after each recording session.

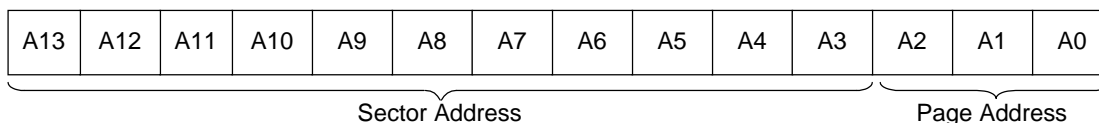
Addressable Memory Space and Addressing Unit

The ML2517's on-chip Flash memory has a total capacity of 4 Mbit cells (4,096,000 bit cells). The entire memory space is divided into 2,048 Sectors, 2,000 bit cells for each Sector. Further, each Sector is divided into 8 Pages, 250 bit cells for each Page.

A3 to A13 address bits are assigned to define a Sector address, and A0 to A2 to define a Page address.



Addressing Bits



1. Addressing in Sequential Recording/Playback Mode

In Sequential Recording/Playback Mode, you need to specify the Recording-Start Address for a phrase in Sectors (A3 to A13), while the Recording-Stop Address for the phrase may be specified in Pages (A0 to A13). For Play operation in Sequential Mode, you can also specify both the Start and Stop addresses in Pages (A0 to A13).

The following table shows the minimum operational time unit at each sampling frequency.

Start/Stop Address	Address to be Specified	Min. Recording/Play Time Unit		
		6.4 kHz	5.3 kHz	4.0 kHz
Recording-Start Address	A3 to A13	312.5 msec	377.35 msec	500 msec
Recording-Stop Address	A0 to A13	39.06 msec	46.88 msec	62.5 msec
Play-Start/Play-Stop Address				

2. Addressing in Random Block Recording/Playback Mode

In Random Block Recording/Playback Mode, you need to specify the Recording-Start Address for a phrase in Sectors (A3 to A13), while the Recording-Stop Address for the phrase may be specified in Pages (A0 to A13). For Play operation in Random Block Recording/Playback Mode, you can specify both the Start and Stop addresses in Pages.

Once Recording/Playback operation gets started, specify the first sector address within a block in order to designate the next recording/playing block.

A Block size is user-selectable. You can select a size for a block from 4 different sizes, ranging from 2 sectors to 16 sectors, by using the MODE command (see “Mode Command” later in this document).

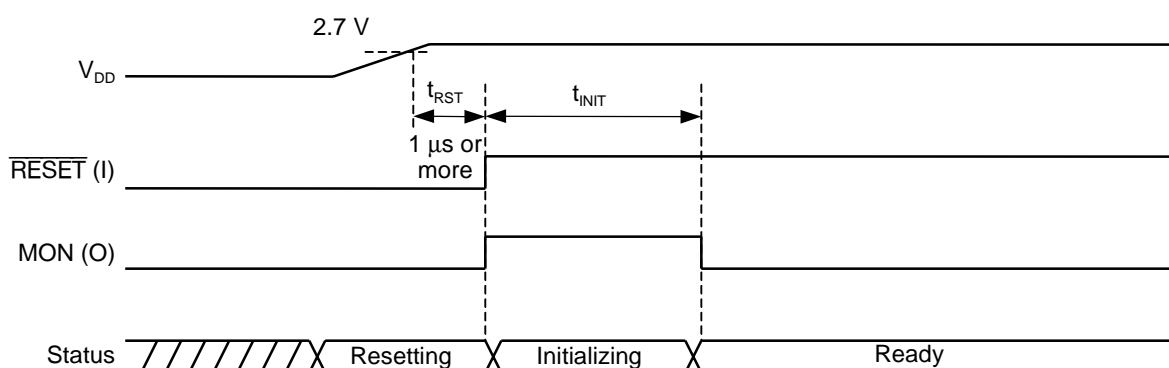
The following table shows the minimum operational time unit at each sampling frequency.

Address Type	Block Size	Address to be Specified	Min. Recording/Play Time Unit		
			6.4 kHz	5.3 kHz	4.0 kHz
Recording-Start Address	—	A3 to A13	312.5 msec	377.35 msec	500 msec
Next Block Address for Recording/Play	2 Sectors	A4 to A13	625 msec	750 msec	1.0 sec
	4 Sectors	A5 to A13	1.25 sec	1.5 sec	2.0 sec
	8 Sectors	A6 to A13	2.5 sec	3.0 sec	4.0 sec
	16 Sectors	A7 to A13	5.0 sec	6.0 sec	8.0 sec
Recording-Stop Address Playing-Start/Playing-Stop Address	—	A0 to A13	39.06 msec	46.88 msec	62.5 msec

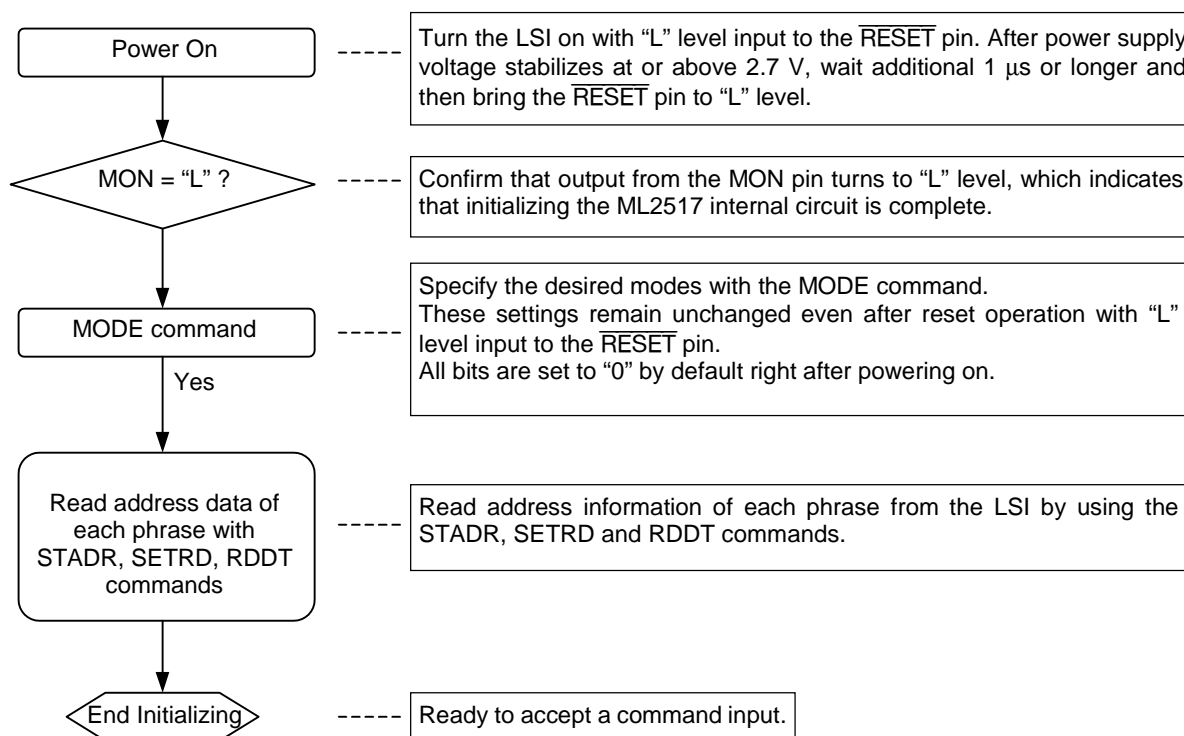
Operational Timings at Power-On

You need to input a “L” pulse to the $\overline{\text{RESET}}$ pin at the timing as shown below whenever you turn the device on. This is required to initialize ML2517’s internal circuit. The LSI starts initializing after turning the $\overline{\text{RESET}}$ pin to “H” level. During this initializing process, the LSI outputs “H” level to the MON pin. When the MON pin is brought back to “L” level, the LSI enters Ready state for accepting a command such as REC or PLAY

Timing for RESET Pulse Input at Power-On



Meanwhile, the LSI performs its operations using the internal oscillation circuit during the initializing process. The “H” level output duration of the MON pin is up to 110 ms. The following section describes a sample workflow of the initializing process at power-on.

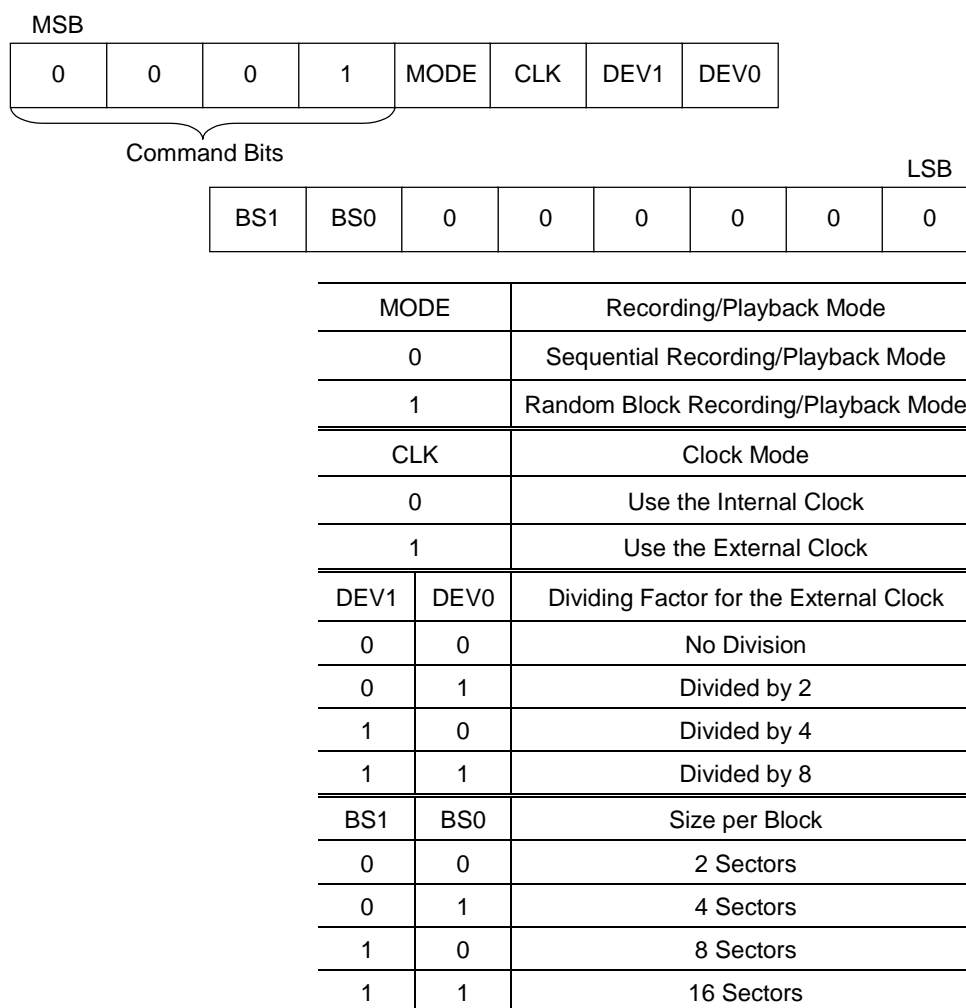


Control Commands

You can control ML2517's operations by inputting commands via the serial interface.

1. MODE Command (1H)

By using the 12-bit data following the MODE command, you can define a recording/playback mode, clock mode, dividing factor for the external clock, and a block size for Random Block Mode. Be sure to set the last 6-bit data to "0" (zero) because the ML2517 uses the data for internal circuit testing.



By default, every data bit is set to "0" right after powering on. However, each data bit remains unchanged after Reset input.

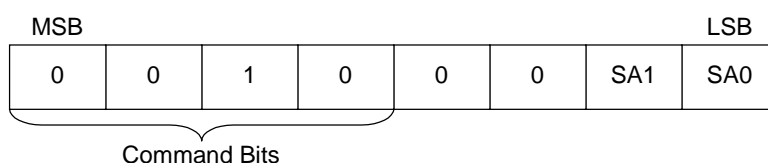
You should also select a proper dividing factor so that you can get 1.024 MHz \pm 3% clock frequency, if you use an external clock.

2. REC Command (2H)

The REC command is used to start recording and can be used alike in both Sequential and Random Block Recording/Playback Modes. Inputting this command causes the LSI to start recording from the address specified with the STADR command.

The 4-bit data following this command determines a sampling frequency. If you neglect to define a sampling frequency (input the 4-bit command only), recording starts at the sampling frequency previously defined.

By default the sampling frequency is set automatically to 6.4 kHz after $\overline{\text{RESET}}$ input or powering on.



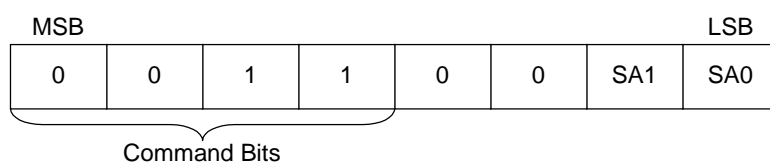
SA1	SA0	Sampling Frequency
0	0	4.0 kHz
0	1	5.3 kHz
1	0	6.4 kHz (default value)
1	1	Unused

3. PLAY Command (3H)

The PLAY command is used to start playback and can be used alike in both Sequential and Random Block Recording/Playback Modes. Inputting this command causes the LSI to start playing from the address specified with the STADR command.

The 4-bit data following this command determines a sampling frequency. If you neglect to define a sampling frequency (input the 4-bit command only), playback starts at the sampling frequency previously defined.

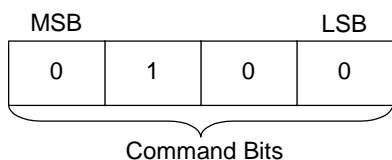
By default the sampling frequency is set automatically to 6.4 kHz after $\overline{\text{RESET}}$ input or powering on.



SA1	SA0	Sampling Frequency
0	0	4.0 kHz
0	1	5.3 kHz
1	0	6.4 kHz (default value)
1	1	Unused

4. STOP Command (4H)

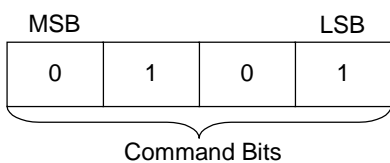
The STOP command is used to stop recording or playing and can be used alike in both Sequential and Random Block Recording/Playback Modes. Inputting this command causes the LSI to stop recording/playing. Any data following this command is disregarded.



5. PAUSE Command (5H)

The PAUSE command is used to temporarily suspend recording or playing and can be used alike in both Sequential and Random Block Recording/Playback Modes. Inputting this command causes the LSI to suspend recording/playing. Any data following this command is disregarded.

Re-input of this command resumes the suspended operation. If the STOP command is input while pausing, the LSI will stop recording or playing operation.

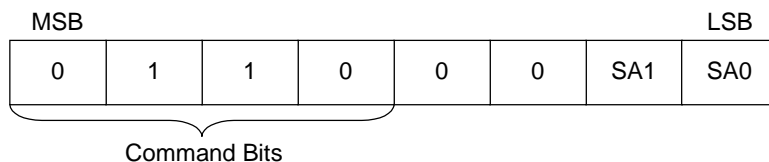


6. ERASE Command (6H)

The ERASE command is used to erase a recorded phrase and can be used alike in both Sequential and Random Block Recording/Playback Modes. Inputting this command causes the LSI to overwrite the existing data with silence data starting at the address specified with the STADR command. When you input the command, the analog input signal line is forced to be switched to SG level internally. Except the foregoing, the LSI operates just alike in recording operation with the REC command.

The 4-bit data following this command determines a sampling frequency. If you neglect to define a sampling frequency (input the 4-bit command only), erasing (recording silence) starts at the sampling frequency previously defined.

By default the sampling frequency is set automatically to 6.4 kHz after RESET input or powering on.



SA1	SA0	Sampling Frequency
0	0	4.0 kHz
0	1	5.3 kHz
1	0	6.4 kHz (default value)
1	1	Unused

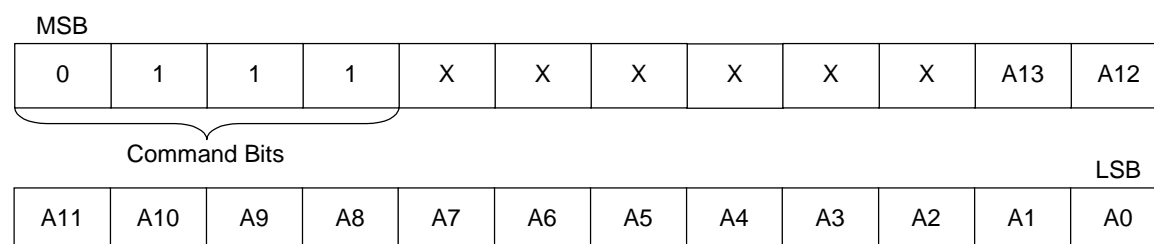
7. STADR Command (7H)

In Sequential Recording/Playback Mode, use the STADR command to specify a Recording/Play Start Address, while in Random Block Recording/Playback Mode, use this command to specify a Recording/Play Start Address and Block Address for recording or playing.

In addition, you can also use the STADR command to specify an address for digital data Read or Write operation.

14-bit data following the STADR command is for addressing. You must run this command prior to REC, PLAY, ERASE, WRDT1, WRDT2 and SETRD commands. If you neglect to run the STADR command before using those 6 commands, each operation will start at the address defined previously.

By default, the Start Address is set automatically to the head address of the memory after RESET input or powering on.



In Sequential Recording/Playback Mode, you specify a Recording Start Address in Sectors, thus Page address bits (A0 through A2) are ignored. However, a Play Start Address can be specified in Pages, which means the entire 14-bit address data is valid.

In Random Block Recording/Playback Mode, you specify a Recording Start Address in Sectors, thus Page address bits (A0 through A2) are ignored. However, you can specify a Playback Start Address in Pages, which means the entire 14-bit address data is valid.

Once recording/playback operation gets started, specify the first sector address within a Block in order to designate the next recording/playing block. When you make addressing in Blocks, the following address bits are disregarded as shown in the table below.

Block Size	Address Bits Disregarded
2 Sectors	A0 to A3
4 Sectors	A0 to A4
8 Sectors	A0 to A5
16 Sectors	A0 to A6

When you run the WRDT1 command to write digital data, A0 to A2 address bits are disregarded. Also when you run the WRDT2 command to write digital data, A0 to A3 address bits are disregarded.

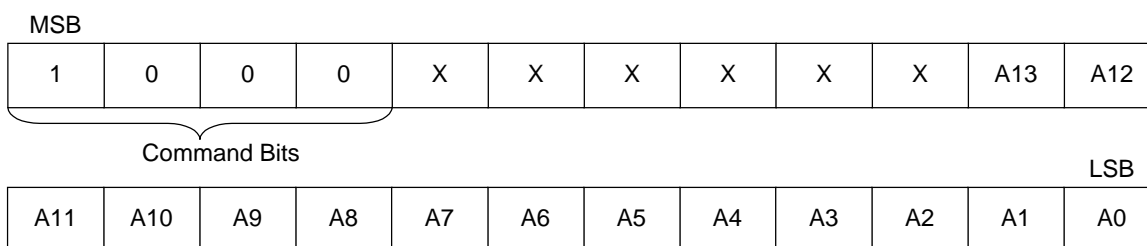
8. SPADR Command (8H)

The SPADR command is used to specify the Stop Address for a recording/playback session and can be used alike in both Sequential and Random Block Recording/Playback Modes.

The 14-bit data following this command determines the Stop Address. The entire 14-bit data is valid as you can specify the address in Pages.

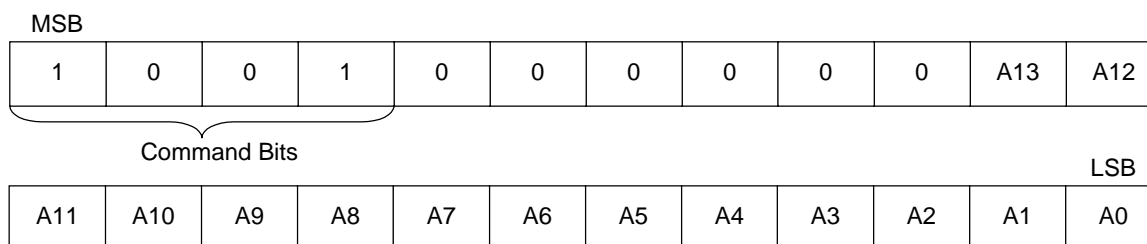
You must run this command prior to REC, PLAY and ERASE commands. If you neglect to do so, each operation keeps going on until the last defined Stop Address is reached.

By default, the Stop Address is set automatically to the last address of the memory after RESET input or powering on.

**9. RDADR Command (9H)**

The RDADR command is used to read the current value of the memory address counter via the serial interface and can be used alike in both Sequential and Random Block Recording/Playback Modes.

In sync with SCK clock input that follows this command, the LSI outputs 6-bit dummy data and 14-bit memory address counter data to the DO pin, starting with the MSB.



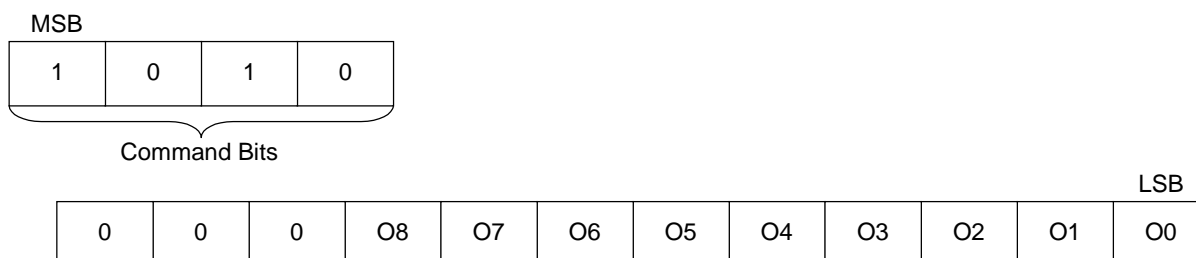
This command enables you to read out the Stop Address of the phrase that has been recorded, allowing you to manage and control phrase addresses by using an external MCU.

You can input the RDADR command during recording, playing or erasing operation or while pausing these operations.

10. RDSTAT Command (AH)

The RDSTAT command is used to read out the values of ML2517's internal status register via the serial interface. By performing this operation, you can learn ML2517's status as shown in the table below.

In sync with SCK clock input that follows the RDSTAT command bits, the LSI outputs 3-bit dummy data and 9-bit status register data to the DO pin, starting with the MSB.



Data Bit	Name	Status
O8	MON	This data bit is set to "1" during the following operations; Recording, Playback, Erase, Read/Write digital data The duration includes such time periods as stabilizing at the beginning of each operation, erasing memory and end-operation processing, in addition to physical Read/Write time. Outputs the identical value to the MON pin output.
O7	REC	Is set to "1" during Write-to-memory operation for recording.
O6	PLAY	Is set to "1" during Read-from-memory operation for playing.
O5	ERASE	Is set to "1" during Write-to-memory operation for erasing.
O4	PAUSE	Is set to "1" while pausing Recording/Playback or Erase operation.
O3	FULL	Is set to "1" simultaneously as the MON falling to "L", when Recording/Playback/Erase operation stops after the last address of the memory has been reached. This data bit is reset to "0" when REC, PLAY, ERASE, WRDT1, WRDT2 or SETRD command is input. This data bit is also fixed at "0" in Random Block Recording/Playback Mode.
O2	NAR	Is set to "1" when the next address input is enabled in Random Block Recording/Playback Mode. Outputs the identical value to the NAR pin output.
O1	PGM	Is set to "1" while writing digital data.
O0	READ	Is set to "1" while reading digital data.

11. WRDT1 Command (BH)

The WRDT1 command is used to erase the entire Sector (i.e. a memory area of 2,000 bits) and to write 250-bit digital data to the memory. Addressing is made in Sectors. The page address (A0 to A2) is automatically set to "0H".

By repeating this command eight times in succession, you can write 2,000-bit digital data. The page address within the Sector is automatically incremented.

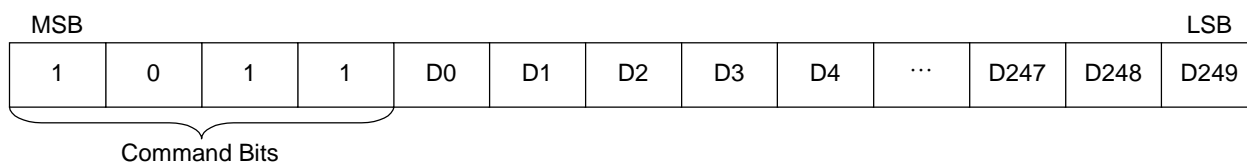
Remember that ML2517's on-chip flash memory is capable of storing both analog and digital data. Since there is no partitioning to differentiate the analog storage area from the digital storage area, you need to allocate a memory space for digital data storage where you are not planning to use for recording data.

The D0 to D249 digital data following the WRDT1 command is transferred to the internal register. When the data transfer is complete (after \overline{CS} input signal rising to "H"), the device starts writing data automatically to the specified address. During this Write operation the MON pin outputs "H" level.

To write the next 250-bit digital data within the specified Sector, run the WRDT1 command again after confirming the MON pin has fallen to "L" level. Do not input RESET nor any other commands than RDSTAT, RDADR and RDDT while repeating the WRDT1 command. Should you input RESET or any other commands than the above, the LSI will erase the specified Sector again to resume writing 250-bit data starting from 0H page address.

When a series of digital data Write session is complete, be sure to run a dummy command such as STOP. Once the WRDT1 command is executed, the LSI enters the ready state for the next WRDT1 command input, keeping the high-voltage circuit active, thus it consumes more power.

To write digital data to another Sector address, run the STADR command first for addressing and then run the WRDT1 command again, after confirming the MON pin has fallen to "L" level.



If the length of data to be transferred is less than 250 bits, the LSI writes the entire 250-bit data to memory assuming any blank data bits is "0".

You can't run the WRDT1 command during recording, playback, or erase operation.

12. WRDT2 Command (CH)

The WRDT2 command is used to erase two Sectors (i.e. a memory area of 4,000 bits) entirely and to write 250-bit digital data to the memory. Addressing is made in Sectors, but the lowest sector address bit (A3) and the Page address (A0 to A2) are automatically set to “0H”.

By repeating this command 16 times in succession, you can write 4,000-bit digital data. Page address within the Sector is automatically incremented.

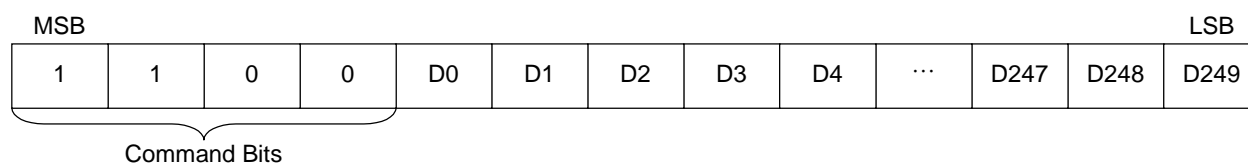
Remember that ML2517’s on-chip flash memory is capable of storing both analog and the digital data. Since there is no partitioning to differentiate the analog storage area from the digital storage area, you need to allocate a memory space for digital data storage where you are not planning to use for recording data.

The D0 to D249 digital data following the WRDT2 command is transferred to the internal register. When the data transfer is complete (after \overline{CS} input signal rising to “H”), the device starts writing data automatically to the specified address. During the Write operation the MON pin outputs “H” level.

To write the next 250-bit digital data within the specified Sector, run the WRDT2 command again after confirming the MON pin has fallen to “L” level. Do not input RESET nor any other commands than RDSTAT, RDADR and RDDT while repeating the WRDT1 command. Should you input RESET or any other commands than the above, the LSI will erase the specified Sector again to resume writing 250-bit data starting from 0H page address.

When a series of digital data Write session is complete, be sure to run a dummy command such as STOP. Once the WRDT2 command is executed, the LSI enters the ready state for the next WRDT1 command input, keeping the high-voltage circuit active, thus it consumes more power.

To write digital data to another Sector address, run the STADR command first for addressing and then run the WRDT2 command again, after confirming the MON pin has fallen to “L” level.



If the length of data to be transferred is less than 250 bits, the LSI writes the entire 250-bit data to memory assuming any blank data bits is “0”.

You can’t run the WRDT2 command during recording, playback, or erase operation.

13. SETRD Command (DH)

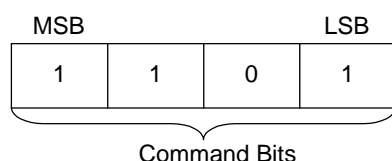
The SETRD command is used to transfer 250-bit digital data stored in the memory to the internal register. Prior to running this command, you need to specify a memory address from which the LSI retrieves data, by using the STADR command. Addressing is made in Pages.

The MON pin outputs “H” level while reading digital data.

After confirming the MON pin has fallen to “L”, you can use the RDDT command to output the data transferred to the internal register via the serial interface.

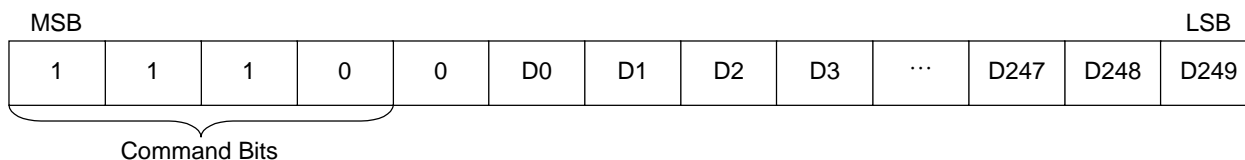
Any data following this command is disregarded.

Since the page address is not automatically incremented after running the SETRD command, you need to specify the next address with the STADR command before re-inputting the SETRD command, if you want to read out digital data from the following page.

**14. RDDT Command (EH)**

The RDDT command is used to output digital data from the internal register via the serial interface. Up to 250-bit digital data can be output in a single operation. Before running this command, the data should have been transferred to the internal register with the SETRD command. Addressing with the STADR command is also required prior to the transfer operation.

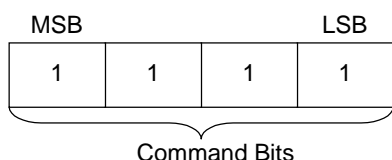
The data is output to the DO pin in sync with SCK clock input that follows RDDT command bits.

**15. PDWN Command (FH)**

Inputting the PDWN command causes the LSI to stop all of its internal operations and to enter low power consumption mode (Power-down mode).

Any data following this command is disregarded.

To reactivate the LSI, input “L” level to the $\overline{\text{RESET}}$ or $\overline{\text{CS}}$ pin.



16. Command List

Command Bits				Data Bits																Com- mand Name	Function							
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	...	260			
0	0	0	0	0	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NOOP	No particular function
				1	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Sequential Recording/Playback Mode
				X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Random Block Recording/Playback Mode
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Use Internal Clock
				0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Use External Clock, No dividing
				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Use External Clock, Divided by 2
				0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Use External Clock, Divided by 4
				0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Use External Clock, Divided by 8
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Block Size = 2-sector
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Block Size = 4-sector
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Block Size = 8-sector
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Block Size = 16-sector
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start recording at default/last-defined sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start recording at 4.0 kHz sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start recording at 5.3 kHz sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start recording at 6.4 kHz sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start playing at default/last-defined sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start playing at 4.0 kHz sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start playing at 5.3 kHz sampling frequency
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start playing at 6.4 kHz sampling frequency
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Stop recording/playing/erasing
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Pause/Resume recording/playing/erasing
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start erasing at default/last-defined sampling frequency
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start erasing at 4.0 kHz sampling frequency
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start erasing at 5.3 kHz sampling frequency
				0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Start erasing at 6.4 kHz sampling frequency
				0	1	1	0	0	X	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	—	—		Specify Start/Block Address
				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Specify Stop Address
				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Read Address
				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Read Status Register Value
				1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Write Digital Data 1
				1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Write Digital Data 2
				1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Transfer Retrieved Digital Data to internal Register
				1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Read Digital Data
				1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Power Down

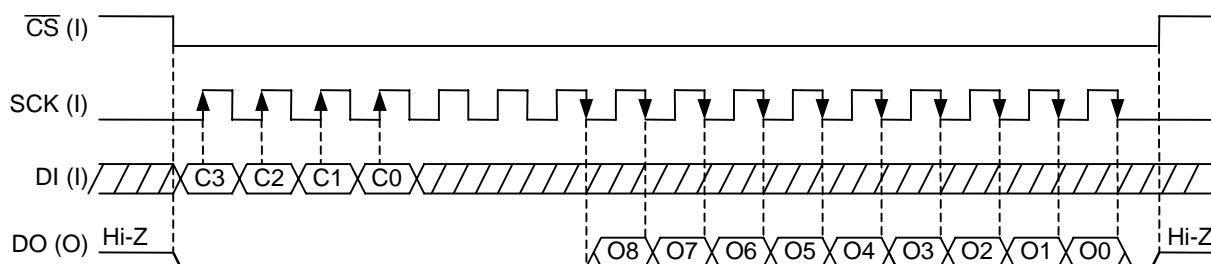
Serial Peripheral Interface (SPI)

The ML2517 uses the industry-standard Serial Peripheral Interface (SPI) to interface with an external MCU. The LSI determines Mode 0 or Mode 1 automatically with the SCK level at \overline{CS} pin's falling edge. When the SCK is "L" level at \overline{CS} pin's falling edge, it selects Mode 0, while if the SCK pin is "H" level at \overline{CS} pin's falling edge, Mode 1 is selected.

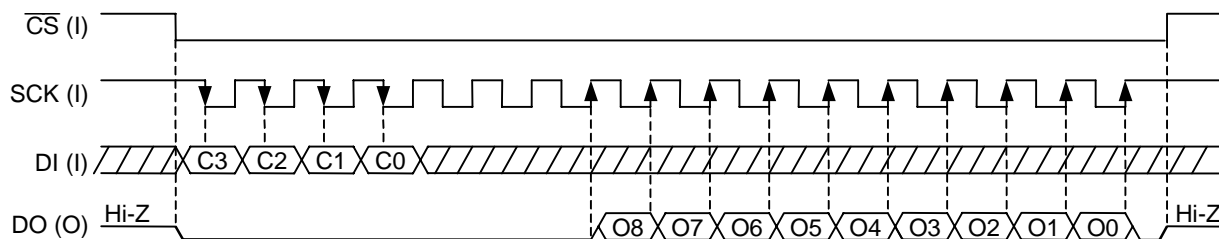
In Mode 0, the LSI captures the DI pin input at a SCK's rising edge and outputs data to the DO pin at a SCK's falling edge. On the other hand, the LSI captures the DI pin input at a SCK's falling edge and outputs data to the DO pin at a SCK's rising edge in Mode 1.

The following diagrams show timings for data input/output in Mode 0 and Mode 1.

Timings for Data Input/Output in Mode 0



Timings for Data Input/Output in Mode 1



1. Timings for Writing a Command and Data

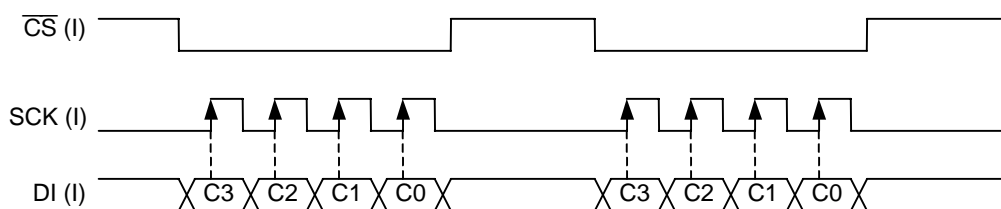
This section describes timings for writing a command and data in Mode 0.

After “L” level input to the \overline{CS} pin, input a command followed by data in serial order, starting with the MSB, to the DI pin in sync with the SCK signal. The data on the DI pin is loaded to the LSI’s internal shift register at SCK’s rising edges. The command is executed at \overline{CS} ’s rising edge.

However, for RDADR, RDSTAT, WRDT1, WRDT2 and RDDT commands, the command are executed as soon as 4-bit command bits are input. For any other commands than the above, the command input is disregarded when the \overline{CS} pin turns to “H” level at any other bits than 4th, 8th, 16th or 24th bit.

Please note that settings defined by the MODE command and sampling frequency defined by REC, PLAY and ERASE commands will be changed whenever the \overline{CS} pin turns to “H” level at any bit.

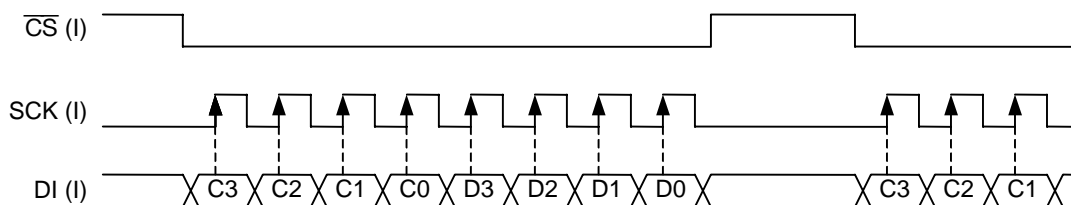
4-bit Command Format



<Applicable Commands>

REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN commands

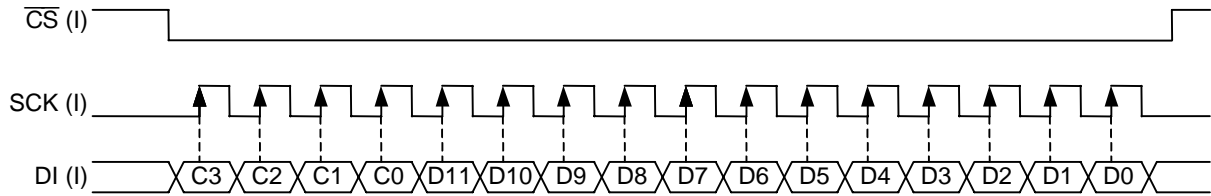
8-bit Command Format



<Applicable Commands>

MODE, REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN commands

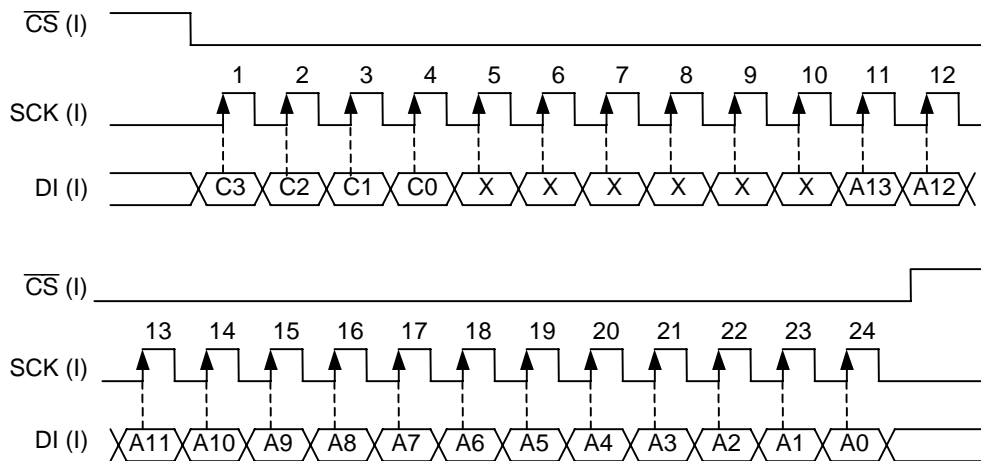
16-bit Command Format



<Applicable Commands>

MODE, REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN commands

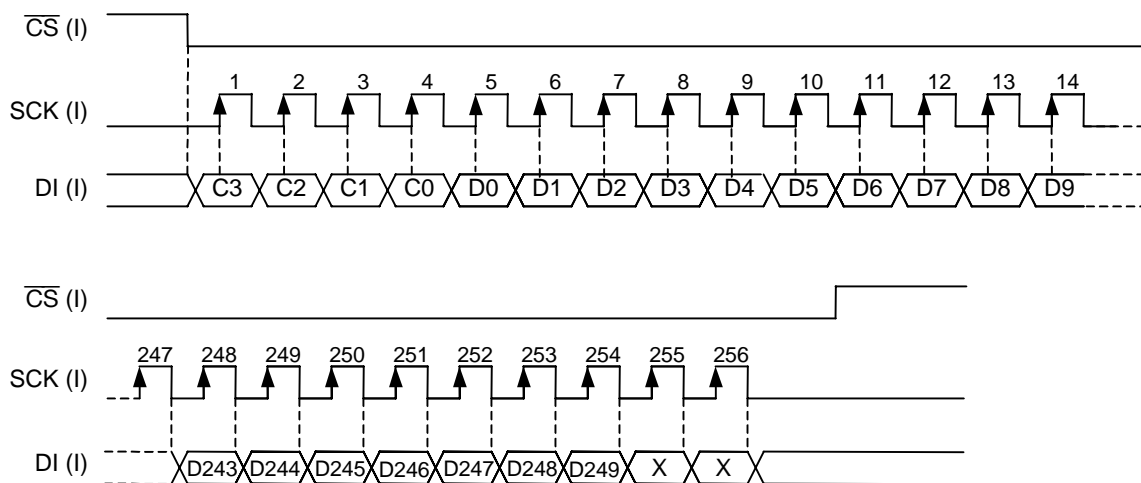
24-bit Command Format



<Applicable Commands>

STADR, SPADR, MODE, REC, PLAY, STOP, PAUSE, ERASE, SETRD, PDWN commands

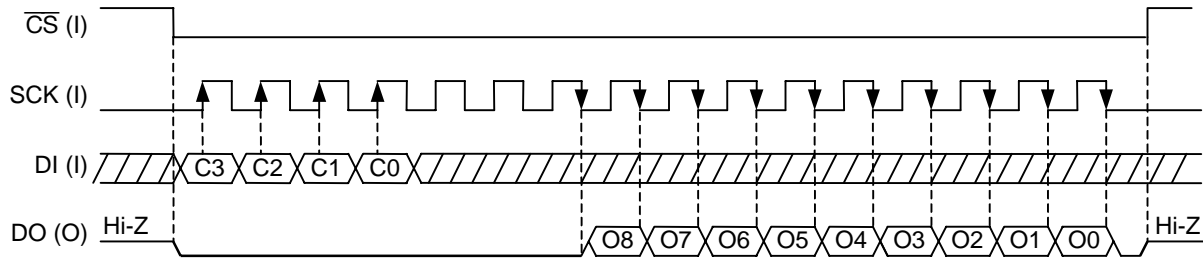
Timings for Writing Digital Data (WRDT1, WRDT2 commands)



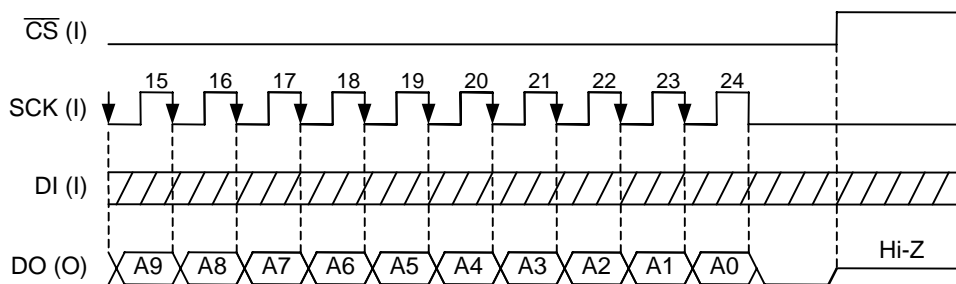
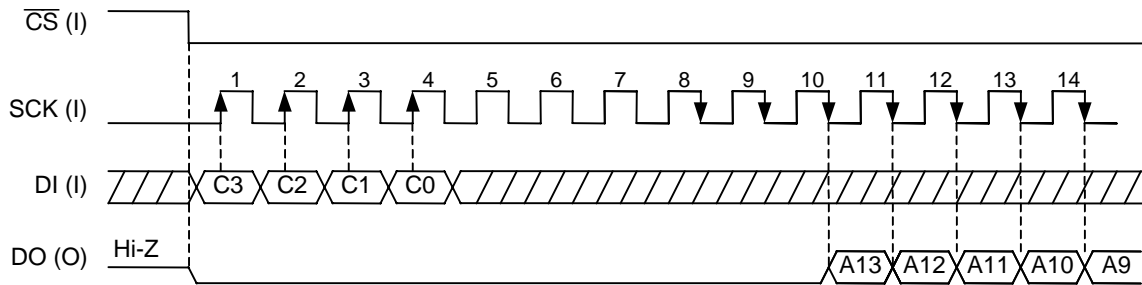
2. Timings for READ Commands

This section describes timings for reading data with RDSTAT, RDADR and RDDT commands in Mode 0. With the \overline{CS} pin at "L" level, the LSI outputs serial data starting with the MSB, to the DO pin in sync with the SCK's third pulse falling edge after 4-bit command input. After reading data, bringing the \overline{CS} pin to "H" level returns the DO pin to Hi-Z state, regardless of SCK pulse count.

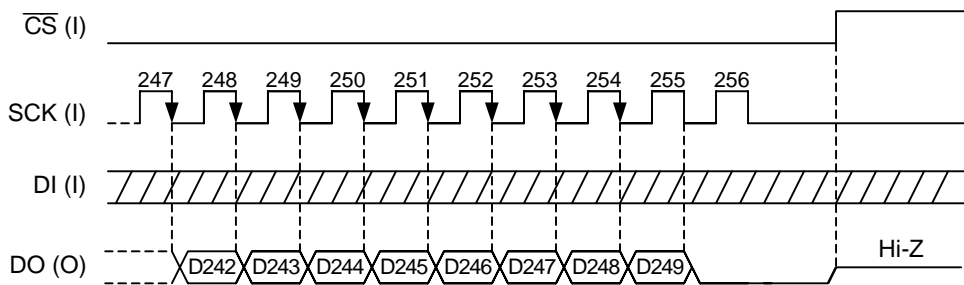
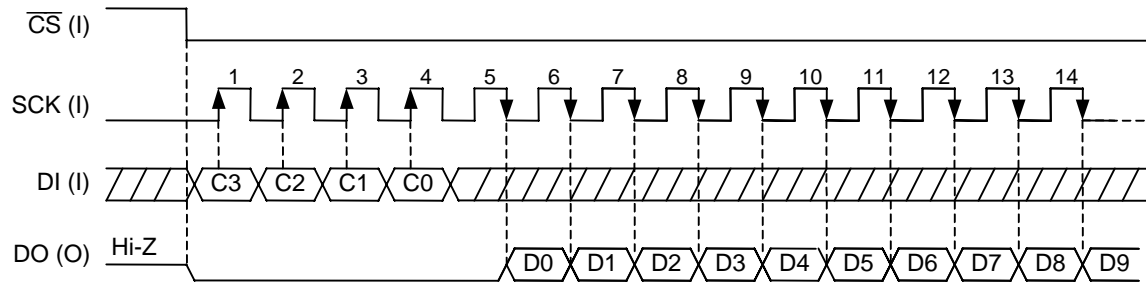
Timings for reading Status Register Data (RDSTAT Command)



Timings for reading Memory Address Counter Data (RDADR Command)



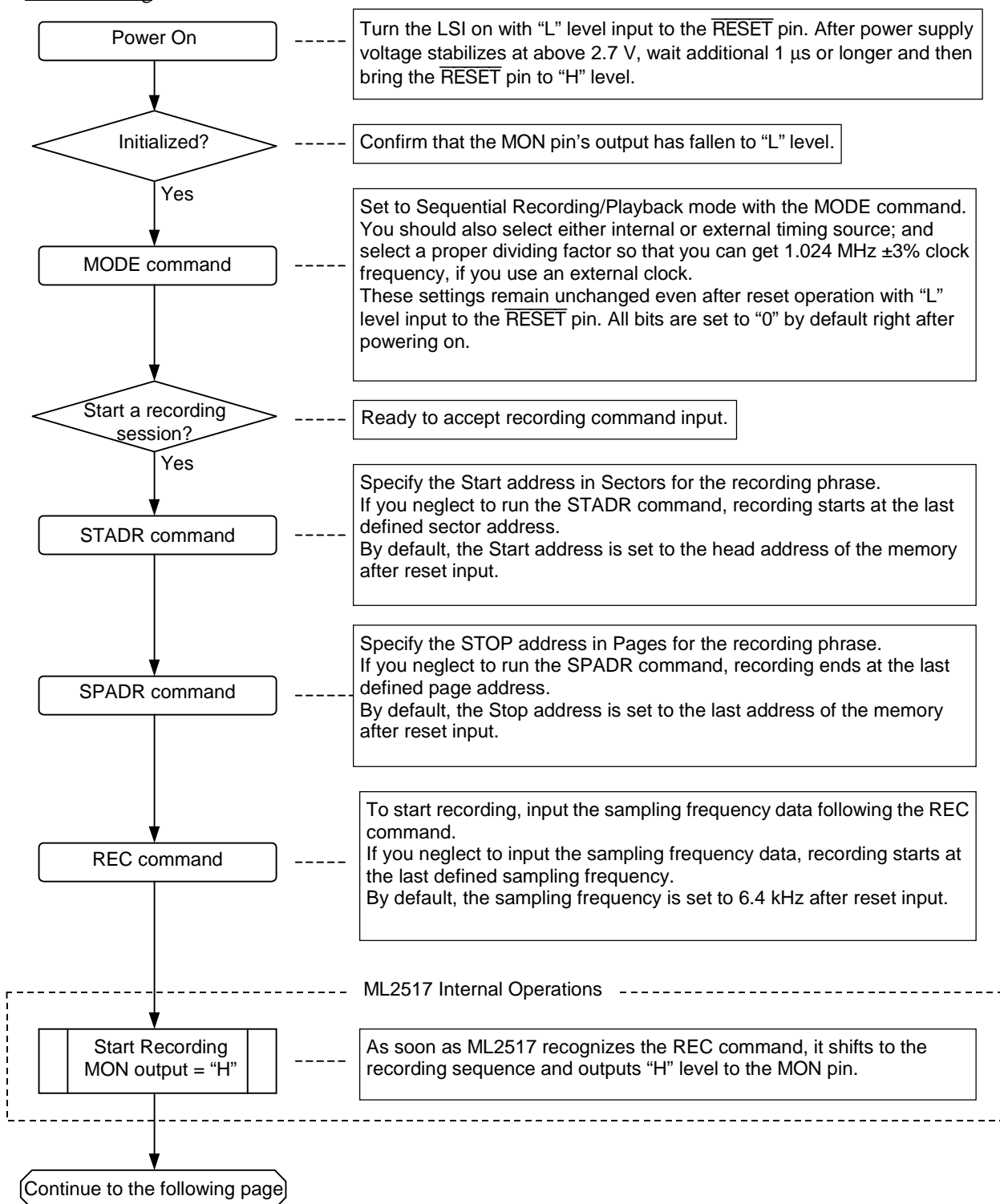
Timings for Reading Digital Data (RDDT command)

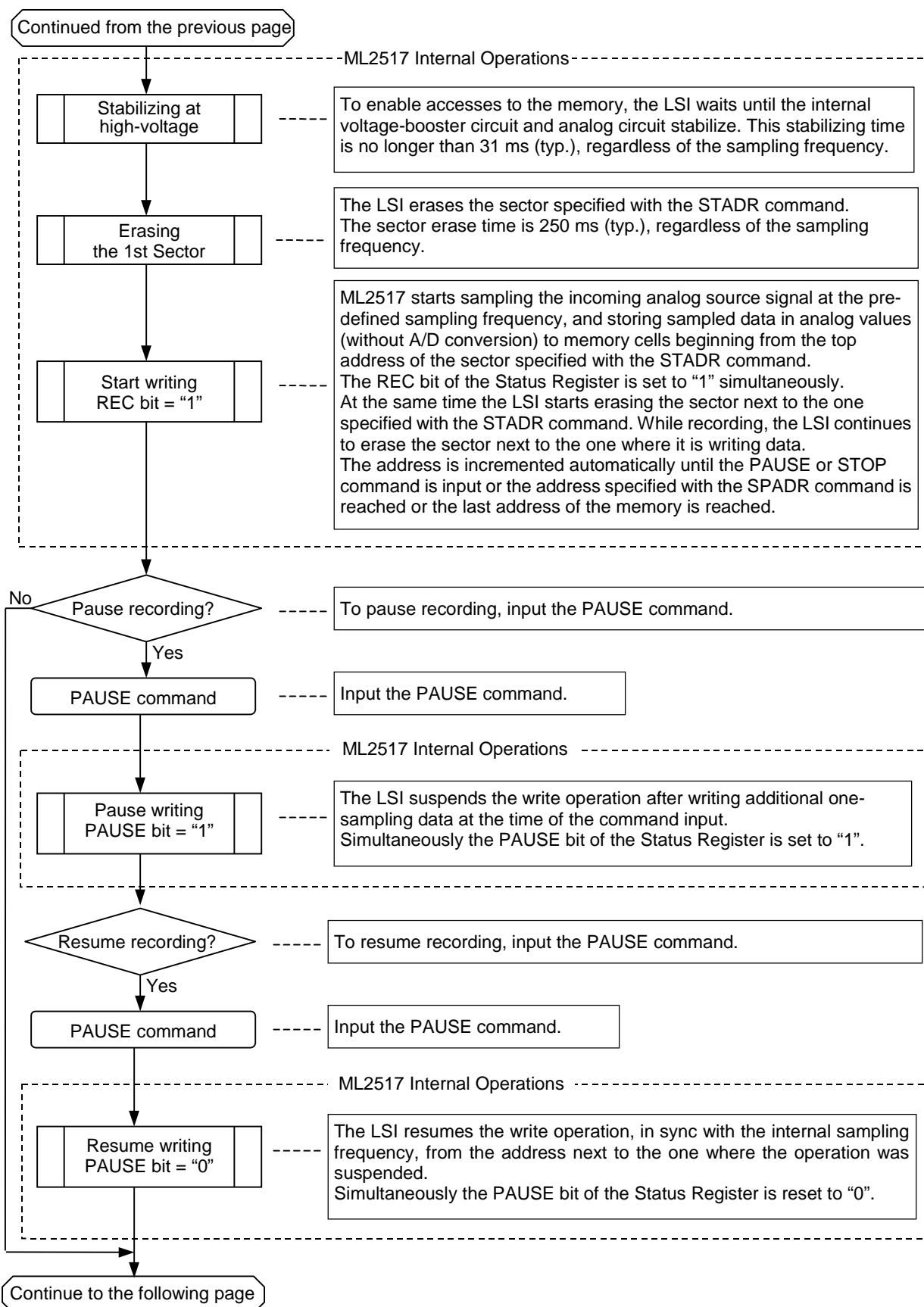


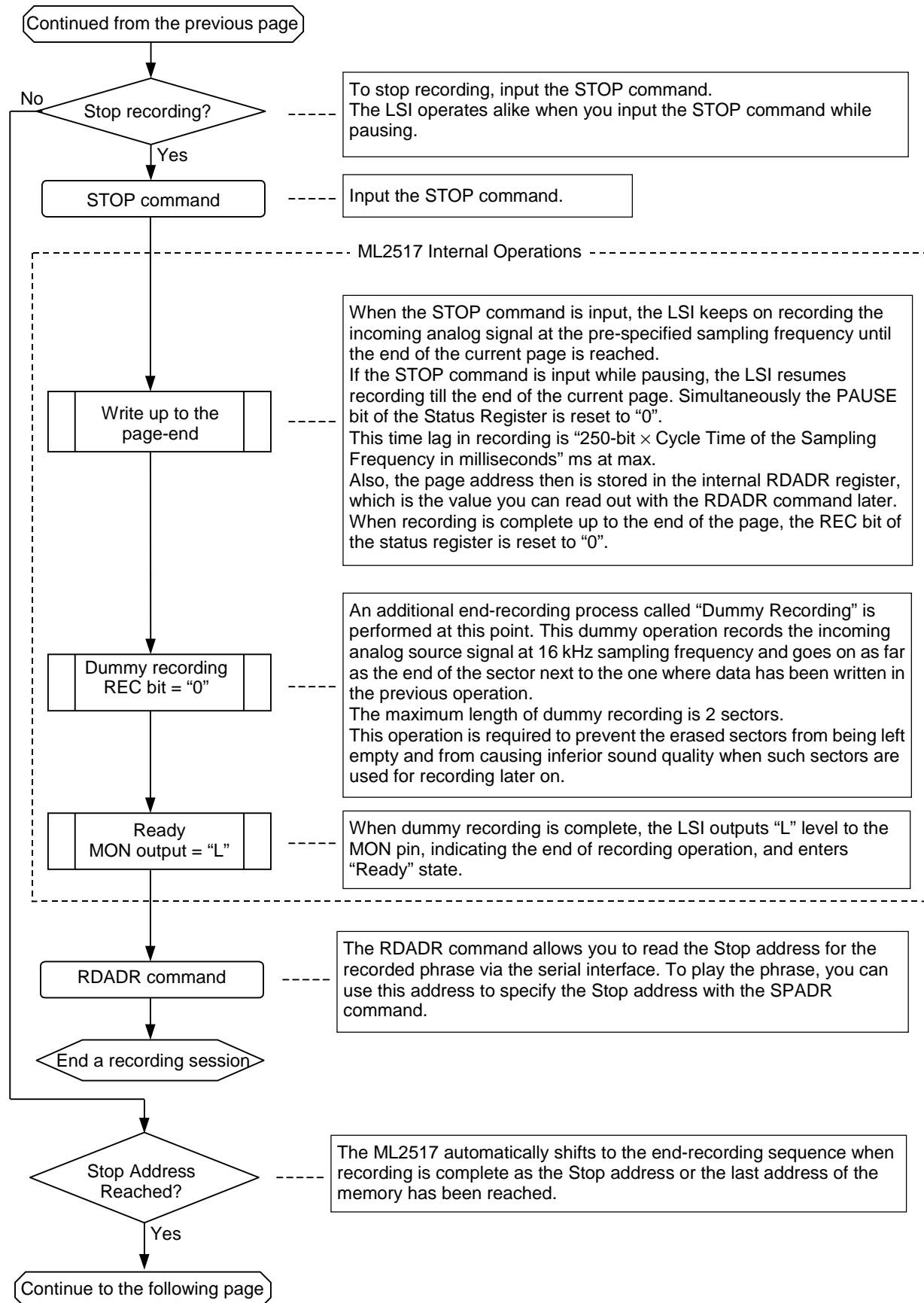
Operations in Sequential Recording/Playback Mode

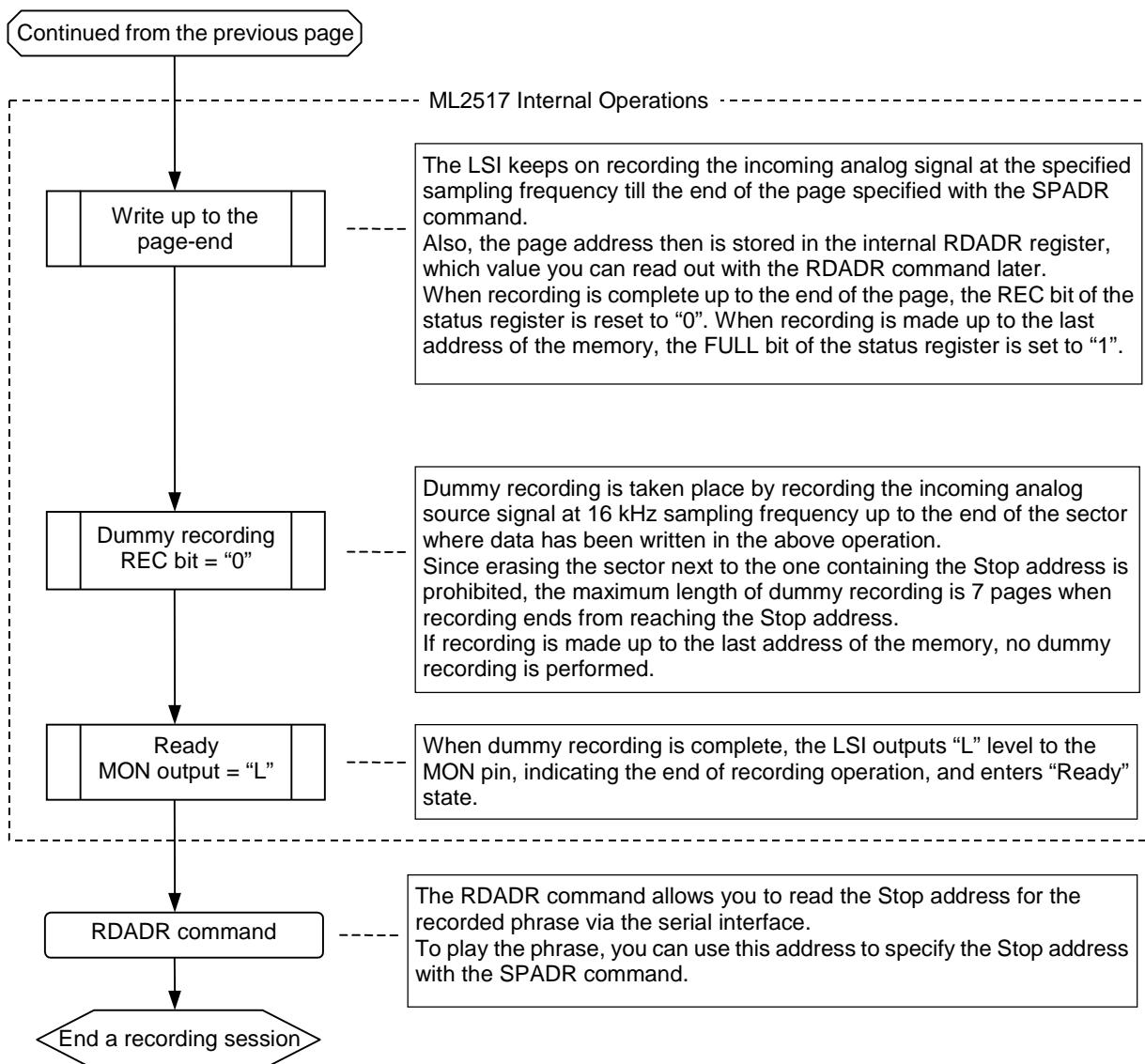
This section describes how to control Recording, Playback and Erase operations in Sequential Recording/Playback mode.

1. Recording

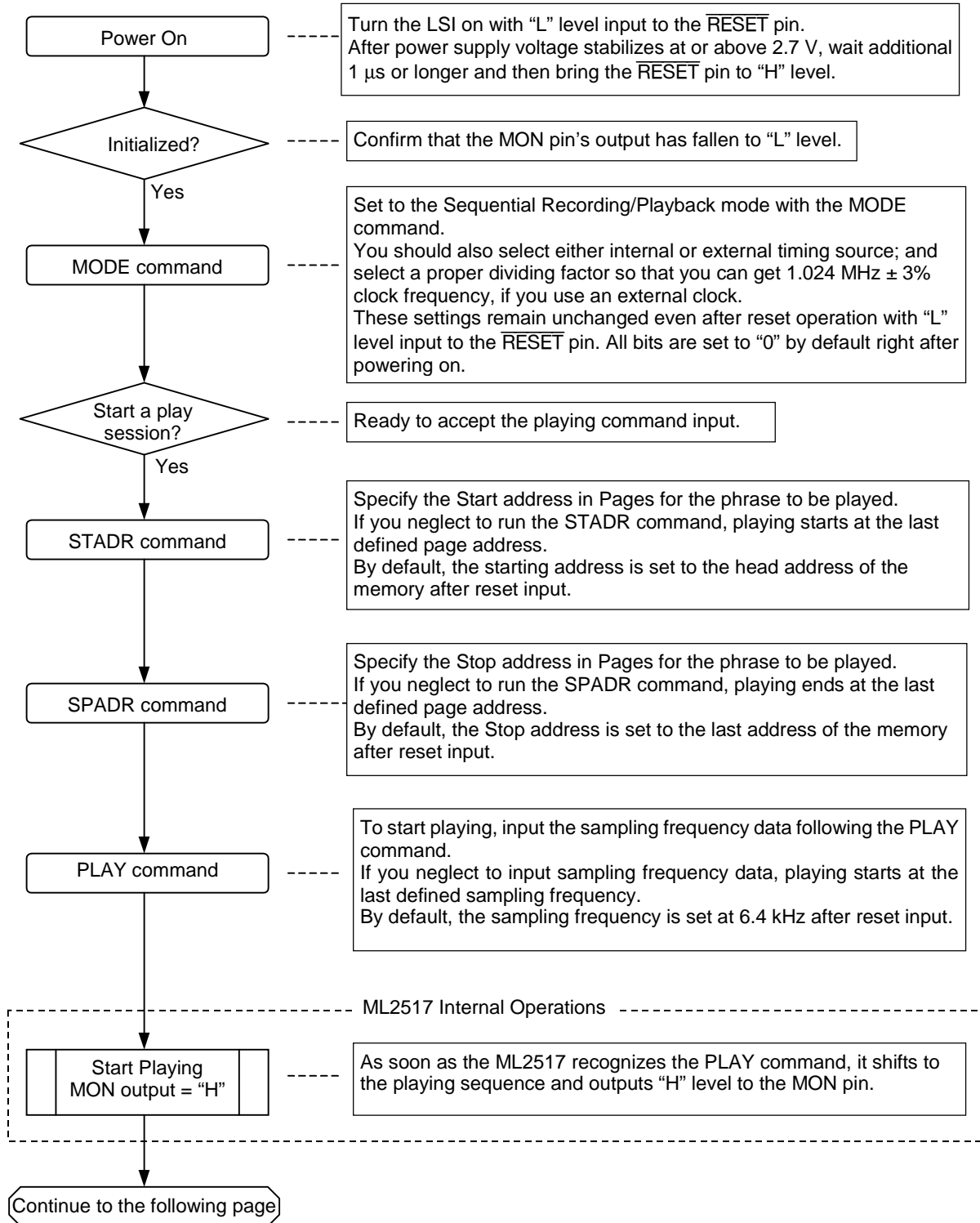


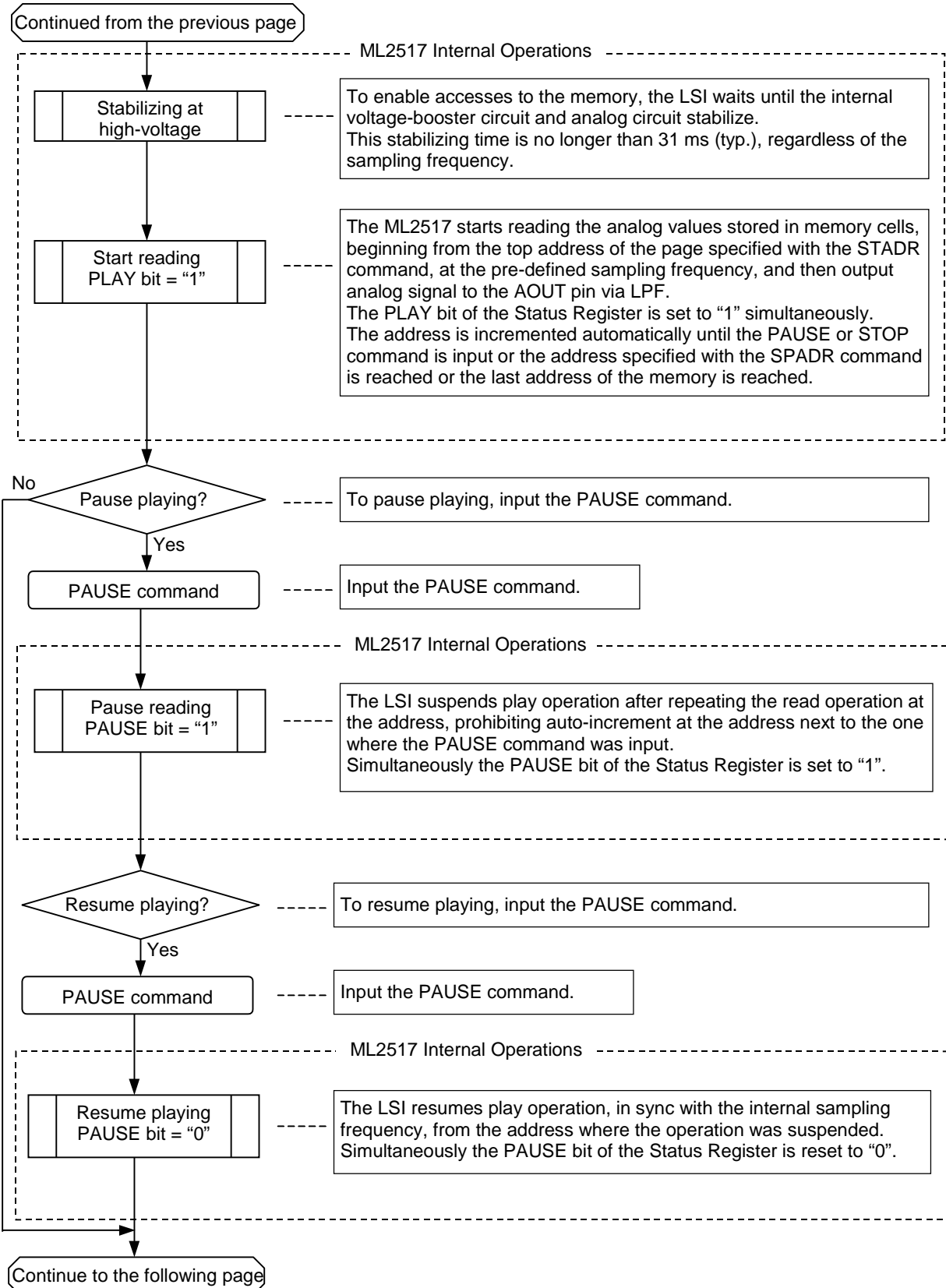


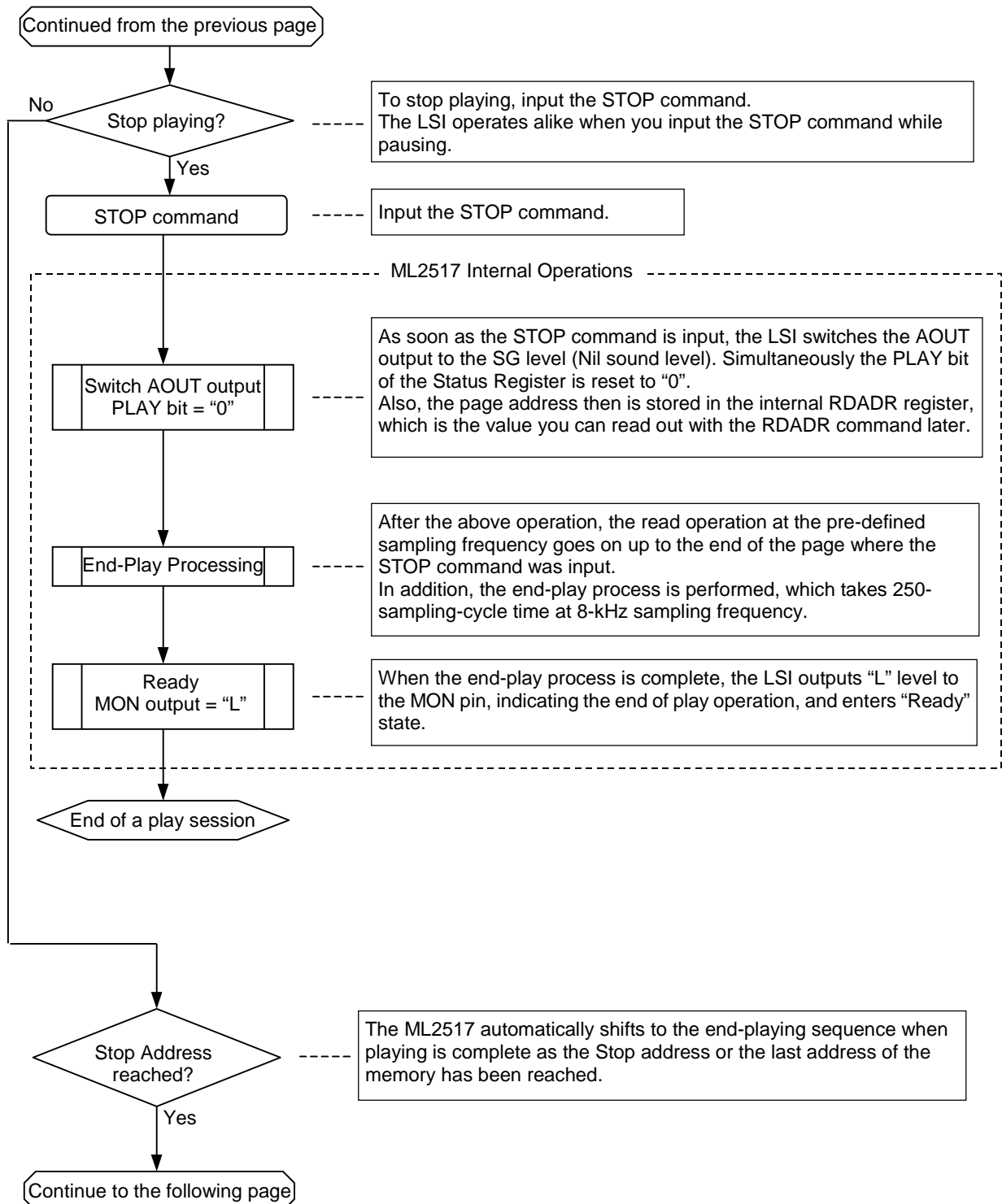


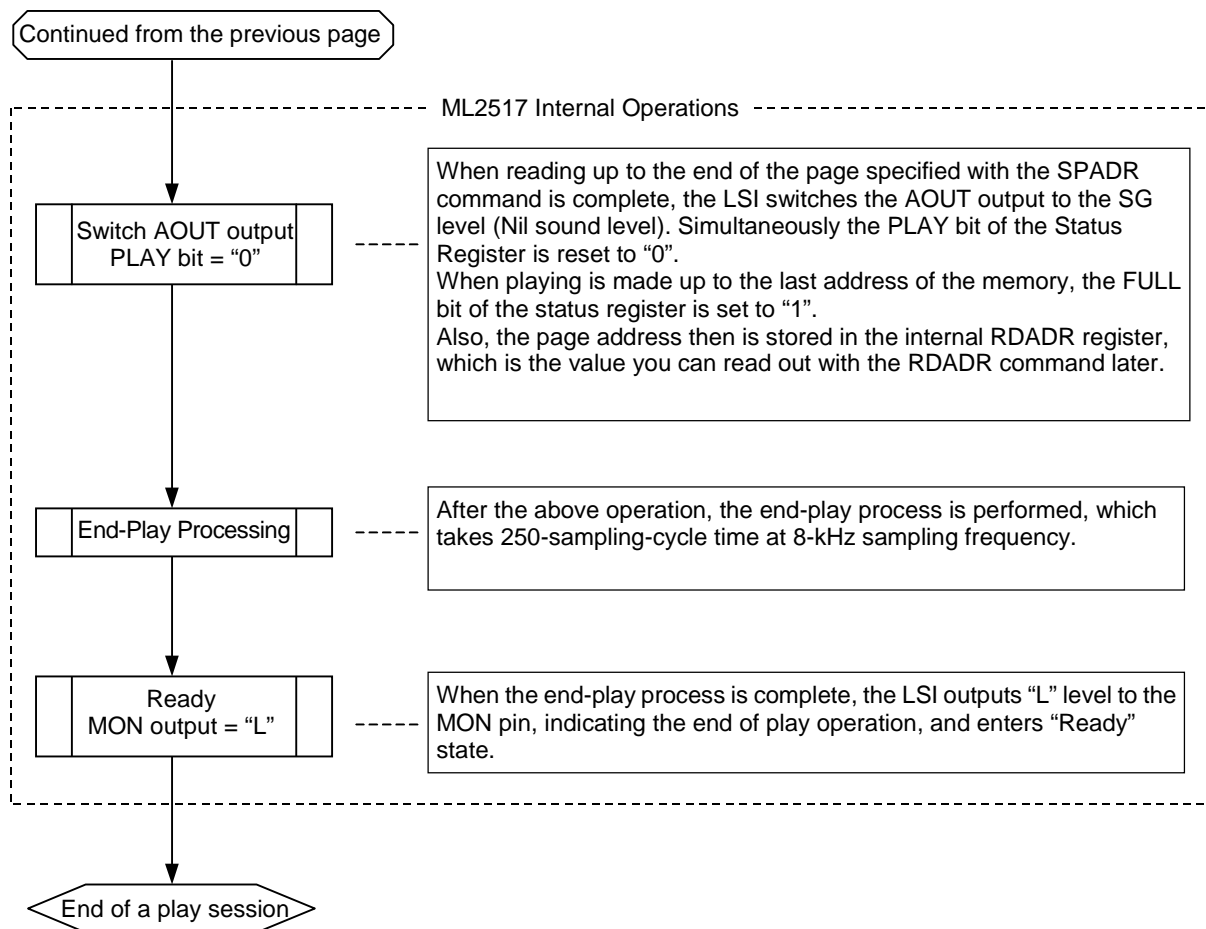


2. Playing









3. Erasing

An erasing operation with the ERASE command is identical to the recording operation with the REC command, except that the analog input signal line is forced to be switched to the SG level internally.

4. Controlling Phrase Addresses

In Sequential Recording/Playback Mode, you can record or play each phrase by controlling the Start and Stop addresses for each phrase.

1) Addressing during record operation

You can specify the Start address for recording in Sectors (A3 to A13) by using the STADR command. The page address is automatically set to "0H" and recording starts at the top address of each sector. Meanwhile, you can specify the Stop address for recording in Pages (A0 to A13) by using the SPADR command.

To read an address during recording or at the end of recording, use the RDADR command.

2) Addressing during play operation

You can specify the Start address for playing in Pages (A0 to A13) by using the STADR command. You also can specify the Stop address for playing in Pages (A0 to A13) by using the SPADR command. To read an address during playing or at the end of playing, use the RDADR command.

3) Sample operations of controlling addresses

This section describes a sample operation of controlling addresses for 8-phrase recording/playing. The total memory space is divided into 8 equal-space memory areas that are assigned to each phrase. To start recording a phrase, input the REC command after setting up the Recording-Start and Recording-Stop addresses by using the STADR and SPADR commands, as shown in the following table.

Phrase	Recording/Playing-Start Address	Recording-Stop Address	Playing-Stop Address (Examples)
1	0000H	07FFH	06E3H
2	0800H	0FFFH	0DF2H
3	1000H	17FFH	1700H
4	1800H	1FFFH	1A11H
5	2000H	27FFH	25FEH
6	2800H	2FFFH	2CC0H
7	3000H	37FFH	35DFH
8	3800H	3FFFH	3E63H

When recording a phrase is complete, you should save the last address of the recorded phrase, which can be used to specify the Playing-Stop Address for the phrase. To start playing a phrase, input the PLAY command after setting up the Playing-Start and Playing-Stop addresses by using the STADR and SPADR commands.

These addresses can also be stored by using a part of the ML2517's memory.

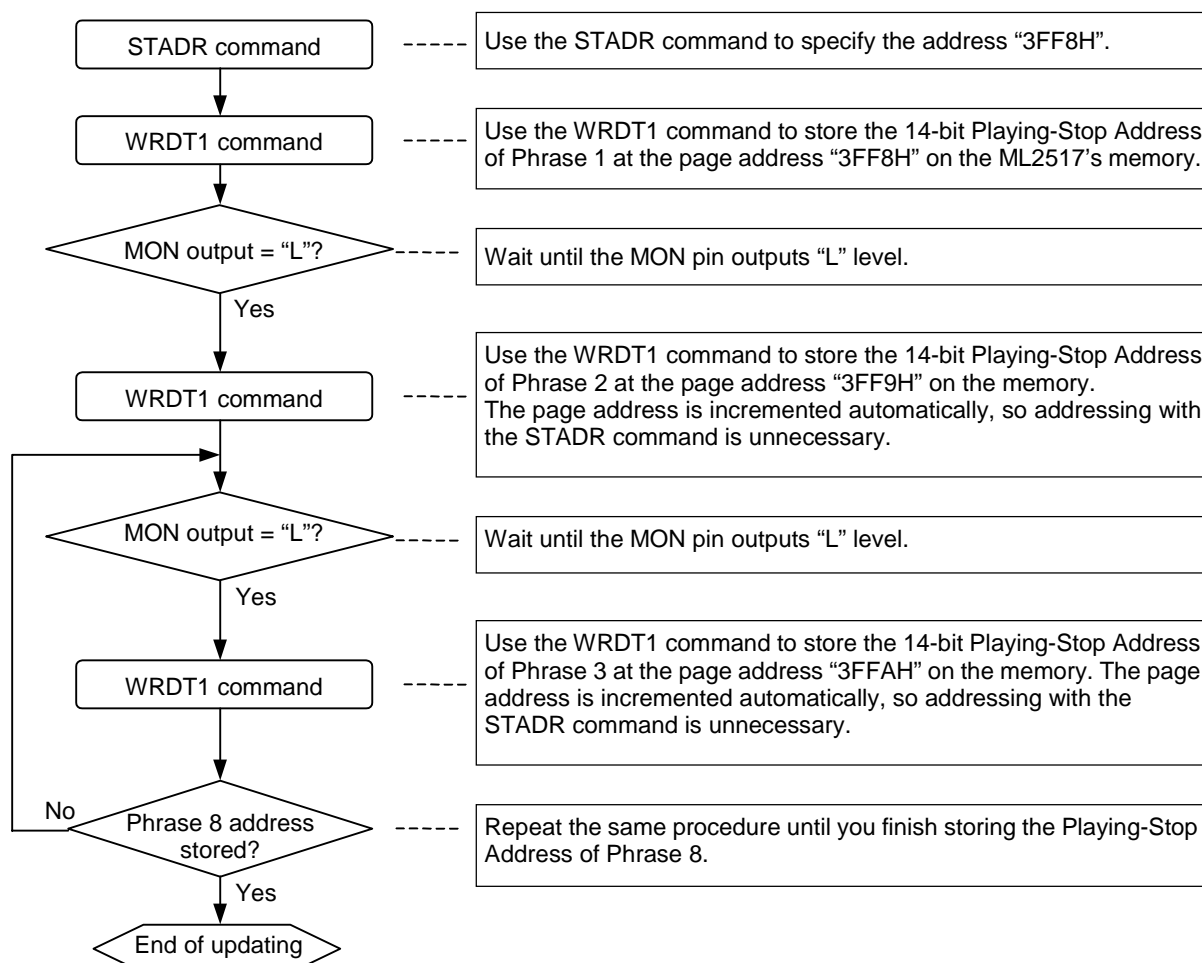
Here's another sample operation where you record or play 8 phrases and store the Playing-Stop Address of each phrase in the ML2517's memory.

Memory areas for recording each phrase and for storing the Playing-Stop Address of each phrase are assigned as shown in the following table.

Phrase	Recording/Playing-Start Address	Recording-Stop Address	Page Address for Storing Playing-Stop Address
1	0000H	07FFH	3FF8H
2	0800H	0FFFH	3FF9H
3	1000H	17FFH	3FFAH
4	1800H	1FFFH	3FFBH
5	2000H	27FFH	3FFCH
6	2800H	2FFFH	3FFDH
7	3000H	37FFH	3FFEH
8	3800H	3FF7H (Note)	3FFFH

(Note) The memory area assigned to Phrase 8 is smaller than the other phrases.

To update the Playing-Stop Address of each phrase, follow the workflow shown below:



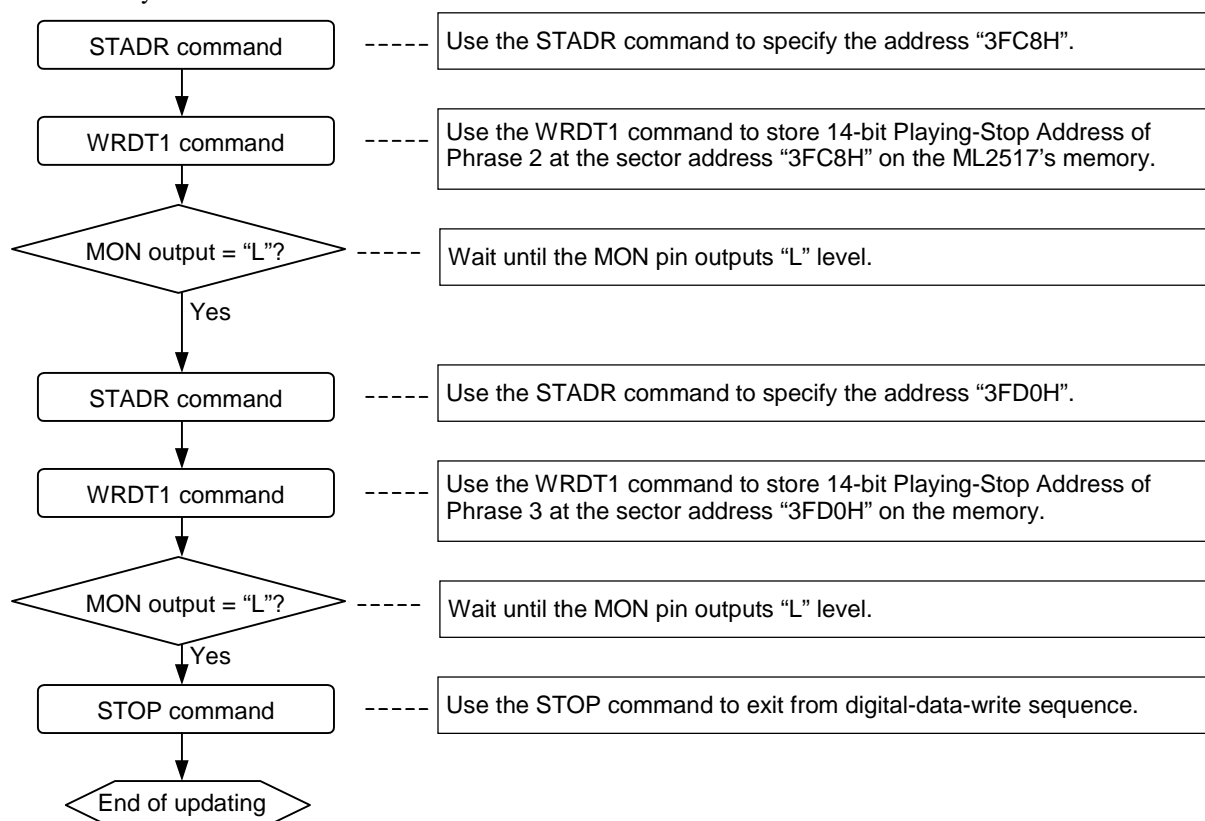
Because executing the first WRDT command erases data at 3FF8H to 3FFFH, you should store Playing-Stop Address data for all 8 phrases.

Here's another sample operation that allows you to update the Playing-Stop Address of modified phrases only, instead of storing the addresses of all 8 phrases. This becomes possible by assigning a Sector address for storing the Playing-Stop Address of each phrase.

Phrase	Recording/Playing-Start Address	Recording-Stop Address	Sector Address for Storing Playing-Stop Address
1	0000H	07FFH	3FC0H
2	0800H	0FFFH	3FC8H
3	1000H	17FFH	3FD0H
4	1800H	1FFFH	3FD8H
5	2000H	27FFH	3FE0H
6	2800H	2FFFH	3FE8H
7	3000H	37FFH	3FF0H
8	3800H	3FBFH (Note)	3FF8H

(Note) The memory area assigned to Phrase 8 is smaller than the other phrases.

The following diagram shows a workflow to update the Playing-Stop Addresses of Phrase 2 and Phrase 3 only:

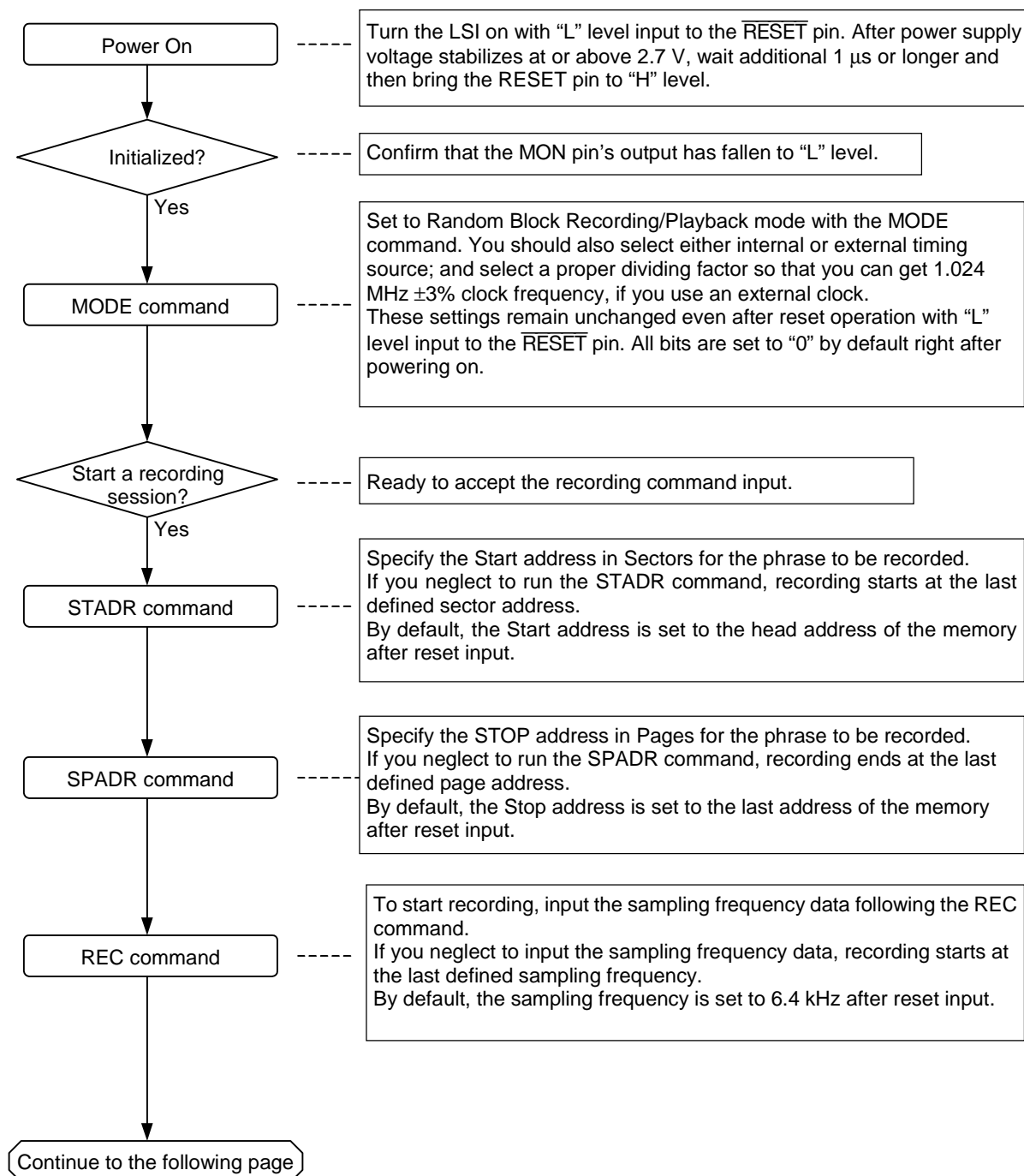


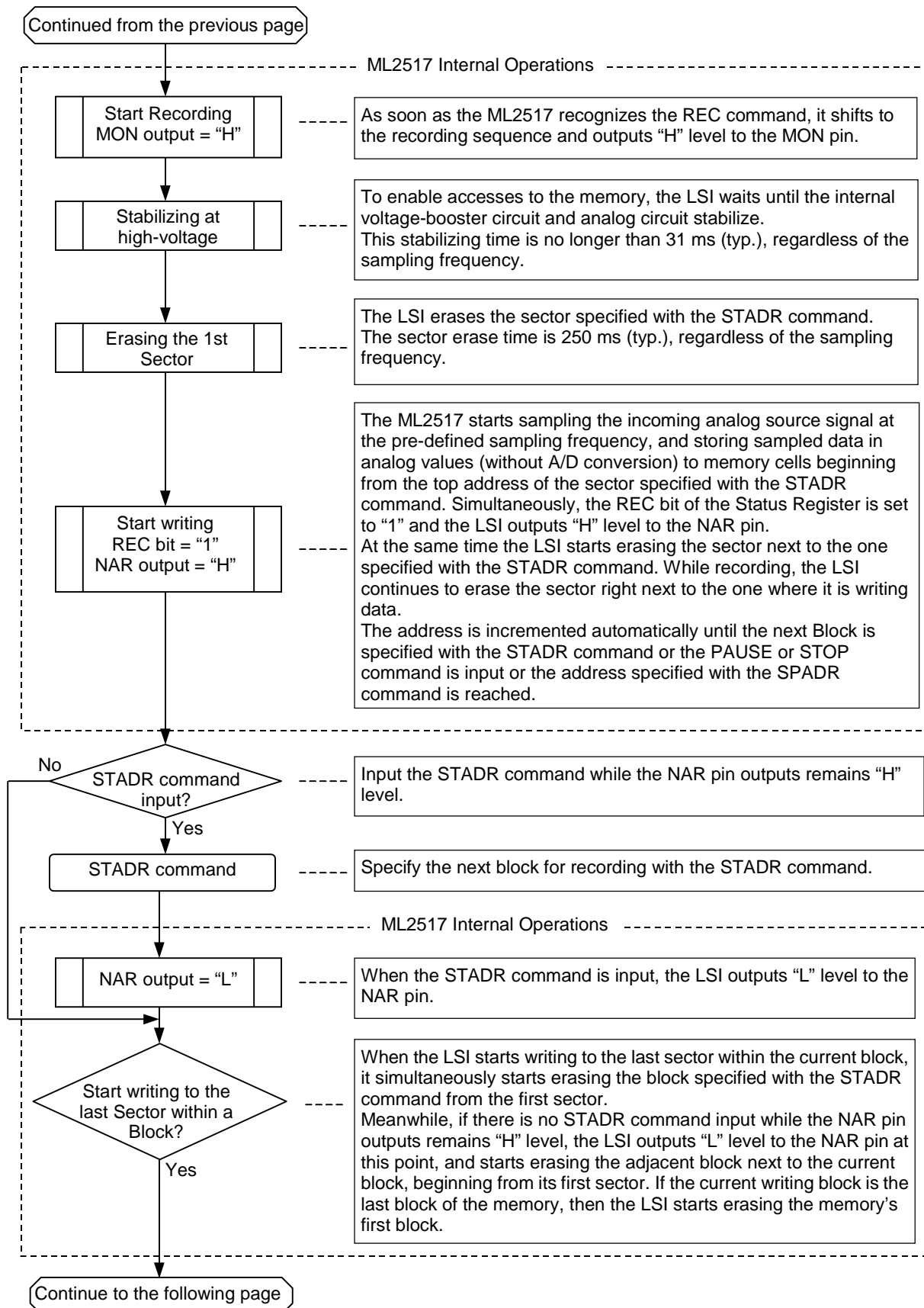
In the above operation, first you should specify a sector address for storing, and after series of data storing operations, you must input the STOP command.

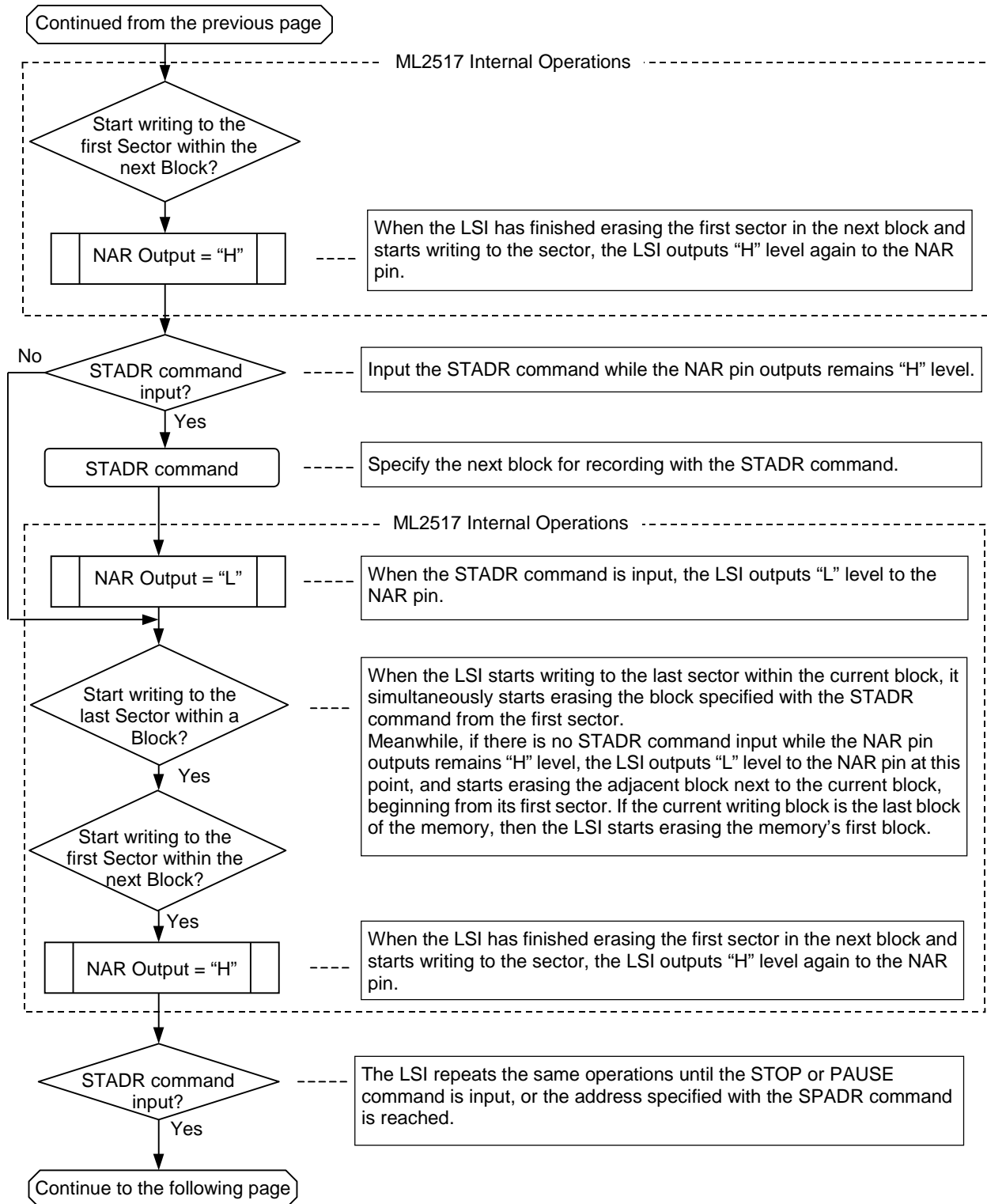
Operations in Random Block Recording/Playback Mode

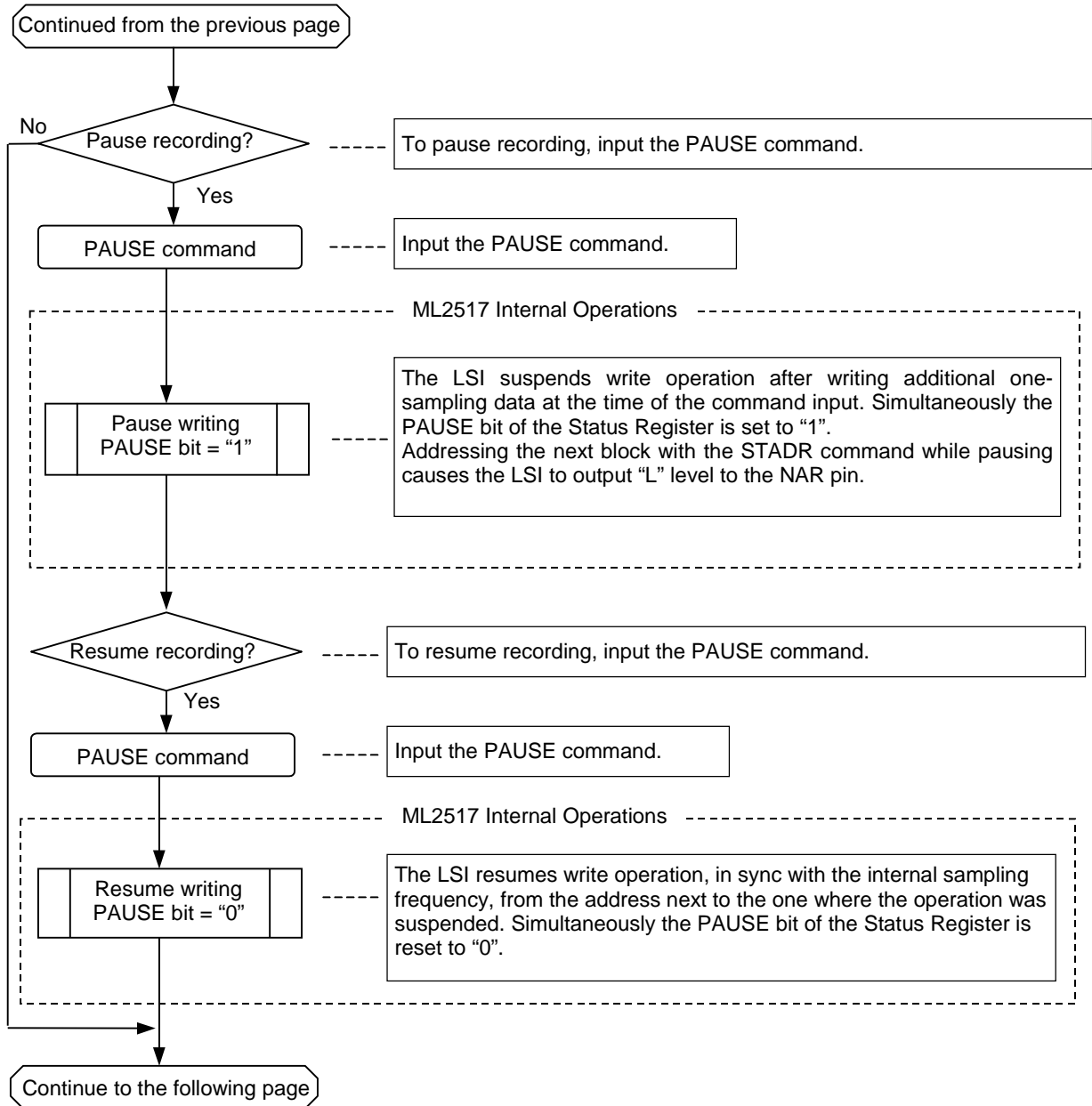
This section describes how to control Recording, Playing and Erasing operations in Random Block Recording/Playback mode.

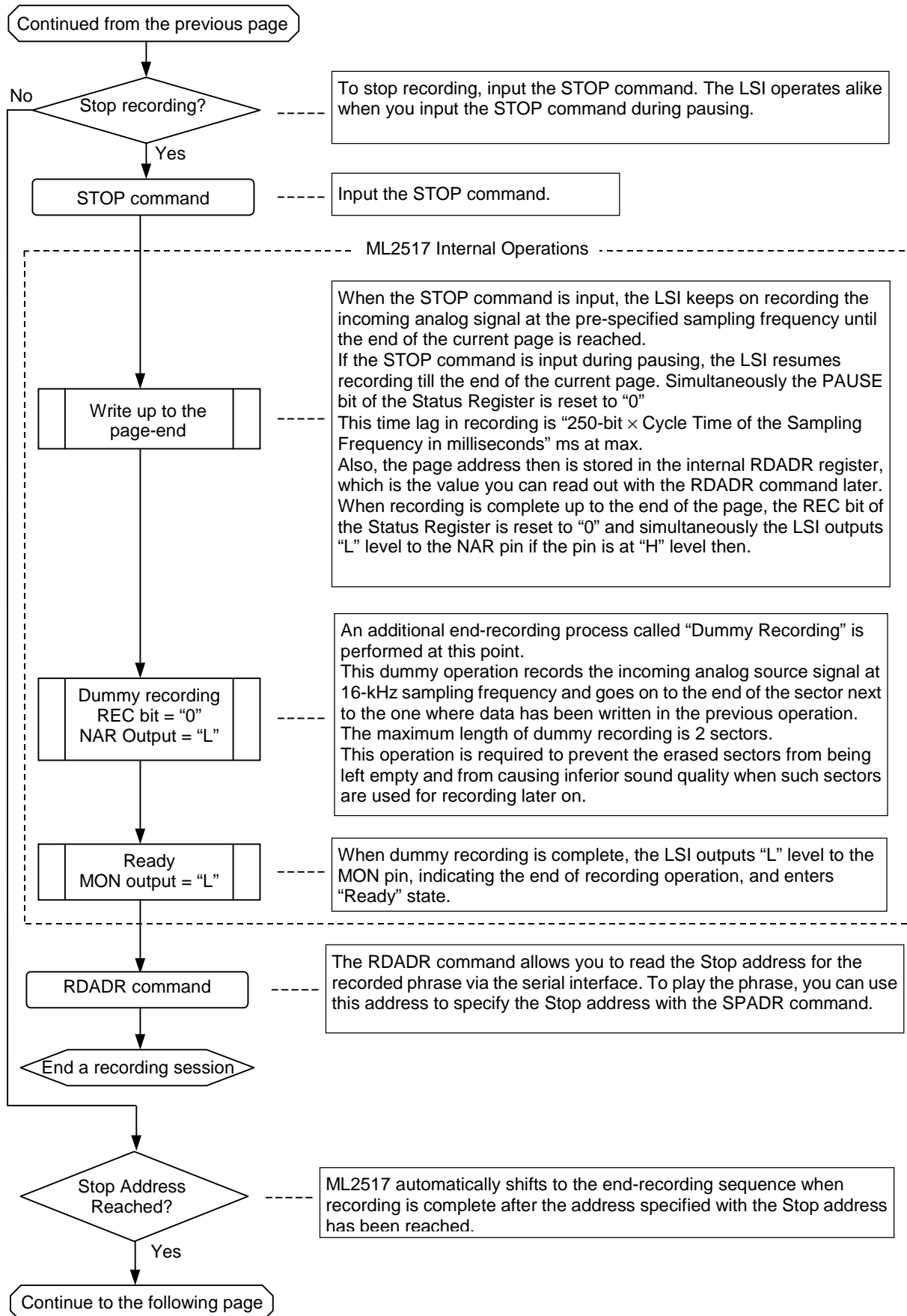
1. Recording

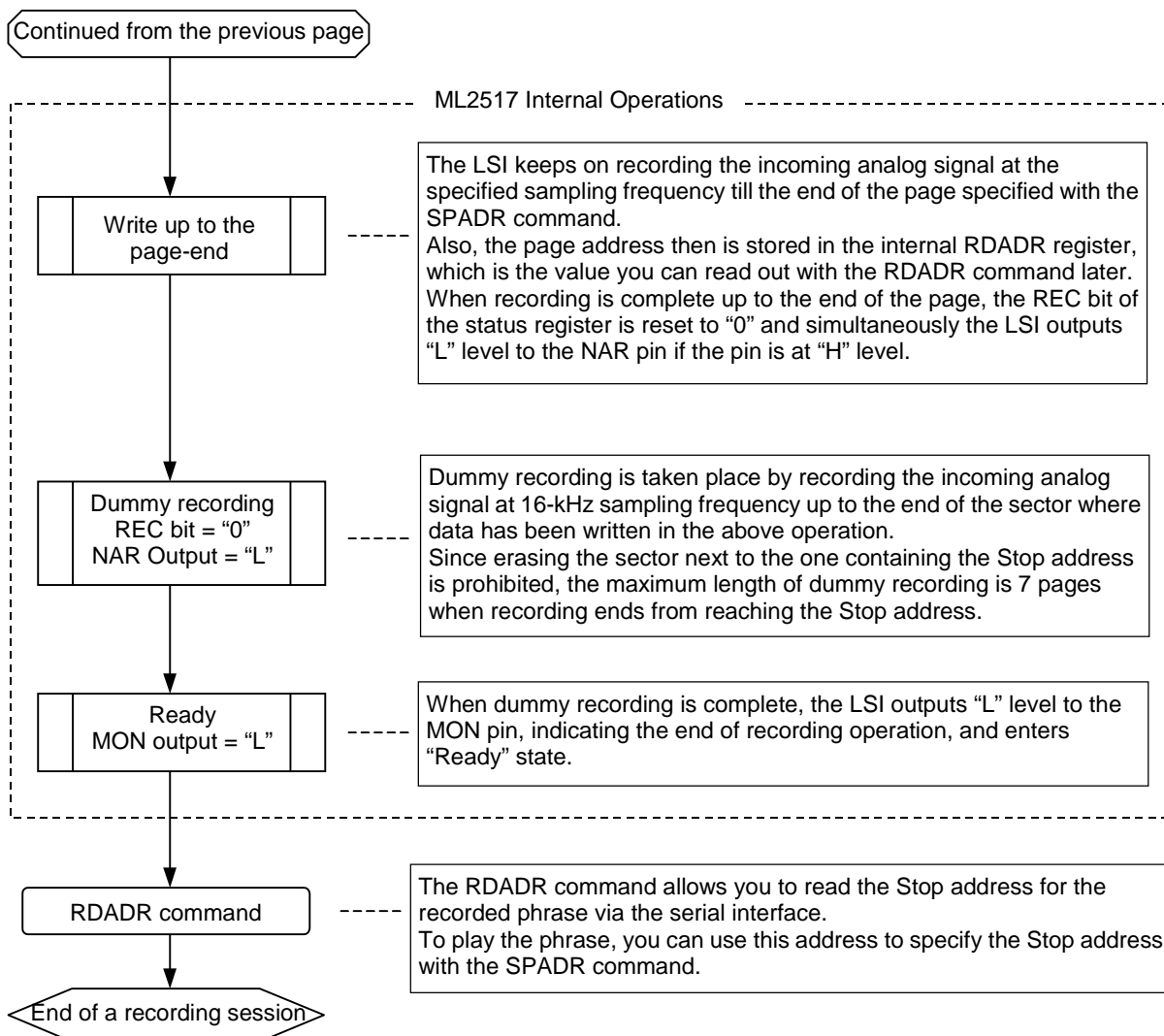




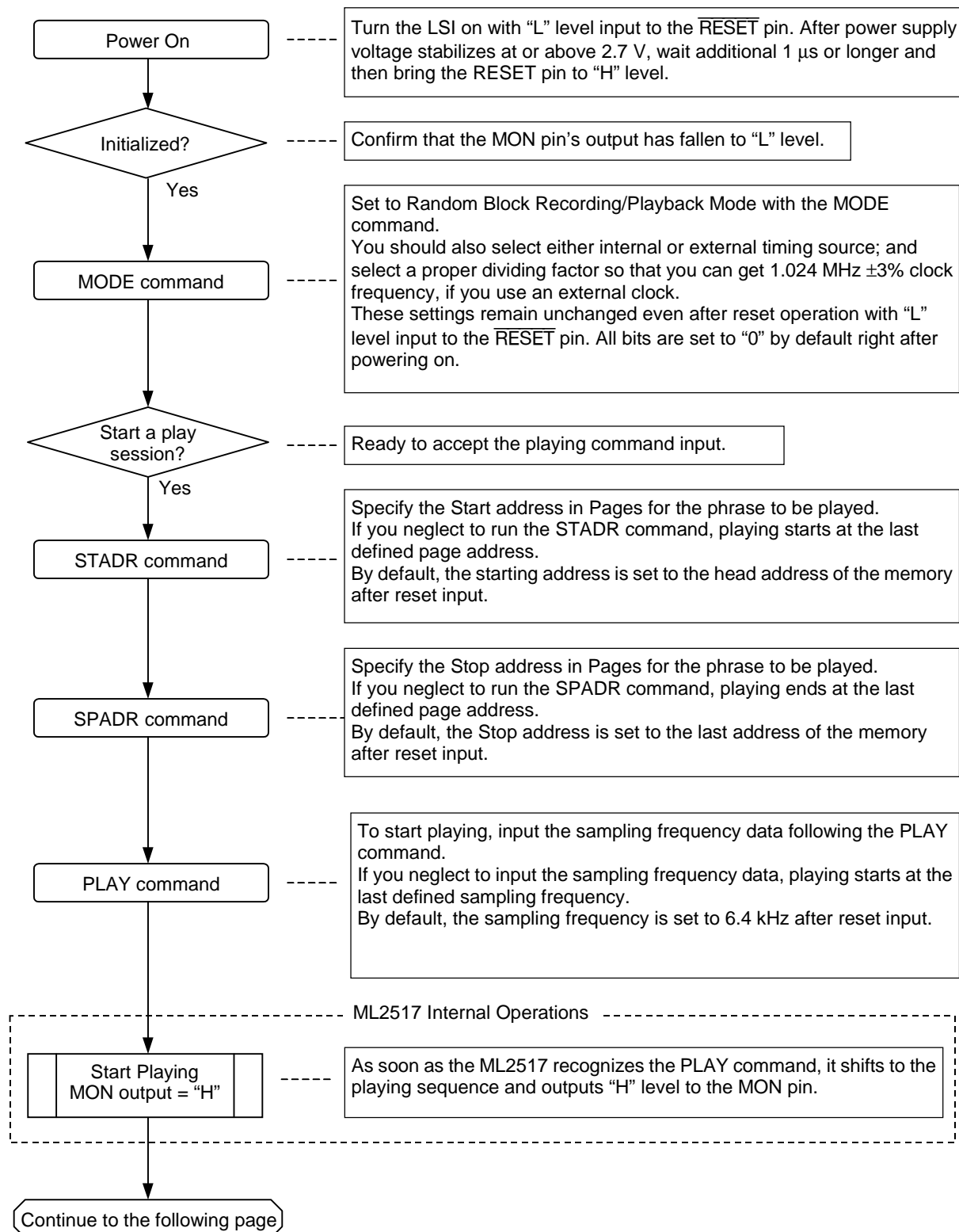


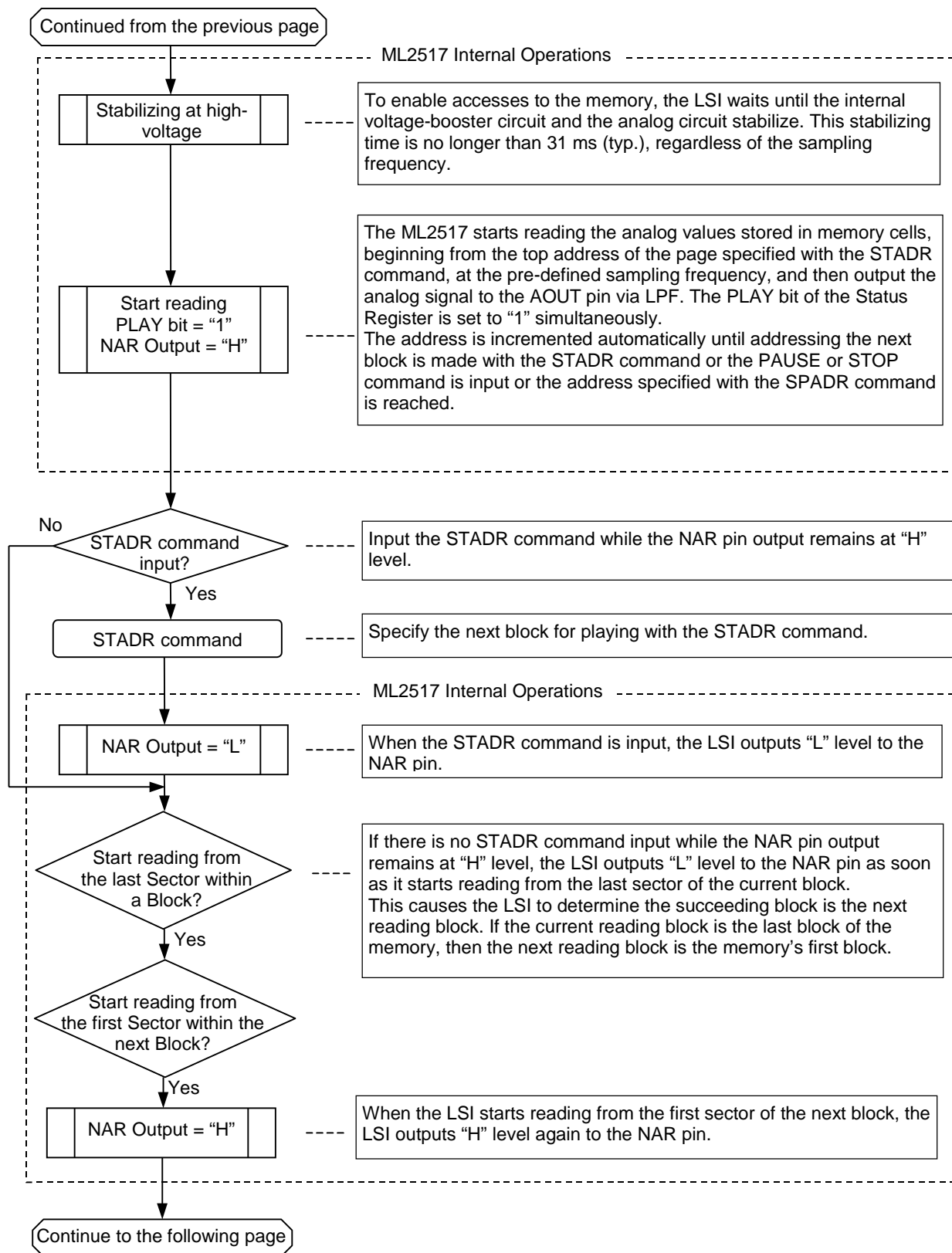


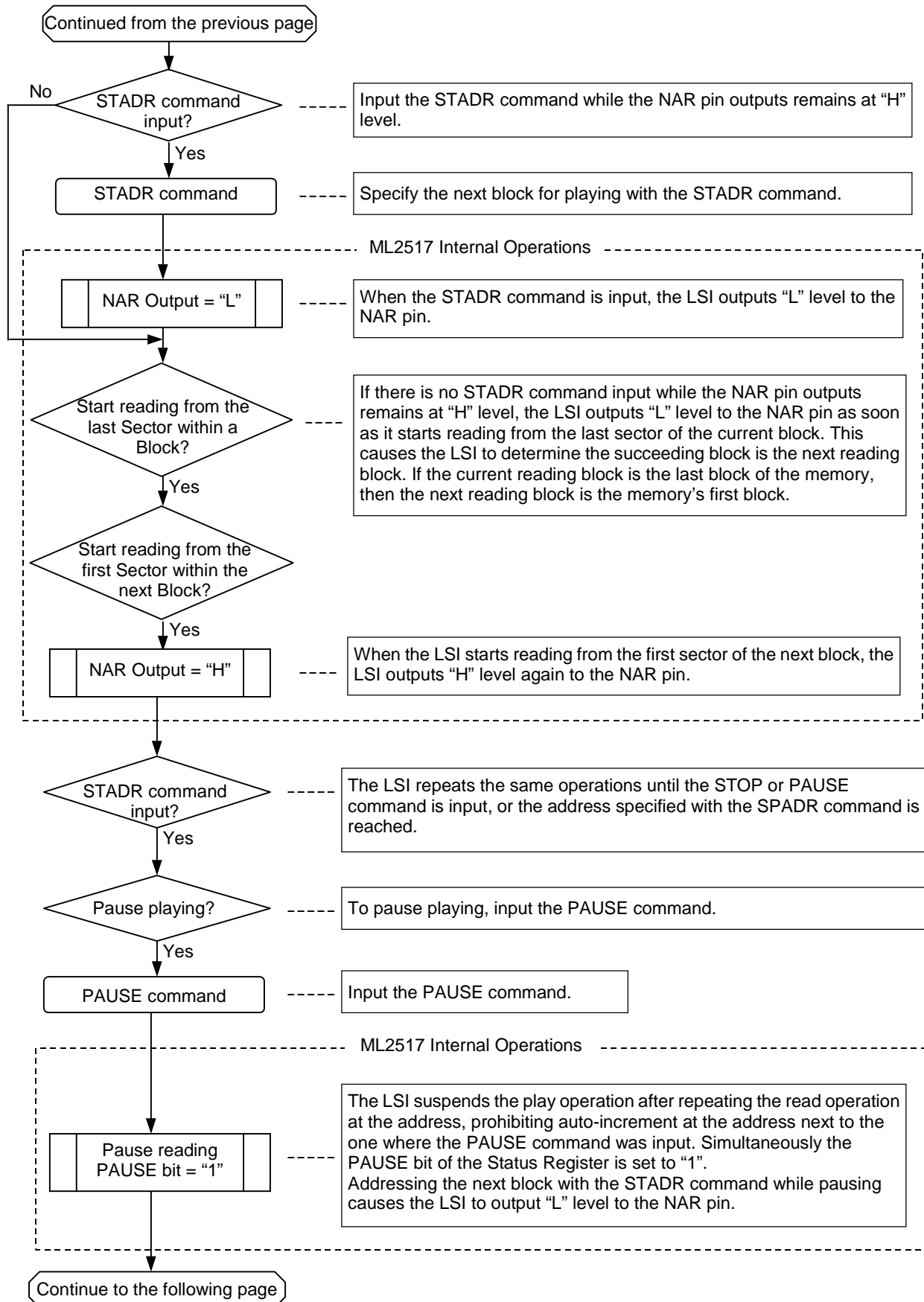


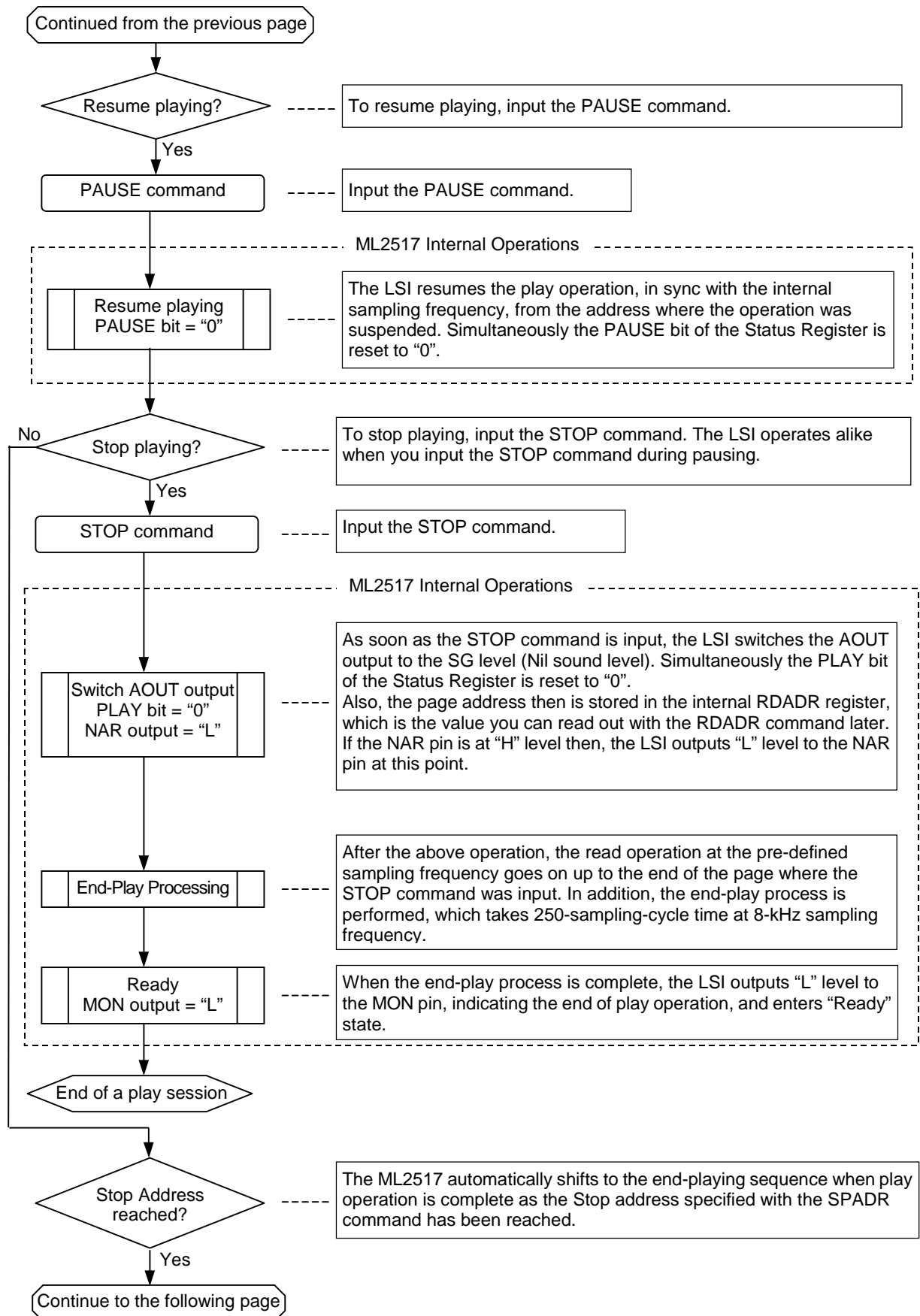


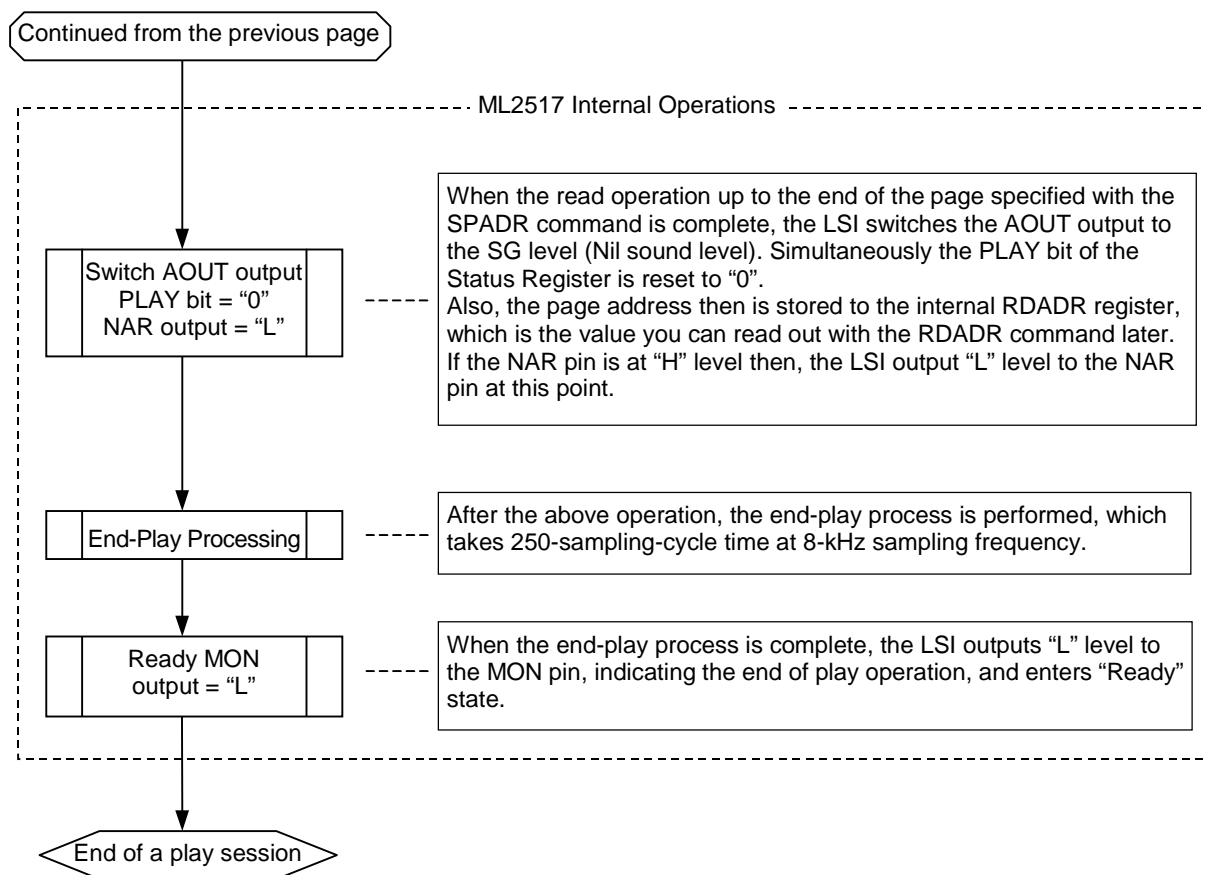
2. Playing











3. Erasing

The erasing operation with the ERASE command is identical to the recording operation with the REC command, except that the analog input signal line is forced to be switched to the SG level internally.

4. Controlling Phrase Addresses

In Random Block Recording/Playback Mode, you can record or play each phrase by controlling the Start and Stop addresses and Block address used for each phrase.

1) Addressing during recording operation

You can specify the Start address for recording in Sectors (A3 to A13) by using the STADR command. The Page address is automatically set to "0H" and recording starts at the top address of each sector. The sector address specified is not necessarily the first sector within the block.

Meanwhile, you can specify the Stop address for recording in Pages (A0 to A13) by using the SPADR command.

During recording, you can specify the memory area to be used in Blocks with STADR command. The size of a block varies depending on your setting. The following table shows valid address bits when you input the STADR command and number of blocks for each block size.

Block Size	Valid Address Bits	Number of Blocks
2 Sectors	A4 to A13	1024
4 Sectors	A5 to A13	512
8 Sectors	A6 to A13	256
16 Sectors	A7 to A13	128

The invalid lower address bits are set to "0H" automatically.

To read an address during recording or at the end of recording, use the RDADR command.

2) Addressing during playing operation

You can specify the Start address for playing in Pages (A0 to A13) by using the STADR command.

You also can specify the Stop address for playing in Pages (A0 to A13) by using the SPADR command.

During playing, you can specify the memory area to be used in Blocks with STADR command. The valid address bits for each block size are identical to those for recording.

To read an address during playing or at the end of playing, use the RDADR command.

3) Sample operations of controlling addresses

This section describes a sample operation of controlling addresses for 8-phrase recording/playing.

You prepare a memory map as shown below, to see used and unused blocks in the entire memory and used blocks by each phrase.

These sample operations assume that a block consists of 16 sectors, and the total number of blocks is 128.

Memory Map before Recording

Phrase	Block No.												
	1	2	3	4	5	6	7	8	9	10	11	...	128
Entire memory	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 1	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 2	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 3	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 4	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 5	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 6	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 7	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 8	0	0	0	0	0	0	0	0	0	0	0	...	0

The above table shows the memory map when the entire memory is unused.

“0” represents an unused block while “1” represents a used block.

When you record Phrase 1 for the first time, the entire memory has not been used yet. So, you can specify “0000H” (the memory’s top address) for the Start address and “3FFFH” (the memory’s last address) for the Stop address by using the STADR and SPADR commands respectively. Then, input the REC command. When you specify the next recording block after confirming NAR Output = “H”, use the STADR command to select a block starting from Block No. 2 in serial order.

The memory map below shows an example after recording Phrase 1.

Memory Map after Recording Phrase 1

Phrase	Block No.												
	1	2	3	4	5	6	7	8	9	10	11	...	128
Entire memory	1	1	1	1	0	0	0	0	0	0	0	...	0
Phrase 1	1	1	1	1	0	0	0	0	0	0	0	...	0
Phrase 2	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 3	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 4	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 5	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 6	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 7	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 8	0	0	0	0	0	0	0	0	0	0	0	...	0

When Phrase 1 used Block No. 1 through No. 4, change the bit of corresponding cells to “1”, as shown in the table above.

When you record Phrase 2, you can specify “0200H” (the first sector address of Block No. 5) for the Start address and “3FFFH” (the memory’s last address) for the Stop address by using the STADR and SPADR commands. Then, input the REC command. When you specify the next recording block after confirming NAR Output = “H”, use the STADR command to select a block starting from Block No. 6 in serial order. The memory map below shows an example after recording Phrase 2.

Memory Map after Recording Phrase 2

Phrase	Block No.												
	1	2	3	4	5	6	7	8	9	10	11	...	128
Entire memory	1	1	1	1	1	1	1	0	0	0	0	...	0
Phrase 1	1	1	1	1	0	0	0	0	0	0	0	...	0
Phrase 2	0	0	0	0	1	1	1	0	0	0	0	...	0
Phrase 3	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 4	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 5	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 6	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 7	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 8	0	0	0	0	0	0	0	0	0	0	0	...	0

If you want to redo Phrase 1, change cells used for Phrase 1 and corresponding cells for entire memory back to “0”.

Memory Map before Redoing Phrase 1

Phrase	Block No.												
	1	2	3	4	5	6	7	8	9	10	11	...	128
Entire memory	0	0	0	0	1	1	1	0	0	0	0	...	0
Phrase 1	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 2	0	0	0	0	1	1	1	0	0	0	0	...	0
Phrase 3	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 4	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 5	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 6	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 7	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 8	0	0	0	0	0	0	0	0	0	0	0	...	0

When you redo Phrase 1, you can specify “0000H” (the memory’s top address) for the Start address and “3FFFH” (the memory’s last address) for the Stop address, same as in the first recording session. Then, input the REC command. If you specify the next recording block after confirming NAR Output = “H”, use the STADR command to select a block starting from Block No. 2 in serial order. However, after block No. 4 you need to jump to Block No. 8 because Block No. 5 through 7 has been used for Phrase 2.

Memory Map after Redoing Phrase 1

Phrase	Block No.												
	1	2	3	4	5	6	7	8	9	10	11	...	128
Entire memory	1	1	1	1	1	1	1	1	1	0	0	...	0
Phrase 1	1	1	1	1	0	0	0	1	1	0	0	...	0
Phrase 2	0	0	0	0	1	1	1	0	0	0	0	...	0
Phrase 3	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 4	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 5	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 6	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 7	0	0	0	0	0	0	0	0	0	0	0	...	0
Phrase 8	0	0	0	0	0	0	0	0	0	0	0	...	0

When recording a phrase is complete, you should save the above memory map information and the Start and Stop address for the phrase. You can read the last address of a recorded phrase by using the RDADR command after each recording, which can be used to specify the Play Stop Address later.

You can save memory map information as well as the Start and Stop address by using a part of the ML2517's memory.

To start playing a phrase, input the PLAY command after setting up the Play Start and Play Stop addresses by using the STADR and SPADR commands. If you specify the next reading block after confirming NAR Output = "H", use the STADR command according to memory map information.

As described in this section, Random Block Recording/Playback Mode enables you to make more efficient use of memory space by recording in Blocks than recording in Sequential Recording/Playback Mode.

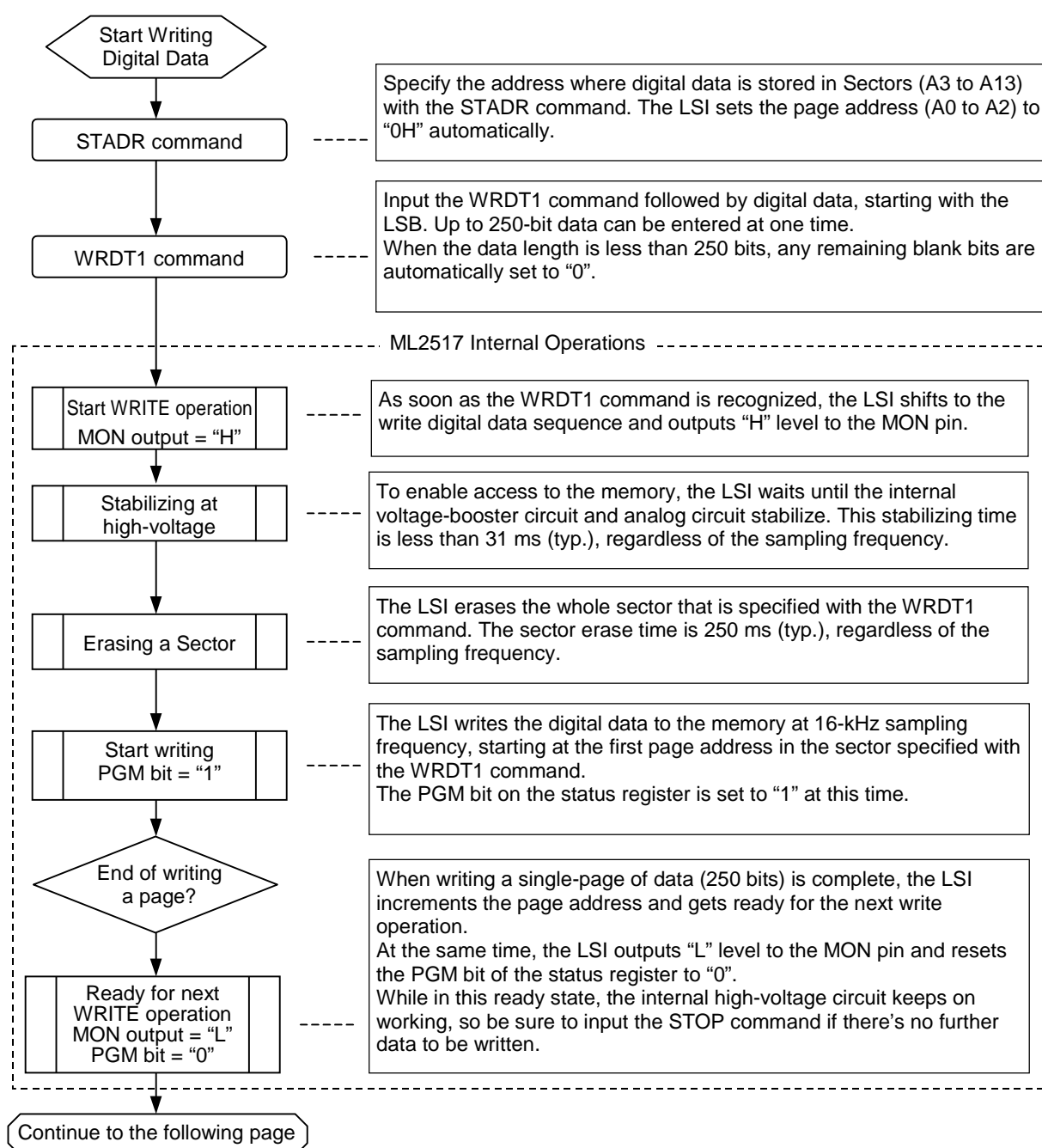
Writing Digital Data

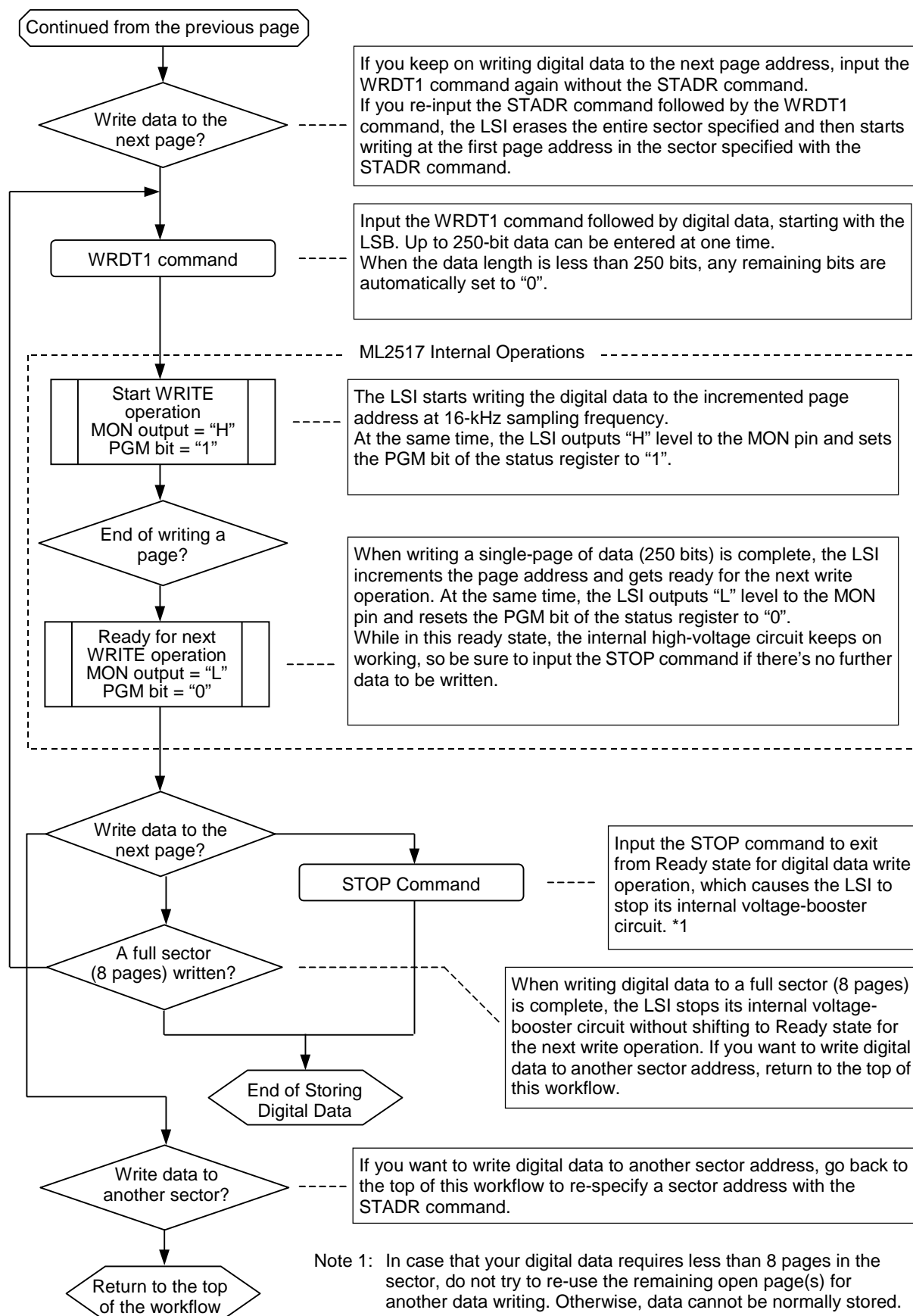
This section describes the procedure for writing digital data to the ML2517's on-chip memory by using the WRDT1 and WRDT2 commands. Writing digital data using these commands can be performed alike both in Sequential/Random Block Recording/Playback modes.

Do not allow digital and analog data to coexist in either Digital Data Area or Analog Data Area. The sound quality may be deteriorated if you store any sound data in the memory area where digital data has been stored.

1. Write Operation with the WRDT1 Command

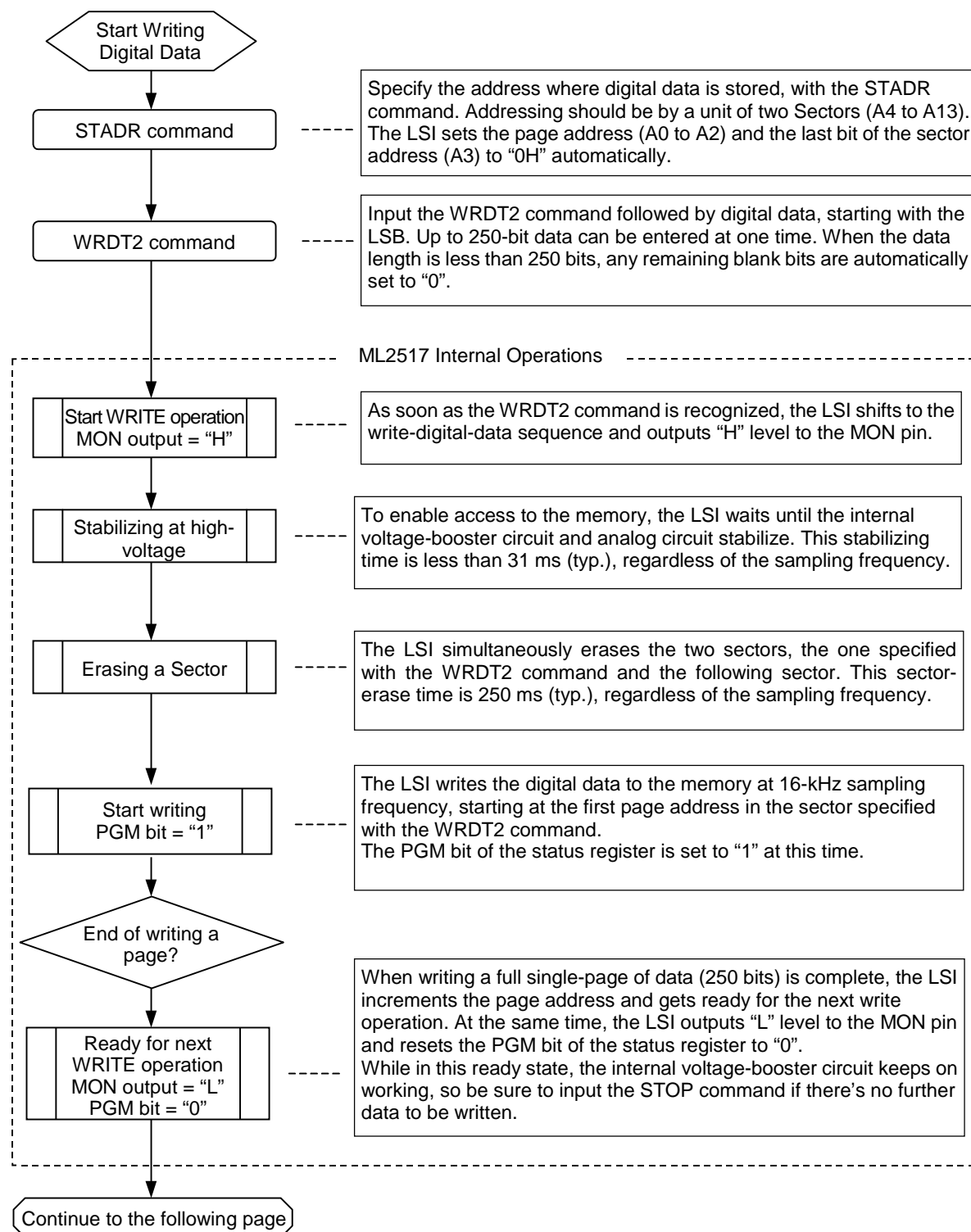
The WRDT1 command allows you to erase an entire Sector (a 2000-bit memory area) and to write digital data in pages (250-bit unit) to the memory area.

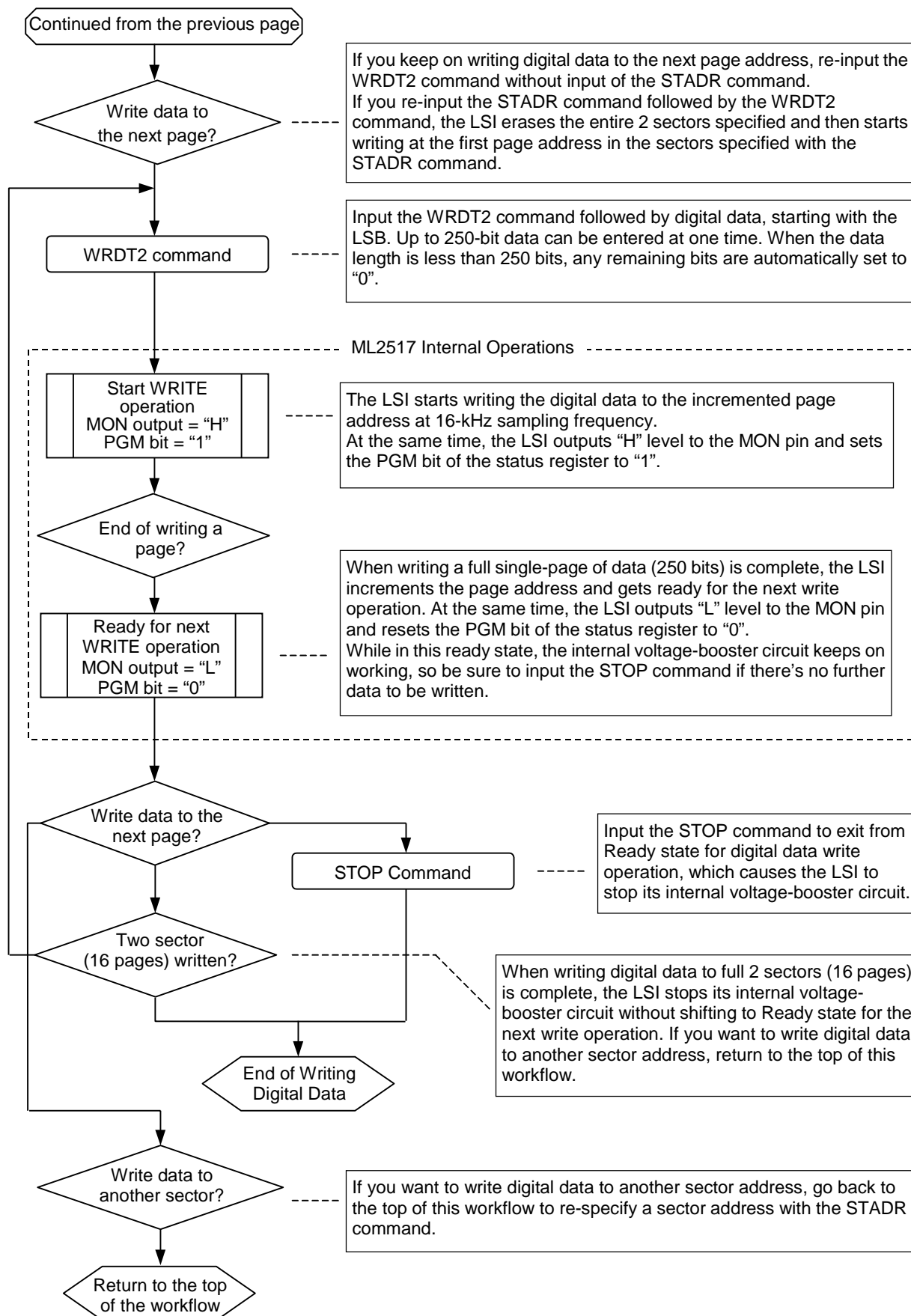




2. Write Operation with the WRDT2 Command

The WRDT2 command allows you to erase entire two Sectors (a 4000-bit memory area) and to write digital data in pages (250-bit unit) to the memory area.



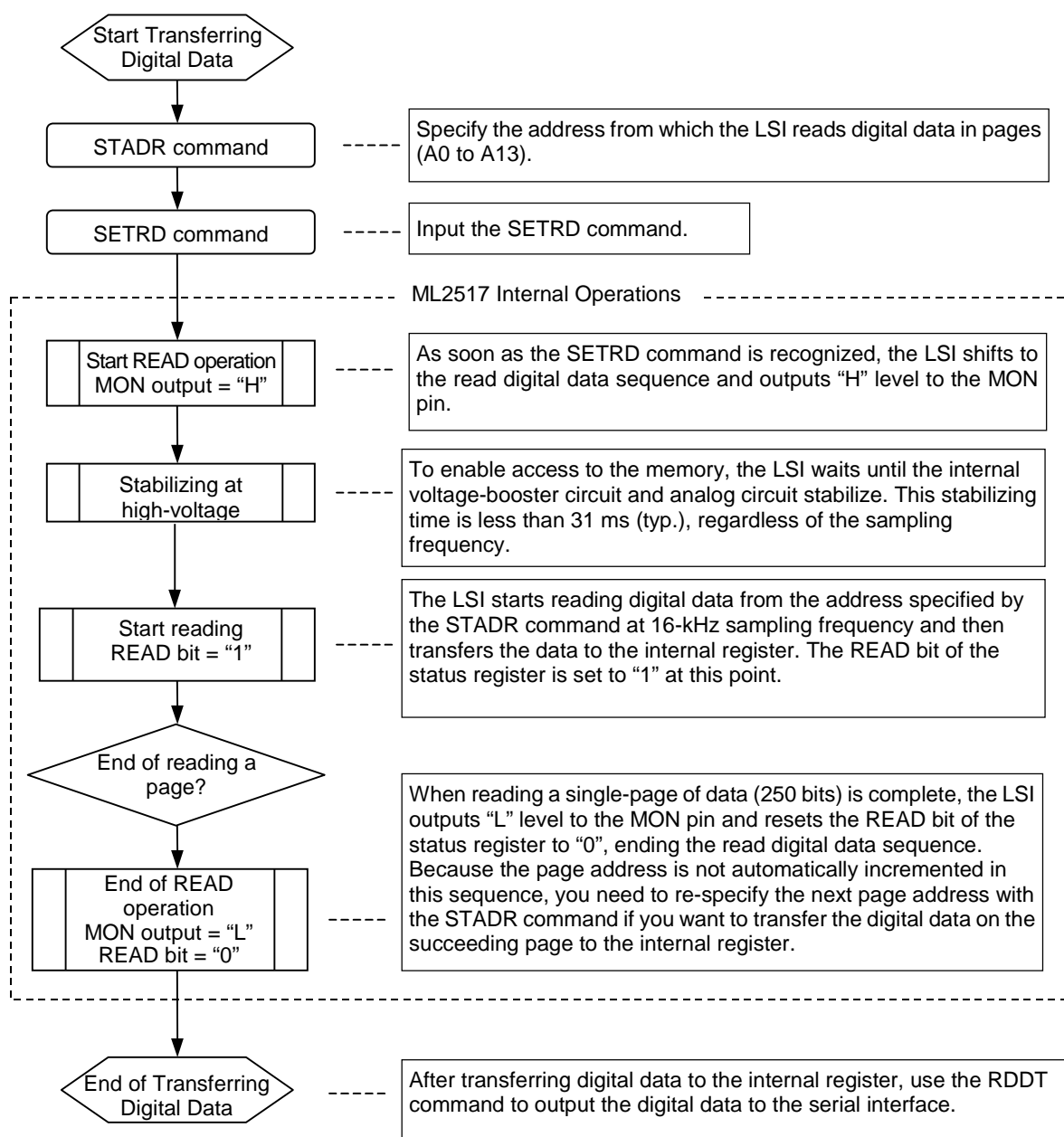


Reading Digital Data

This section describes the procedure for reading digital data stored in the ML2517's on-chip memory by using the SETRD and RDDT commands. Reading digital data with these commands can be performed alike in both Sequential and Random Block Recording/Playback modes.

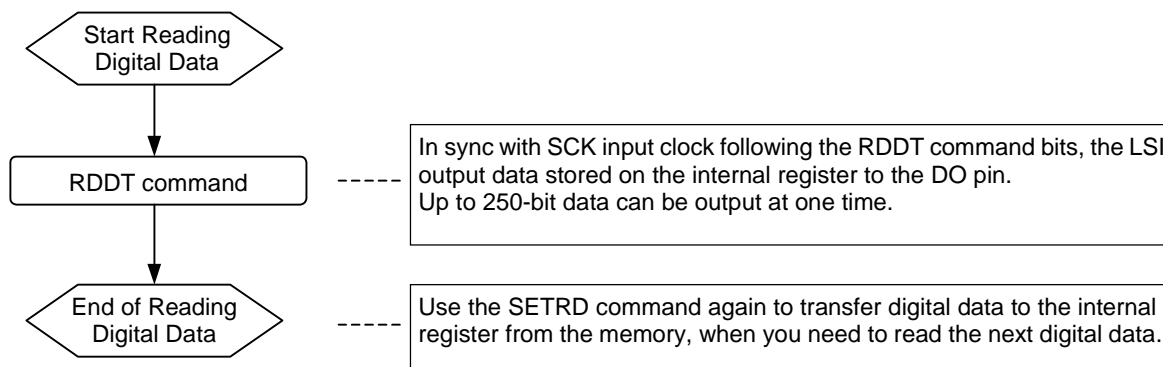
1. Data Transfer Operation with the SETRD Command

By using the SETRD command, you can transfer digital data stored in ML2517's on-chip memory to the internal register in units of 250 bits (in pages).



2. Read Data Operation with the RDDT Command

By using the RDDT command, you can output digital data, that has been transferred to the internal register from the on-chip memory with the SETRD command, to the serial interface in units of 250 bits (in pages).



Power Up and Power Down Operations

The PDWN command input or "L" level input to the $\overline{\text{RESET}}$ pin causes the ML2517 to stop its internal operations and enter a power-down state in the low-power-consumption mode. Transition to power-down state takes up to 100 μs after the PDWN command input/ $\overline{\text{RESET}}$ input. In this state, outputs from the SG, MOUT, LOUT and AOUT pins are fixed at the GND level.

To power up the LSI again from the power-down state, you can either

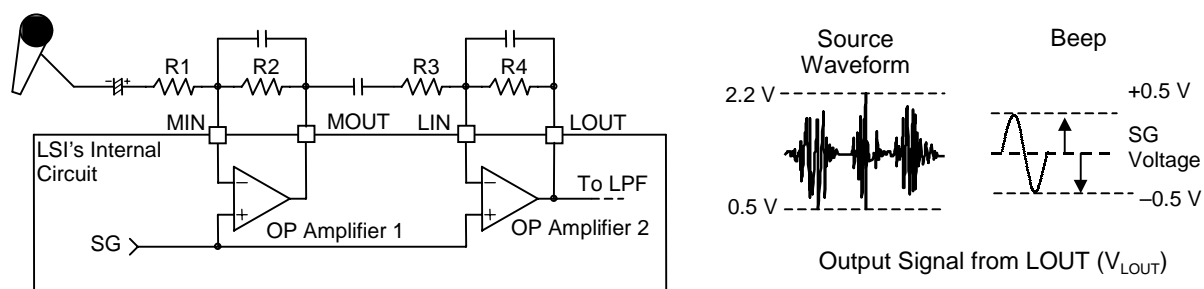
1. Input a "L" pulse to the $\overline{\text{RESET}}$ pin, or
2. Input a "L" pulse to the $\overline{\text{CS}}$ pin.

The "L" pulse width should be 1 μs or longer in both cases. It also should be noted that it takes up to 1 ms until the LSI's internal circuit stabilizes after "L" pulse input to the $\overline{\text{RESET}}$ or $\overline{\text{CS}}$ pin. So, input any operational command only after this stabilizing time. In case that you insert a capacitor between the SG and AGND pins, the SG voltage stabilizing time can vary depending on the capacitance, therefore you can input any command only after the SG voltage has stabilized.

Designing Analog Input/Output Amplifying Circuit

Two OP amplifiers are built in the ML2517 for amplifying the microphone input. The inverting input and the output from these amplifiers are directly connected to the corresponding pins of the LSI, and the non-inverting input is internally connected to the Signal Ground (Analog circuit reference voltage).

To amplify the signal input from a microphone, use the inverting amplifier circuit as shown in the figure below. Output from the LOUT pin, that is an incoming source signal for recording, is input to the internal LPF.

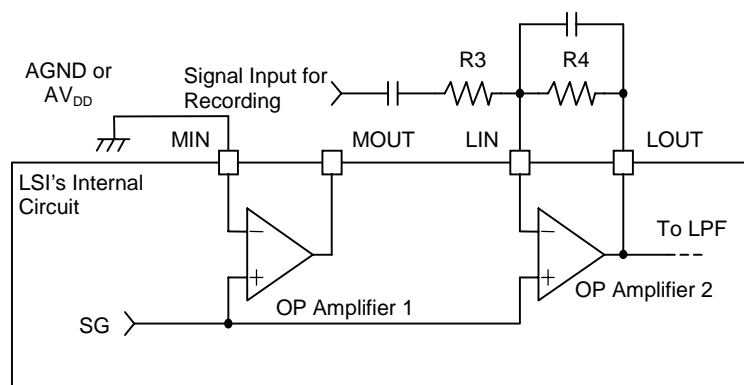


The amplitude of output signal from the LOUT pin (V_{LOUT}) needs to be adjusted by external resistors (R1 to R4) so that it may stay within the LOUT output voltage ranges shown in the table below. When V_{LOUT} goes beyond these ranges, the LPF output waveform may be distorted. This may also cause a shorter memory life cycle.

Source for Recording	Condition	LOUT Output Voltage Range	
		Min.	Max.
Voice	—	0.5 V	2.2 V
Beep	At center of SG voltage	-0.5 V	+0.5 V

The minimum value for the ROUTA, an output load resistor for each OP amplifier, is 200 kΩ. Therefore, the feedback resistors, R2 and R4, for the inverting amplifier circuit should be 200 kΩ or larger.

In case that you use OP Amplifier 2 only, without using OP Amplifier 1, connect the MIN pin to AGND or AV_{DD} and keep the MOUT pin open, as shown below. Even if an input signal for recording doesn't need amplification, the signal must go through OP Amplifier 2. In that case, use a 200-kΩ resistor for both R3 and R4 as shown in the figure below, to set the amplitude of OP Amplifier 2 to a single of amplification.



SG Pin Wiring

The voltage from the SG pin is used as the reference voltage (the Signal Ground) for the built-in OP amplifier and Low Pass Filter. Therefore, it is recommended to insert a capacitor between this pin and the GND pin to prevent the pin from carrying any noise. The recommended value for the capacitor is 0.1 μF , but the value should be determined after evaluating the sound quality of your application.

Since the SG voltage is fixed at the GND level during the power down mode, the stabilizing time of the voltage and the internal analog circuit gets longer as capacitance of the capacitor connected to the SG pin increases. Therefore, perform any operation after the SG voltage stabilizing time whenever you reset the power down mode.

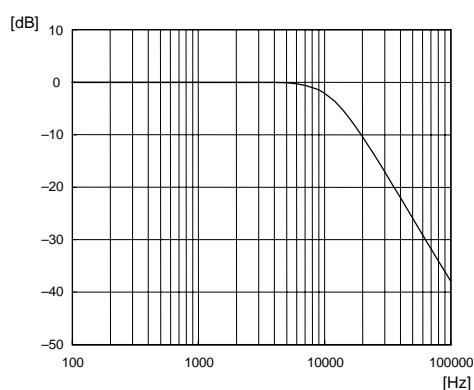
LPF Characteristics

The ML2517 has a built-in 4-stage LPF, which utilizes the Switched Capacitor Filter (SCF) technology, and a 2-stage active LPF. The 2-stage active LPF functions as SCF's fold-back noise filter during recording operation, during playing operation it works as a smoothing filter for SCF output.

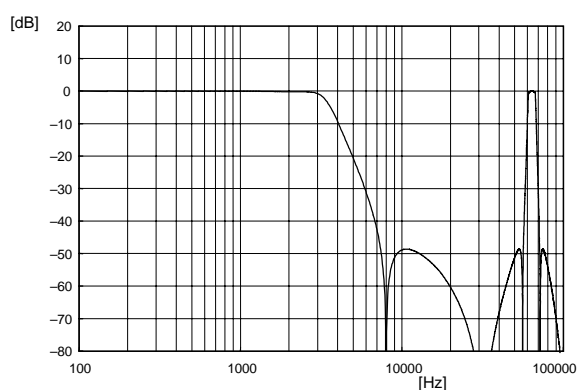
The cut-off frequency of the 2-stage active LPF is set to about 10 kHz.

The SCF's attenuation is -40 dB and its cut-off frequency and frequency characteristics can vary in proportion to the sampling frequency. The cut-off frequency is set at $4/10$ of the sampling frequency.

The following figures show Frequency Characteristics of the active LPF and the SCF at 6.4-kHz sampling frequency.



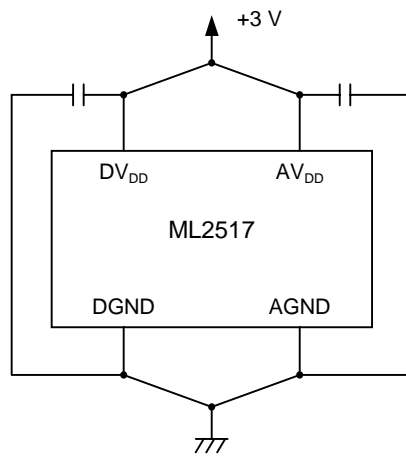
Active LPF Frequency Characteristics



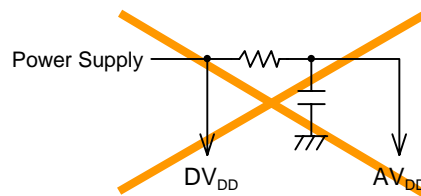
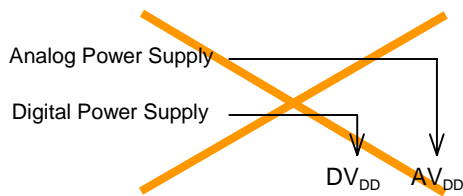
SCF Frequency Characteristics
($f_s = 6.4$ kHz)

Power Supply Circuit

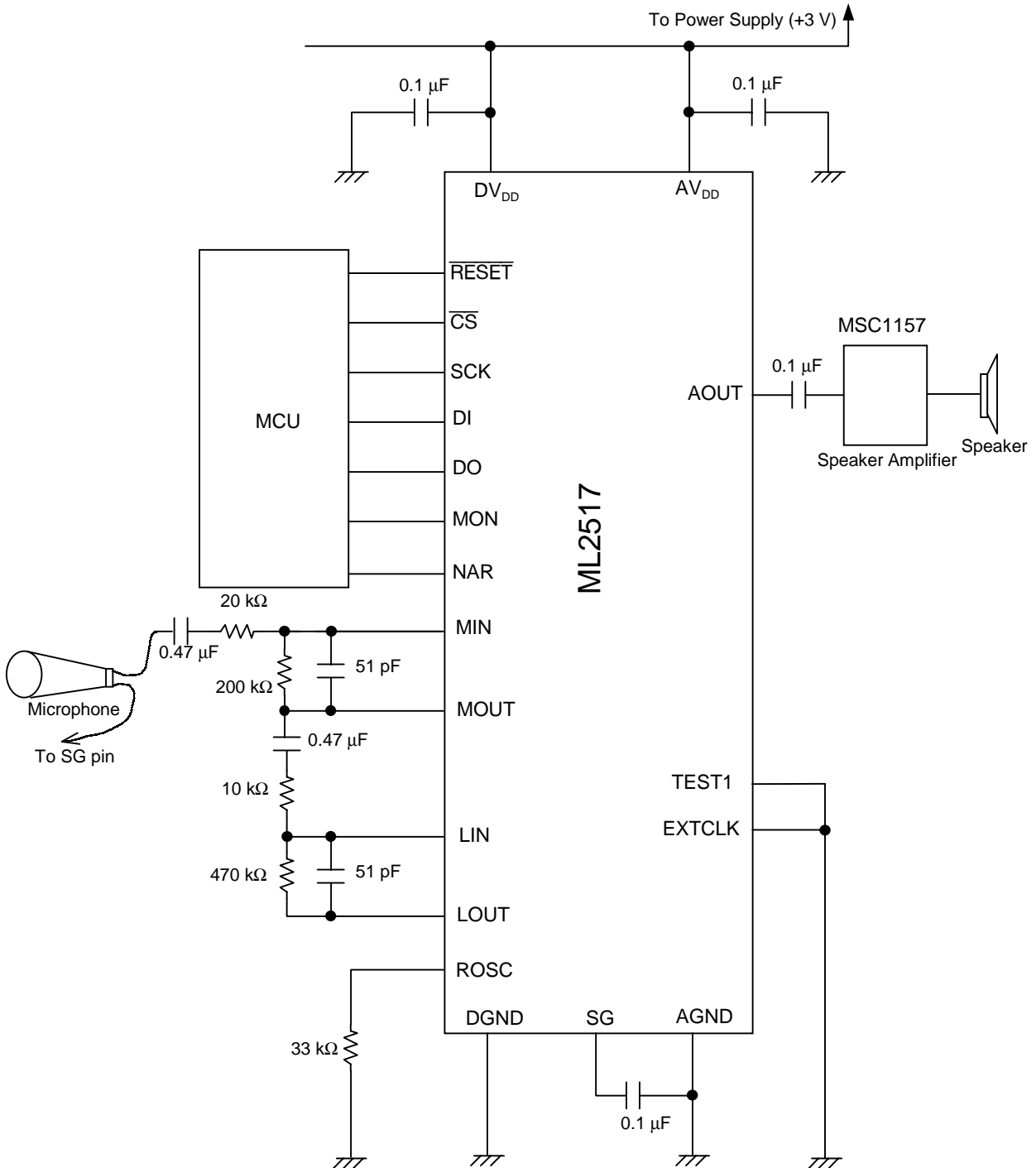
As shown in the figure below, supply to the ML2517 should come from a single power source and divided into analog and digital sections through wiring.



The following are bad examples that you should avoid.

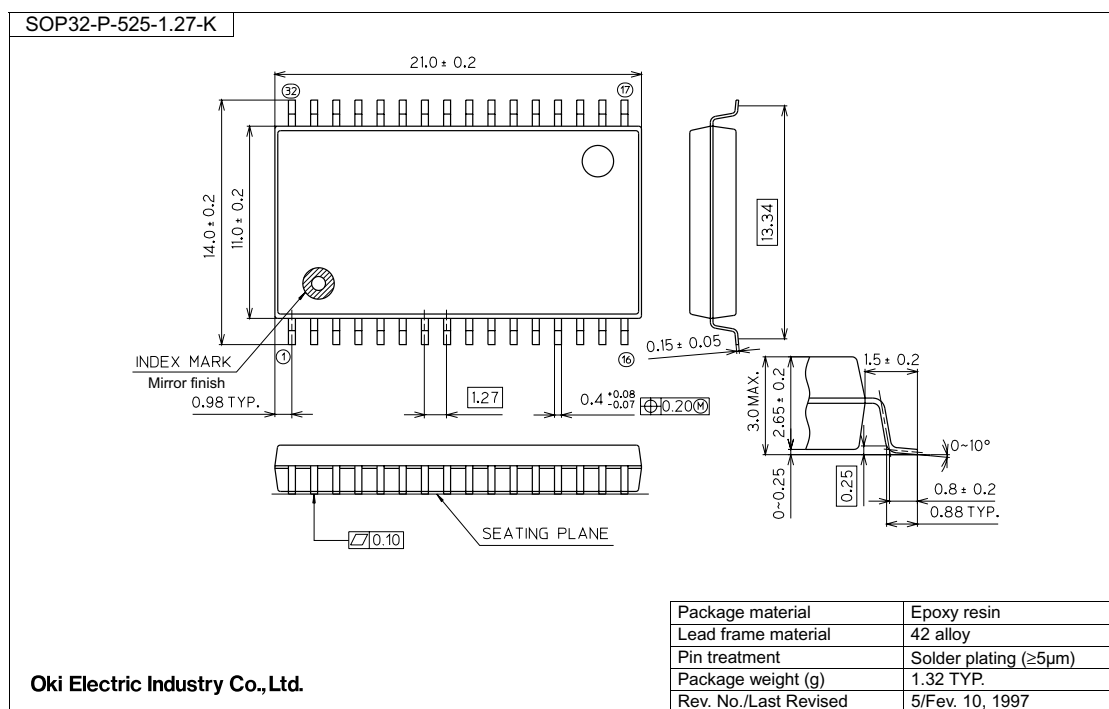


APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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