LITEON®
OPTOELECTRONICS

Optical Sensor
Product Data Sheet
LTR-706PS-01

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LITE-ON DCC

RELEASE

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OPTICAL SENSOR
LTR-706PS-01

Description

The **LTR-706PS-01** is an integrated low voltage I2C proximity sensor [PS] with built-in emitter, in a single miniature chipled lead-free surface mount package.

With built-in proximity sensor (VCSEL emitter and detector), LTR-706PS-01 offers the feature to detect object at a user configurable distance. This sensor features 2-level fault detection that allows further protection against un-intended VCSEL current trigger or surge caused by short circuit.

The sensor supports an interrupt feature that removes the need to poll the sensor for a reading which improves system efficiency. The sensor also supports several features that help to minimize the occurrence of false triggering. This CMOS design and factory-set one time trimming capability ensure minimal sensor-to-sensor variations for ease of manufacturability to the end customers.

Application

To control object detection

- Touch Panel Control in mobile/portable devices

Features

- I2C interface (Fast Mode: 400kbit/s)
- Ultra-small ChipLed L package
- Built-in temperature compensation circuit
- Low active power consumption with standby mode
- Supply voltage range from 2.7V to 3.6V capable of 1.7V logic voltage
- Operating temperature range from -30 ºC to +70ºC
- RoHS and Halogen free compliant

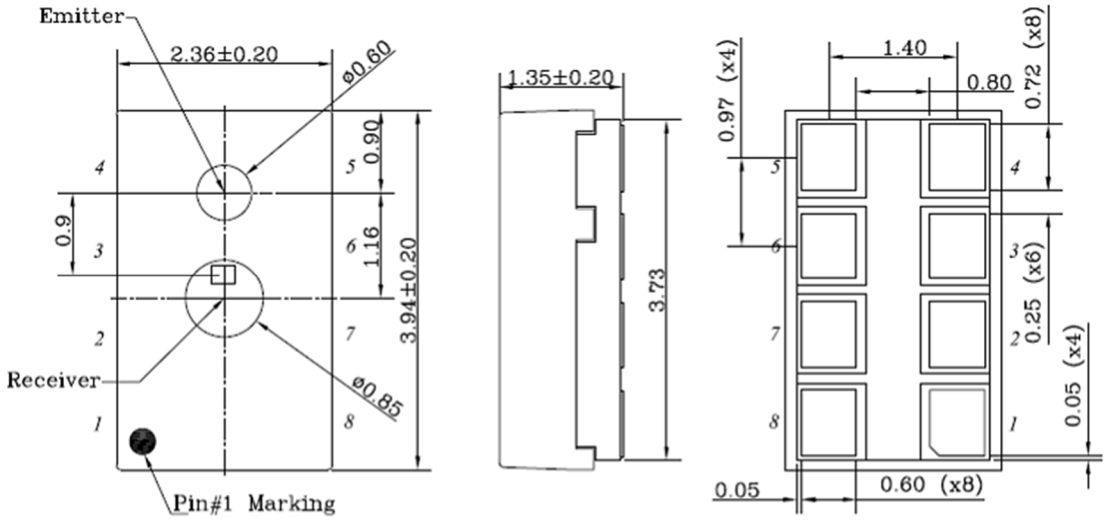
- **Proximity Sensor**
  - Built-in VCSEL driver, VCSEL emitter and detector with 2-level fault detection for VCSEL.
  - Programmable VCSEL drive settings
  - 11-bit effective resolution
  - High ambient light suppression

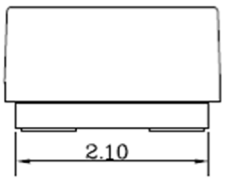
Ordering Information

Part Number	Packaging Type	Package	Quantity
LTR-706PS-01	Tape and Reel	8-pins Chip-Led package	8000

OPTICAL SENSOR
LTR-706PS-01

1. Outline Dimensions and Pins Configuration





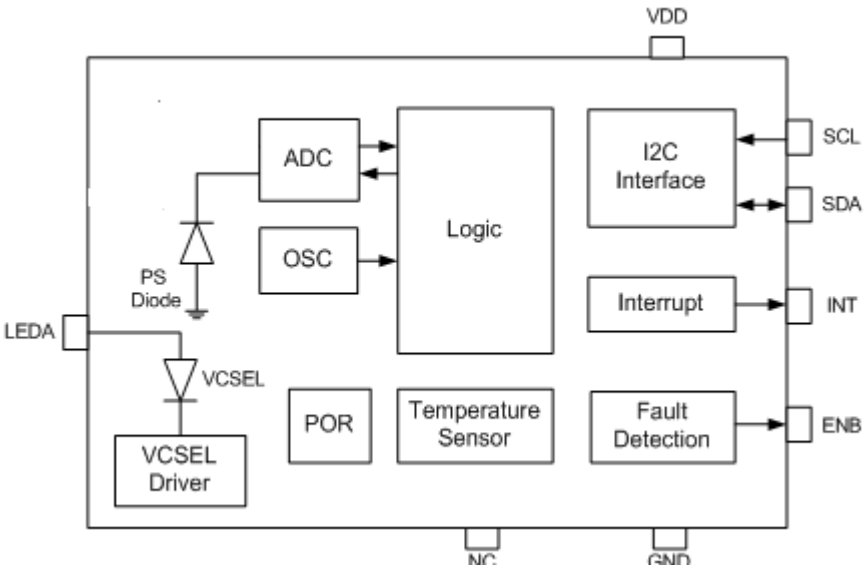
Pin-Out Assignment:

1. SDA	*5. LEDA*
2. INT	*6. GND*
3. NC	*7. SCL*
4. En-b	*8. VDD*

Note:

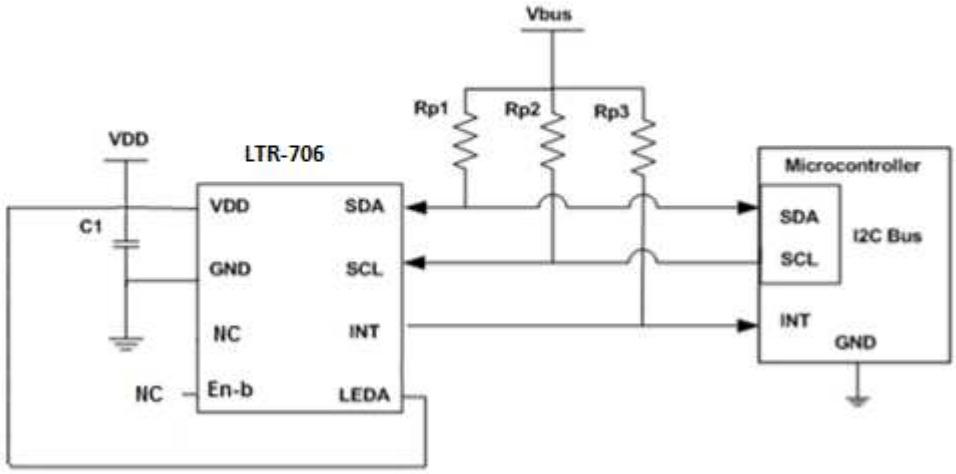
1. All dimensions are in millimeters

2. Functional Block Diagram



3. Application Circuit

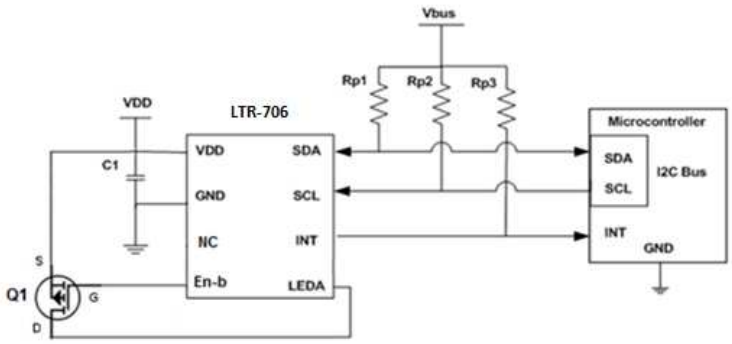
Application Circuit
For Implementing Level1 VCSEL Fault Detection



Recommended Application Circuit Components

Component	Recommended Value
Rp1, Rp2, Rp3 [1]	1 kΩ to 10 kΩ
C1	1uF ± 20%, X7R Ceramic

Application Circuit
For Implementing Full (Level1&2) VCSEL Fault Detection



Recommended Application Circuit Components

Component	Recommended Value
Rp1, Rp2, Rp3 [1]	1 kΩ to 10 kΩ
C1	1uF ± 20%, X7R Ceramic
Q1	External PMOS transistor Ron<0.45Ω@V_{GS} = −2.7V, Cin≤150pF, Example : NTA4151PT1G

Notes:

[1] Selection of pull-up resistors value is dependent on bus capacitance values. For more details, please refer to I2C Specifications: http://www.nxp.com/documents/user_manual/UM10204.pdf

I/O Pins Configuration Table

Pin	I/O Type	Symbol	Description
1	IN/OUT	SDA	I^2C serial data.
2	OUT	INT	Level Interrupt Pin. This pin is an open drain output.
3	NC	NC	No Connect.
4	OUT	En-b	Controlling external power switch for fault detection use. This is a digital output pin (not open drain). Under normal operation this output pin will be at logic low so as to turn on the external PMOS switch which is connected to the VCSEL. When fault is detected this output pin will be at logic high and will shutdown the external PMOS and also the VCSEL.
5	IN	LED A	VCSEL LED Anode.
6	Ground	GND	Ground
7	IN	SCL	I^2C serial clock.
8	Supply	VDD	Power Supply Voltage

4. Rating and Specification

4.1 Absolute Maximum Rating at Ta=25℃

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	3.8	V
Digital Voltage Range	SCL, SDA, INT	-0.5 to 3.8	V
Digital Output Current	SCL, SDA, INT	-1 to 20	mA
Storage Temperature	T_{stg}	-40 to 85	°C
VCSEL Forward DC Current	I_f	15	mA
Electrostatic Discharge Protection (Human Body Model JESD22-A114)[1]	V_{HBM}	2000	V

Notes:

[1] V_{HBM} for LEDA PAD is 200V due to VCSEL behavior.

Exceeding these ratings could cause damage to the sensor. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

4.2 Recommended Operating Conditions (VDD= 3V, Ta = +25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.7		3.6	V
Interface Bus Power Supply Voltage	VIO	1.7		3.6	V
I2C Bus Input Pin High Voltage	VIH_SCL, VIH _SDA	1.2			V
I2C Bus Input Pin Low Voltage	VIL_SCL, VIL_SDA			0.6	V
Operating Temperature	T_{ope}	-30		70	°C

4.3 Electrical & Optical Specifications

All specifications are at VDD = 3.0V, T_{ope} = 25°C, unless otherwise noted.

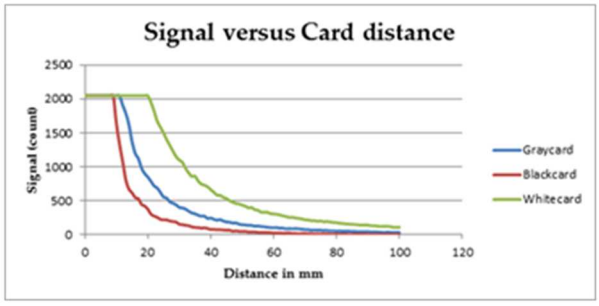
Parameter	Min.	Typ.	Max.	Unit	Condition
Supply Current		150		uA	PS in active mode
Standby Current			5	uA	Standby / Sleep Mode
Initial Startup Time			50	ms	Min wait time after power up (supply ramp-up to 2.4V) before sending I2C commands
Wakeup Time from Standby			10	ms	Max wait time after turning device from stand-by to active before measurements starts
Leakage Current	-5		5	uA	SDA, SCL, INT pins

4.4 Characteristics Proximity Sensor

Parameter	Min.	Typ.	Max.	Unit	Condition
PS Resolution		11 bit			
Full ADC count			2047	count	
Detection Distance		100		mm	5mA, 48 pulses, 18% Gray Card
No of VCSEL Pulse	1		64	pulses	
VCSEL Pulse Frequency		125		kHz	
VCSEL Duty Cycle		25		%	
VCSEL Pulse Current	2		14	mA	
Peak Wavelength, λP	840	850	860	nm	IF = 9mA
Ambient Light Suppression			50k	lux	Direct Sunlight

4.5 Typical Device Parameter
(VDD = 3.0V, Ta=25℃, default power-up settings, un less otherwise noted)

PS response



5 mA, 48 pulse

Figure 4.3 PS count Vs distance (without window)

Angular of LED

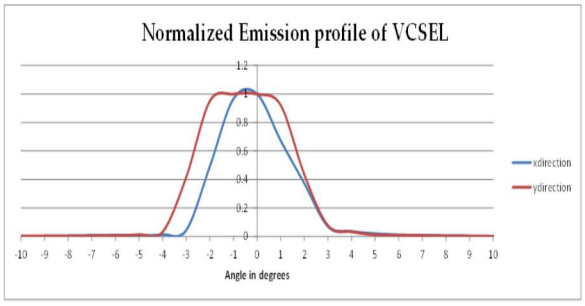
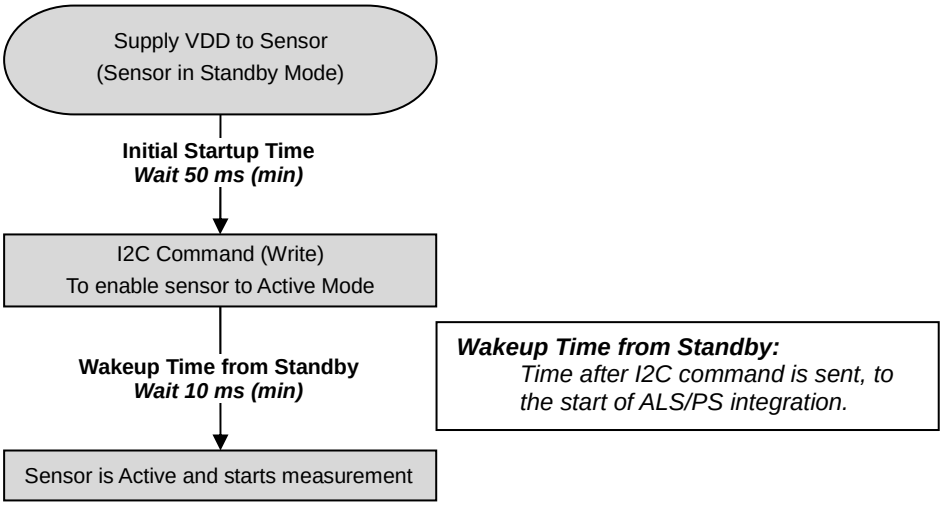


Figure 4.4 LED Angular of incidence

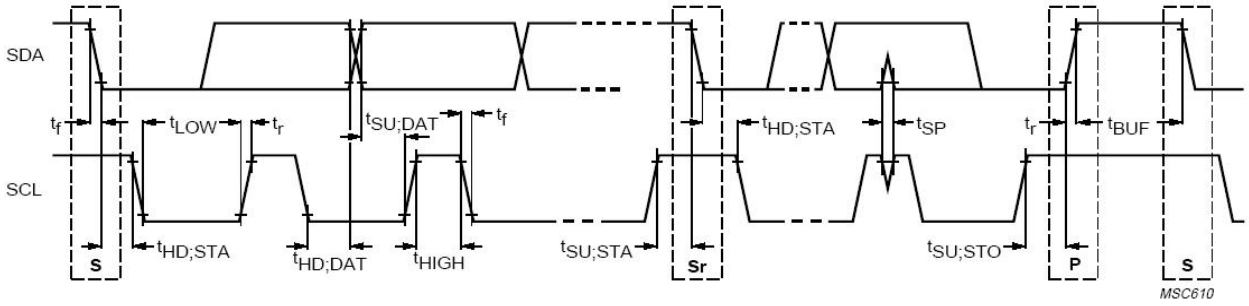
4.6 Startup Sequence



4.7 AC Electrical Characteristics

All specifications are at V_{DD} = 3.0V, T_{ope} = 25°C, unless otherwise noted.

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	1	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3		us
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6		us
LOW period of the SCL clock	t_{LOW}	1.3		us
HIGH period of the SCL clock	t_{HIGH}	0.6		us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6		us
Set-up time for STOP condition	$t_{SU;STO}$	0.6		us
Rise time of both SDA and SCL signals	t_r	30	300	ns
Fall time of both SDA and SCL signals	t_f	30	300	ns
Data hold time	$t_{HD;DAT}$	30		s
Data setup time	$t_{SU;DAT}$	100		ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns

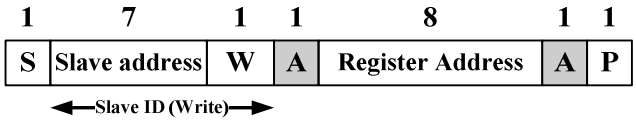


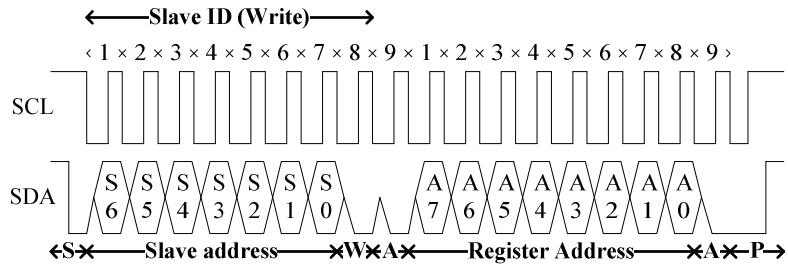
Definition of timing for I²C bus

5. Principle of Operation

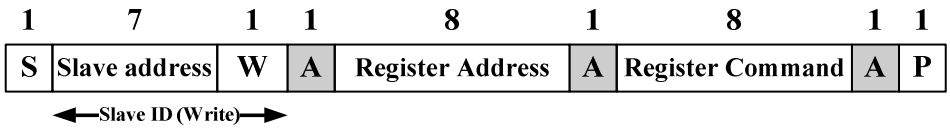
5.1 I2C Protocol

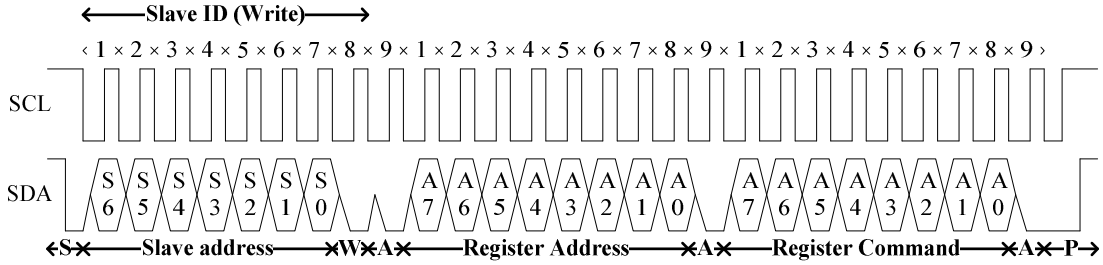
5.1.1 I2C Write Protocol (type 1)



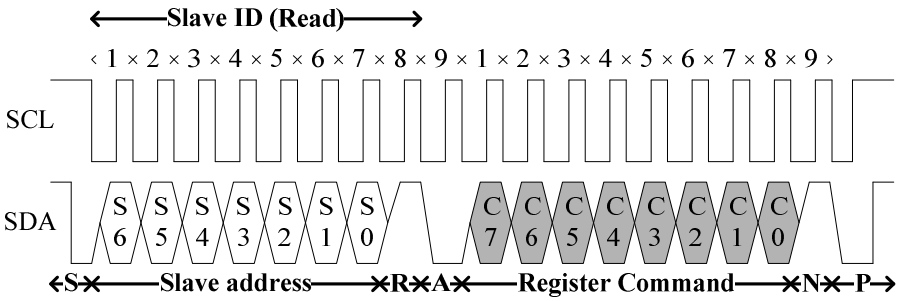


5.1.2 I2C Write Protocol (type 2)





5.1.3 I2C Read Protocol



A	AcknowVcselge (0 for an ACK)	**N**	Non-AcknowVcselge(1 for an NACK)
S	Start condition	**Sr**	Repeated Start condition
P	Stop condition		
W	Write (0 for writing)	**R**	Read (1 for read)
	Slave-to-master		Master-to-Slave

5.2 I2C Slave Address

The 7 bits slave address for this sensor is 0x23H. A read/write bit should be appended to the slave address by the master device to properly communicate with the sensor.

I²C Slave Address									
Command Type	(0x23H)							(0x23H)	(0x23H)
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Write	0	1	0	0	0	1	1	0	0x46H
Read	0	1	0	0	0	1	1	1	0x47H

6. Register Set

Address	R / W	Register Name	Description	Reset Value
0x80	R / W	CLK_ON register	Internal Clock control and SW reset	0x00
0x81	R / W	PS_CONTR	PS operation mode control	0x40
0x82	R / W	PS_LED	PS LED setting	0x76
0x83	R / W	PS_N_PULSES	PS number of pulses	0x01
0x84	R / W	PS_MEAS_RATE	PS measurement rate in active mode	0x04
0x86	R	PART_ID	Part Number ID and Revision ID	0x05
0x87	R	MANUFAC_ID	Manufacturer ID	0x05
0x90	R	PS_STATUS	PS new data status	0x00
0x91	R	PS_DATA_0	PS measurement data, lower byte	0x00
0x92	R	PS_DATA_1	PS measurement data, upper byte	0x00
0x93	R / W	INTERRUPT	Interrupt settings	0x00
0x94	R / W	INTERTUPT_PERSIST	PS interrupt persist setting	0x00
0x95	R / W	PS_THRES_UP_0	PS interrupt upper threshold, lower byte	0xFF
0x96	R / W	PS_THRES_UP_1	PS interrupt upper threshold, upper byte	0x07
0x97	R / W	PS_THRES_LOW_0	PS interrupt lower threshold, lower byte	0x00
0x98	R / W	PS_THRES_LOW_1	PS interrupt lower threshold, upper byte	0x00
0x9F	R / W	FAULT DETECTION	Fault detection control and status register	0x00
0xA0	R	FD STATUS	Fault detection status	0x00

6.1 CLK_ON Register (0x80)

The CLK_ON register can turn on the chip's internal clock to be able to run Fault Detection without turning ON the PS.

0x80	PS_CONTR (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved		*ON Clock*	*Reserved*			*SW reset*	*Reserved*

Field	Bits	Default	Type	Description	
Reserved	7:6	00	RW	--	Must write 00
ON CLOCK	5	0	R/W	0	System clock OFF(default)
				1	System clock ON
Reserved	4:2	000	--	--	Must write 000
SW_Reset	1	0	RW	0	No action (default)
				1	Reset registers to default value
Reserved	0	0	--	--	Must write 0

6.2 PS _CONTR Register (0x81)

The PS_CONTR register controls the PS operation modes. The PS sensor can be set to either standby mode or active mode. At either of these modes, the I^2C circuitry is always active. The default mode after power up is standby mode. During standby mode, there is no PS measurement performed but I^2C communication is allowed to enable read/write to all the registers. PS Gain controls the gain setting for the PS sensor. FTN/NTF EN controls the FTN/NTF Status Reporting.

0x81	PS_CONTR (default = 0x40)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved		*FTN/NTF EN*	*Reserved*	*PS Gain*		*PS Mode*	*Reserved*

Field	Bits	Default	Type	Description	
Reserved	7:6	01	--	--	Must be 01
FTN/NTF_EN	5	0	R/W	0	Disable FTN/NTF Status Reporting(default)
				1	Enable FTN/NTF Status Reporting
Reserved	4:2	000	--	--	Must be 0
PS Mode	1	0	R/W	1	Active Mode
				0	Stand-by Mode(default)
Reserved	0	0	--	--	Reserved

6.3 PS_LED Register(0x82)

The PS_LED register controls the LED pulse modulation frequency, VCSEL current duty cycle and VCSEL peak current.

0x82	PS_VCSEL (default = 0x76)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved		*Reserved*		*VCSEL Peak Current*			

Field	Bits	Default	Type	Description	
Reserved	7:4	0111	R/W	----	Must write 0101
VCSEL Current	3:0	0110	R/W	0000	2mA
				0001	3mA
				0010	4mA
				0011	5mA
				0100	6mA
				0101	7mA
				0110	8mA **(default)**
				0111	9mA
				1000	10mA
				1001	11mA
				1010	12mA
				1011	13mA
				1100	14mA
				1101	Reserved
				1110	Reserved
				1111	Reserved

6.4 PS_N_Pulses Register (0x83)

The PS_N_Pulses register controls the number of VCSEL pulses to be emitted.

0x83	PS_N_Pulses (default = 0x01)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved	*No of VCSEL Pulse*						

Field	Bits	Default	Type	Description	
VCSEL Pulse Count	7	0	--	--	Must be 0
	6:0	0000001	R/W	0000000	Reserved
				0000001	Number of pulses = 1 (default)
				0000010	Number of pulses = 2
				0000011	Number of pulses = 3
				-----	--------
				0111111	Number of pulses = 63
				1000000	Number of pulses = 64

6.5 PS_MEAS_RATE Register (0x84)

The PS_MEAS_RATE register controls the timing of the periodic measurements of the PS in active mode. PS Measurement Repeat Rate is the interval between PS_DATA registers update.

0x84	PS_MEAS_RATE (default = 0x04)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					*PS Measurement Rate*		

Field	Bits	Default	Type	Description	
Reserved	7:3	00000	--	--	--
PS Measurement Rate	2:0	100	RW	000	6.125ms
				001	12.5ms
				010	25ms
				011	50ms
				100	100ms **(default)**
				101	200ms
				110	400ms
				111	800ms

6.6 PART_ID Register (0x86) (Read Only)

The PART_ID register defines the part number and revision identification of the sensor.

0x86	PART_ID (default = 0x05)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Part Number ID						*Revision ID*	

Field	Bits	Default	Type	Description
Part Number ID	7:2	000001	R	--
Revision ID	1:0	01	R	--

6.7 MANUFAC_ID Register (0x87) (Read Only)

The MANUFAC_ID register defines the manufacturer identification of the sensor.

0x87	MANUFAC_ID (default = 0x05)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Manufacturer ID							

Field	Bits	Default	Type	Description
Manufacturer ID	7:0	00000101	R	Manufacturer ID (0x05H)

6.8 PS_STATUS Register (0x90) (Read Only)

The PS_STATUS register stores the information about interrupt status and PS data status. New data means data has not been read yet. When the measurement is completed and data is written to the data register, the data status bit will be set to logic 1. When the data register is read, the data status bit will be set to logic 0. Interrupt status determines if the PS interrupt criteria are met. It will check if the PS measurement data is outside of the range defined by the upper and lower threshold limits.

0x90	PS_STATUS (default = 0x00)							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
	Reserved						***PS Interrupt Status***	***PS Data Status***

Field	Bits	Default	Type	Description	
Reserved	7:2	0	R	Reserved	
PS Interrupt Status	1	0	R	0	Interrupt signal INACTIVE (default)
				1	Interrupt signal ACTIVE
PS Data Status	0	0	R	0	OLD data (data already read), (default)
				1	NEW data (first time data is being read)

6.9 PS_DATA_0 Register (0x91 / 0x92) (Read Only)

The PS ADC channel data are expressed as a 11-bit data spread over two registers. The PS_DATA_0 and PS_DATA_1 registers provide the lower and upper byte respectively. When the I^2C read operation starts, both the registers are locked until the I^2C read operation is completed. This will ensure that the data in the registers is from the same measurement even if an additional integration cycle ends during the read operation. New measurement data is stored into temporary registers and the PS_DATA registers are updated as soon as there is no on-going I^2C read operation.

0x91	PS_DATA_0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Data Low							

0x92	PS_DATA_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					***PS Data High***		

Field	Address	Bits	Default	Type	Description	
PS Data, Low	0x8D	7:0	00000000	R	--	PS ADC lower byte data
Reserved	0x8E	7:3	00000	--	--	--
PS Data, High	0x8E	2:0	000	R	--	PS ADC upper byte data

6.10 INTERRUPT Register (0x93)

The INTERRUPT register controls the operation of the interrupt pin and functions. When the Interrupt Mode is set to 00, the INT output pin 2 is inactive / disabled and will not trigger any interrupt. However at this condition, the PS_STATUS register will still be updated.

Note that when this register is to be set with values other than its default values, it should be set before device is in Active mode.

0x93	INTERRUPT (default = 0x00)							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
	FTN	***NTF***	***Reserved***			***Interrupt Polarity***	***Interrupt Mode***	

Field	Bits	Default	Type	Description	
FTN	7	0	R	0	No far to near object detected (default)
				1	Far to near object detected
NTF	6	0	R	0	No near to far object detected (default)
				1	Near to far object detected
Reserved	5:3	0	-	-	-
Interrupt Polarity	2	0	RW	0	INT pin is considered active when it is a logic 0 (default)
				1	INT pin is considered active when it is a logic 1
Interrupt Mode	1:0	00	RW	00	Interrupt pin is INACTIVE / high impedance state (default)
				01	PS measurement can trigger interrupt
				10	Reserved
				11	Reserved

6.11 INTERRUPT PERSIST Register (0x94)

The INTERRUPT PERSIST register controls the N number of times the measurement data is outside the range defined by the upper and lower threshold limits before asserting the interrupt.

0x94	INTERRUPT PERSIST (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Persist				***Reserved***			

Field	Bits	Default	Type	Description	
PS persist	7:4	0000	RW	0000	Every PS value out of threshold range (default)
				0001	1 consecutive PS values out of threshold range
				.....	.....
				1111	16 consecutive PS values out of threshold range
Reserved	3:0	0000	RW	Reserved	

6.12 PS_THRES Register (0x95 / 0x96 / 0x97 / 0x98)

The PS_THRES_UP and PS_THRES_LOW registers determines the upper and lower limit of the interrupt threshold value respectively. These two values form a range and the interrupt function compares if the measurement value in PS_DATA registers is inside or outside the range. The interrupt function is active if the measurement data is outside the range defined by the upper and lower limits. The data format for PS_THRES must be the same as PS_DATA registers.

0x95	PS_THRES_UP_0 (default = 0xFF)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Upper Threshold Low							

0x96	PS_THRES_UP_1 (default = 0x07)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					***PS Upper Threshold High***		

0x97	PS_THRES_LOW _0 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	PS Lower Threshold Low							

0x98	PS_THRES_LOW_1 (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved					*PS Lower Threshold High*		

Field	Address	Bits	Default	Type	Description
PS Upper Threshold Low	0x95	7:0	11111111	RW	PS upper threshold lower byte
Reserved	0x96	7:3	00000	--	Reserved
PS Upper Threshold High	0x96	2:0	111	RW	PS upper threshold upper byte
PS Lower Threshold Low	0x97	7:0	00000000	RW	PS lower interrupt threshold value, lower byte
Reserved	0x98	7:3	00000	--	Reserved
PS Lower Threshold High	0x98	2:0	000	RW	PS lower interrupt threshold value, upper byte

6.18 Fault Detection Control Register (0x9F) and Status (0xA0) Register

The FAULT DETECTION CONTROL register controls fault detection timing and enable fault detection function. Each PS cycle starts with a process to check whether there is a fault before the actual PS measurement. Two types of fault detection can be selected using Register 0x9F bit1, the Level1 and full (Level1&2) fault detection.

Level1 VCSEL Fault Detection

In this level of fault detection, the IC will check the VCSEL cathode whether it is shorted to ground potentially causing high current surge in the VCSEL. If it is shorted to ground the “VCSEL Fault” flag (Register 0xA0 bit 0) will be asserted. This fault detection works with the application circuit that does not require an external pmos transistor.

Full (Level1&2) VCSEL Fault Detection

This 2-level fault detection works with the application circuit that requires an external PMOS transistor to switch the VCSEL to the power supply. In addition to the above Level1 fault detection, the IC will look for further external circuit failures focusing on the ENB output pin and the external PMOS transistor. In this fault check, the logic level of the ENB output pin (which is connected to the external PMOS gate) is measured by the IC to determine whether it is permanently stuck low or high (i.e. cannot be controlled). If the ENB output pin is found to be stuck low, the “ENB Gate stuck low” flag (Register 0xA0 bit 3) will be set. If the ENB output pin is found to be stuck high, the “ENB Gate stuck high” flag (Register 0xA0 bit 2) will be set. Following this stuck high and low test, the IC will also check whether the external PMOS transistor can be turned OFF. This is flagged as “ENB Fault” (Register 0xA0 bit 1). The IC will also check leakage current from VCSEL Cathode to ground. If there is a resistive short from VCSEL Cathode to ground which is 5Kohms and lower, this is flagged as “VCSEL leakage (Register 0xA0 bit 4)”

A list of flags corresponding to each checking process is as below:

- VCSEL leakage – resistive short from VCSEL Cathode to ground which is < 5Kohms
- ENB Gate stuck low – this flag reporting ENB output pin (i.e. external PMOS gate) stuck low
- ENB Gate stuck high – this flag reporting ENB output pin (i.e. External PMOS gate) stuck high
- ENB Fault – this flag reporting PMOS switch faulty (i.e. cannot turn OFF switch).
- VCSEL Fault – this flag reporting VCSEL Cathode is shorted to ground which will cause high driving current to the VCSEL.

Besides flags reporting from FAULT DETECTION status register, an INTERRUPT will be generated from the IC to the host controller, regardless the settings of INTERRUPT Register (0x93, Bit 1:0). When fault is detected, the chip will send/pull ENB pin to high state and turn off the VCSEL. It is recommended to have host controller immediate attention once it received the interrupt signal, to switch off the VLED supply as fault detected.

FD Self Check (Register 0x9F bit4) – This is used when the user want to force a fault detection check. Normally, the fault detection check will be ON during PS enable state. Fault detection will not be active if the PS is in the OFF or DISABLE state. However the user can force a fault detection check when the PS is in the off state. This is done by setting the FD Self Check bit and also the ON CLOCK bit in the register 0x80. It is recommended to force a fault detection check whenever the device is power on so that fault can be immediately detected.

0x9F	FAULT_DETECTION_CONTROL (default = 0x01)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved			*FD Self Check*	*Reserved*			*FD Level*

Field	Bits	Default	Type	Description	
Reserved	7:5	00	RW	Must be write as 00	
FD Self Check	4	0	-	0	Self Check Fault Detection disabled (default)
				1	Run Self Check Fault Detection
Reserved	3:1	000	--	000	Must write 0
FD Level	0	0	RW	0	Level 2 Fault Detection
				1	Level 1 Fault Detection **(default)**

0xA0	FAULT_DETECTION_STATUS (default = 0x00)							
	B7	B6	B5	B4	B3	B2	B1	B0
	Reserved			*VCSEL leakage*	*ENB Gate stuck low*	*ENB Gate stuck high*	*ENB Fault*	*VCSEL Fault*

Field	Bits	Default	Type	Description	
Reserved	7:5	00	R	Reserved	
VCSEL leakage	4	0	R	0	No leakage **(default)**
				1	VCSEL leak to GND, level 2 FD only
ENB Gate stuck low	3	0	R	0	ENB gate controllable **(default)**
				1	ENB gate stuck at logic low, for level 2 FD
ENB Gate stuck high	2	0	R	0	ENB gate controllable **(default)**
				1	ENB gate stuck at logic high, for level 2 FD
ENB Fault	1	0	R	0	External CMOS switch normal **(default)**
				1	External CMOS switch Faulty, for level 2 FD
VCSEL FAULT	0	0	R	0	VCSEL Cathode not short to GND **(default)**
				1	VCSEL Cathode short to GND, level 1 and level 2 FD

7 Application Information

7.5 Operating Modes

Stand-by Mode

The device is by default in stand-by mode after power-up. No measurement activity done in PS. I^2C communication is allowed to be able to read/write to the registers. The device can be reset from MCU by setting appropriate register control (SW reset). Start-up sequence is exactly the same as that when power-on reset is triggered.

Active Mode

The PS can simultaneously be in active mode (see Fig 1). Measurement data is expected to be available within a known fixed time (refer to measurement time parameter from PS specification).

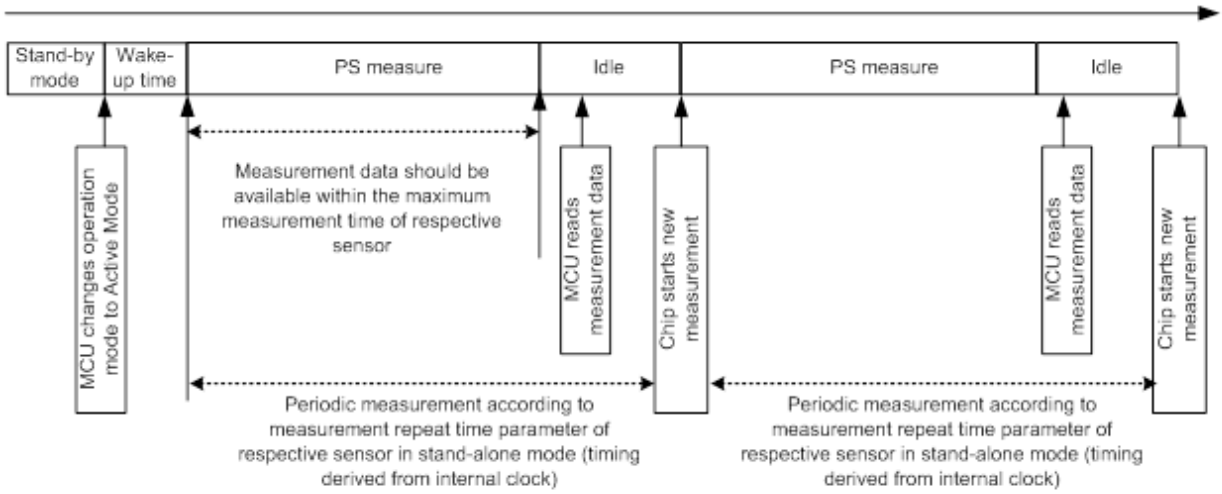


Figure 7.1 : PS measurement sequence

7.6 Interrupt Features

The interrupt function is active if PS measurements are outside of the upper and lower absolute threshold levels set in the appropriate threshold register. Refer to Figure 2 for the illustration. Only newly measured data is compared to the threshold levels set such that old data will not cause triggering of the INT pin if in case the threshold levels are changed in between measurements.

The status of interrupt can be monitored directly through the interrupt (INT) pin or by checking contents of the interrupt register. Interrupt pin can either be enable or disabled. Possible to invert interrupt output of LOW or HIGH state.

Interrupt pin IO requirements are exactly the same as those of the I2C bus pins SDA and SCL.

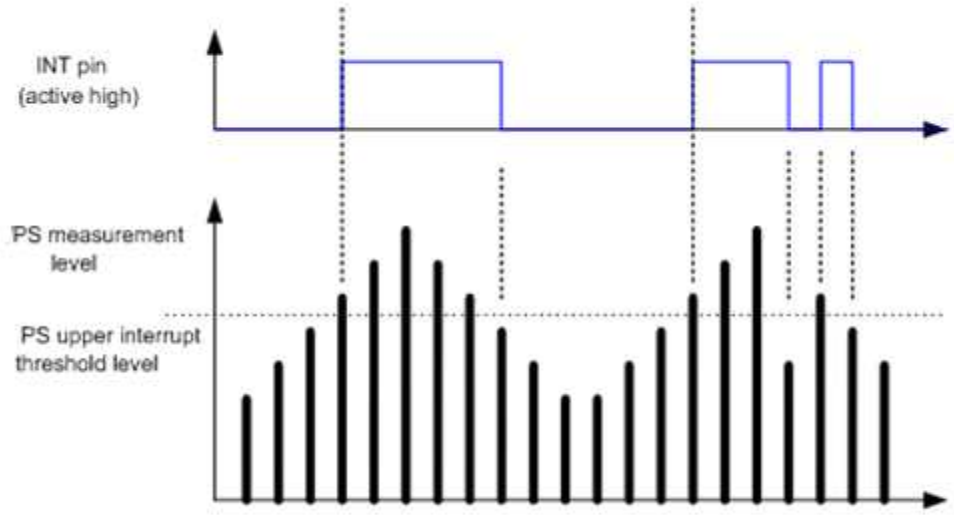


Figure 7.2 : Interrupt pin illustration for absolute threshold

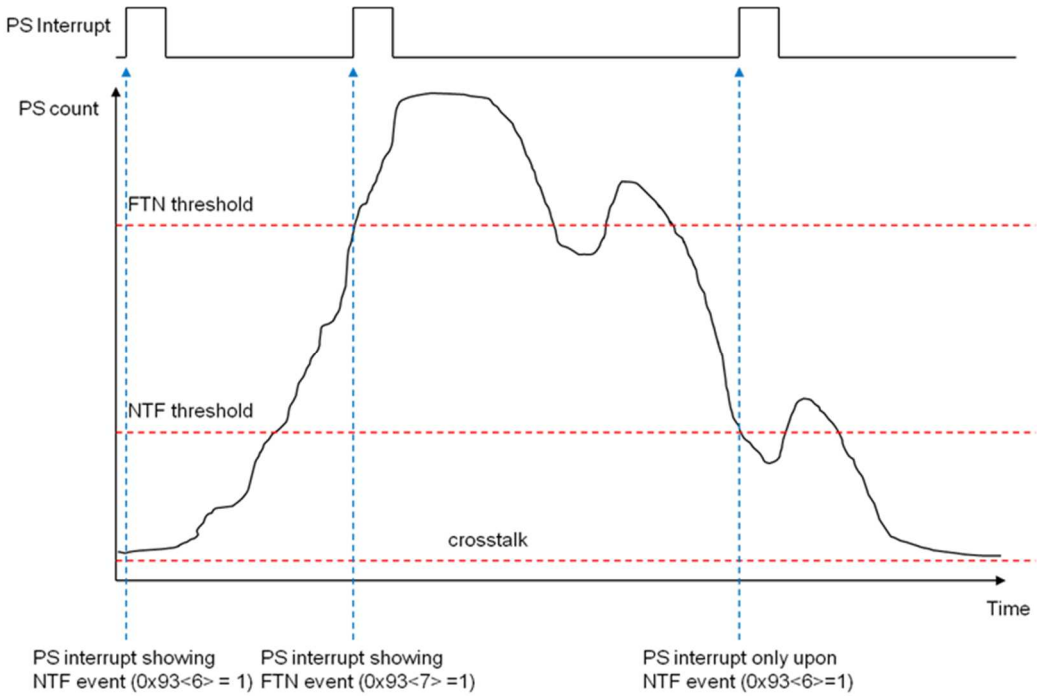
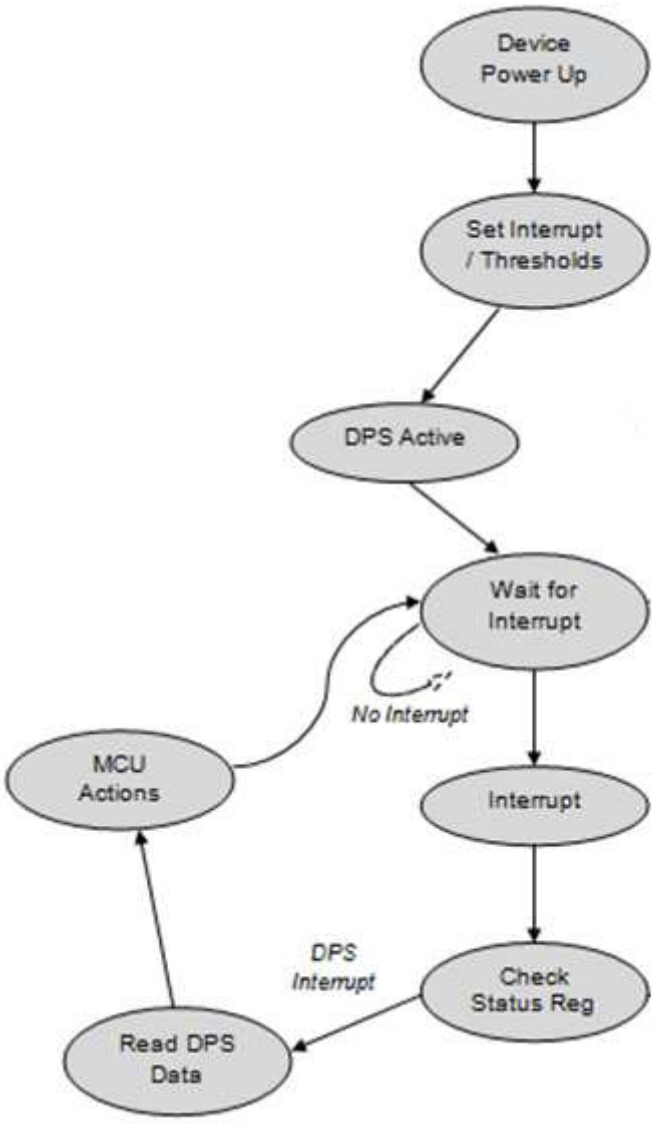


Figure 7.3 : Interrupt pin illustration FTN/NTF status reporting

Below flow diagram illustrates the LTR-706PS-01 operation involving the use of Thresholds and interrupt.



7.7 Example Pseudo Code

Control Registers

// The Control Registers define the operating modes and gain settings of the PS of LTR-706PS-01
// Default settings are 0x00 and 0x40 for PS registers (0x40).

```
Slave_Addr = 0x23                    // Slave address of LTR-706PS-01 device

Register_Addr = 0x80                 // Clock on register


// Enable PS
Register_Addr = 0x81                 // PS_CONTR register
Command = 0x42
WriteByte(Slave_Addr, Register_Addr, Command)
```

PS LED Registers

// The PS VCSEL Registers define the VCSEL pulse modulation pulse width, duty cycle and peak current.
// Default setting is 0x76 (15.625kHz, 12.5% Duty Cycle, 6mA).

```
Slave_Addr = 0x23                    // Slave address of LTR-706PS-01 device

Register_Addr = 0x82                 // PS_LED register
Command = 0x76                       // Pulse Duty Cycle 12.5%, 32us pulse width, peak current 6mA

WriteByte(Slave_Addr, Register_Addr, Command)
```

PS LED Number of pulses

// Default setting is 0x76 (15.625kHz, 12.5% Duty Cycle, 6mA).

```
Slave_Addr = 0x23                    // Slave address of LTR-706PS-01 device

Register_Addr = 0x83                 // PS_LED Register for Number of pulses
Command = 0x08                       // Number of pulses = 8

WriteByte(Slave_Addr, Register_Addr, Command)
```

PS Measurement Rate

// The PS_MEAS_RATE register controls the PS measurement rate.
// Default setting of the register is 0x04 (repeat rate 100ms)

```
Slave_Addr = 0x23                    // Slave address of LTR-706PS-01 device

// Set PS Repeat Rate 50ms
Register_Addr = 0x84                 // PS_MEAS_RATE register
Command = 0x06                       // Meas rate = 400ms

WriteByte(Slave_Addr, Register_Addr, Command)
```

PS Status Register (Read Only)

// The PS_STATUS Register contains the information on Interrupt, PS data availability status.

// This register is read only.

Slave_Addr = 0x23 // Slave address of LTR-706PS-01 device

// Read back Register
Register_Addr = 0x90 // PS_STATUS register address
ReadByte(Slave_Addr, Register_Addr, Data)

Interrupt_Status = Data & 0x0A // Interrupt_Status = 2(decimal) ➔ PS Interrupt

NewData_Status = Data & 0x05 // NewData_Status = 1(decimal) ➔ PS New Data

PS Data Registers (Read Only)

// The PS Data Registers contain the ADC output data.
// These registers should be read as a group, with the lower address being read first.

Slave_Addr = 0x23 // Slave address of LTR-706PS-01 device

// Read back PS_DATA registers
Register_Addr = 0x91 // PS_DATA low byte address
ReadByte(Slave_Addr, Register_Addr, Data0)

Register_Addr = 0x92 // PS_DATA high byte address
ReadByte(Slave_Addr, Register_Addr, Data1)

PS_ADC_Data = (Data1 << 8) | Data0 // Combining lower and upper bytes to give 16-bit PS data

Interrupt Registers

// The Interrupt register controls the operation of the interrupt pins and function.
// The default value for this register is 0x08 (Interrupt inactive)

Slave_Addr = 0x23 // Slave address of LTR-706PS-01 device

// Set Interrupt Polarity for Active Low, PS trigger
Register_Addr = 0x93 // Interrupt Register address
Command = 0x03 // Interrupt is Active Low and PS can trigger

WriteByte(Slave_Addr, Register_Addr, Command)

PS Threshold Registers

// The PS_THRES_UP and PS_THRES_LOW registers determines the upper and
// lower limit of the interrupt threshold value.
// Following example illustrates the setting of the PS dynamic threshold with hysteresis interruption for
// decimal value 1000 (for NEAR detection) and 500 (for FAR detection)

Slave_Addr = 0x23 // Slave address of LTR-706PS-01 device

//For NEAR detection (decimal 1000)
PS_Upp_Threshold_Reg_0 = 0x95 // PS Upper Threshold Low Byte Register address
PS_Upp_Threshold_Reg_1 = 0x96 // PS Upper Threshold High Byte Register address
Data1 = 1000 >> 8 // To convert decimal 1000 into two eight bytes register values
Data0 = 1000 & 0xFF
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_1, Data1)

PS_Low_Threshold_Reg_0 = 0x97 // PS Lower Threshold Low Byte Register address
PS_Low_Threshold_Reg_1 = 0x98 // PS Lower Threshold High Byte Register address

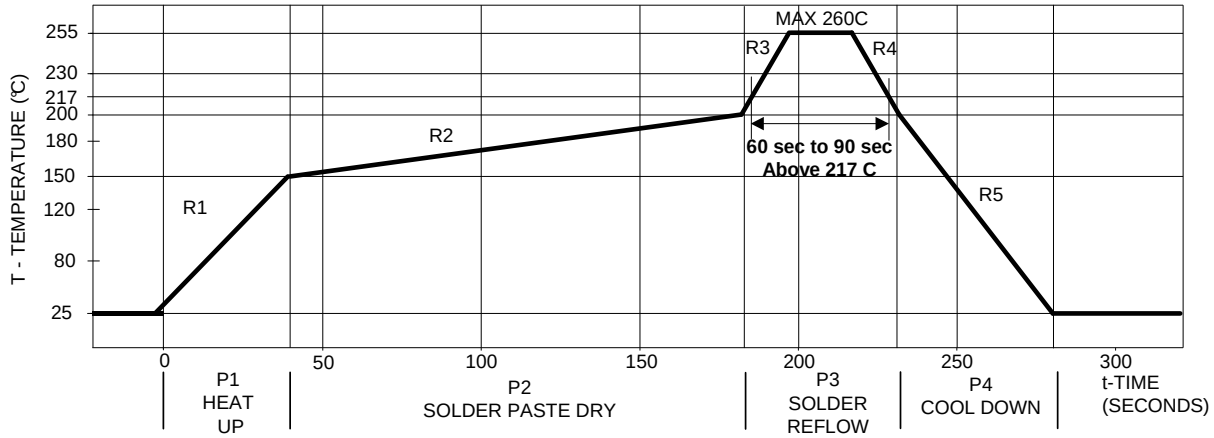
```
Data1 = 0 >> 8                                  // To convert decimal 0 into two eight bytes register values
Data0 = 0 & 0xFF
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_1, Data1)

//For FAR detection (decimal 500)
PS_Upp_Threshold_Reg_0 = 0x95                   // PS Upper Threshold Low Byte Register address
PS_Upp_Threshold_Reg_1 = 0x96                   // PS Upper Threshold High Byte Register address
Data1 = 2047 >> 8                               // To convert decimal 2047 into two eight bytes register values
Data0 = 2047 & 0xFF
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Upp_Threshold_Reg_1, Data1)

PS_Low_Threshold_Reg_0 = 0x97                   // PS Lower Threshold Low Byte Register address
PS_Low_Threshold_Reg_1 = 0x98                   // PS Lower Threshold High Byte Register address
Data1 = 500 >> 8                                // To convert decimal 500 into two eight bytes register values
Data0 = 500 & 0xFF
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_0, Data0)
WriteByte(Slave_Addr, PS_Low_Threshold_Reg_1, Data1)
```

Fault Detection Control Register

```
// Upon power up and before PS is enable, it is recommended that the fault detection is activated.
//This is done by the following instructions.
Slave_Addr = 0x23                               // Slave address of LTR-706PS-01 device

Register Addr = 0x9F                            //  Fault detection register
Command = 0x80                                  //  0x80 for Force detection of Full (Level1&2) fault detection
WriteByte(Slave_Addr, Register_Addr, Command)   //  0x90 for Force detection of Level1 fault detection

Command = 0x10                                  //  Activate the CLOCK to force a fault detection
WriteByte(Slave_Addr, Register_Addr, Command)

Register_Addr = 0x9F                            // Fault detection register
ReadByte(Slave_Addr, Register_Addr, Data)
Interrupt_Status = Data & 0x0F                  // Fault status = 8(decimal) ➔ ENB Gate stuck low
                                                // Fault status = 4(decimal) ➔ ENB Gate stuck high
                                                // Fault status = 2(decimal) ➔ ENB Fault
                                                // Fault status = 1(decimal) ➔ VCSEL fault

Command = 0x00                                  //  De-Activate the CLOCK to stop the fault detection
WriteByte(Slave_Addr, Register_Addr, Command)


// Setting the fault level of the fault detection.
//This is done by the following instructions.
Slave_Addr = 0x23                               // Slave address of LTR-706PS-01 device

Register_Addr = 0x65                            // Enable write permission for register 0x9F
Command = 0x79                                  // Enable write permission for register 0x9F
WriteByte(Slave_Addr, Register_Addr, Command)

Register Addr = 0x03                            // Enable write permission for register 0x9F
Command = 0x82                                  // Enable write permission for register 0x9F
WriteByte(Slave_Addr, Register_Addr, Command)

Register Addr = 0x9F                            //  Fault detection register
Command = 0x00                                  //  0x00 for Force detection of Full (Level1&2) fault detection
WriteByte(Slave_Addr, Register_Addr, Command)   //  0x10 for Force detection of Level1 fault detection

Register_Addr = 0x83                            // PS_LED Register for Number of pulses
Command = 0x08                                  // Number of pulses = 8
```

```
Register_Addr = 0x81                    // PS_CONTR register
Command = 0x02                          // PS ON
WriteByte(Slave_Addr, Register_Addr, Command)

Register_Addr = 0x9F                    // Fault detection register
ReadByte(Slave_Addr, Register_Addr, Data)
Interrupt_Status = Data & 0x0F          // Fault status = 8(decimal) ➔ ENB Gate stuck low
                                        // Fault status = 4(decimal) ➔ ENB Gate stuck high
                                        // Fault status = 2(decimal) ➔ ENB Fault
                                        // Fault status = 1(decimal) ➔ VCSEL fault
```

8 Recommended Lead-free Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point , 217°C		> 217°C	60s to 90s
Peak Temperature		260°C	-
Time within 5°C of actual Peak Temperature		> 255°C	20s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

It is recommended to perform reflow soldering no more than three times without rework.

For manual soldering, the soldering iron tip shall not touch the package plastic body, The soldering iron shall only in contact to the circuit board pad and the heat should be conducted to the tin wire and component lead. The temperature of the solder iron can be set as high as 300 degree but the temperature on the tip of the tool shall be 270 to 275ºC. Soldering process shall take a few seconds for each pin/pad. The package maximum temperature shall be kept less than 270ºC and all mechanical stresses in the pin should be minimized. It should be noted that the thermoplastic shield material (PA9T) attached on top of the component has a thermal deflection temperature of around 280 degree and will be damaged if excessive heat above this temperature is used.

9 Moisture Proof Packaging

All LTR-706PS-01 are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC J-STD-033A Level 3.

Time from Unsealing to Soldering

After removal from the moisture barrier bag, the parts should be stored at the recommended storage conditions and soldered within seven days. When the moisture barrier bag is opened and the parts are exposed to the recommended storage conditions for more than seven days, the parts must be baked before reflow to prevent damage to the parts.

Recommended Storage Conditions

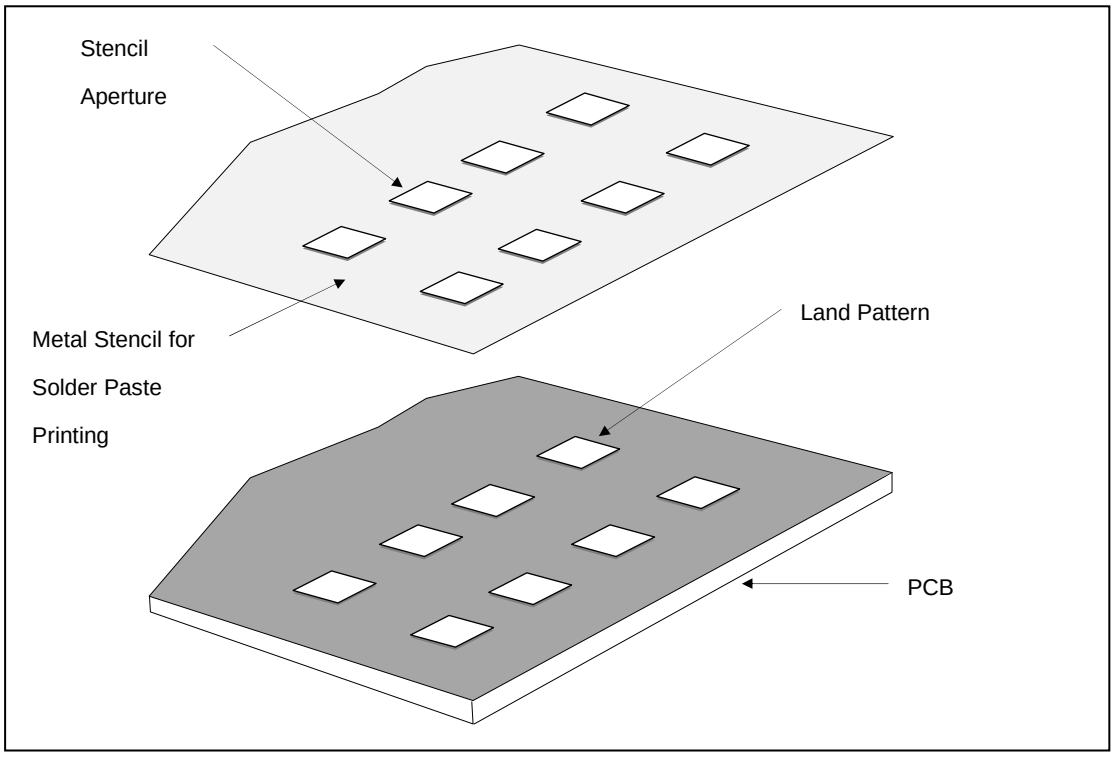
Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Baking Conditions

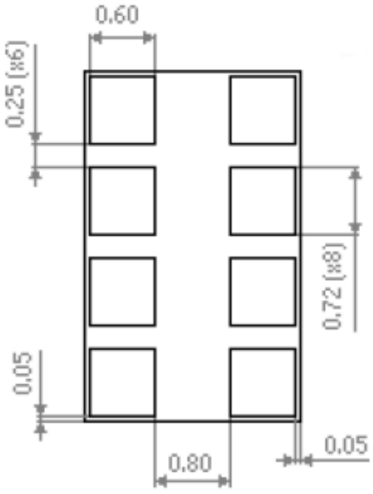
Package	Temperature	Time
In Reels	60°C	48 hours
In Bulk	100°C	4 hours

- Baking should only be done once.

10 Recommended Land Pattern and Metal Stencil Aperture



10.5 Recommended Land Pattern

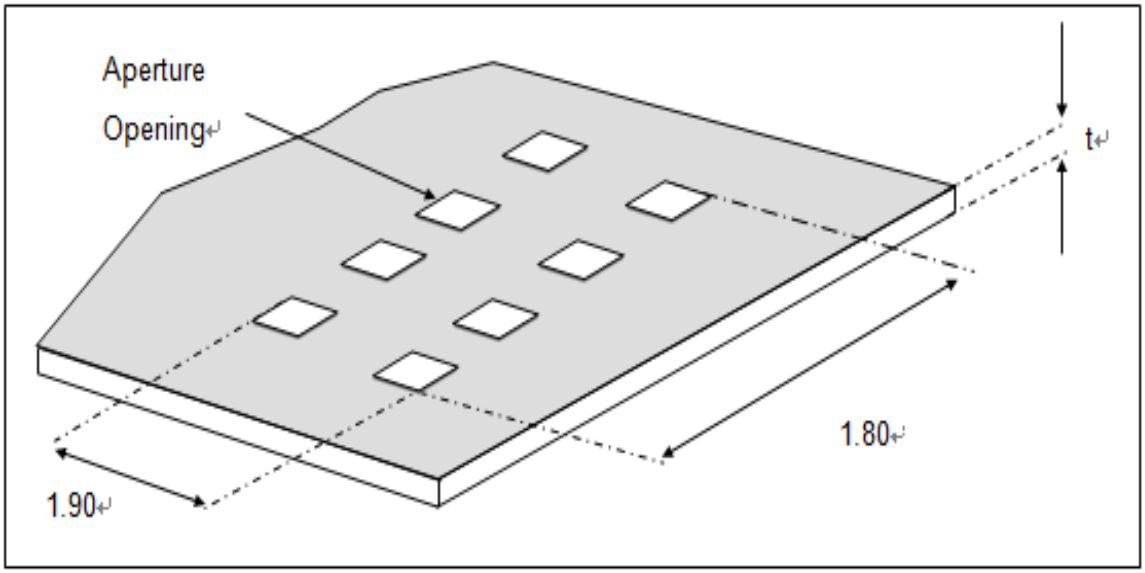


Note: All dimensions are in millimeters.

2. Recommended Metal Stencil Aperture

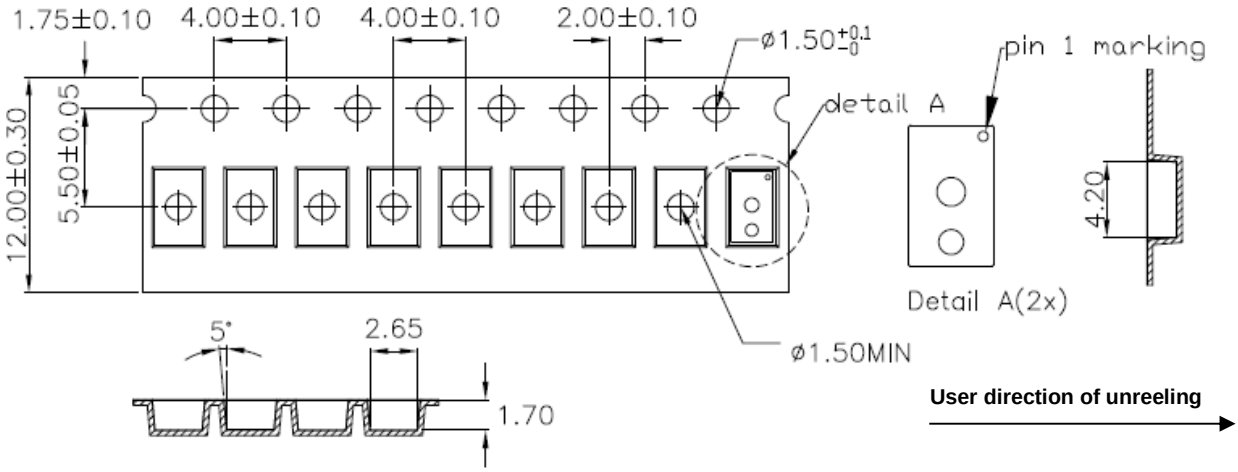
It is recommended that the metal stencil used for solder paste printing has a thickness (t) of 0.11mm (0.004 inches / 4 mils) or 0.127mm (0.005 inches / 5 mils).

The stencil aperture opening is recommended to be 0.30mm x 0.35mm which has the same dimension as the land pattern. This is to ensure adequate printed solder paste volume and yet no shorting.



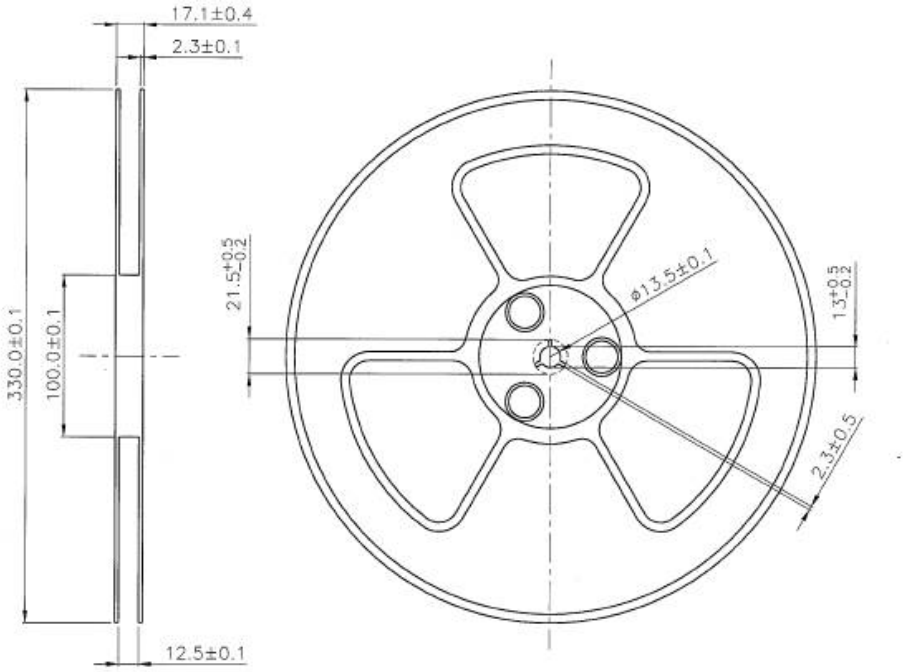
Note: All dimensions are in millimeters.

11 Package Dimension for Tape and Reel



Note:

1. All dimensions are in millimeters



Notes:

1. All dimensions are in millimeters (inches).
2. Empty component pockets sealed with top cover tape.
3. 13 inch reel – 8000 pieces per reel.
4. In accordance with ANSI/EIA 481-1-A-1994 specifications.

12 Revision Table

Version	Update	Page	Date
1.0	Final Datasheet as created	Total 35	06-Sep-16