T-73-65

TELEDYNE COMPONENTS

4860

FAST, 12-BIT SAMPLE/HOLD AMPLIFIER

FEATURES

- Acquisition Time for a 10V Step to ±0.01%FS .....200 ns Max
- Sample-to-Hold Settling Time .....100 ns Max
- Aperture Jitter .....±50 psec
- Feedthrough Attenuation .....74 dB
- TTL Compatible

APPLICATIONS

- Transient Recorders
- Fast Fourier Analysis
- High Speed DASs
- High Speed DDSs
- Analog Delay and Storage

GENERAL DESCRIPTION

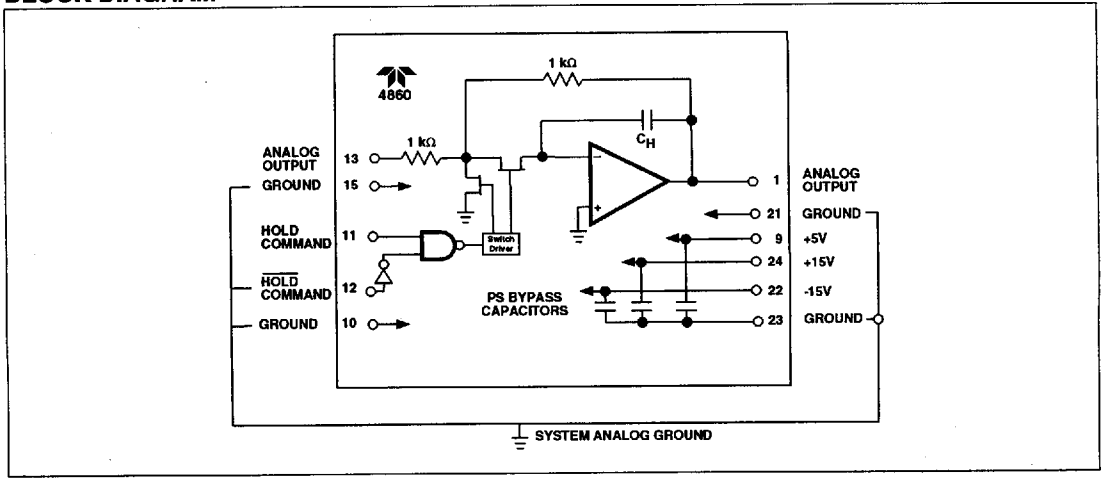
The 4860 is a very fast, high-resolution sample/hold (track/hold) amplifier. Its acquisition time and sample-to-hold settling time (a S/H's two throughput limiting specifications) are guaranteed to ±0.01%, unlike other S/H amplifiers that only achieve ±0.1% or ±1%. The 4860 acquires a 10V signal step to ±0.01% in 200 nsec maximum and then tracks signal components up to 16 MHz. In the track mode, offset error is typically ±0.5 mV, and gain error is typically ±0.05%. When commanded to Hold the 4860's output settles within ±0.01%FS of its final value in 100 nsec maximum. The aperture delay time is 6 nsec, aperture jitter is ±50 psec, and pedestal is a minimal ±2.5 mV. In the hold mode the output droop rate is a low 5 µV/µsec maximum and feedthrough attenuation, at 2.5 MHz, is an impressive 74 dB.

Its 24-pin, dual-in-line package, gain of -1, ±10V input/output range, and TTL compatible logic make the 4860's performance compatible with many industry standard devices. Being a second-generation design, however, the 4860 is superior to these units in almost every performance specification. Faster switching and better feedthrough attenuation are the results of our unique MOSFET switching scheme. Shorter acquisition and settling times and considerably lower droop are the result of our proprietary high speed, FET input op amp designs.

A standard device is specified for 0°C to +70°C. The High Reliability (HR) version is specified for -55°C to +125°C temperature range.

9

BLOCK DIAGRAM



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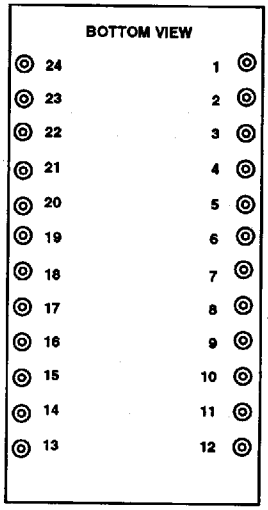
FAST, 12-BIT TRACK/HOLD AMPLIFIER

4860

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	ANALOG OUTPUT	13	ANALOG INPUT
2	NC	14	NC
3	NC	15	GROUND
4	NC	16	NC
5	NC	17	NC
6	NC	18	NC
7	NC	19	NC
8	NC	20	NC
9	+5V SUPPLY	21	GROUND
10	GROUND	22	-15V SUPPLY
11	HOLD	23	GROUND
12	$\overline{\text{HOLD}}$	24	+15V SUPPLY

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC}	±15V Supplies ..... ±18V	T_C	Operating Temperature Range (Case)
V_{DD}	+5V Supply ..... -0.5V to +7V		4860 ..... 0°C to +70°C
V_{IN}	Analog Input ..... $\pm V_{CC}$		4860-HR ..... –55°C to +125°C
V_{ID}	Digital Input ..... -0.5V to +5.5V	T_{STG}	Storage Temperature Range ..... –65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
V_{IN}	Input Voltage Range		±10.25	±11.50	—	±10.25	±11.50	—	V
Z_{IN}	Input Impedance		—	1	—	—	1	—	kΩ
V_{OS}	Input Offset Voltage	Track Mode	—	±0.5	±5	—	±0.5	±5	mV
V_{OS} TC	Input Offset Voltage vs Temperature	T_{MIN} to T_{MAX}	—	±60	±300	—	±60	±300	µV/°C
PSRR	Power Supply Rejection Ratio		—	66	—	—	66	—	dB
V_O	Output Voltage Swing	R_L = 2 kΩ	±10.25	±11.50	—	±10.25	±11.50	—	V
I_O	Output Current		±40	—	—	±40	—	—	mA
Z_O	Output Impedance		—	0.1	—	—	0.1	—	Ω
A_V	Voltage Gain		—	-1	—	—	-1	—	V/V
A_A	Gain Accuracy		—	±0.05	±0.1	—	±0.05	±0.1	%
		T_{MIN} to T_{MAX}	—	±0.05	±0.15	—	±0.05	±0.15	%
A_L	Gain Nonlinearity		—	±0.003	±0.01	—	±0.003	±0.01	%FS
A_V TC	Gain Drift		—	±0.5	±5	—	±0.5	±5	ppm/°C
V_P	Pedestal Voltage	V_{IN} = 0V	—	±2.5	±20	—	±2.5	±20	mV
V_P TC	Pedestal Drift		—	±80	—	—	±80	—	µV/°C

FAST, 12-BIT TRACK/HOLD AMPLIFIER

DC CHARACTERISTICS: (Continued)

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
V_{IH}	Logic "1" Input Voltage		2	—	—	2	—	—	V
V_{IL}	Logic "0" Input Voltage		—	—	**0.8**	—	—	**0.8**	V
$\pm V_{CC}$	Voltage Range	±15V Supply	—	±3	—	—	±3	—	%
		±5V Supply	—	±5	—	—	±5	—	%
$\pm I_{CC}$	Quiescent Current	±15V Supply	—	±21	**±25**	—	±21	**±25**	mA
		±5V Supply	—	17	**25**	—	17	**25**	mA
P_D	Power Dissipation		—	730	**875**	—	730	**875**	mW

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

9

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
t_{acq}	Acquisition Time	10V step to 0.01%FS (±1 mV)	—	160	200	—	160	200	ns
		10V step to 0.1%FS (±10 mV)	—	100	170	—	100	170	ns
		10V step to 1%FS (±100 mV)	—	90	—	—	90	—	ns
		1V step to 1%FS (±100 mV)	—	75	—	—	75	—	ns
t_s	Settling Time, Sample to Hold	to 0.01%FS (±1 mV)	—	60	100	—	60	100	ns
		to 0.1%FS (±10 mV)	—	40	—	—	40	—	ns
V_{TSH}	Sample tof Hold Transient		—	180	—	—	180	—	mVp-p
t_{ad}	Aperture Delay Time		—	30	—	—	30	—	ns
t_{aj}	Aperture Jitter		—	±50	—	—	±50	—	ps
sr	Slew Rate		—	±300	—	—	±300	—	V/µs
BW	Small Signal Bandwidth (-3 dB)		—	16	—	—	16	—	MHz
V_{HD}	Droop Rate		—	±0.5	±5	—	±0.5	±5	µV/µs
F_{RR}	Feedthrough Rejection Ratio	f = 2.5 MHz, V_{IN} = 20 Vp-p	—	74	—	—	74	—	dB

FAST, 12-BIT TRACK/HOLD AMPLIFIER

T-73-65

4860

APPLICATIONS INFORMATION

The 4860 is ideally suited for 12 to 14-bit high speed data acquisition/distribution systems. In a ±10V system, its ±0.01%FS (±0.005%FSR) linearity is equivalent to better than ±1/2LSB in 13 bits. Its low ±50ps aperture uncertainty enables it to accurately (±1/2LSB in 12 bits) sample signals with slew rates up to 24.4V/µsec. Its low, 5µV/µsec, output droop rate enables it to hold signals to ±1/2LSB in 14 bits for up to 125µsec. The 4860 is functionally laser trimmed at the factory to correct offset, pedestal and gain errors, and is designed to be used without external adjustments. If system requirements call for tighter accuracies, units can be selected at the factory or adjustments can be made to the A/D or D/A used with the 4860.

Grounding and Bypassing

With proper grounding and bypassing, the 4860 meets all its published performance specifications without any additional external components. The device has four ground pins (Pins 10, 15, 21 and 23), and all must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the 4860 and have all four ground pins soldered directly to it. Pin 10 is particularly sensitive to ground noise because most of the digital elements that constitute the switch drive circuit are grounded to Pin 10. Noise in the switch drive circuit couples directly to the main op amp summing junction—the most noise-sensitive point in any S/H circuit. Most digital ground currents enter or leave the 4860 through Pin 10, therefore, in order to keep the output clean, care must be taken to ensure that no ground potentials exist between Pin 10 and the other ground pins. This is why Pin 10 must be tied to the analog and not the digital ground system. For the same reason, the +5V digital logic supply (Pin 9) should be kept as clean as possible. This supply (as well as the ±15V supplies, Pins 24 and 22) is bypassed to ground with a 0.01µF ceramic capacitor inside the 4860. In critical applications, additional external 0.1µF to 1µF tantalum bypass capacitors may be required.

Sample/Hold Command

A TTL logic "0" applied to Pin 11, or a logic "1" applied to Pin 12 puts the 4860 into the sample (track) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output follows (tracks) its input. A logic "1" applied to Pin 11 and a logic "0" applied to Pin 12 puts the 4860 into the hold mode, and the output is held constant at the level present when the hold command was given. If Pin 11 is used to control the 4860, Pin 12 must be connected to digital ground. If Pin 12 is used to control the 4860, Pin 11 must be tied to +5V. Pins 11 and 12 each represent 1 TTL load to the digital drive circuit.

Capacitive and Resistive Loading

In order to avoid oscillations, current limiting or performance variations over temperature, the 4860's output loading has certain restrictions. To avoid oscillation the largest capacitive load is typically 250 pF. The largest recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitive loads will affect both acquisition and settling time.

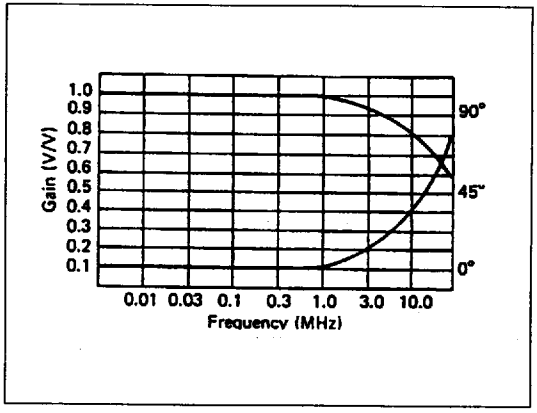


Figure 1. Track Mode Gain Amplitude and Phase Response

Aperature Jitter

The most common use of sample (track)/hold amplifiers is as an input for A/D converters to permit the accurate digitizing of signals with slew rates (frequencies) much higher than the A/D alone could handle. A rule of thumb for obtaining desired accuracy in successive approximation type A/D conversion is to ensure that the analog input signal being converted does not change by more than ±1/2LSB during the conversion. Applying this rule to any given A/D converter, one can calculate an input slew rate limit beyond which accurate digitizing is impossible. The slew rate can then be converted to a frequency limit if you choose to speak in those terms.

Example: For a 12-bit 500ns A/D converter with a ±2.5V input range, 1/2LSB is equivalent to .61 mV. If the input is not allowed to change more than .61 mV in 500 ns, the ADC's input slew rate limit is ±1.22 mV/µsec. If one were trying to accurately digitize a ±2.5V sine wave its frequency would have to be less than 77.7 Hz.

FAST, 12-BIT TRACK/HOLD AMPLIFIER

T-73-65

For example: $dv/dt\ (max) = 2.5\omega\cos\omega t\ (Max)$

$1.22mV/\mu s = 2.5\omega$

$1.22mV/\mu s = 5\pi f$

$77.7\ (Hz) = f\ (Max)$

A sample/hold in front of an A/D converter can "freeze" the converter's input signal whenever a conversion is made. Even though the S/H reduces system throughput, because the S/H acquisition time has to be added to the A/D conversion time, it makes it possible for the A/D to accurately digitize input signals with much higher slew rates (frequencies). How is this accomplished? Let's look at the timing for a conversion that uses a sample/hold input buffer.

Once a S/H (T/H) has acquired an input signal and is tracking it, the S/H can be commanded to hold at any instant. There is normally a small delay between the time the unit is commanded to hold and the time it actually holds. This delay is called aperture delay time or aperture time delay. It normally does not present a problem because the hold command signal can be advanced in time to make the amplifier hold at the correct time. Aperture delay time can vary as a given device takes sample after sample. The sample-to-sample variation in aperture delay time is called aperture jitter. Although aperture delay time is not normally a problem, aperture jitter is a problem. This is because it is impossible to control or compensate for aperture jitter. Since we have no control during the period of aperture jitter, w ould like our input signal to change as little as possible during this period. To return to our rule of thumb, we don't want the input to change by more than ±1/2LSB. Therefore, if we're using a S/H in front of an A/D converter, the slew rate limitation is no longer ±1/2LSB during the conversion time but ±1/2LSB during the aperture jitter time.

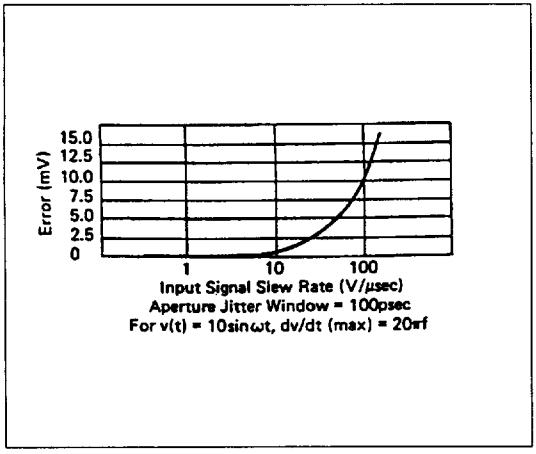


Figure 2. Accuracy Error Due to Aperture Uncertainty

The 4860 has a ±50 psec aperture jitter. This means there is a 100 psec period during which the input signal should not change more than ±1/2LSB. If, for example, you are using the 4860 S/H in front of a 12-bit A/D converter, then 1/2LSB = 0.61 mV. The input signal slew rate limitation for accurate digitizing is then 0.61 mV/100 psec or 6.1V/µsec. This is equivalent to the highest slew rate one would encounter in a ±2.5V sine wave with a frequency of 388 kHz. This is a considerable improvement over the 78 Hz sine wave that a 12-bit, 500 ns ADC could accurately digitize without a S/H. Notice that 388 kHz to 78 Hz is the same ratio as 500 nsec, the ADC's conversion time, to 100 psec, the 4860's aperture jitter.

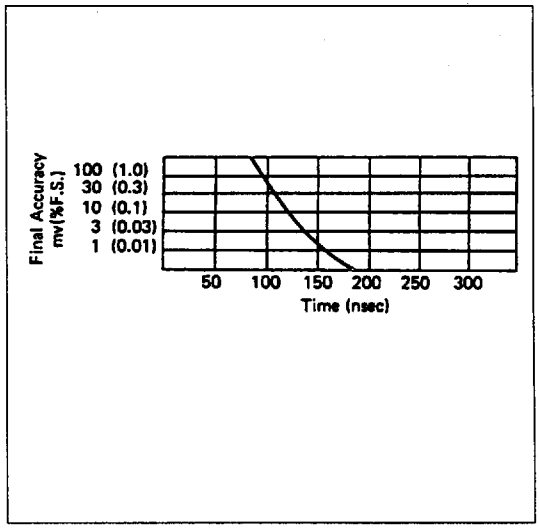


Figure 3. Acquisition Accuracy vs Acquisition Time for 10V Step

This procedure, which determines how fast a signal a given S/H permits one to digitize, assumes that the output droop rate of the chosen sample/hold is low enough to keep the A/D's input constant to within ±1/2LSB during a conversion time. It also assumes that at the input slew rate (frequency) of interest, the S/H's output is not slew rate (bandwidth) limited. Lastly, the fact that a given S/H and A/D combination can accurately digitize the fastest portions of a 388 kHz sine wave does not mean that the same combination can be used to digitize that signal for reproduction purposes. Nyquist criteria state that you have to sample a 388 kHz sine wave at twice its frequency, i.e. you have to take a sample every 1.25µsec. The 4860/ADC combination must sample at least this fast to reproduce the input.

9

FAST, 12-BIT TRACK/HOLD AMPLIFIER

T-73-65

Using the 4860 with A/D Converters

There are two important considerations when using S/Hs to drive successive approximation A/Ds. The first is a dual requirement—the S/H's output stage should exhibit a very low impedance compared to the A/D's input impedance, usually 1 to 10 kΩ, at frequencies up to five times the A/D's clock period; and the S/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, therefore, the S/H will be required to sink or source large, high frequency current transients and recover within one clock period. In the hold mode, the 4860's output impedance is typically 0.1Ω. Its output typically recovers (to ±0.01%) from a 2mA step in less than 100 nsec.

The second consideration involves the S/H's sample-to-hold transient settling time. If the same timing pulse that puts the S/H into the hold mode initiates the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable, accurate input when it makes the final decision on whether its MSB output should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In most applications by using the 4860 in front of a successive approximation A/D converter, the 4860's HOLD or HOLD can be driven directly from the converter's status output. The status output changes state when the converter receives a convert command, and this change can be used to drive the S/H from the track to the hold mode. The reverse change in state of the status output at the end of the conversion can also be used to set the S/H back into the track mode.