FEATURES

- **25, 35, 45 ns Read Access & R/W Cycle Time**
- **Unlimited Read/Write Endurance**
- **Automatic Non-volatile STORE on Power Loss**
- **Non-Volatile STORE Under Hardware or Software Control**
- **Automatic RECALL to SRAM on Power Up**
- **Unlimited RECALL Cycles**
- **200K STORE Cycles**
- **20-Year Non-volatile Data Retention**
- **Single 3.0V + 20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **Small Footprint SOIC & SSOP Packages (RoHS-Compliant)**

DESCRIPTION

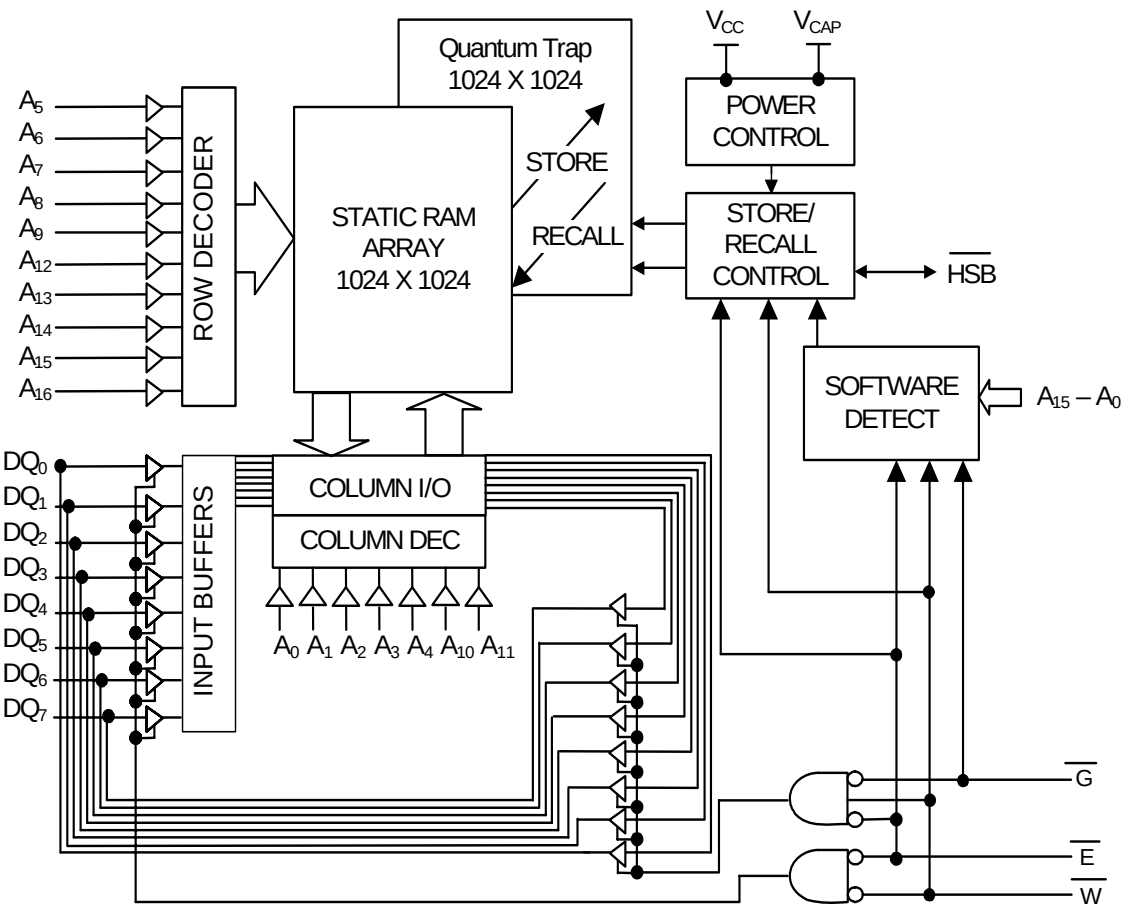
The Simtek STK14CA8 is a 1Mb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

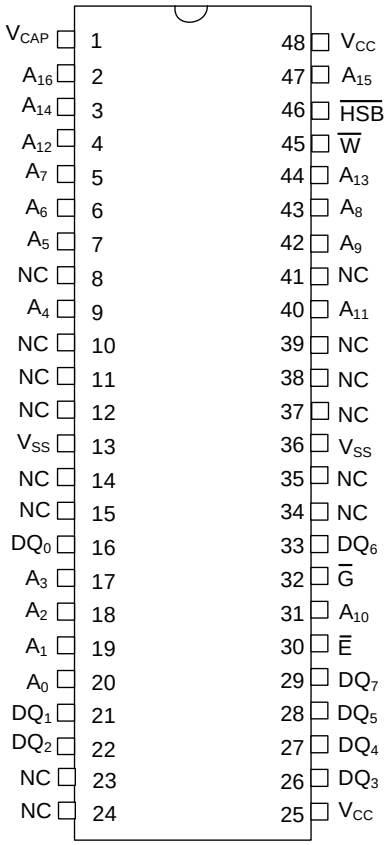
Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power up, data is automatically restored to the SRAM (the *RECALL* operation). Both STORE and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

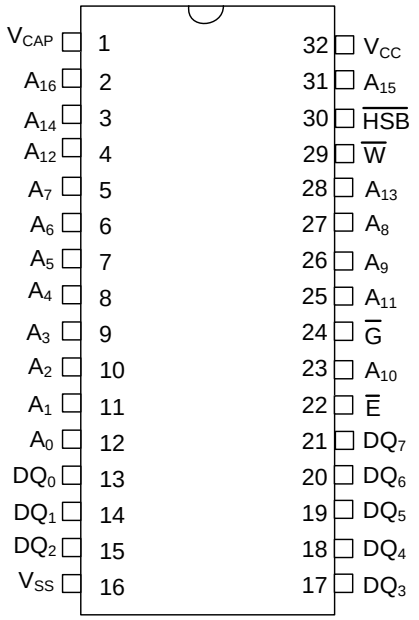
BLOCK DIAGRAM



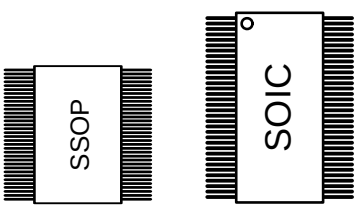
PACKAGES



48-Pin SSOP



32-Pin SOIC



Relative PCB area usage.

See page 17 for detailed package size specifications.

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{16}-A_0	Input	Address: The 17 address inputs select one of 131,072 bytes in the nvSRAM array
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 3.0V, +20%, -10%
$\overline{HSB}$	I/O	$\overline{Hardware\ Store\ Busy}$: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
V_{CAP}	Power Supply	Autostore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V_{SS}	Power Supply	Ground
NC	No Connect	Unlabeled pins have no internal connections.

ABSOLUTE MAXIMUM RATINGS

Voltage on Input Relative to Ground . . . . . –0.5V to 4.1V
Voltage on Input Relative to V_{SS} . . . . . .–0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ . . . . . .–0.5V to (V_{CC} + 0.5V)
Temperature under Bias. . . . . .–55°C to 125°C
Junction Temperature . . . . . .–55°C to 140°C
Storage Temperature . . . . . .–65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NF (SOP-32) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} 5.4 C/W; θ_{ja} 44.3 [0fpm], 37.9 [200fpm], 35.1 C/W [500fpm].

RF (SSOP-48) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} 6.2 C/W; θ_{ja} 51.1 [0fpm], 44.7 [200fpm], 41.8 C/W [500fpm].

DC CHARACTERISTICS

(V_{CC} = 2.7V-3.6V)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}	Average V_{CC} Current		65 55 50		70 60 55	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC_2}	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of STORE cycle (t_{STORE})
I_{CC_3}	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Other Inputs Cycling at CMOS Levels Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC_4}	Average V_{CAP} Current during AutoStore Cycle		3		3	mA	All Inputs Don't Care Average current for duration of STORE cycle (t_{STORE})
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Levels)		3		3	mA	$\overline{E} \geq (V_{CC}$ -0.2V) All Others $V_{IN} \leq$ 0.2V or $\geq (V_{CC}$-0.2V) Standby current level after nonvolatile cycle complete
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} –0.5	0.8	V_{SS} –0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	3.3V + 0.3V
V_{CAP}	Storage Capacitance	17	120	17	120	µF	Between V_{CAP} pin and V_{SS}, 5V rated.
NV_C	Nonvolatile STORE operations	200		200		K	
$DATA_R$	Data Retention	20		20		Years	@ 55 deg C

Note: The HSB pin has I_{OUT}=-10 uA for V_{OH} of 2.4 V, this parameter is characterized but not tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: These parameters are guaranteed but not tested.

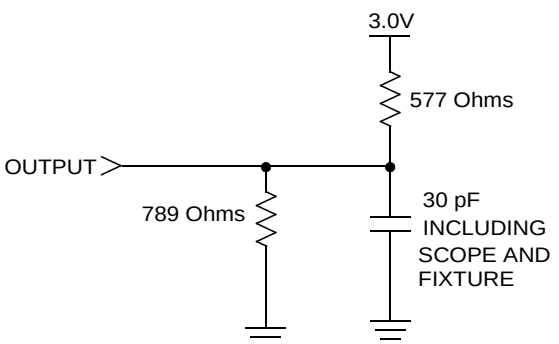


Figure 1: AC Output Loading

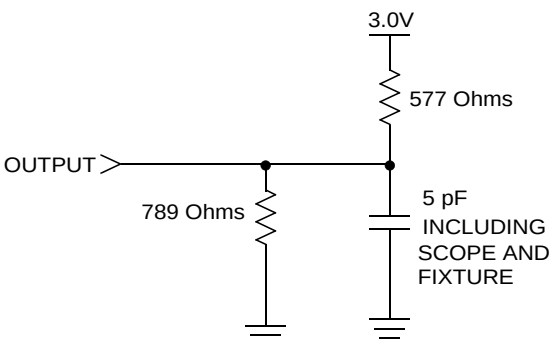


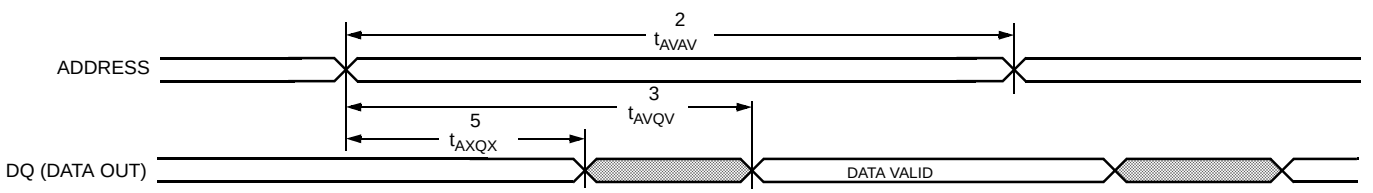
Figure 2: AC Output Loading for Tristate Specs (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ})

SRAM READ CYCLES #1 & #2

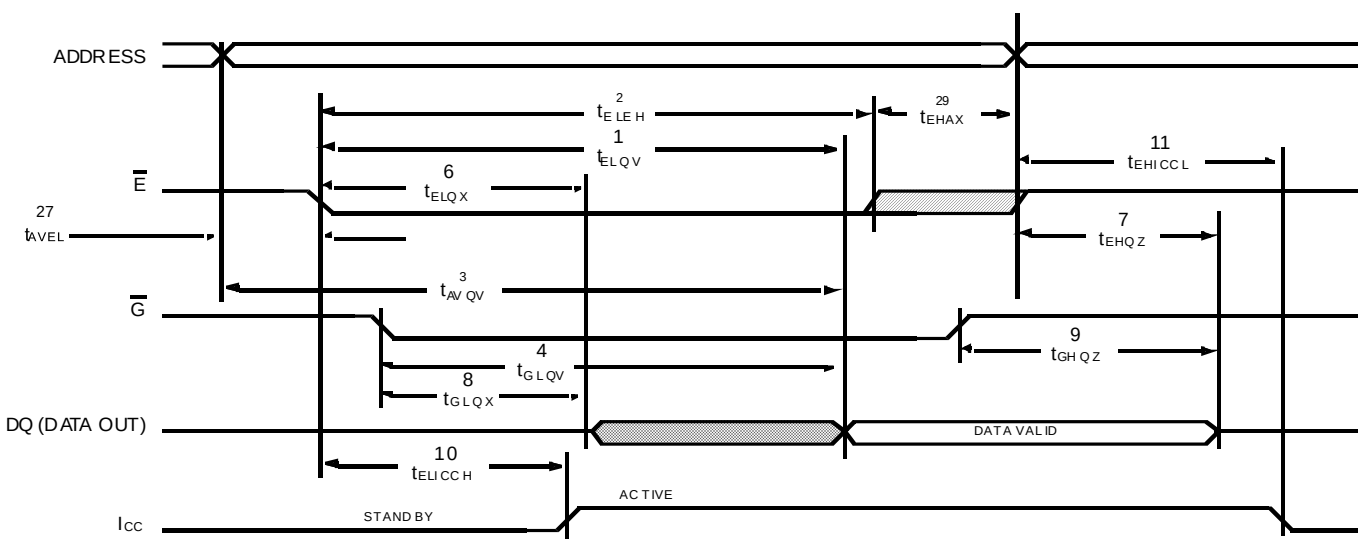
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1		t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[c]	t_{ELEH}[c]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[d]	t_{AVQV}[d]	t_{AA}	Address Access Time		25		35		45	ns
4		t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
5	t_{AXQX}[d]	t_{AXQX}[d]	t_{OH}	Output Hold after Address Change	3		3		3		ns
6		t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	3		3		3		ns
7		t_{EHQZ}[e]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		13		15	ns
8		t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9		t_{GHQZ}[e]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10		t_{ELICCH}[b]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11		t_{EHICCL}[b]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note c: $\overline{W}$ must be high during SRAM READ cycles.
Note d: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low
Note e: Measured ± 200mV from steady state output voltage.
Note f: HSB must remain high during READ and WRITE cycles.

SRAM READ CYCLE #1: Address Controlled[c,d,f]



SRAM READ CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[c,f]

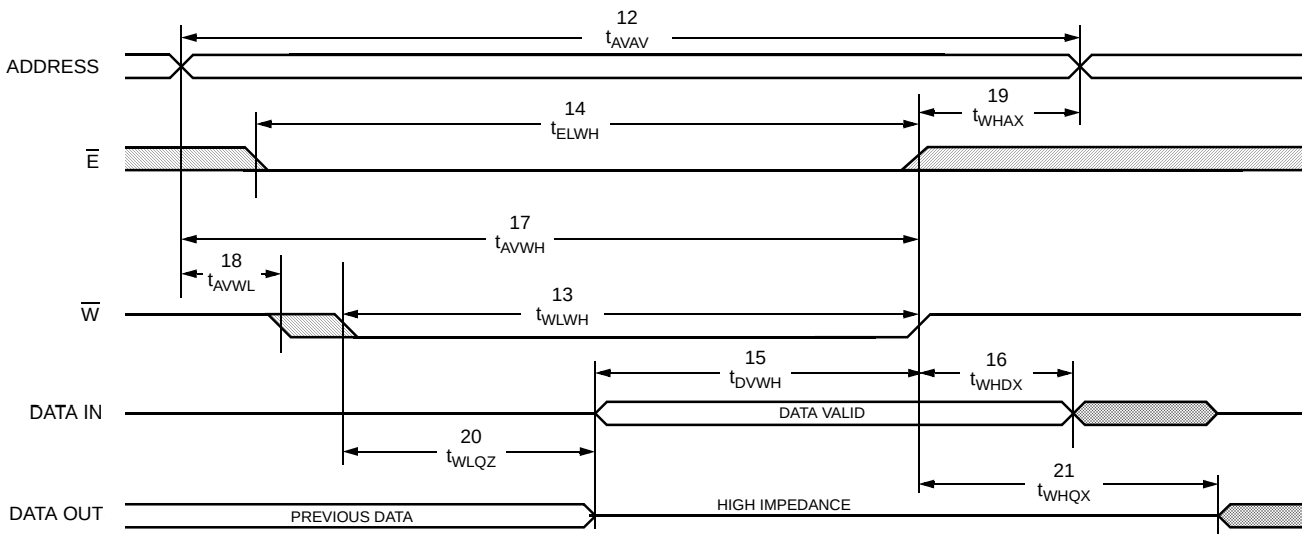


SRAM WRITE CYCLES #1 & #2

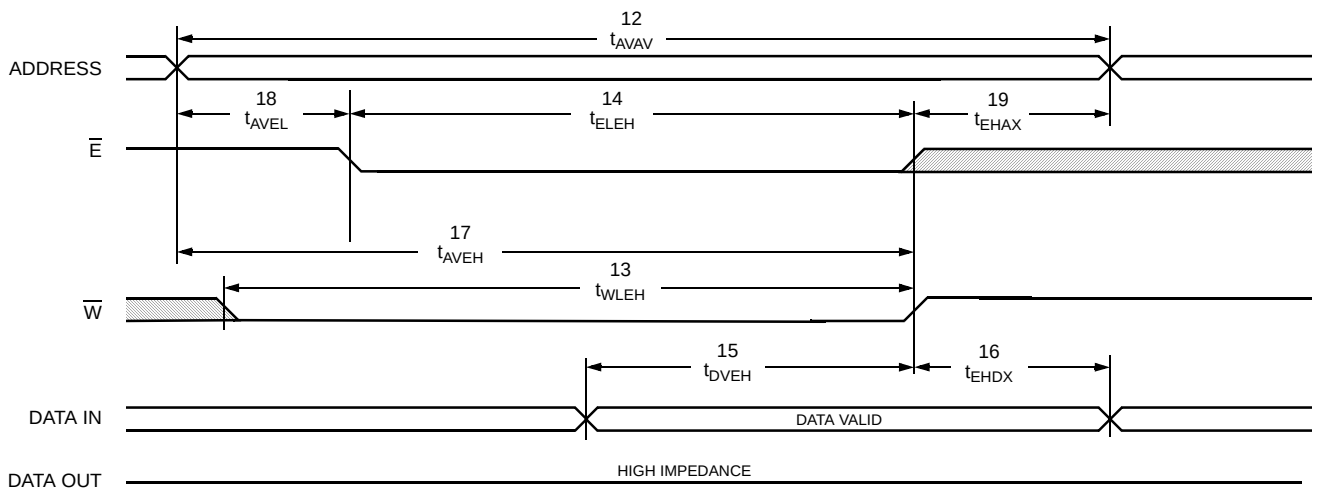
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[e, g]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[g,h]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[g,h]

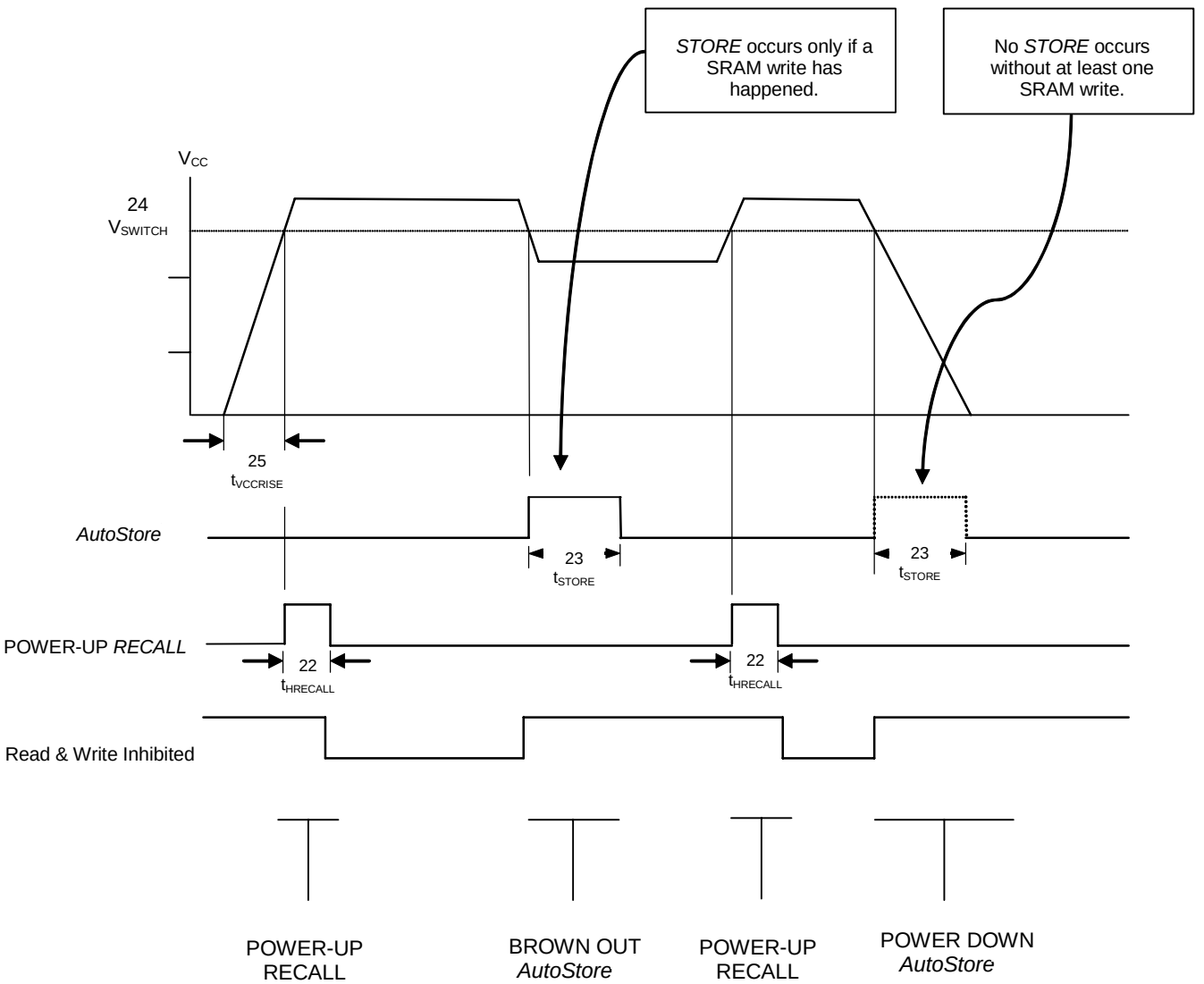


AutoStore/POWER-UP *RECALL*

NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{HRECALL}$		Power-up *RECALL* Duration		20	ms	i
23	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		12.5	ms	j,k
24	V_{SWITCH}		Low Voltage Trigger Level		2.65	V	
25	V_{CCRISE}		V_{CC} Rise Time	150		µs	

Note i: $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}
Note j: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE will take place
Note k: Industrial Grade Devices require 15 ms MAX.

AutoStore/POWER-UP *RECALL*



Note: Read and Write cycles will be ignored during STORE, RECALL and while V_{CC} is below V_{SWITCH}

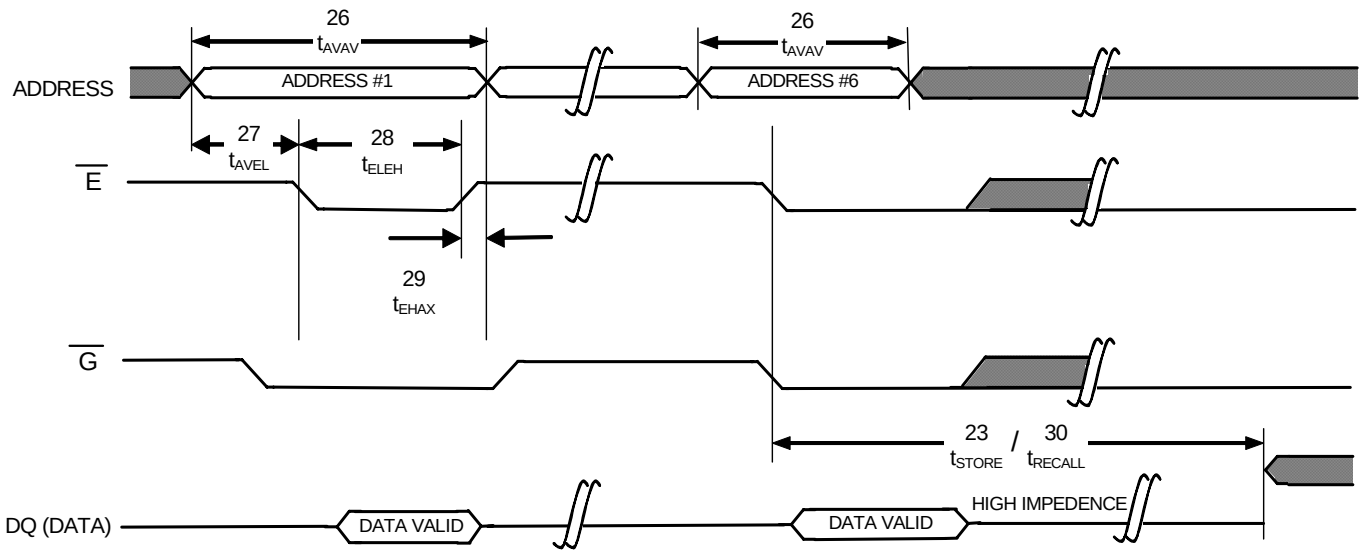
SOFTWARE-CONTROLLED *STORE/RECALL* CYCLE[l,m]

NO.	Symbols			PARAMETER	STK14CA8-35		STK14CA8-35		STK14CA8-45		UNITS	NOTES
	$\overline{E}$ Cont	$\overline{G}$ Cont	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
26	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE/RECALL* Initiation Cycle Time	25		35		45		ns	m
27	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time	0		0		0		ns	
28	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
29	t_{EHAX}	t_{GHAX}		Address Hold Time	1		1		1		ns	
30	t_{RECALL}	t_{RECALL}		*RECALL* Duration		50		50		50	µs	

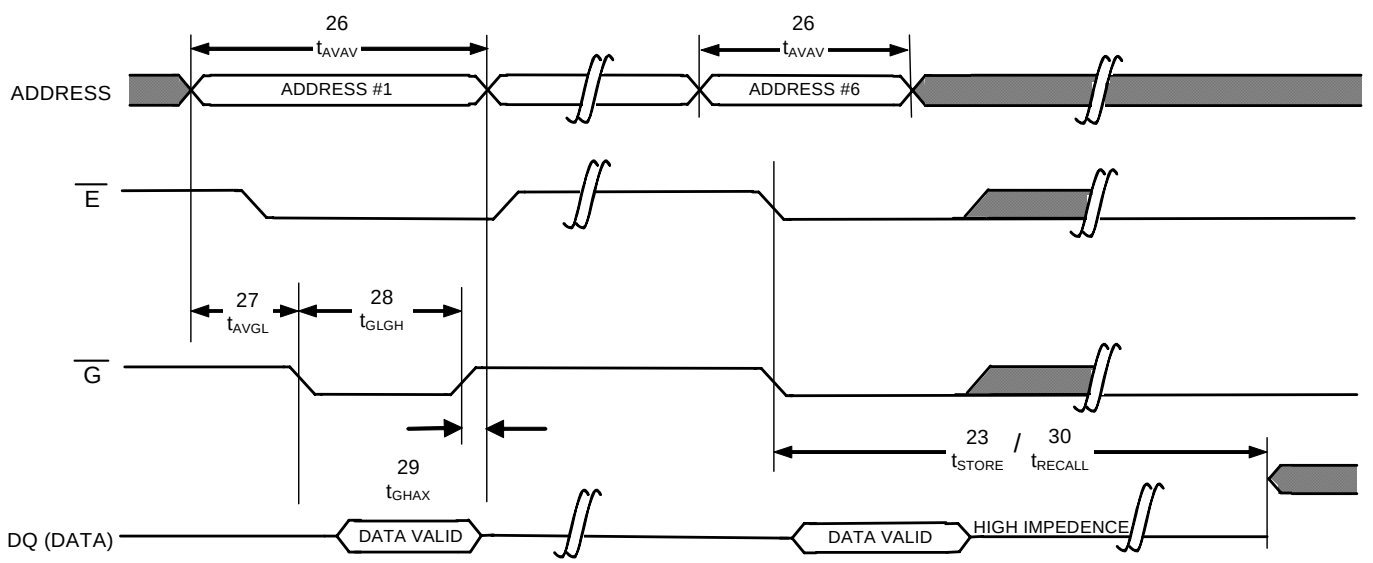
Note l: The software sequence is clocked on the falling edge of $\overline{E}$ controlled READs or $\overline{G}$ controlled READs

Note m: The six consecutive addresses must be read in the order listed in the in the Software *STORE/RECALL* Mode Selection Table. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ CONTROLLED[m]



SOFTWARE *STORE/RECALL* CYCLE: $\overline{G}$ CONTROLLED[m]

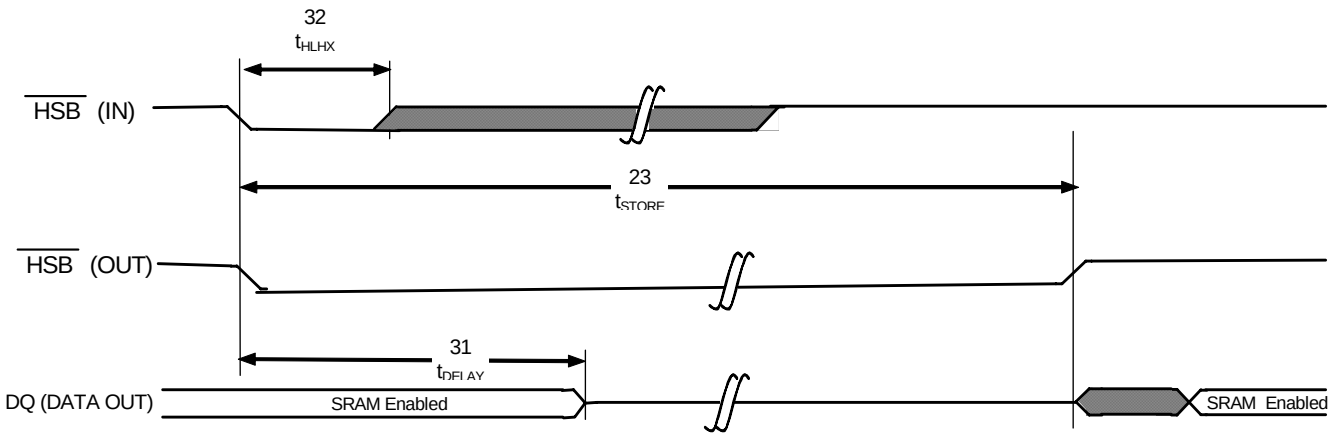


HARDWARE STORE CYCLE

	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
31	t_{DELAY}	t_{HLQZ}	Hardware STORE to SRAM Disabled	1	70	µs	n
32	t_{HLHX}		Hardware STORE Pulse Width	15		ns	

Note n: On a hardware STORE initiation, SRAM operation continues to be enabled for time t_{DELAY} to allow read/write cycles to complete

HARDWARE STORE CYCLE



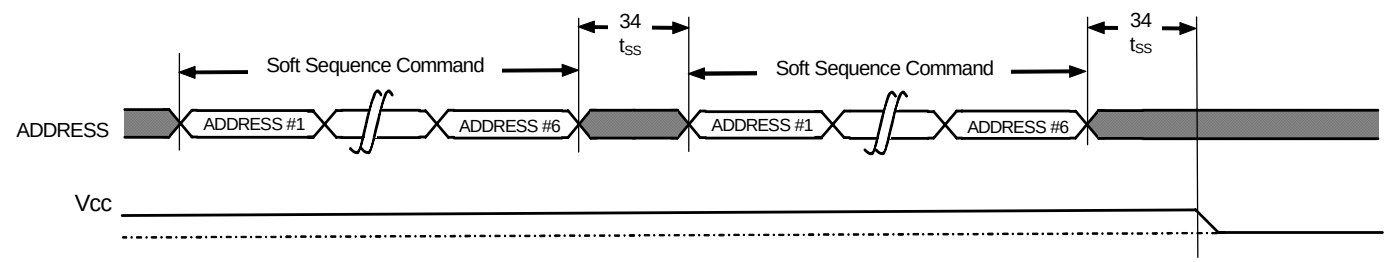
Soft Sequence Commands

NO.	SYMBOLS	PARAMETER	STK14 CA8		UNITS	NOTES
	Standard		MIN	MAX		
34	t_{SS}	*Soft Sequence Processing Time*		70	µs	o,p

Notes:

o: This is the amount of time that it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.

p: Commands like Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{16}-A_0	Mode	I/O	Power	Notes
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	q,r,s
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	q,r,s
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}	q,r,s
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	q,r,s

Notes

q: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

r: While there are 17 addresses on the STK14CA8, only the lower 16 are used to control software modes

s: I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low

nvSRAM OPERATION

nvSRAM

The STK14CA8 nvSRAM is made up of two functional components paired in the same physical cell. These are the SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates like a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The STK14CA8 supports unlimited read and writes like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

SRAM READ

The STK14CA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low while $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-16} determine which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ and $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ and $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ0-7 will be written into memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore OPERATION

The STK14CA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store (activated by HSB), Software Store (activated by an address sequence), and AutoStore (on power down).

AutoStore operation is a unique feature of Simtek Quantum Trap technology is enabled by default on the STK14CA8.

During normal operation, the device will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 3 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of the capacitor. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on $\overline{W}$ to hold it inactive during power up.

To reduce unneeded nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation

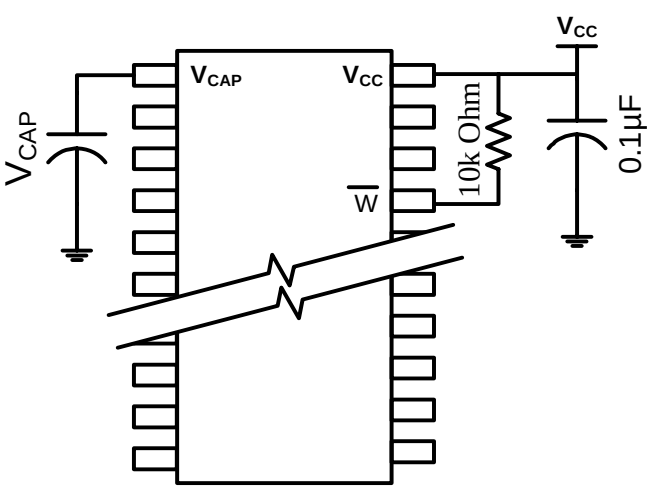


Figure 3. AutoStore Mode

has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an AutoStore cycle is in progress.

HARDWARE STORE ($\overline{HSB}$) OPERATION

The STK14CA8 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin can be used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the STK14CA8 will conditionally initiate a STORE operation after t_{DELAY}. An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the STK14CA8 will continue to allow SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low, it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until HSB returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

HARDWARE RECALL (POWER-UP)

During power up or after any low-power condition (V_{CC}<V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{HRECALL}$ to complete.

SOFTWARE STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK14CA8 software STORE cycle is initiated by executing sequential $\overline{E}$ controlled or $\overline{G}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, previous data is erased and then the new data is programmed into the nonvolatile elements. Once a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed.

To initiate the software STORE cycle, the following READ sequence must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x8FC0	Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence and that $\overline{G}$ is active. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x4C63	Initiate RECALL Cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM will once again be ready for READ or WRITE operations. The RECALL operation in no way alters the data in the nonvolatile storage elements.

DATA PROTECTION

The STK14CA8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low-voltage condition is detected when V_{CC}<V_{SWITCH}.

If the STK14CA8 is in a WRITE mode (both $\overline{E}$ and $\overline{W}$ low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on $\overline{E}$ or $\overline{W}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

NOISE CONSIDERATIONS

The STK14CA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are a short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals will reduce circuit noise.

BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (autostore enabled, etc.). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).
- If autostore has been firmware disabled, it will not reset to "autostore enabled" on every power down event captured by the nvSRAM. The application firmware should re-enable or re-disable autostore on each reset sequence based on the behavior desired.
- The V_{cap} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the nvSRAM internal algorithm calculates V_{cap} charge time based on this max Vcap value. Customers that want to use a larger V_{cap} value to make sure there is extra store charge and store time should discuss their V_{cap} size selection with Simtek to understand any impact on the V_{cap} voltage level at the end of a t_{RECALL} period.

LOW AVERAGE ACTIVE POWER

CMOS technology provides the STK14CA8 with the benefit of power supply current that scales with cycle time. Less current will be drawn as the memory cycle time becomes longer than 50 ns. Figure 4 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC}=3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14CA8 depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for operations
3. The ratio of READs to WRITEs
4. The operating temperature
5. The V_{CC} Level
6. I/O Loading

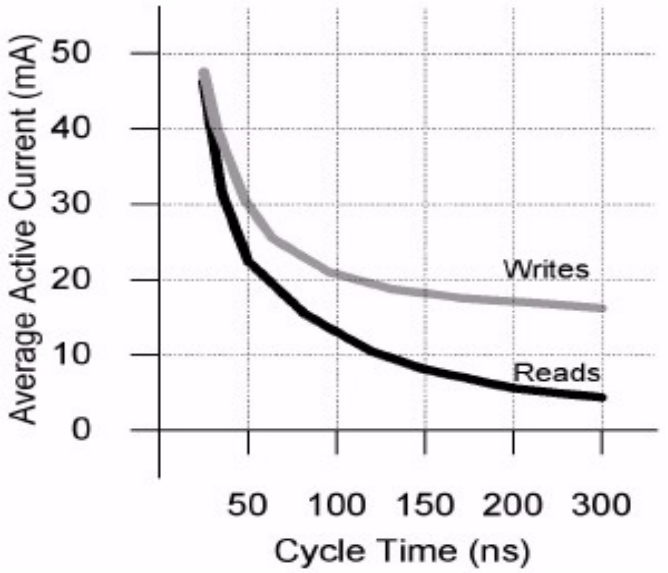


Figure 4 - Current vs Cycle Time

PREVENTING AUTOSTORE

The AutoStore function can be disabled by initiating an *AutoStore Disable* sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the *AutoStore Disable* sequence, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x8B45	AutoStore Disable

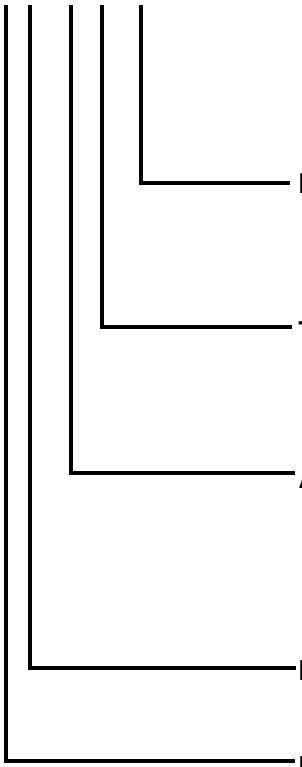
The AutoStore can be re-enabled by initiating an *AutoStore Enable* sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Enable* sequence, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

1	Read Address	0x4E38	Valid READ
2	Read Address	0xB1C7	Valid READ
3	Read Address	0x83E0	Valid READ
4	Read Address	0x7C1F	Valid READ
5	Read Address	0x703F	Valid READ
6	Read Address	0x4B46	AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) needs to be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

ORDERING INFORMATION

STK14CA8-R F 45 I TR



Packing Option

Blank=Tube

TR=Tape and Reel

Temperature Range

Blank=Commercial (0 to +70 C)

I= Industrial (-45 to +85 C)

Access Time

25=25 ns

35=35 ns

45=45 ns

Lead Finish

F=100% Sn (Matte Tin) RoHS Compliant

Package

N=Plastic 32-pin 300 mil SOIC (50 mil pitch)

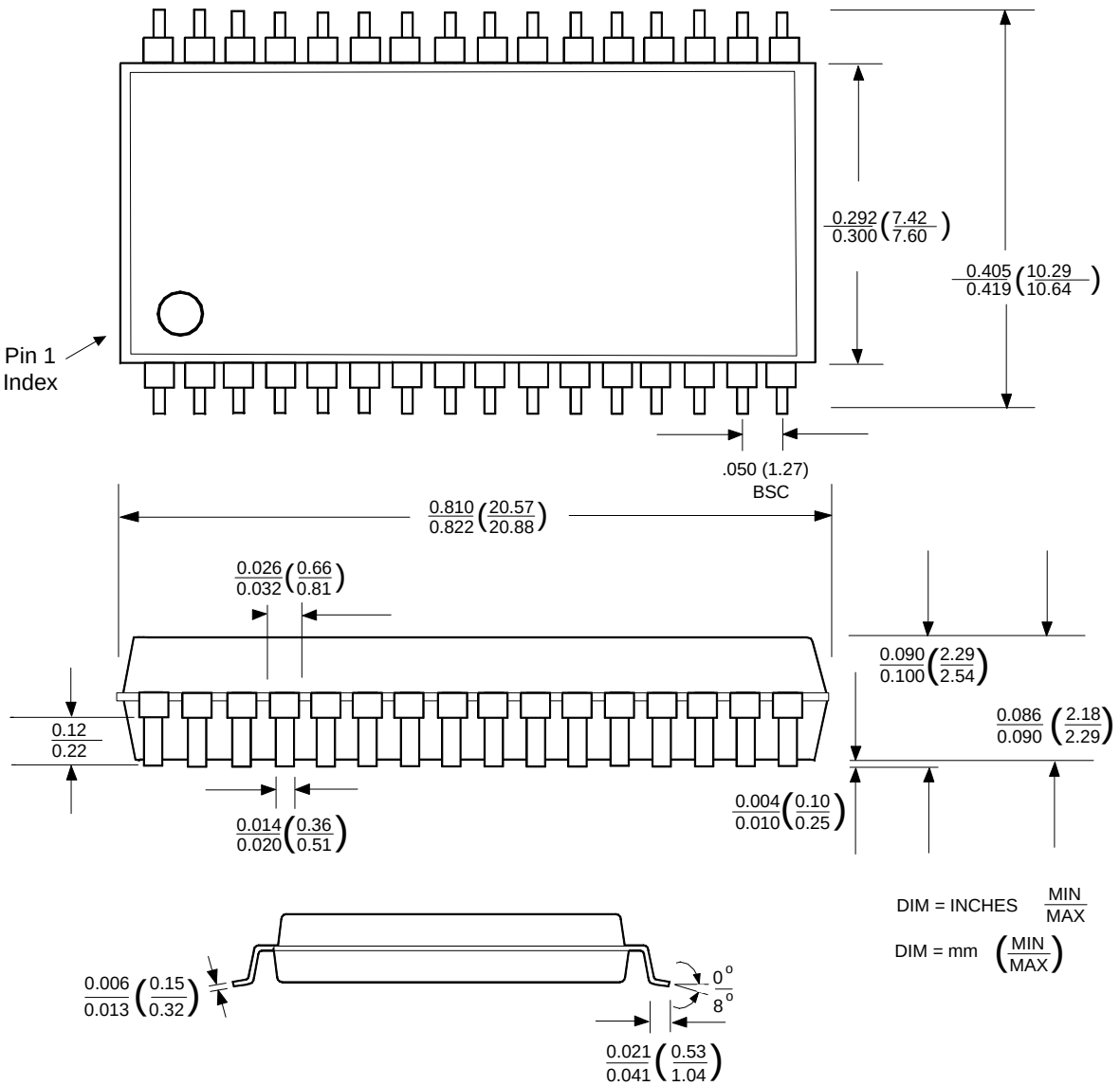
R=Plastic 48-pin 300 mil SSOP (25 mil pitch)

ORDERING CODES

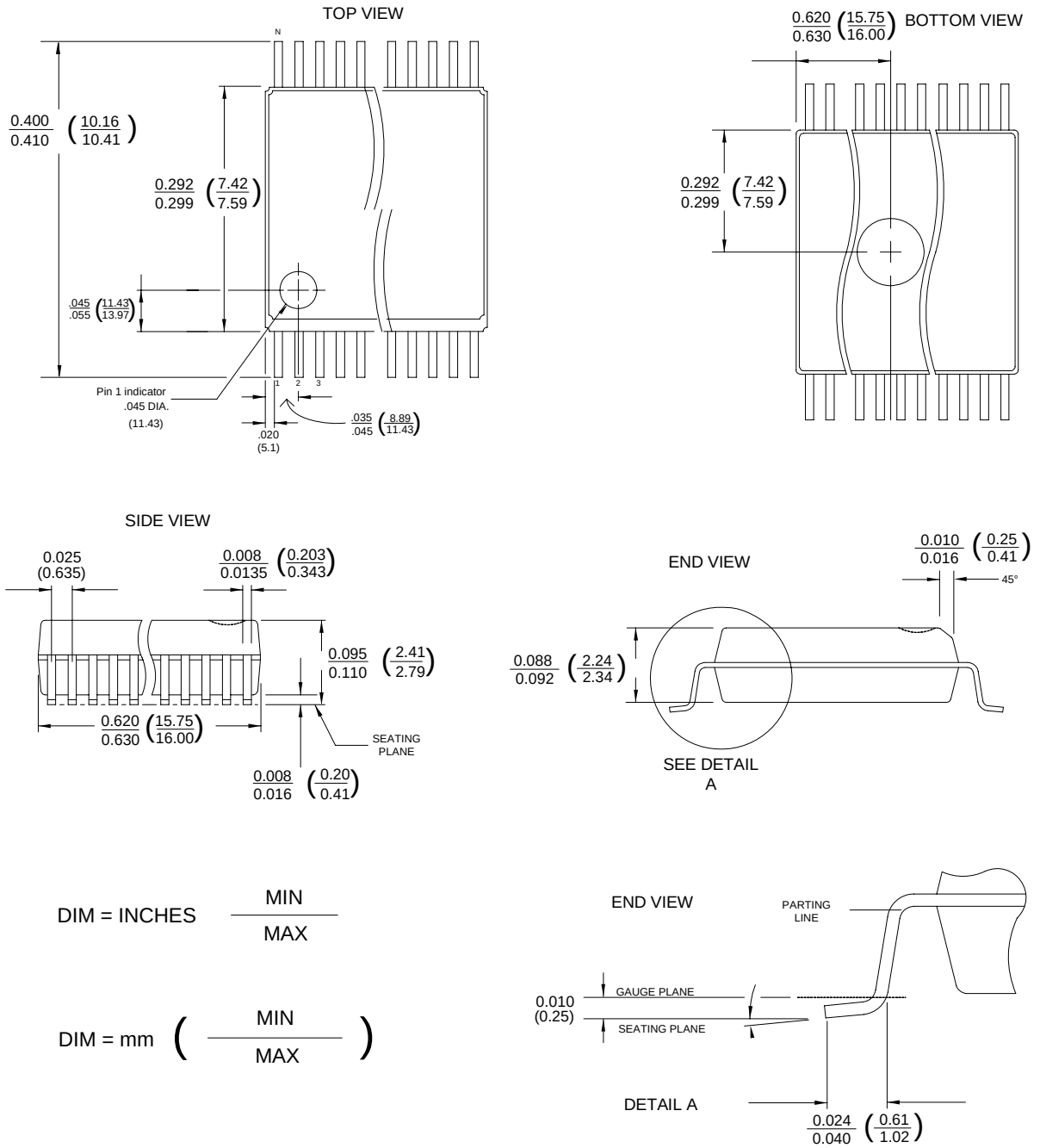
Part Number	Description	Access Times	Temperature
STK14CA8-NF25	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Commercial
STK14CA8-NF35	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14CA8-NF45	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14CA8-NF25TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Commercial
STK14CA8-NF35TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14CA8-NF45TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14CA8-RF25	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns access time	Commercial
STK14CA8-RF35	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns access time	Commercial
STK14CA8-RF45	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns access time	Commercial
STK14CA8-RF25TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns access time	Commercial
STK14CA8-RF35TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns access time	Commercial
STK14CA8-RF45TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns access time	Commercial
STK14CA8-NF25I	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Industrial
STK14CA8-NF35I	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14CA8-NF45I	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial
STK14CA8-NF25ITR	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Industrial
STK14CA8-NF35ITR	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14CA8-NF45ITR	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial
STK14CA8-RF25I	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns access time	Industrial
STK14CA8-RF35I	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns access time	Industrial
STK14CA8-RF45I	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns access time	Industrial
STK14CA8-RF25ITR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns access time	Industrial
STK14CA8-RF35ITR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns access time	Industrial
STK14CA8-RF45ITR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns access time	Industrial

PACKAGE DRAWINGS

32 Pin 300 mil SOIC



48 Pin 300 mil SSOP



Document Revision History

<table>
<tr><th>Rev</th><th>Date</th><th>Change</th></tr>
<tr><td>0.0</td><td>January 2003</td><td>Publish New Datasheet</td></tr>
<tr><td>0.1</td><td>May 2003</td><td>Add 48-pin SSOP, Modify AutoStore Diagram, Update Mode Selection Table and Absolute Maximum Ratings, Added $\overline{G}$ controlled software store.</td></tr>
<tr><td>0.2</td><td>September 2003</td><td>Added lead-free finish</td></tr>
<tr><td>1.0</td><td>December 2004</td><td>
<table>
<tr><th>Parameter</th><th>Old Value</th><th>New Value</th><th>Notes</th></tr>
<tr><td>V_{CAP} Min</td><td>10uF</td><td>17uF</td><td></td></tr>
<tr><td>$t_{VCCRISE}$</td><td>NA</td><td>150 us</td><td>New Spec</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>35 mA</td><td>50 mA</td><td>@45 ns access</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>40 mA</td><td>55 mA</td><td>@35 ns access</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>50 mA</td><td>65 mA</td><td>@25 ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>35 mA</td><td>55 mA</td><td>@45 ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>45 mA</td><td>60 mA</td><td>@35 ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>55 mA</td><td>70 mA</td><td>@25 ns access</td></tr>
<tr><td>I_{CC2} Max</td><td>1.5 mA</td><td>3.0 mA</td><td>Com. & Ind.</td></tr>
<tr><td>I_{CC4} Max</td><td>0.5 mA</td><td>3.0 mA</td><td>Com. & Ind.</td></tr>
<tr><td>$t_{HRECALL}$</td><td>5 ms</td><td>20 ms</td><td></td></tr>
<tr><td>t_{STORE}</td><td>10 ms</td><td>12.5 ms</td><td></td></tr>
<tr><td>t_{RECALL}</td><td>20 us</td><td>40 us</td><td></td></tr>
<tr><td>t_{GLQV}</td><td>10 ns</td><td>12 ns</td><td>25 ns device</td></tr>
</table>
</td></tr>
<tr><td>1.1</td><td>August 2005</td><td>
<table>
<tr><th>Parameter</th><th>Old Value</th><th>New Value</th><th>Notes</th></tr>
<tr><td>I_{CC3} Max Com.</td><td>5 mA</td><td>10 mA</td><td></td></tr>
<tr><td>I_{CC3} Max Ind.</td><td>5 mA</td><td>10 mA</td><td></td></tr>
<tr><td>I_{SB} Max Com.</td><td>2 mA</td><td>3 mA</td><td></td></tr>
<tr><td>I_{SB} Max Ind.</td><td>2 mA</td><td>3 mA</td><td></td></tr>
<tr><td>t_{RECALL}</td><td>40 us</td><td>50 us</td><td>Soft Recall</td></tr>
<tr><td>t_{STORE}</td><td>12.5 ms</td><td>15 ms</td><td>Industrial Grade Only</td></tr>
<tr><td>NVc</td><td>$1x10^6$</td><td>$5x10^5$</td><td>Contact Simtek For Details</td></tr>
</table>
</td></tr>
</table>

Rev	Date	Change
1.2	September 2005	Added an Extended Temperature Range device tested from -55 degree C to +85 degree C
1.3	December 2005	
1.4	March 2006	Removed Lead Plated Lead Finish
1.5	February 2007	

Parameter	Old Value	New Value	Notes
t_{RECALL}	60 us	50 us	Typographical Error In Datasheet
t_{SS}	Undefined	70 us	
$DATA_R$	100 Years at Unspecified Temperature	20 Years @ Max Temperature	New Data Retention Specification

Parameter	Old Value	New Value	Notes
NV_C	500K	200K	New Nonvolatile Store Cycle Spec
$DATA_R$	20 Years @ 85 C	20 Years @ 55 C	New Data Retention Spec
V_{SWITCH} Min.	2.55 V		No Min. Spec
I_{OUT} (HSB)		-10 uA	Not Specified Before
t_{ELAX}, t_{GLAX}	20 ns		Removed
t_{EHAX}, t_{GHAX}		1 ns	New Spec
t_{DELAY} Max.		70 us	New Spec
t_{HLBL}	300ns		Spec Not Required
t_{SS}	70 uS Min.	70 uS Max.	Typo
V_{CAP} Max	57 uF	120 uF	Supports Upgrades From 14C88-3

Deleted -G Extended Temperature Option
Added tape and reel ordering option
Added product order code listing
Added package drawings
Reformatted Entire Document

Rev	Date	Change
2.0	January 2008	page 3: added thermal characteristics. page 5: in the SRAM Read Cycles #1 and #2 table, revised parameter description for t_{ELQX} and t_{EHQZ} and changed Symbol #2 to t_{ELEH} for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram and changed title to add G controlled. page 8: revised the notes below the Software-Controlled Store/Recall Cycle diagram. page 10: in the Mode Selection table, changed column to A_{16}-A_0. In the values in this column, added a zero after each instance of “0x.” On fifth row, changed AutoStore Enable value to 0x04B46. page 11: under AutoStore Operation, revised text to read: “Refer to the DC CHARACTERISTICS table for the size of the capacitor.” page 12: under Hardware Store ($\overline{HSB}$) Operation, revised first paragraph to read “The $\overline{HSB}$ pin has a very resistive pullup...” page 13: added best practices section. page 16: added access times column to the Ordering Codes.
2.1	January 2008	Corrected pin assignments in package drawings on page 2.