

**MC14517B**

**Dual 64-Bit Static Shift Register**

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

**MAXIMUM RATINGS** (Voltages referenced to V<sub>SS</sub>)

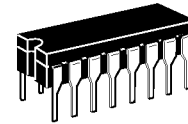
| Symbol                             | Parameter  | Value                          | Unit |
|------------------------------------|--|--------------------------------|------|
| V <sub>DD</sub>                    | DC Supply Voltage                                  | - 0.5 to + 18.0                | V    |
| V <sub>in</sub> , V <sub>out</sub> | Input or Output Voltage (DC or Transient)          | - 0.5 to V <sub>DD</sub> + 0.5 | V    |
| I <sub>in</sub> , I <sub>out</sub> | Input or Output Current (DC or Transient), per Pin | ± 10                           | mA   |
| P <sub>D</sub>                     | Power Dissipation, per Package†                    | 500                            | mW   |
| T <sub>stg</sub>                   | Storage Temperature                                | - 65 to + 150                  | °C   |
| T <sub>L</sub>                     | Lead Temperature (8-Second Soldering)              | 260                            | °C   |

\* Maximum Ratings are those values beyond which damage to the device may occur.

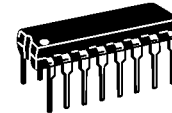
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



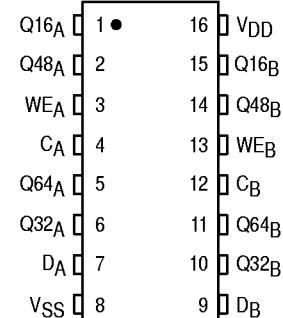
**DW SUFFIX**  
SOIC  
CASE 751G

**ORDERING INFORMATION**

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBDW SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

**PIN ASSIGNMENT**



**FUNCTIONAL TRUTH TABLE** (X = Don't Care)

| Clock | Write Enable | Data                      | 16-Bit Tap                      | 32-Bit Tap                      | 48-Bit Tap                      | 64-Bit Tap                  |
|-------|--------------|---------------------------|---------------------------------|---------------------------------|---------------------------------|-----------------------------|
| 0     | 0            | X                         | Content of 16-Bit Displayed     | Content of 32-Bit Displayed     | Content of 48-Bit Displayed     | Content of 64-Bit Displayed |
| 0     | 1            | X                         | High Impedance                  | High Impedance                  | High Impedance                  | High Impedance              |
| 1     | 0            | X                         | Content of 16-Bit Displayed     | Content of 32-Bit Displayed     | Content of 48-Bit Displayed     | Content of 64-Bit Displayed |
| 1     | 1            | X                         | High Impedance                  | High Impedance                  | High Impedance                  | High Impedance              |
| ↗     | 0            | Data entered into 1st Bit | Content of 16-Bit Displayed     | Content of 32-Bit Displayed     | Content of 48-Bit Displayed     | Content of 64-Bit Displayed |
| ↗     | 1            | Data entered into 1st Bit | Data at tap entered into 17-Bit | Data at tap entered into 33-Bit | Data at tap entered into 49-Bit | High Impedance              |
| ↘     | 0            | X                         | Content of 16-Bit Displayed     | Content of 32-Bit Displayed     | Content of 48-Bit Displayed     | Content of 64-Bit Displayed |
| ↘     | 1            | X                         | High Impedance                  | High Impedance                  | High Impedance                  | High Impedance              |

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

| Characteristic  | Symbol                    | $V_{DD}$<br>Vdc | -55°C                                     |           | 25°C  |               |           | 125°C |           | Unit      |
|---|---------------------------|-----------------|---|-----------|-------|---------------|-----------|-------|-----------|-----------|
|   |                           |                 | Min                                       | Max       | Min   | Typ #         | Max       | Min   | Max       |           |
| Output Voltage<br>$V_{in} = V_{DD}$ or 0<br><br>$V_{in} = 0$ or $V_{DD}$  | "0" Level<br><br>$V_{OL}$ | 5.0             | —   | 0.05      | —     | 0             | 0.05      | —     | 0.05      | Vdc       |
|   |                           | 10              | —   | 0.05      | —     | 0             | 0.05      | —     | 0.05      |           |
|   |                           | 15              | —   | 0.05      | —     | 0             | 0.05      | —     | 0.05      |           |
|   | "1" Level<br><br>$V_{OH}$ | 5.0             | 4.95                                      | —         | 4.95  | 5.0           | —         | 4.95  | —         | Vdc       |
|   |                           | 10              | 9.95                                      | —         | 9.95  | 10            | —         | 9.95  | —         |           |
|   |                           | 15              | 14.95                                     | —         | 14.95 | 15            | —         | 14.95 | —         |           |
| Input Voltage<br>"0" Level<br>( $V_O = 4.5$ or $0.5$ Vdc)<br>( $V_O = 9.0$ or $1.0$ Vdc)<br>( $V_O = 13.5$ or $1.5$ Vdc)<br><br>"1" Level<br>( $V_O = 0.5$ or $4.5$ Vdc)<br>( $V_O = 1.0$ or $9.0$ Vdc)<br>( $V_O = 1.5$ or $13.5$ Vdc) | $V_{IL}$                  | 5.0             | —   | 1.5       | —     | 2.25          | 1.5       | —     | 1.5       | Vdc       |
|   |                           | 10              | —   | 3.0       | —     | 4.50          | 3.0       | —     | 3.0       |           |
|   |                           | 15              | —   | 4.0       | —     | 6.75          | 4.0       | —     | 4.0       |           |
|   | $V_{IH}$                  | 5.0             | 3.5                                       | —         | 3.5   | 2.75          | —         | 3.5   | —         | Vdc       |
|   |                           | 10              | 7.0                                       | —         | 7.0   | 5.50          | —         | 7.0   | —         |           |
|   |                           | 15              | 11  | —         | 11    | 8.25          | —         | 11    | —         |           |
| Output Drive Current<br>( $V_{OH} = 2.5$ Vdc)<br>( $V_{OH} = 4.6$ Vdc)<br>( $V_{OH} = 9.5$ Vdc)<br>( $V_{OH} = 13.5$ Vdc)<br><br>( $V_{OL} = 0.4$ Vdc)<br>( $V_{OL} = 0.5$ Vdc)<br>( $V_{OL} = 1.5$ Vdc)                                | Source<br><br>$I_{OH}$    | 5.0             | -3.0                                      | —         | -2.4  | -4.2          | —         | -1.7  | —         | mAdc      |
|   |                           | 5.0             | -0.64                                     | —         | -0.51 | -0.88         | —         | -0.36 | —         |           |
|   |                           | 10              | -1.6                                      | —         | -1.3  | -2.25         | —         | -0.9  | —         |           |
|   | Sink<br><br>$I_{OL}$      | 5.0             | 0.64                                      | —         | 0.51  | 0.88          | —         | 0.36  | —         | mAdc      |
|   |                           | 10              | 1.6                                       | —         | 1.3   | 2.25          | —         | 0.9   | —         |           |
|   |                           | 15              | 4.2                                       | —         | 3.4   | 8.8           | —         | 2.4   | —         |           |
| Input Current   | $I_{in}$                  | 15              | —   | $\pm 0.1$ | —     | $\pm 0.00001$ | $\pm 0.1$ | —     | $\pm 1.0$ | $\mu$ Adc |
| Input Capacitance<br>( $V_{in} = 0$ )   | $C_{in}$                  | —               | —   | —         | —     | 5.0           | 7.5       | —     | —         | pF        |
| Quiescent Current<br>(Per Package)  | $I_{DD}$                  | 5.0             | —   | 5.0       | —     | 0.005         | 5.0       | —     | 150       | $\mu$ Adc |
|   |                           | 10              | —   | 10        | —     | 0.010         | 10        | —     | 300       |           |
|   |                           | 15              | —   | 20        | —     | 0.015         | 20        | —     | 600       |           |
| Total Supply Current**†<br>(Dynamic plus Quiescent,<br>Per Package)<br>( $C_L = 50$ pF on all outputs, all<br>buffers switching)  | $I_T$                     | 5.0             | $I_T = (4.2 \mu\text{A/kHz}) f + I_{DD}$  |           |       |               |           |       |           | $\mu$ Adc |
|   |                           | 10              | $I_T = (8.8 \mu\text{A/kHz}) f + I_{DD}$  |           |       |               |           |       |           |           |
|   |                           | 15              | $I_T = (13.7 \mu\text{A/kHz}) f + I_{DD}$ |           |       |               |           |       |           |           |
| Three-State Leakage Current   | $I_{TL}$                  | 15              | —   | $\pm 0.1$ | —     | $\pm 0.0001$  | $\pm 0.1$ | —     | $\pm 3.0$ | $\mu$ Adc |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

| Characteristic   | Symbol             | V <sub>DD</sub> | Min               | Typ #             | Max               | Unit |
|--|--------------------|-----------------|-------------------|-------------------|-------------------|------|
| Output Rise and Fall Time<br>$t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.65 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | $t_{TLH}, t_{THL}$ | 5.0<br>10<br>15 | —<br>—<br>—       | 100<br>50<br>40   | 200<br>100<br>80  | ns   |
| Propagation Delay Time<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 390 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 115 \text{ ns}$     | $t_{PLH}, t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>—       | 475<br>210<br>140 | 770<br>300<br>215 | ns   |
| Clock Pulse Width  | $t_{WH}$           | 5.0<br>10<br>15 | 330<br>125<br>100 | 170<br>75<br>60   | —<br>—<br>—       | ns   |
| Clock Pulse Frequency  | $f_{cl}$           | 5.0<br>10<br>15 | —<br>—<br>—       | 3.0<br>6.7<br>8.3 | 1.5<br>4.0<br>5.3 | MHz  |
| Clock Pulse Rise and Fall Time   | $t_{TLH}, t_{THL}$ | 5.0<br>10<br>15 | **See Note        |                   |                   | —    |
| Data to Clock Setup Time   | $t_{su}$           | 5.0<br>10<br>15 | 0<br>10<br>15     | -40<br>-15<br>0   | —<br>—<br>—       | ns   |
| Data to Clock Hold Time  | $t_h$              | 5.0<br>10<br>15 | 150<br>75<br>35   | 75<br>25<br>10    | —<br>—<br>—       | ns   |
| Write Enable to Clock Setup Time   | $t_{su}$           | 5.0<br>10<br>15 | 400<br>200<br>110 | 170<br>65<br>50   | —<br>—<br>—       | ns   |
| Write Enable to Clock Release Time   | $t_{rel}$          | 5.0<br>10<br>15 | 380<br>180<br>100 | 160<br>55<br>40   | —<br>—<br>—       | ns   |

\* The formulas given are for the typical characteristics only at 25°C.

# Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\* When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

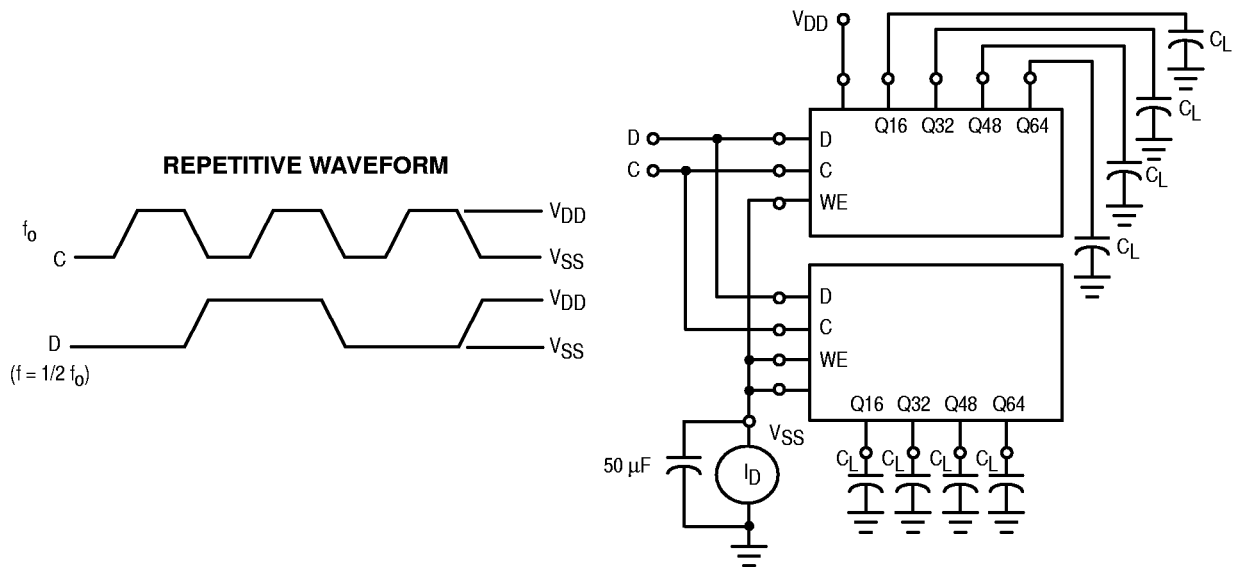
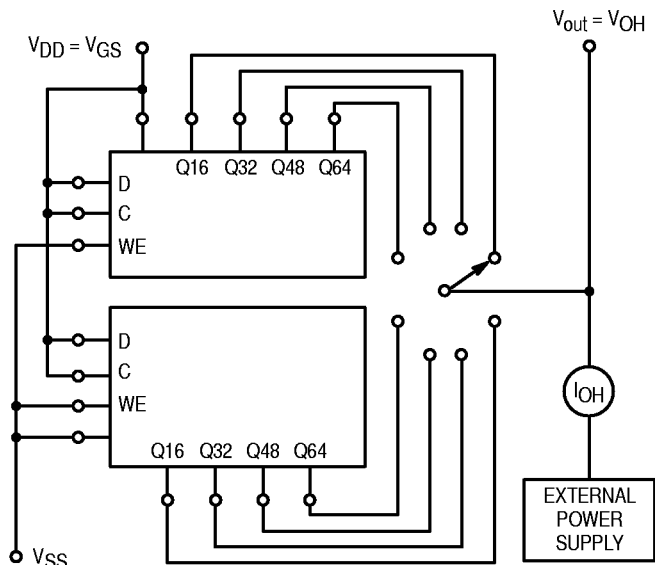
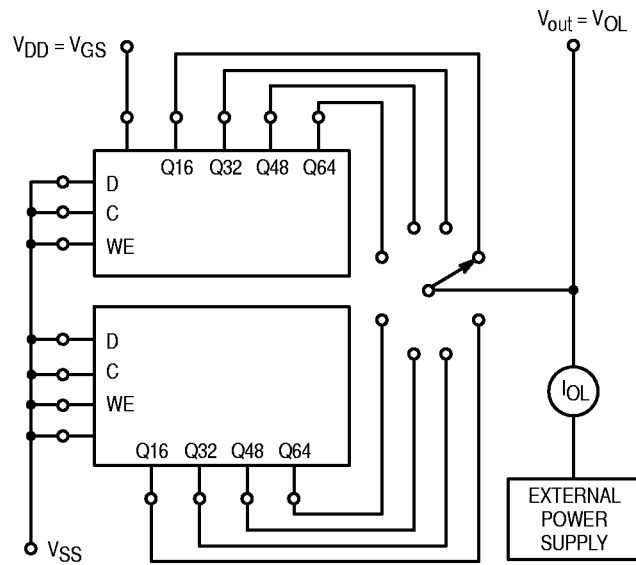


Figure 1. Power Dissipation Test Circuit and Waveform



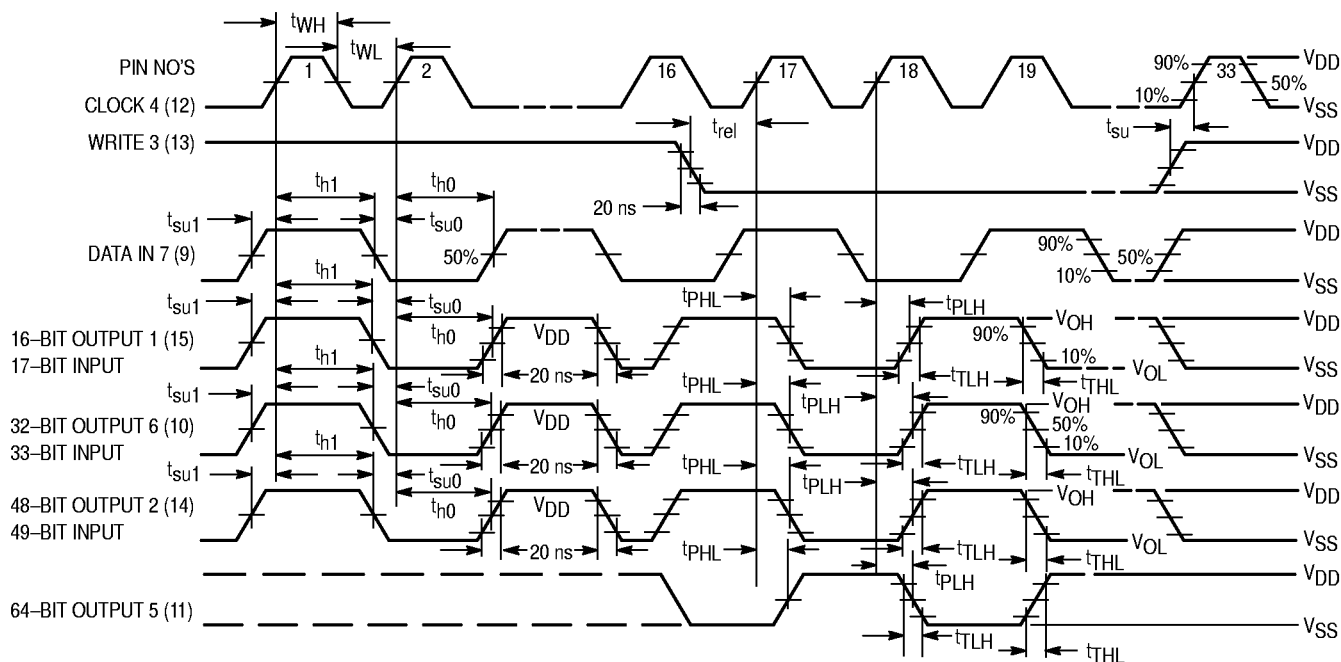
(Output being tested should be in the high-logic state)



(Output being tested should be in the low-logic state)

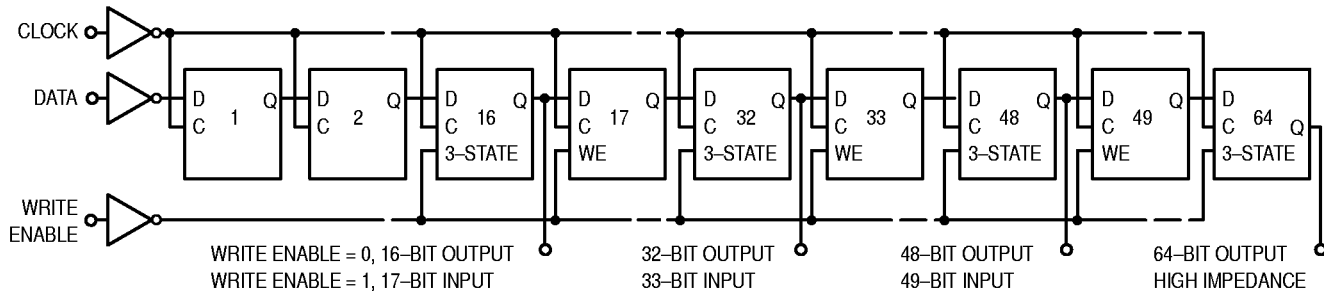
**Figure 2. Typical Output Source Current Characteristics Test Circuit**

**Figure 3. Typical Output Sink Current Characteristics Test Circuit**



**Figure 4. AC Test Waveforms**

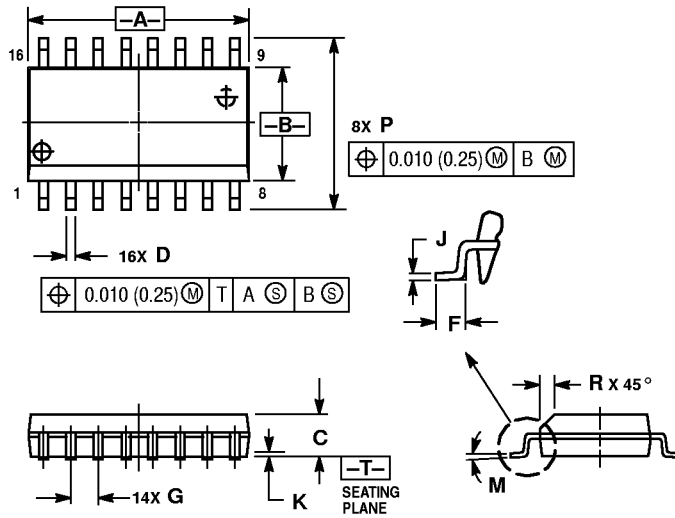
**EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)**





## OUTLINE DIMENSIONS


### DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 10.15       | 10.45 | 0.400     | 0.411 |
| B   | 7.40        | 7.60  | 0.292     | 0.299 |
| C   | 2.35        | 2.65  | 0.093     | 0.104 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.50        | 0.90  | 0.020     | 0.035 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.25        | 0.32  | 0.010     | 0.012 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 10.05       | 10.55 | 0.395     | 0.415 |
| R   | 0.25        | 0.75  | 0.010     | 0.029 |

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MC14517B/D

