

SN751508, SN751518 DC PLASMA DISPLAY DRIVERS

SLDS035 – JANUARY 1987 – REVISED NOVEMBER 1989

- Each Device Drives 32 Lines
- –120-V PNP Open-Collector Parallel Outputs
- High-Speed Serially Shifted Data Inputs
- CMOS-Compatible Inputs
- Strobe and Sustain Inputs Provided
- Serial Data Output for Cascade Operation

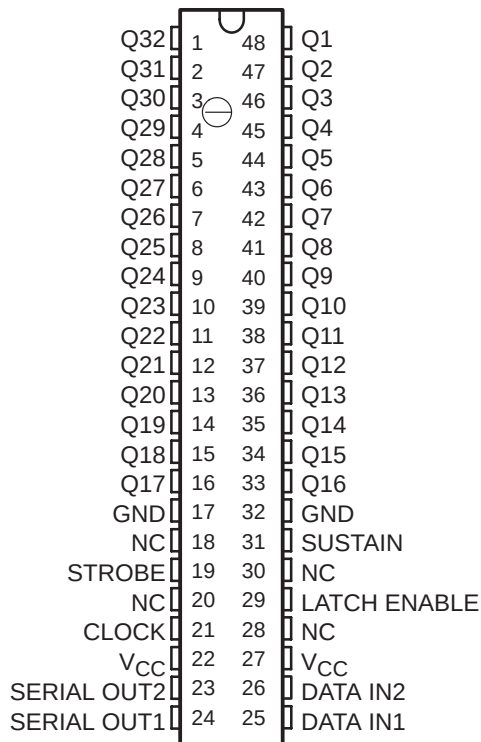
description

The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed-circuit-board layout.

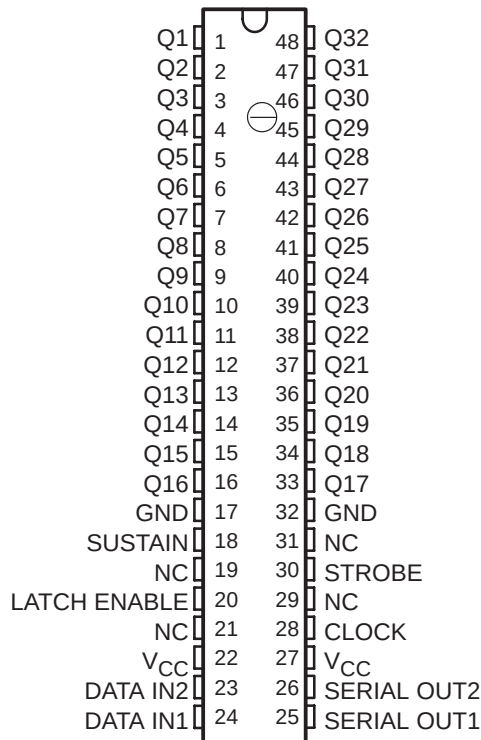
Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 pnp open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high is placed on the data input of the output AND gates. When STROBE is low and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN forces all outputs to their off state. Drivers can be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.

SN751508 . . . FT PACKAGE
(TOP VIEW)



SN751518 . . . FT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



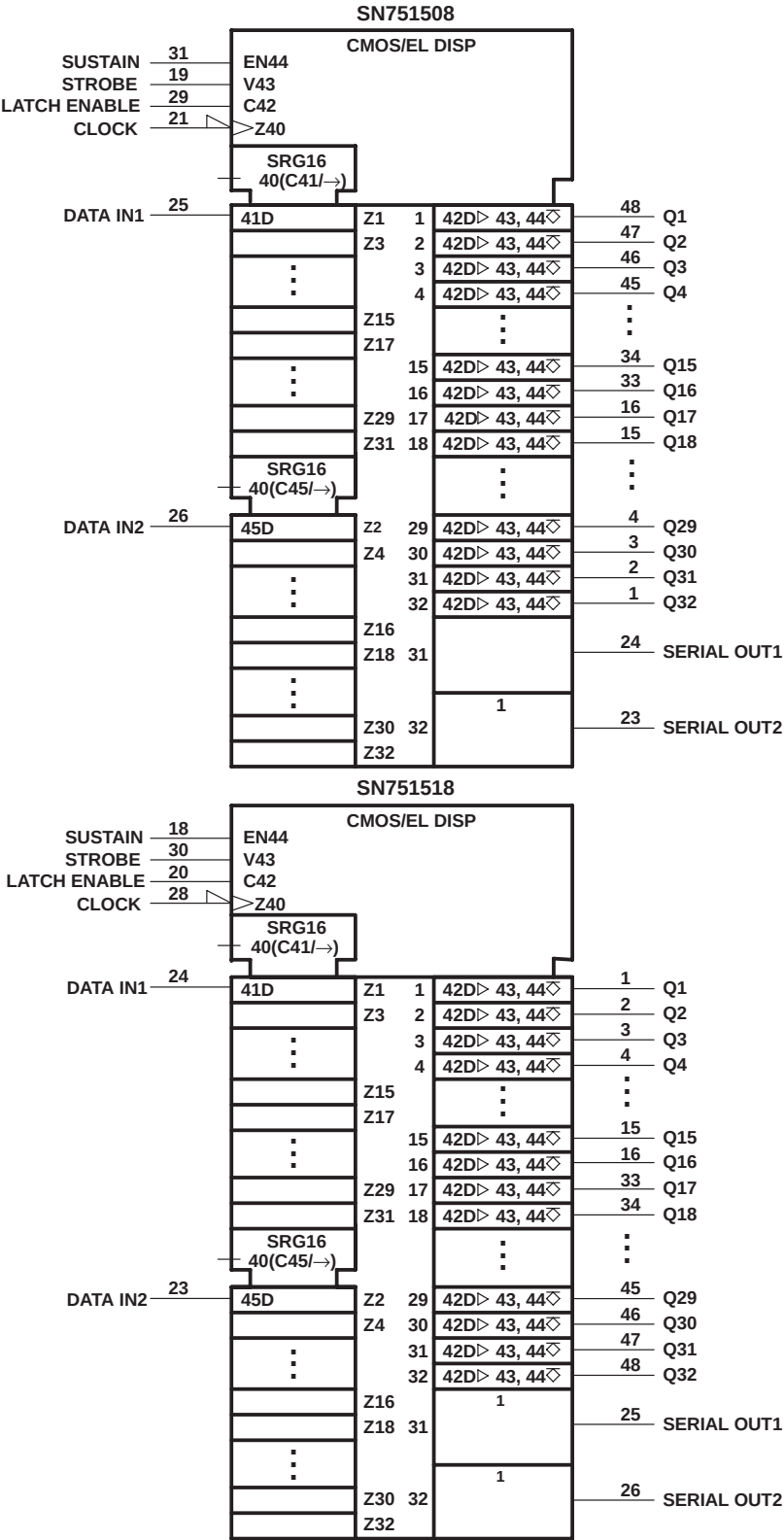
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SN751508, SN751518
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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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The diagram illustrates a 32-bit shift register architecture. It consists of two parallel 16-bit shift registers, labeled 'Shift Register 1' and 'Shift Register 2'. Each shift register is composed of 16 D-type flip-flops (labeled '1D' and 'C1'). The outputs of the shift registers are connected to 32 latches (labeled 'C2' and '2D'). The latches are organized into two groups of 16, each corresponding to one of the shift registers. The outputs of the latches are connected to 32 output lines, labeled Q1 through Q32. The shift registers are controlled by a common 'CLOCK' signal and a 'LATCH ENABLE' signal. The 'SUSTAIN' and 'STROBE' signals are also shown as inputs. The diagram shows the internal structure of the shift registers and latches, including the '1D' and 'C1' inputs of the flip-flops and the 'C2' and '2D' inputs of the latches. The outputs of the shift registers are labeled R1 through R32. The outputs of the latches are labeled LC1 through LC32. The final outputs are Q1 through Q32, which are connected to 'SERIAL OUT1' and 'SERIAL OUT2'.

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FUNCTION TABLE

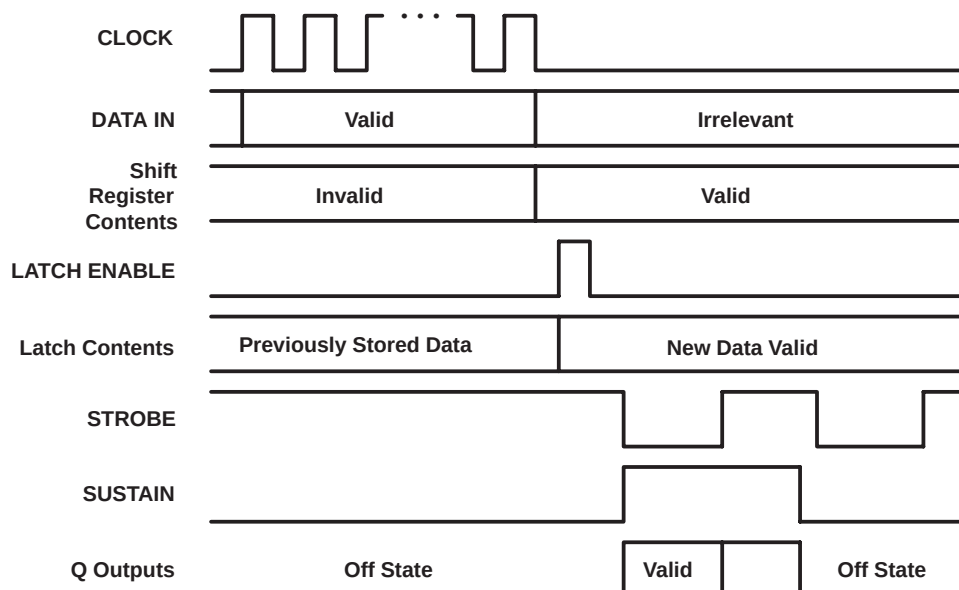
FUNCTION	CONTROL INPUTS				SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS		
	CLOCK	LATCH ENABLE	STROBE	SUSTAIN			SERIAL		Q1 THRU Q32
							S01	S02	
Load	↓ No ↓	X X	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R31	R32	Determined by SUSTAIN and STROBE
Latch Enable	X X	L H	X X	X X	As determined above	Stored data New data	R31	R32	Determined by SUSTAIN and STROBE
Strobe	X X	X X	L H	H H	As determined above	Determined by LATCH ENABLE‡	R31	R32	LC1 thru LC32 All on (high)
Sustain	X	X	X	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

[†] Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, ... R4 takes on the state of R2, R2 takes on the state of DATA IN2, R31 takes on the state of R29, R29 takes on the state of R27, ... R3 takes on the state of R1, and R1 takes on the state on DATA IN1.

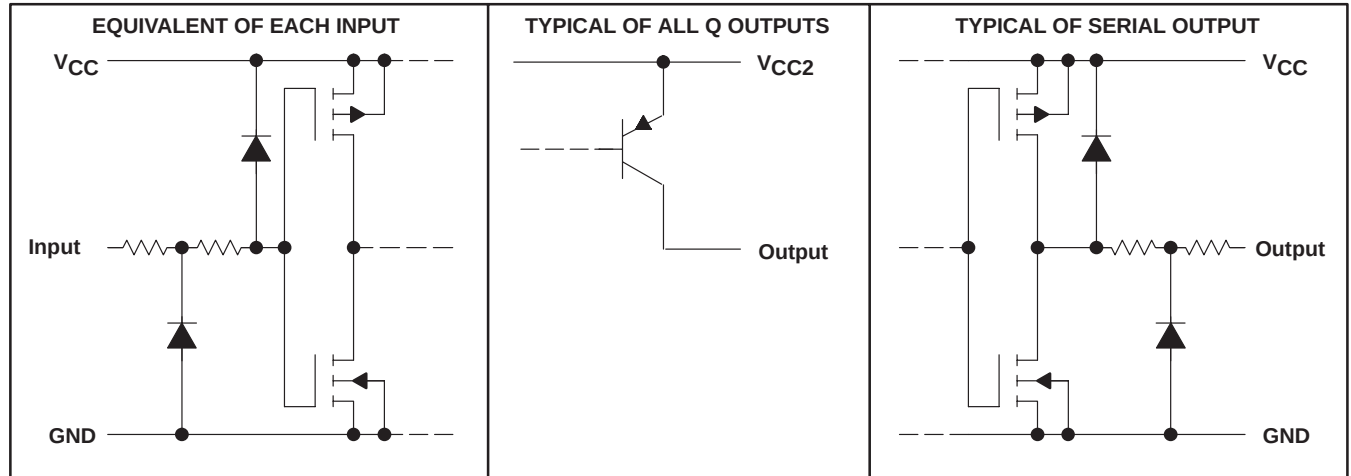
[‡] New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

typical operating sequence



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	–0.4 to 7 V
On-state Q output voltage range, V_O	–120 V to $V_{CC} + 0.4$ V
Input voltage range, V_I	–0.4 V to $V_{CC} + 0.4$ V
Serial output voltage range	–0.4 V to $V_{CC} + 0.4$ V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	1025 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltages values are with respect to GND.

2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Output voltage, V_O				-75	V
High-level input voltage, V_{IH}	$V_{CC} = 4.5\text{ V}$	3.6			V
	$V_{CC} = 5.5\text{ V}$	4.4			
Low-level input voltage, V_{IL}	$V_{CC} = 4.5\text{ V}$			0.9	V
	$V_{CC} = 5.5\text{ V}$			1	
Output current, I_O ($T_A = 25^\circ\text{C}$)				-1.2	mA
Clock frequency, f_{clock}				5	MHz
Pulse duration, t_W (see Figure 1)	CLOCK	75			ns
	DATA IN	160			
	LATCH ENABLE	90			
	STROBE	2			μs
	SUSTAIN	2			
Setup time, t_{su} (see Figure 1)	DATA IN before CLOCK↓	20			ns
	CLOCK low before LATCH ENABLE↑	50			
	LATCH ENABLE low before CLOCK↓	0			
	LATCH ENABLE high before STROBE↓	0			
	LATCH ENABLE high before SUSTAIN↑	0			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 1)		50			μs
Operating free-air temperature, T_A		0		70	$^\circ\text{C}$

electrical characteristics over operating free-air temperature range, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{OH} High-level output voltage	Q outputs	$I_{OH} = -0.5\text{ mA}$		4	4.5		V
	SERIAL OUT 1, 2	$V_{CC} = 5.5\text{ V}$	$I_{OH} = -100\text{ }\mu\text{A}$	4.3	4.6		
			$I_{OH} = -20\text{ }\mu\text{A}$	4.4			
		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -100\text{ }\mu\text{A}$	3.4	3.6		
V_{OL} Low-level output voltage	SERIAL OUT 1, 2	$V_{CC} = 5.5\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.9	1.2	V
			$I_{OL} = 20\text{ }\mu\text{A}$			1.1	
		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.9	1.1	
			$I_{OL} = 20\text{ }\mu\text{A}$			0.9	
I_{OH} High-level Q output current		$T_A = 25^\circ\text{C}$,	$V_O = 3\text{ V}$	-1.2			mA
I_{OL} Low-level Q output current		$T_A = 25^\circ\text{C}$,	$V_O = -75\text{ V}$			-500	μA
I_{IH} High-level input current		$T_A = 25^\circ\text{C}$,	$V_I = V_{CC}$			1	μA
I_{IL} Low-level input current		$T_A = 25^\circ\text{C}$,	$V_I = 0$			-1	μA
I_{CC} Supply current	All Q outputs high,		$V_{CC} = 5.5\text{ V}$		17	25	mA
	All Q outputs low					3	
C_i Input capacitance						15	pF

[†] All typical values are at $T_A = 25^\circ\text{C}$.



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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd} Propagation delay time, CLOCK to SERIAL OUT			100	150	ns
t_{DLH} Delay time, low-to-high-level Q output from SUSTAIN or STROBE	$R_L = 91\text{ k}\Omega$, See Figures 1 and 2		$0.3^\ddagger$	1	μs
t_{DHL} Delay time, high-to-low-level Q output from SUSTAIN or STROBE			$1^\ddagger$	2.5	μs
t_{TLH} Transition time, low-to-high-level Q output			2	5	μs
t_{THL} Transition time, high-to-low-level Q output			11	18	μs

‡ Typical values for delay times are measured from SUSTAIN.



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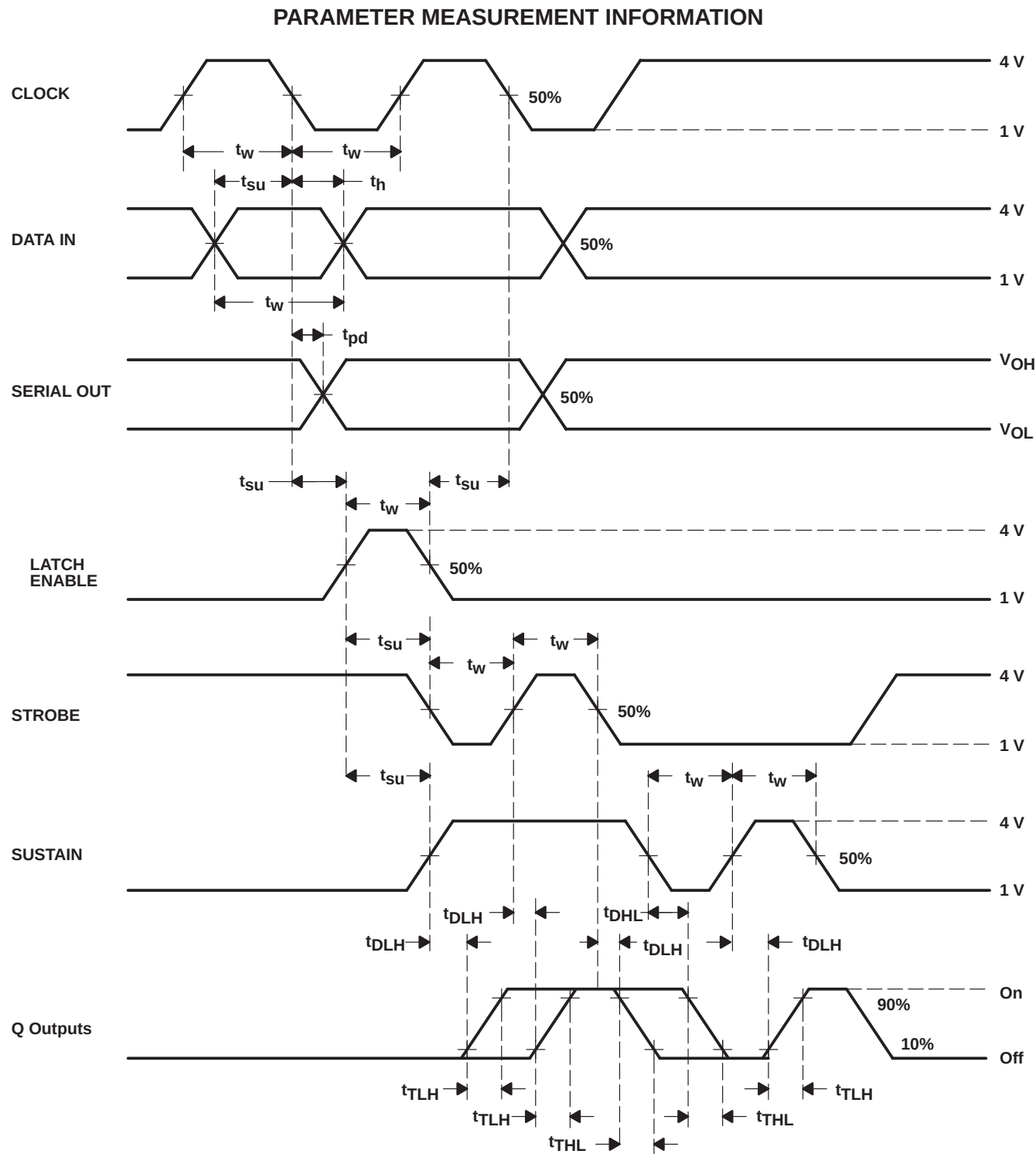
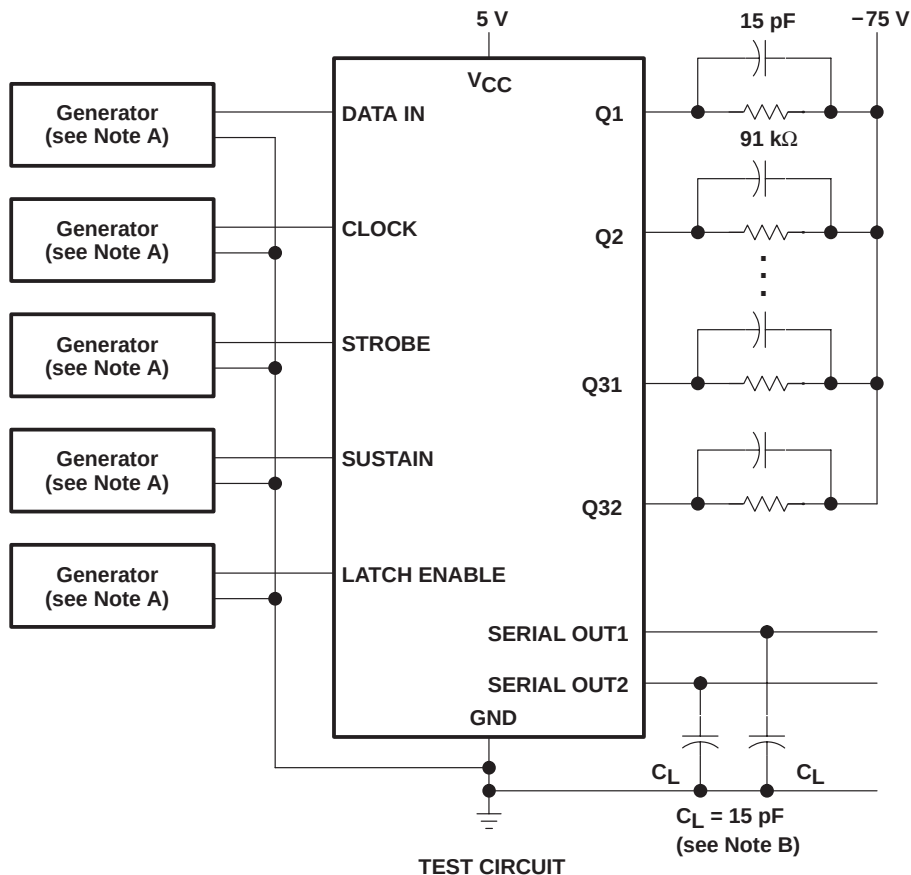


Figure 1. Input Timing and Switching Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_W = 100 \text{ ns}$, $\text{PRR} \leq 5 \text{ MHz}$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

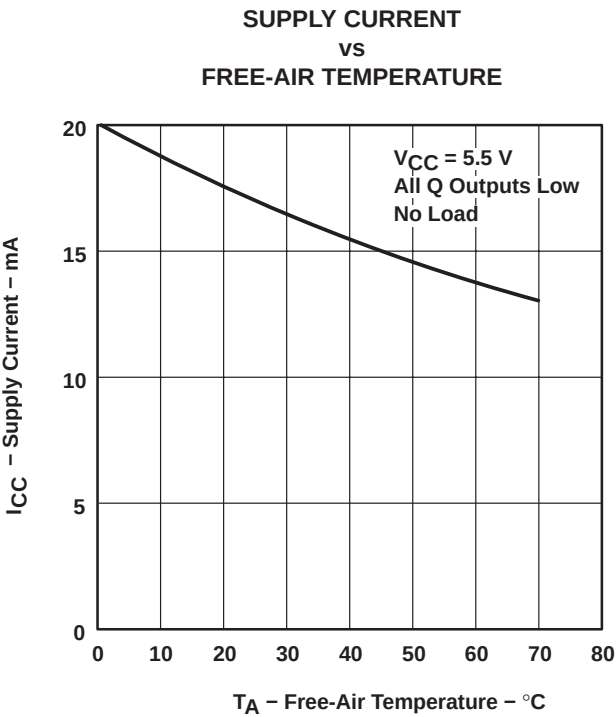


Figure 3

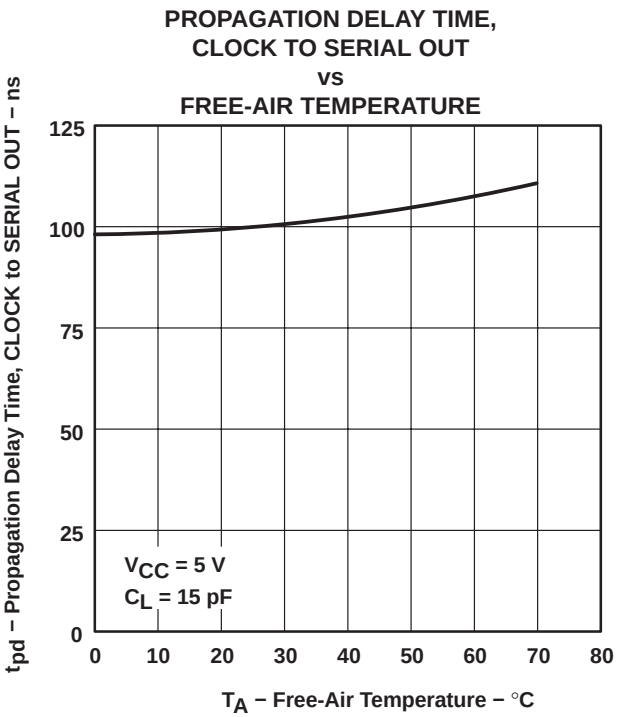


Figure 4

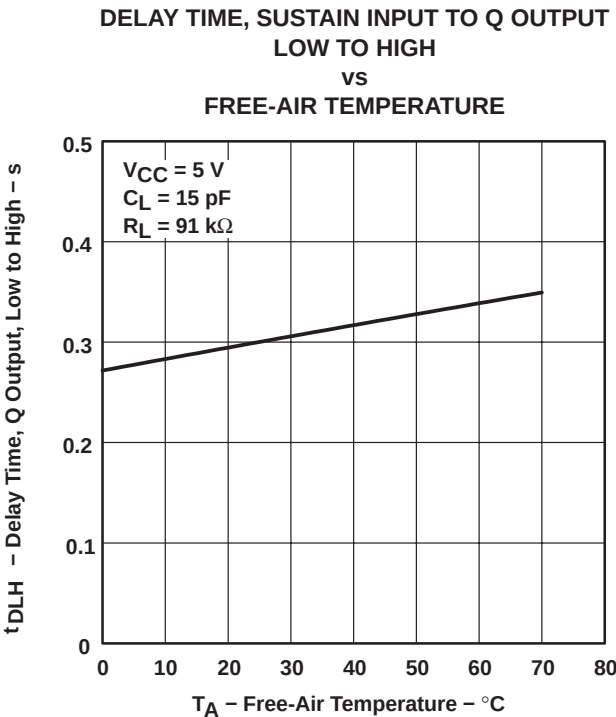


Figure 5

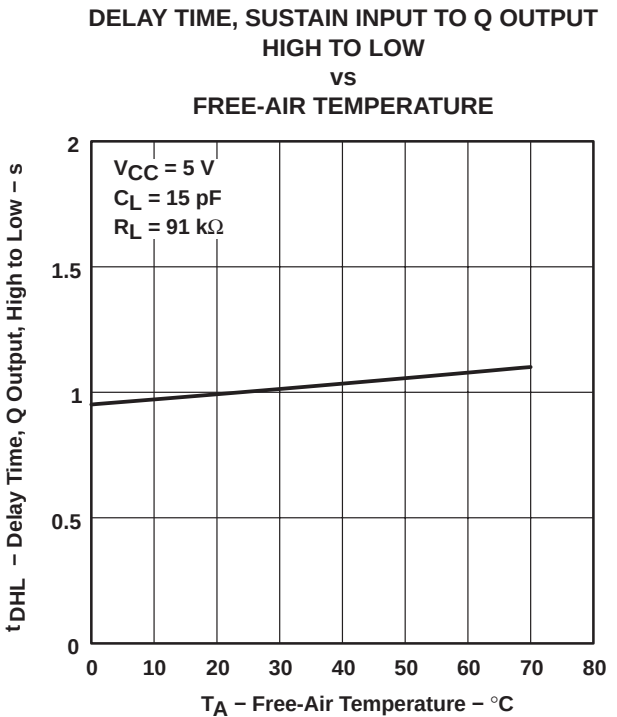


Figure 6

TYPICAL CHARACTERISTICS

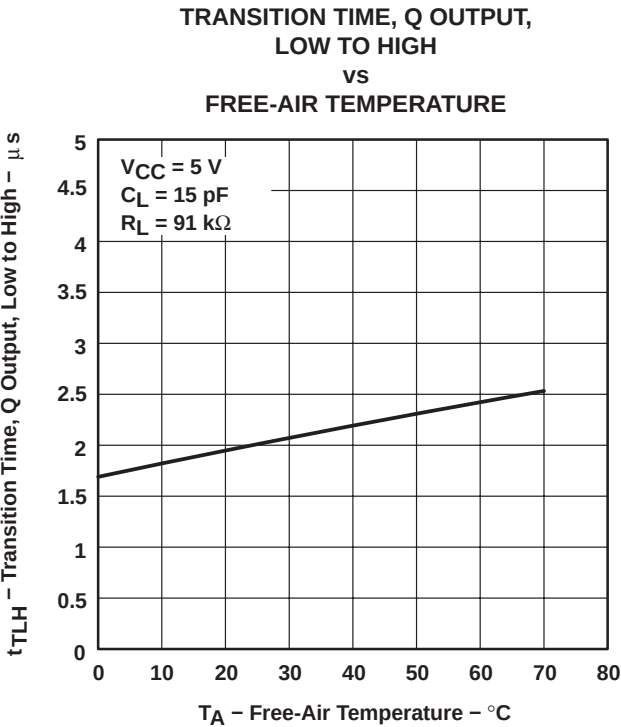


Figure 7

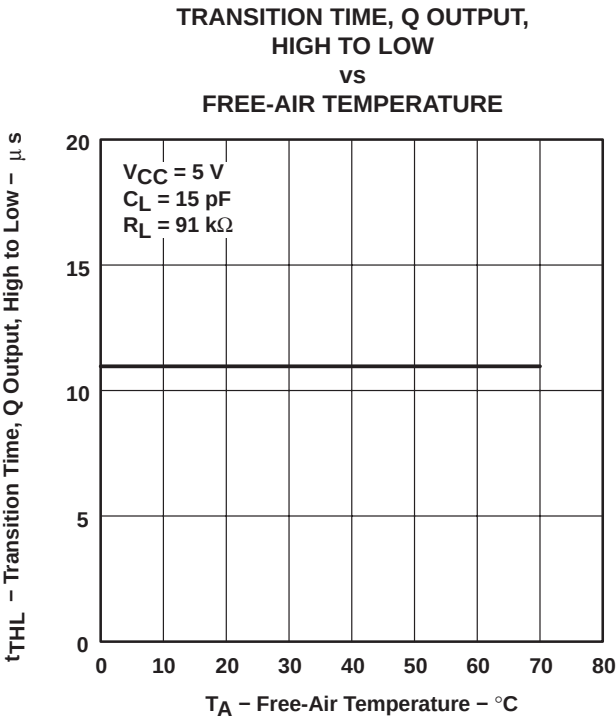


Figure 8

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN751508FT	OBSOLETE	DFP	FT	48		TBD	Call TI	Call TI
SN751518FT	OBSOLETE	DFP	FT	48		TBD	Call TI	Call TI
SN751518FT	OBSOLETE	DFP	FT	48		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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